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POWER ELECTRONICS HANDBOOK

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Preface

Introduction

The purpose of *Power Electronics Handbook* is to provide a reference that is both concise and useful for engineering students and practicing professionals. It is designed to cover a wide range of topics that make up the field of power electronics in a well-organized and highly informative manner. The Handbook is a careful blend of both traditional topics and new advancements. Special emphasis is placed on practical applications, thus, this Handbook is not a theoretical one, but an enlightening presentation of the usefulness of the rapidly growing field of power electronics. The presentation is tutorial in nature in order to enhance the value of the book to the reader and foster a clear understanding of the material.

The contributors to this Handbook span the globe, with fifty-four authors from twelve different countries, some of whom are the leading authorities in their areas of expertise. All were chosen because of their intimate knowledge of their subjects, and their contributions make this a comprehensive state-of-the-art guide to the expanding field of power electronics and its applications covering:

- the characteristics of modern power semiconductor devices, which are used as switches to perform the power conversions from ac-dc, dc-dc, dc-ac, and ac-ac;
- both the fundamental principles and in-depth study of the operation, analysis, and design of various power converters; and
- examples of recent applications of power electronics.

Power Electronics Backgrounds

The first electronics revolution began in 1948 with the invention of the silicon transistor at Bell Telephone Laboratories by Bardeen, Bratain, and Schockley. Most of today's advanced electronic technologies are traceable to that invention, and modern microelectronics has evolved over the years from these silicon semiconductors. The second electronics revolution began with the development of a commercial thyristor by the General Electric Company in 1958. That was the beginning of a new era of *power electronics*. Since then, many different types of power semiconductor devices and conversion techniques have been introduced.

The demand for energy, particularly in electrical forms, is ever-increasing in order to improve the standard of living. *Power electronics* helps with the efficient use of electricity, thereby reducing power consumption. Semiconductor devices are used as switches for power conversion or processing, as are solid state electronics for efficient control of the amount of power and energy flow. Higher efficiency and lower losses are sought for devices for a range of applications, from microwave ovens to high-voltage dc transmission. New devices and power electronic systems are now evolving for even more effective control of power and energy.

Power electronics has already found an important place in modern technology and has revolutionized control of power and energy. As the voltage and current ratings and switching characteristics of power semiconductor devices keep improving, the range of applications continues to expand in areas such as lamp controls, power supplies to motion control, factory automation, transportation, energy storage, multi-megawatt industrial drives, and electric power transmission and distribution. The greater efficiency and tighter control features of power electronics are becoming attractive for applications in motion control by replacing the earlier electro-mechanical and electronic systems. Applications in power transmission include high-voltage dc (VHDC) converter stations, flexible ac transmission system (FACTS), and static-var compensators. In power distribution these include dc-to-ac conversion, dynamic filters, frequency conversion, and Custom Power System.

Almost all new electrical or electromechanical equipment, from household air conditioners and computer power supplies to industrial motor controls, contain power electronic circuits and/or systems. In order to keep up, working engineers involved in control and conversion of power and energy into applications ranging from several hundred voltages at a fraction of an ampere for display devices to about 10,000 V at high-voltage dc transmission, should have a working knowledge of power electronics.

Organization

The Handbook starts with an introductory chapter and moves on to cover topics on power semiconductor devices, power converters, applications and peripheral issues. The book is organized into six areas, the first of which includes chapters on operation and characterizations of power semiconductor devices: power diode, thyristor, gate turn-off thyristor (GTO), power bipolar transistor (BJT), power MOSFET, insulated gate bipolar transistor, MOS controlled thyristor (MCT), and static induction devices.

The next topic area includes chapters covering various types of power converters, the principles of operation and the methods for the analysis and design of power converters. This also includes gate drive circuits and control methods for power converters. The next three chapters cover applications in power supplies, electronics ballasts, renewable energy sources, HVDC transmission, VAR compensation, and capacitor charging.

The following six chapters focus on the operation, theory and control methods of motor drives, and automotive systems. We then move on to two chapters on power quality issues and active filters, and two chapters on computer simulation, packaging and smart power systems.

Locating Your Topic

A table of contents is presented at the front of the book, and each chapter begins with its own table of contents. The reader should look over these tables of contents to become familiar with the structure, organization, and content of the book.

Audience

The Handbook is designed to provide both students and practicing engineers with answers to questions involving the wide spectrum of power electronics. The book can be used as a textbook for graduate students in electrical or systems engineering, or as a reference book for senior undergraduate students and for engineers who are interested and involved in operation, project management, design, and analysis of power electronics equipment and motor drives.

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Introduction

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1.1 Power Electronics Defined[1]

It has been said that people do not use electricity, but rather they use communication, light, mechanical work, entertainment, and all the tangible benefits of both energy and electronics. In this sense, electrical engineering is a discipline very much involved in energy conversion and information. In the general world of electronics engineering, the circuits engineers design and use are intended to convert information, with energy merely a secondary consideration in most cases. This is true of both analog and digital circuit design. In radio frequency applications, energy and information are sometimes on a more equal footing, but the main function of any circuit is that of information transfer.

What about the conversion and control of electrical energy itself? Electrical energy sources are varied and of many types. It is natural, then, to consider how electronic circuits and systems can be applied to the challenges of energy conversion and management. This is the framework of *power electronics*, a discipline that is defined in terms of *electrical energy conversion, applications*, and *electronic devices*. More specifically,

> **DEFINITION** *Power electronics* involves the study of electronic circuits intended to control the flow of electrical energy. These circuits handle power flow at levels much higher than the individual device ratings.

Rectifiers are probably the most familiar example of circuits that meet this definition. Inverters (a general term for dc-ac converters) and dc-dc converters for power supplies are also common applications. As shown in Fig. 1.1, power electronics represents a median point at which the topics of energy systems, electronics, and control converge and combine [1]. Any useful circuit design for the control of power must address issues of both devices and control, as well as of the energy itself. Among the unique aspects of power electronics are its emphasis on large semiconductor devices, the application of magnetic devices for energy storage, and special control methods that must be applied to nonlinear systems. In any study of electrical engineering, power electronics must be placed on a level with digital, analog, and radio-frequency electronics if we are to reflect its distinctive design methods and unique challenges.

The history of power electronics [2,3,4,5] has been closely allied with advances in electronic devices that provide the capability to handle high-power levels. Only in the past decade has a transition been made from a "device-driven" field to an

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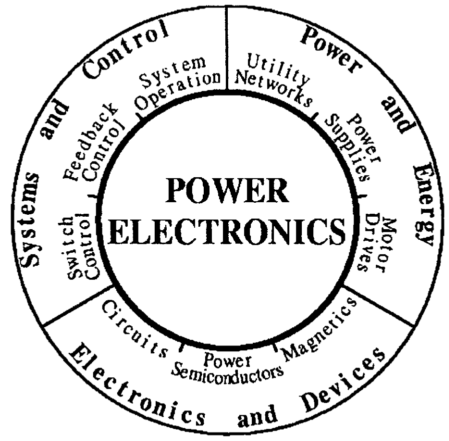


FIGURE 1.1 Control, energy, and power electronics are interrelated.

"applications-driven" field. This transition has been based on two factors: advanced semiconductors with suitable power ratings exist for almost every application of wide interest; and the general push toward miniaturization is bringing advanced power electronics into a growing variety of products.

1.2 Key Characteristics

All power electronic circuits manage the flow of electrical energy between some sort of source and a load. The parts in a circuit must direct electrical flows, not impede them. A general power conversion system is shown in Fig. 1.2. The function of the power converter positioned at the middle is that of controlling energy flow between a given electrical source and a given load. For our purposes, the power converter will be implemented with a power electronic circuit. As a power converter appears between a source and a load, any energy used within the converter is lost to the overall system. A crucial point emerges — to build a power converter, we should consider only lossless components. A realistic converter design must approach 100% efficiency.

A power converter connected between a source and a load also affects system reliability. If the energy source is perfectly reliable (it is on all the time), then a failure in the converter affects the user (the load) just as if the energy source had failed. An unreliable power converter creates an unreliable system. To put this in perspective, consider that a typical American household loses electric power only a few minutes a year. Therefore, energy is available 99.999% of the time. A converter must be even better than this if system degradation is to be prevented. An ideal converter implementation will not suffer any failures over its application lifetime. In many cases, extremely high reliability can be a more difficult objective than that of high efficiency.

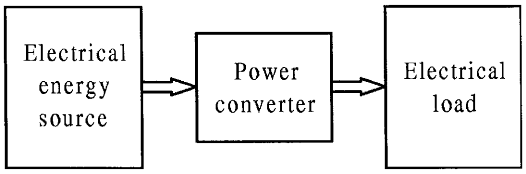


FIGURE 1.2 General system for electric power conversion. (From Reference [2], copyright © 1998, Oxford University Press, Inc.: used by permission.)

1.2.1 The Efficiency Objective — The Switch

A circuit element as simple as a light switch reminds us that the extreme requirements in power electronics are not especially novel. Ideally, when a switch is on, it has zero voltage drop and will carry any current imposed on it. When a switch is off, it blocks the flow of current regardless of the voltage across it. *Device power*, the product of the switch voltage and current, is identically zero at all times. The switch controls energy flow with no loss. In addition, reliability is also high. Household light switches perform over decades of use and perhaps 100,000 operations. Of course, a mechanical light switch does not meet all practical needs. A switch in a power supply often must function 100,000 times each second. Since even the best mechanical switch will not last beyond a few million cycles, semiconductor switches (without this limitation) are the devices of choice in power converters.

A circuit built from ideal switches will be lossless. As a result, switches are the main components of power converters, and many people equate power electronics with the study of switching power converters. Magnetic transformers and lossless storage elements such as capacitors and inductors are also valid candidates for use in power converters. The complete concept, shown in Fig. 1.3, illustrates a *power electronic system.* Such a system consists of an energy source, an electrical load, a *power electronic circuit*, and control functions. The power electronic circuit contains switches, lossless energy storage elements, and magnetic transformers. The controls take information from the source, load, and designer and then determine how the switches operate to achieve the desired conversion. The controls are usually built up with conventional low-power analog and digital electronics.

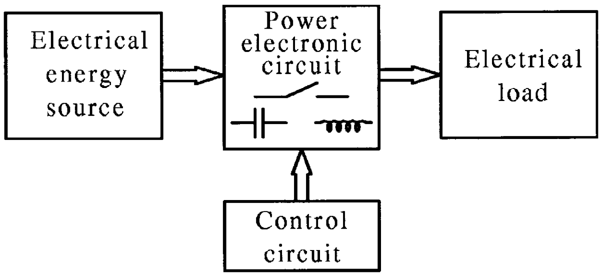


FIGURE 1.3 A basic power electronic system. (From Reference [2], copyright © 1998, Oxford University Press, Inc.; used by permission.)

Switching devices are selected based on their *power handling* rating the product of their voltage and currents ratings rather than on power dissipation ratings. This is in contrast to other applications of electronics, in which power dissipation ratings dominate. For instance, a typical stereo receiver performs a conversion from ac line input to audio output. Most audio amplifiers do not use the techniques of power electronics, and the semiconductor devices do not act as switches. A commercial 100 W amplifier usually is designed with transistors big enough to dissipate the full 100 W. The semiconductor devices are used primarily to reconstruct audio information rather than to manipulate energy flows. When the devices are used as switches instead, the power levels increase considerably, as suggested by the following examples.

> **Example** 1.1. The 2N2222A is a popular bipolar transistor with a rated collector-emitter breakdown voltage of 30 V, a maximum collector current of 0.8 A, and rated power dissipation of 0.5 W. In a conventional analog circuit, it usually handles energy within its 0.5 W power dissipation rating. In principle, this device can manipulate the flow of 0.8 A in a 30 V circuit and so a power electronics engineer would list its power handling rating as 24 W. The ability to control up to 24 W, combined with good switching characteristics, makes this device common as an auxiliary element in power supplies.

> **Example** 1.2. The MTW20N50 is a metal-oxide-semiconductor field-effect transistor (MOSFET) with a drain current rating of 20 A, a maximum drain-source breakdown voltage of 500 V, and rated power dissipation of 250 W. The power handling rating is 10 kW. Several manufacturers have developed power electronic controllers for domestic refrigerators, air conditioners, and even electric vehicles based on this device and its relatives.

The second part of the definition of power electronics in Section 1.1 points out that the circuits handle power at levels much higher than that of the ratings of individual devices. In the first Example, a 2N2222A might be used to handle 24 W as compared with its individual rating of 0.5 W. The MTW20N50 is used to handle up to 10 kW, compared to its rating of 250 W. These ratios, 48 and 40, respectively, are high, but not unusual in power electronics contexts. In contrast, the same ratio in a conventional audio amplifier is close to unity.

1.2.2 The Reliability Objective Simplicity and Integration

High-power applications lead to interesting issues. For example, in an inverter the semiconductors often manipulate 40 times their rated power or more. A small design error, unexpected thermal problem, or minor change in layout could alter this somewhat, perhaps to a factor of 45. This small change puts large additional stresses on the devices, and can lead to quick failure. The first issue for reliability in power electronic circuits is that of managing device voltage, current, and power dissipation levels to keep them well within rating limits. This can be challenging when power handling levels are high.

The second issue for reliability is simplicity. It is well-established in military electronics that the more parts there are in a system, the more likely it is to fail. Power electronic circuits tend to have few parts, especially in the main energy flow paths. Necessary operations must be carried out through shrewd use of these parts. Often, this means that sophisticated control strategies are applied to seemingly simple conversion circuits.

The third issue for reliability is integration. One way to avoid the reliability–complexity tradeoff is to integrate multiple components and functions on a single substrate. A microprocessor, for example, might contain more than a million gates. As all interconnections and signals flow within a single chip, the reliability is nearly that of a single part. An important parallel trend in power electronic devices involves the integrated module [6]. Manufacturers seek ways to package several switching devices, with their interconnections and protection components together as a unit. Control circuits for converters are also integrated as much as possible to keep reliability high. The package itself becomes a fourth issue for reliability, and one that is as yet only partly understood. Semiconductor packages include small bonding wires that can be susceptible to thermal or vibration damage. The small geometries tend to enhance electromagnetic interference among the internal circuit components.

1.3 Trends in Power Supplies

As costs of electronics decline, the power supply becomes a larger fraction of system cost and design effort. One major manufacturer estimates that power supply cost will soon reach 50 of the total cost of a typical electronic product such as a cordless telephone or personal computer. Thus, new technology developments in power supplies are critically important. In the past, bulky *linear power supplies* were designed with transformers and rectifiers from the ac line frequency to provide low-level dc voltages for electronic circuits. Late in the 1960s, use of dc sources in aerospace applications led to the development of power electronic dc-dc conversion circuits for power supplies. In a typical power electronics arrangement today, an ac source from a wall outlet is rectified without any transformation; the resulting high dc voltage is converted through a dc-dc circuit to the 5 V, 12 V, or other level required. These *switched-mode power supplies* are rapidly supplanting linear supplies across the full spectrum of circuit applications.

A personal computer commonly requires three different 5 V supplies, two +12 V supplies, a −12 V supply, a 24 V supply, and perhaps a few more. This does not include supplies for video display or peripheral devices. Only a switched-mode supply can support such complex requirements without high costs. The bulk and weight of linear supplies make them infeasible for hand-held communication devices, calculators, notebook computers, and similar equipment. Switched-mode supplies often take advantage of MOSFET semiconductor technology. Trends toward high reliability, low cost, and miniaturization have reached the point at which a 5 V power supply sold today might last 1,000,000 hr (more than 100 yr), provide 100 W of output in a package with volume $< 15\ \text{cm}^3$, and sell for a price of $<$ \$0.30 watt. This type of supply brings an interesting dilemma: the ac line cord to plug it in actually takes up more space than the power supply itself. Innovative concepts such as integrating a power supply within a connection cable will be used in the future.

Device technology for power supplies is being driven by expanding needs in the automotive and telecommunications industries as well as in markets for portable equipment. The automotive industry is making a transition to 42 V systems to handle increasing electric power needs. Power conversion for this industry must be cost effective, yet rugged enough to survive the high vibration and wide temperature range to which a passenger car is exposed. Global communication is possible only when sophisticated equipment can be used almost anywhere. This brings a special challenge, because electrical supplies are neither reliable nor consistent throughout much of the world. While in North America voltage swings in the domestic ac supply are often $< \pm 5\%$ around a nominal value, in many developing nations the swing can be $\pm 25\%$ when power is available. Power converters for communications equipment must tolerate these swings, and must also be able to make use of a wide range of possible backup sources. Given the enormous size of worldwide markets for telephones and consumer electronics, there is a clear need for flexible-source equipment. Designers are challenged to obtain maximum performance from small batteries, and to create equipment with minimal energy requirements.

1.4 Conversion Examples

1.4.1 Single-Switch Circuits

Electrical energy sources can come in the form of dc voltage sources at various values, sinusoidal ac sources, polyphase sources, and many others. A power electronic circuit might be asked to transfer energy between two different dc voltage levels, between an ac source and a dc load, or between sources at different frequencies. It might be used to adjust an output voltage or power level, drive a nonlinear load, or control a load current. In this section, we consider a few basic converter arrangements and discuss energy conservation as a tool for analysis.

Example 1.3. Consider the circuit shown in Fig. 1.4. It contains an ac source, a switch, and a resistive load. It is a simple but complete power electronic system. Let us assign a (somewhat arbitrary) control scheme to the switch. What if the switch is turned on whenever $V_{ac} > 0$, and turned off otherwise? The input and output voltage waveforms are shown in Fig. 1.5. The input has a time average of 0, and root mean square (RMS) value equal to $V_{peak}/\sqrt{2}$, where V_{peak} is the maximum value of V_{ac}. The output has a nonzero average value given by:

$$\begin{aligned}\langle v_{out}(t)\rangle &= \frac{1}{2\pi}\left(\int_{-\pi/2}^{\pi/2} V_{peak}\cos\theta\, d\theta + \int_{\pi/2}^{3\pi/2} 0\, d\theta\right)\\ &= \frac{V_{peak}}{\pi} = 0.3183 V_{peak} \qquad (1.1)\end{aligned}$$

and an RMS value equal to $V_{peak}/2$. Since the output has nonzero dc voltage content, the circuit can be used as an ac-dc converter. To make it more useful, a lowpass filter would be added between the output and the load to smooth out the ac portion. This filter needs to be lossless, and will be constructed from only inductors and capacitors.

The circuit in the preceding Example acts as a half-wave rectifier with a resistive load. With the hypothesized switch action, a diode can be substituted for the ideal switch. The example confirms that a simple switching circuit can perform power conversion functions. However, notice that a diode is not, in general, the same as an ideal switch. A diode places restrictions on the current direction, while a true switch would not. An ideal switch allows control over whether it is on or off, while a diode's operation is constrained by circuit variables.

Consider a second half-wave circuit, now with a series *L-R* load, as shown in Fig. 1.6.

Example 1.4. A series diode-*L-R* circuit has ac voltage-source input. This circuit operates much differently than the half-wave rectifier with resistive load. A diode will be on if forward biased, and off if reverse biased. In this circuit, an off diode will give a current of zero. When the diode is on, the circuit is the ac source with *L-R* load. Let

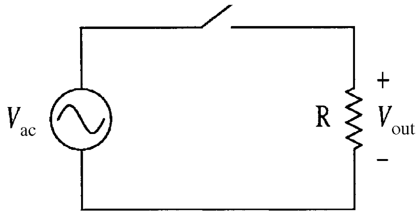


FIGURE 1.4 A simple power electronic system. (From Reference [2], copyright © 1998, Oxford University Press, Inc.; used by permission.)

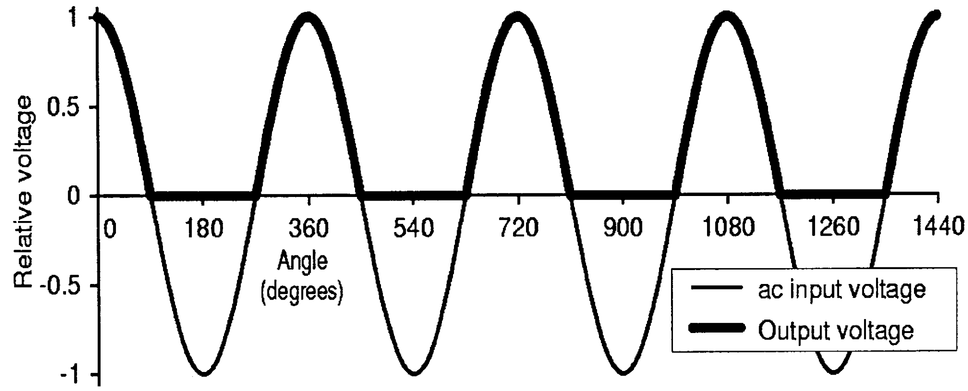


FIGURE 1.5 Input and output waveforms for Example 1.4.

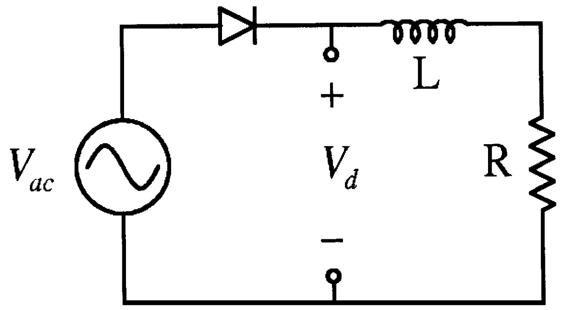


FIGURE 1.6 Half-wave rectifier with L-R load for Example 1.5.

the ac voltage be $V_0 \cos(\omega t)$. From Kirchhoff's voltage law (KVL),

$$V_0 \cos(\omega t) = L\frac{di}{dt} + Ri \tag{1.2}$$

Let us assume that the diode is initially off (this assumption is arbitrary, and we will check it out as the example is solved). If the diode is off, the diode current $i = 0$, and the voltage across the diode will be v_{ac}. The diode will become forward-biased when v_{ac} becomes positive. The diode will turn on when the input voltage makes a zero-crossing in the positive direction. This allows us to establish initial conditions for the circuit: $i(t_0) = 0$, $t_0 = -\pi/(2\omega)$. The differential equation can be solved in a conventional way to give

$$i(t) = V_0\left[\frac{\omega L}{R^2 + \omega^2 L^2}\exp\left(\frac{-t}{\tau} - \frac{\pi}{2\omega\tau}\right) + \frac{R}{R^2 + \omega^2 L^2}\cos(\omega t) + \frac{\omega L}{R^2 + \omega^2 L^2}\sin(\omega t)\right] \tag{1.3}$$

where τ is the time constant L/R. What about diode turn-off? One first guess might be that the diode turns off when the voltage becomes negative, but this is not correct. We notice from the solution that the current is not zero when the voltage first becomes negative. If the switch attempts to turn off, it must drop the inductor current to zero instantly. The derivative of current in the inductor di/dt would become negative infinite. The inductor voltage $L(di/dt)$ similarly becomes negative infinite and the devices are destroyed. What really happens is that the falling current allows the inductor to maintain forward bias on the diode. The diode will turn off only when the *current* reaches zero. A diode has definite properties that determine circuit action, and both voltage and current are relevant. Figure 1.7 shows the input and output waveforms for a time constant τ equal to $\approx 1/3$ of the ac waveform period.

1.4.2 The Method of Energy Balance

Any circuit must satisfy conservation of energy. In a lossless power electronic circuit, energy is delivered from source to load, which is possible through an intermediate storage step. The energy flow must balance over time such that the energy drawn from the source matches that delivered to the load. The converter in Fig. 1.8 serves as an example of how the method of energy balance can be used to analyze circuit operation.

EXAMPLE 1.5. The switches in the circuit of Fig. 1.8 are controlled cyclically to operate in alternation: when the left switch is on, the right one is off, and so on. What does the circuit do if each switch operates half the time? The inductor and capacitor have large values.

When the left switch is on, the source voltage V_{in} appears across the inductor. When the right switch is on, the output voltage V_{out} appears across the inductor. If this circuit is to be a useful converter, we want the inductor to receive energy from the source, then deliver it to the load without loss. Over time, this means that energy does not build up in the inductor (instead it flows through on average). The power into the inductor therefore must equal the power out, at least over a cycle. Therefore, the *average* power in should equal the *average*

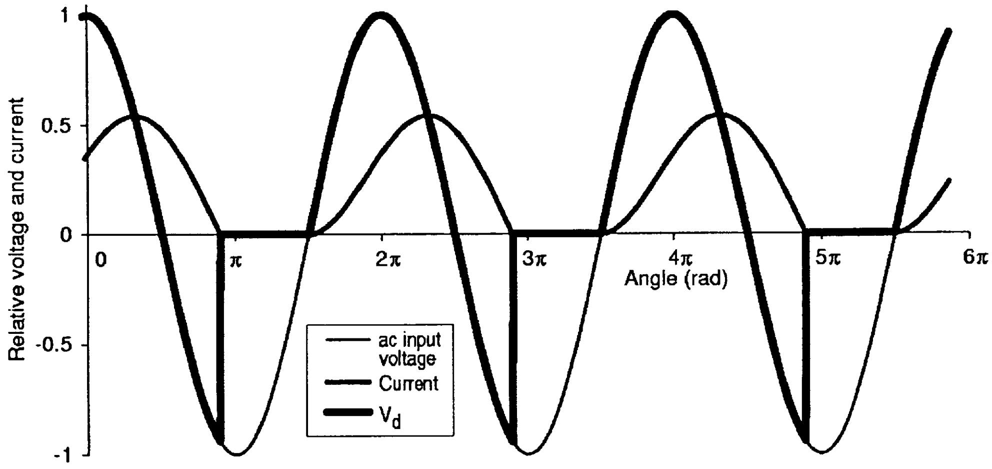


FIGURE 1.7 Input and output waveforms for Example 1.5.

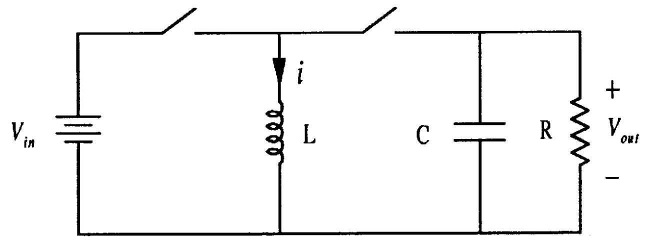


FIGURE 1.8 Energy transfer switching circuit for Example 1.5. (From Reference [2], copyright © 1998, Oxford University Press, Inc.; used by permission.)

power out of the inductor. Let us denote the inductor current as i. The input is a constant voltage source. Because L is large, this constant voltage source will not be able to change the inductor current quickly, and we can assume that the inductor current is also constant. The average power into L over the cycle period T is

$$P_{\text{in}} = \frac{1}{T}\int_0^{T/2} V_{\text{in}} i \, dt = \frac{V_{\text{in}} i}{2} \tag{1.4}$$

For the average power out of L, we must be careful about current directions. The current *out* of the inductor will have a value $-i$. The average output power is

$$P_{\text{out}} = \frac{1}{T}\int_{T/2}^{T} -iV_{\text{out}} \, dt = -\frac{V_{\text{out}} i}{2} \tag{1.5}$$

For this circuit to be useful as a converter, there is net energy flow from the source to the load over time. The power conservation relationship $P_{\text{in}} = P_{\text{out}}$ requires that $V_{\text{out}} = -V_{\text{in}}$.

The method of energy balance shows that when operated as described in the example, the circuit of Fig. 1.8 serves as a polarity reverser. The output voltage magnitude is the same as that of the input, but the output polarity is negative with respect to the reference node. The circuit is often used to generate a negative supply for analog circuits from a single positive input level. Other output voltage magnitudes can be achieved at the output if the switches alternate at unequal times.

If the inductor in the polarity reversal circuit is moved instead to the input, a step-up function is obtained. Consider the circuit of Fig. 1.9 in the following example.

Example 1.6. The switches in Fig. 1.9 are controlled cyclically in alternation. The left switch is on for 2/3 of each cycle, and the right switch for 1/3 of each cycle. Determine the relationship between V_{in} and V_{out}.

The inductor's energy should not build up when the circuit is operating normally as a converter. A power balance calculation can be used to relate the input and output voltages. Again let i be the inductor current.

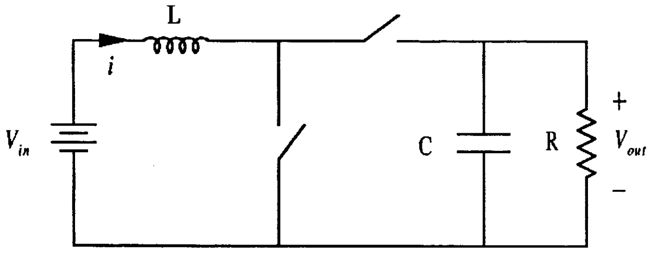


FIGURE 1.9 Switching converter Example 1.6. (From Reference [2], copyright © 1998, Oxford University Press, Inc.; used by permission.)

When the left switch is on, power is injected into the inductor. Its average value is

$$P_{\text{in}} = \frac{1}{T}\int_{0}^{2T/3} V_{\text{in}} i \, dt = \frac{2V_{\text{in}} i}{3} \tag{1.6}$$

Power leaves the inductor when the right switch is on. Again we need to be careful of polarities, and remember that the current should be set to negative to represent output power. The result is

$$P_{\text{out}} = \frac{1}{T}\int_{2T/3}^{T} -(V_{\text{in}} - V_{\text{out}}) i \, dt = -\frac{V_{\text{in}} i}{3} + \frac{V_{\text{out}} i}{3} \tag{1.7}$$

When the input and output power are equated,

$$\frac{2V_{\text{in}} i}{3} = -\frac{V_{\text{in}} i}{3} + \frac{V_{\text{out}} i}{3}, \quad \text{and} \quad 3V_{\text{in}} = V_{\text{out}} \tag{1.8}$$

and we see that the output voltage is triple the input. Many seasoned engineers find the dc-dc step-up function of Fig. 1.9 to be surprising. Yet Fig. 1.9 is just one example of such an action. Others (including flyback circuits related to Fig. 1.8) are used in systems from CRT electron guns to spark ignitions for automobiles.

All the circuits in the preceding examples have few components, provide useful conversion functions, and are efficient. If the switching devices are ideal, each circuit is lossless. Over the history of power electronics, development has tended to flow around the discovery of such circuits, that is, a circuit with a particular conversion function is discovered, analyzed, and applied. As the circuit moves from simple laboratory testing to a complete commercial product, control and protection functions are added. The power portion of the circuit remains close to the original idea. The natural question arises as to whether a systematic approach to conversion is possible. Can we start with a desired function and design an appropriate converter, rather than starting from the converter and working backwards toward the application? What underlying principles can be applied to design and analysis? In this introductory chapter, we will introduce a few of the key concepts. Keep in mind that while many of the circuits look deceptively simple, all are nonlinear systems with unusual behavior.

1.5 Tools for Analysis and Design

1.5.1 The Switch Matrix

The most readily apparent difference between a power electronic circuit and other types of electronic circuits is the switch action. In contrast to a digital circuit, the switches do not indicate a logic level. Control is effected by determining the times at which switches should operate. Whether there is just one switch or a large group, there is a complexity limit: If a converter has m inputs and n outputs, even the densest possible collection of switches would have a single switch between each input line and each output line. The $m \times n$ switches in the circuit can be arranged according to their connections. The pattern suggests a matrix, as shown in Fig. 1.10.

Power electronic circuits fall into two broad classes:

1. *Direct switch matrix circuits.* In these circuits, energy storage elements are connected to the matrix only at the input and output terminals. The storage elements effectively become part of the source or load. A rectifier with an external lowpass filter is an example of a direct switch matrix circuit. In the literature, these circuits are sometimes called *matrix converters.*
2. *Indirect switch matrix circuits*, also termed *embedded converters.* These circuits, like the polarity-reverser example, have energy storage elements connected *within* the matrix structure. There are usually very few storage elements. Indirect switch matrix circuits are most commonly analyzed as a cascade connection of direct switch matrix circuits with the storage in between.

The switch matrices in realistic applications are small. A 2 × 2 switch matrix, for example, covers all possible cases with a single-port input source and a two-terminal load. The matrix is commonly drawn as the *H-bridge* shown in Fig. 1.11. A more complicated example is the three-phase bridge rectifier shown in Fig. 1.12. There are three possible inputs, and the two terminals of the dc circuit provide outputs, which give a 3 × 2 switch matrix. In a personal computer power supply, there are commonly five separate dc loads, and the switch matrix is 2 × 10. Very few practical converters have more than ≈24 switches, and most designs use fewer than 12.

A switch matrix provides a way to organize devices for a given application. It also helps to focus the effort into three major task areas. Each of these areas must be addressed

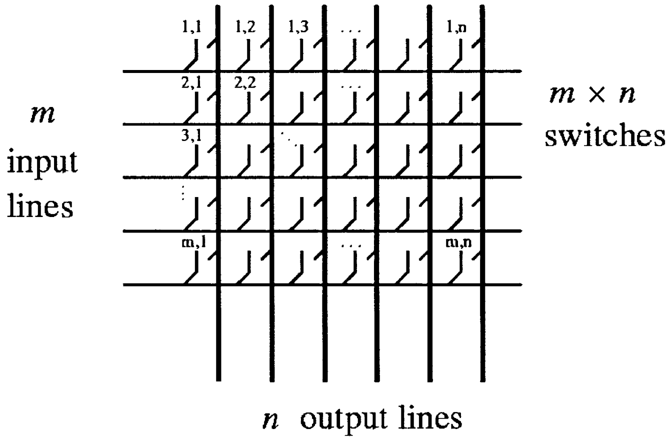


FIGURE 1.10 The general switch matrix.

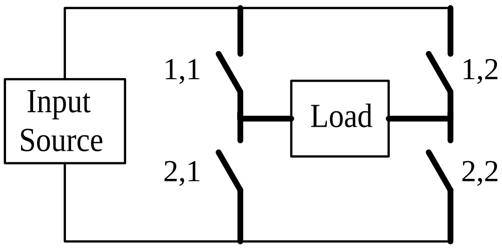


FIGURE 1.11 H-bridge configuration of a 2 × 2 switch matrix..

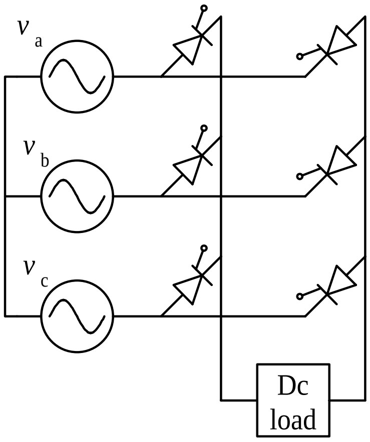


FIGURE 1.12 Three-phase bridge rectifier circuit, a 3 × 2 switch matrix.

effectively in order to produce a useful power electronic system.

- The **Hardware** Task→Build a switch matrix. This involves the selection of appropriate semiconductor switches and the auxiliary elements that drive and protect them.
- The **Software** Task→Operate the matrix to achieve the desired conversion. All operational decisions are implemented by adjusting switch timing.
- The **Interface** Task→Add energy storage elements to provide the filters or intermediate storage necessary to meet the application requirements. Unlike most filter applications, lossless filters with simple structures are required.

In a rectifier or other converter, we must choose the electronic parts, how to operate them, and how best to filter the output to satisfy the needs of the load.

1.5.2 Implications of Kirchhoff's Voltage and Current Laws

A major challenge of switch circuits is their capacity to "violate" circuit laws. Consider first the simple circuits of Fig. 1.13. The circuit of Fig. 1.13a is something we might try for ac-dc conversion. This circuit has problems. Kirchhoff's voltage law (KVL) tells us that the "sum of voltage drops around a closed loop is zero." However, with the switch closed, the sum of voltages around the loop is not zero. In reality, this is not a valid result. Instead, a very large current will flow and cause a large $I \cdot R$ drop in the wires. The KVL *will* be satisfied by the wire voltage drop, but a fire or, better yet, fuse action, might result. There is, however, nothing that would prevent an operator from trying to close the switch. The KVL, then, implies a crucial restriction: A switch matrix must not attempt to interconnect unequal voltage sources directly. Notice that a wire, or dead short, can be thought of as a voltage source with $V = 0$, so KVL is a generalization for avoiding shorts across an individual voltage source.

A similar constraint holds for Kirchhoff's current law (KCL). The KCL states that "currents into a node must sum to zero." When current sources are present in a converter, we must avoid any attempts to violate KCL. In Fig. 1.13b, if the current sources are different and the switch is opened, the sum of the currents into the node will not be zero. In a real circuit, high voltages will build up and cause an arc to create another current path. This situation has real potential for damage, and a fuse will not help. The KCL implies a restriction in which a switch matrix must not attempt to interconnect unequal current sources directly. An open circuit can be thought of as a current source with $I = 0$, so KCL applies to the problem of opening an individual current source.

In contrast to conventional circuits, in which KVL and KCL are automatically satisfied, switches do not "know" KVL or KCL. If a designer forgets to check, and accidentally shorts two voltages or breaks a current source connection, some problem or damage will result. On the other hand, KVL and KCL place necessary constraints on the operating strategy of a switch matrix. In the case of voltage sources, switches must not act to create short-circuit paths among dissimilar sources. In the case of KCL, switches must act to provide a path for currents. These constraints drastically reduce the number of valid switch operating conditions in a switch matrix, and lead to manageable operating design problems.

When energy storage is included, there are interesting implications for the current law restrictions. Figure 1.14 shows two "circuit law problems." In Fig. 1.14a, the voltage source will cause the inductor current to ramp up indefinitely because $V = L\, di/dt$. We might consider this to be a "KVL problem," since the long-term effect is similar to shorting the source. In Fig. 1.14b, the current source will cause the capacitor voltage to ramp toward infinity. This causes a "KCL problem"; eventually, an arc will form to create an additional current path, just as if the current source had been opened. Of course, these connections are not problematic if they are only temporary. However, it should be evident that an inductor will not support dc voltage, and a capacitor will not support dc current. On average over an extended time interval,

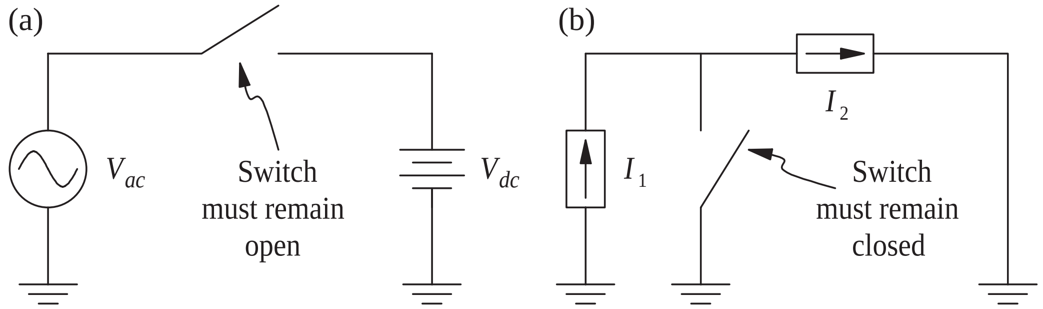


FIGURE 1.13 Hypothjetical power converters: (a) Possible ac-dc converter; (b) Possible dc-dc converter. (From [2], copyright © 1998, Oxford University Press Inc., used by permission.)

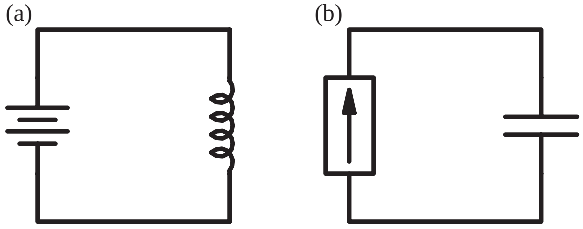


FIGURE 1.14 Short-term KVL and KCL problems in energy storage circuits: (a) An inductor cannot sustain dc voltage indefinitely; (b) A capacitor cannot sustain dc current indefinitely.

the voltage across an inductor must be zero, and the current into a capacitor must be zero.

1.5.3 Resolving the ardware Problem Semiconductor Devices

A switch is either on or off. An ideal switch, when on, will carry any current in any direction. When off, it will never carry current, no matter what voltage is applied. It is entirely lossless, and changes from its on state to its off state instantaneously. A *real switch* can only approximate an ideal switch. Those aspects of real switches that differ from the ideal include the following:

- limits on the amount and direction of on-state current;
- a nonzero on-state voltage drop (such as a diode forward voltage);
- some level of leakage current when the device is supposed to be off;
- limitations on the voltage that can be applied when off; and
- operating speed. The time of transition between the on and off states can be important.

The degree to which properties of an ideal switch must be met by a real switch depends on the application. For example, a diode can easily be used to conduct dc current; the fact that it conducts only in one direction is often an advantage, not a weakness.

Many different types of semiconductors have been applied in power electronics. In general, these fall into three groups:

- Diodes, which are used in rectifiers, dc-dc converters, and in supporting roles.
- Transistors, which in general are suitable for control of single-polarity circuits. Several types of transistors are applied to power converters. The most recent type, the insulated gate bipolar transistor (IGBT) is unique to power electronics and has good characteristics for applications such as inverters.
- Thyristors, which are multijunction semiconductor devices with latching behavior. Thyristors in general can be switched with short pulses, and then maintain their state until current is removed. They act only as switches. The characteristics are especially well-suited to controllable rectifiers, although thyristors have been applied to all power conversion applications.

Some of the features of the most common power semiconductors are listed in Table 1.1. This table shows a wide variety of speeds and rating levels. As a rule, faster speeds apply to lower ratings. For each device type, cost tends to increase both for faster devices and for devices with higher power-handling capacity.

Conducting direction and blocking behavior are fundamentally tied to the device type, and these basic characteristics constrain the choice of device for a given conversion function. Consider again a diode. It carries current in only one direction and always blocks current in the other. Ideally, the diode exhibits no forward voltage drop or off-state leakage current. Although it lacks all the features of an ideal switch, the ideal diode is an important switching device. Other real devices operate with polarity limits on current and voltage and have corresponding ideal counterparts. It is convenient to define a special type of switch to represent this behavior: the *restricted switch.*

DEFINITION A *restricted switch* is an ideal switch with the addition of restrictions on the direction of current

TABLE 1.1 Some modern semiconductor switch types and their basic characteristics

DEVICE TYPE	CHARACTERISTICS OF POWER DEVICES
Diode	Current ratings from <1 to >5000 A. Voltage ratings from 10 V to 10 kV or more. The fastest power devices switch in 20 ns, while the slowest require 100 μs or more. The function of a diode applies in rectifiers and dc-dc circuits.
BJT	(Bipolar Junction Transistor) Conducts collector current (in one direction) when sufficient base current is applied. Power device current ratings from 0.5 to 500 A or more; voltages from 30 to 1200 V. Switching times from 0.5 to 100 μs. The function applies to dc-dc circuits; combinations with diodes are used in inverters. Power BJTs are being supplanted by FETs and IGBTs.
FET	(Field Effect Transistor) Conducts drain current when sufficient gate voltage is applied. Power FETs (nearly always enhancement-mode MOSFETs) have a parallel connected reverse diode by virtue of their construction. Ratings from ≈ 1 to ≈ 100 A and 30 up to 1000 V. Switching times are fast, from 50 or less up to 200 ns. The function applies to dc-dc conversion, where the FET is in wide use, and to inverters.
IGBT	(Insulated Gate Bipolar Transistor) A special type of power FET that has the function of a BJT with its base driven by a FET. Faster than a BJT of similar ratings, and easy to use. Ratings from 10 to 600 A, with voltages of 600 to 1700 V. The IGBT is popular in inverters from ≈ 1 to 100 kW or more. It is found almost exclusively in power electronics applications.
SCR	(Silicon Controlled Rectifier) A thyristor that conducts like a diode after a gate pulse is applied. Turns off only when current becomes zero. Prevents current flow until a pulse appears. Ratings from 10 up to more than 5000 A, and from 200 V up to 6 kV. Switching requires 1 to 200 μs. Widely used for controlled rectifiers. The SCR is found almost exclusively in power electronics applications, and is the most common member of the thyristor family.
GTO	(Gate Turn-Off Thyristor) An SCR that can be turned off by sending a negative pulse to its gate terminal. Can substitute for BJTs in applications where power ratings must be very high. The ratings approach those of SCRs, and the speeds are similar as well. Used in inverters rated >100 kW.
TRIAC	A semiconductor constructed to resemble two SCRs connected in reverse parallel. Ratings from 2 to 50 A and 200 to 800 V. Used in lamp dimmers, home appliances, and hand tools. Not as rugged as many other device types, but very convenient for many ac applications.
MCT	(MOSFET Controlled Thyristor) A special type of SCR that has the function of a GTO with its gate driven from a FET. Much faster than conventional GTOs, and easier to use. These devices are supplanting GTOs in some application areas.

> flow and voltage polarity. The *ideal diode* is one example of a restricted switch.

The diode always permits current flow in one direction, while blocking flow in the other. It therefore represents a *forward-conducting reverse-blocking* restricted switch, and operates in one quadrant on a graph of device current vs voltage. This FCRB function is automatic the two diode terminals provide all the necessary information for switch action. Other restricted switches require a third *gate* terminal to determine their state. Consider the polarity possibilities given in Table 1.2. Additional functions such as bidirectional-conducting reverse-blocking can be obtained simply by reverse connection of one of the five types in the table.

The quadrant operation shown in the table indicates polarities. For example, the current in a diode will be positive when on and the voltage will be negative when off. This means diode operation is restricted to the single quadrant comprising the upper vertical (current) axis and the left horizontal (voltage) axis. The other combinations appear in the table. Symbols for restricted switches can be built up by interpreting the diode's triangle as the current-carrying direction and the bar as the blocking direction. The five types can be drawn as in Table 1.2. Although the symbols are used infrequently, they are valuable for showing the polarity behavior of switching devices. A circuit drawn with restricted switches represents an idealized power converter.

Restricted switch concepts guide the selection of devices. For example, consider an inverter intended to deliver ac load current from a dc voltage source. A switch matrix built to perform this function must be able to manipulate ac current and dc voltage. Regardless of the physical arrangement of the matrix, we would expect bidirectional-conducting forward-blocking switches to be useful for this conversion. This is a correct result: Modern inverters operating from dc voltage sources are built with FETs or with IGBTs arranged with reverse-parallel diodes. As new power devices are introduced to the market, it is straightforward to determine what types of converters will use them.

1.5.4 Resolving the Software Problem Switching Functions

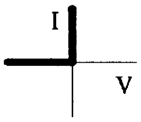
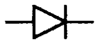
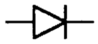
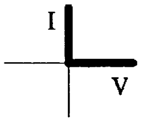
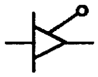
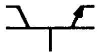
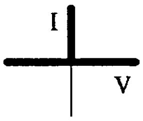
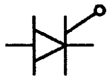
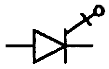
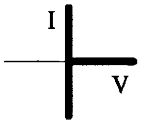
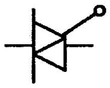
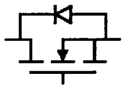
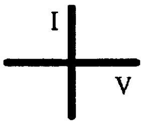
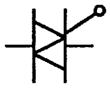
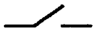
The physical $m \times n$ switch matrix can be associated with a mathematical $m \times n$ *switch state matrix*. Each element of this matrix, called a *switching function*, shows whether the corresponding physical device is on or off.

> **DEFINITION** A *switching function* $q(t)$ has a value of unity when the corresponding physical switch is on and 0 when it is off. Switching functions are discrete-valued functions of time, and control of switching devices can be represented with them.

Figure 1.15 shows a typical switching function. It is periodic, with period T, representing the most likely repetitive switch action in a power converter. For convenience, it is drawn on a relative time scale that begins at 0 and draws out the square wave period-by-period. The actual timing is arbitrary, so the center of the first pulse is defined as a specified time t_0 in the figure. In many converters, the switching function is generated as an actual control voltage signal that might drive the gate of either a MOSFET or some other semiconductor switching device.

The timing of switch action is the only alternative for control of a power converter. As switch action can be repre-

TABLE 1.2 The types of restricted switches

Action	Device	Quadrants	Restricted Switch Symbol	Device Symbol
Carries current in one direction, blocks in the other (forward-conducting reverse-blocking)	Diode			
Carries or blocks current in one direction (forward-conducting, forward-blocking)	BJT			
Carries in one direction or blocks in both directions (forward-conducting, bidirectional-blocking)	GTO			
Carries in both directions, but blocks only in one direction (bidirectional-carrying, forward-blocking)	FET			
Fully bidirectional	Ideal switch			

sented with a discrete-valued switching function, the timing can be represented within the switching function framework. Based on Fig. 1.15, a generic switching function can be characterized completely with three parameters:

1. The *duty ratio D* is the fraction of time during which the switch is on. For control purposes the pulse width can be adjusted to achieve a desired result. We can term this adjustment process *pulse-width modulation* (PWM), perhaps the most important process for implementing control in power converters.
2. The frequency $f_{\text{switch}} = 1/T$ (with radian frequency $\omega = 2\pi f_{\text{switch}}$) is most often constant, although not in all applications. For control purposes, frequency can be adjusted. This is unusual in power converters because the operating frequencies are often dictated by the application.
3. The time delay t_0 or phase $\phi_0 = \omega t_0$. Rectifiers often make use of *phase control* to provide a range of adjustment. A few specialized ac-ac converter applications use phase modulation.

With just three parameters to vary, there are relatively few possible ways to control any power electronic circuit. The dc-dc converters usually rely on duty ratio adjustment (PWM) to alter their behavior. Phase control is common in controlled rectifier applications. Pulse-width modulation is used formally for many types of inverters.

Switching functions are very powerful tools for general representation of converter action [7]. The most widely used

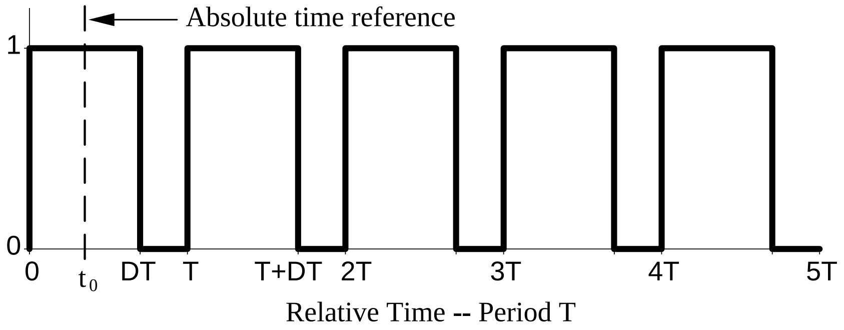


FIGURE 1.15 A generic switching function with period T, durty ratio D, and time reference t_0.

control approaches derive from averages of switching functions [2, 8]. Their utility comes from their application in writing circuit equations. For example, in the boost converter of Fig. 1.9, the loop and node equations change depending on which switch is acting at a given moment. The two possible circuit configurations each have distinct equations. Switching functions allow them to be combined. By assigning switching functions $q_1(t)$ and $q_2(t)$ to the left and right switching devices, respectively, we obtain

$$q_1\left(V_{\text{in}} - L\frac{di_L}{dt} = 0\right),\ q_1\left(C\frac{dv_C}{dt} + \frac{v_C}{R} = 0\right),\ \text{left switch on}$$

$$q_2\left(V_{\text{in}} - L\frac{di_L}{dt} = v_C\right),\ q_2\left(C\frac{dv_C}{dt} + \frac{v_C}{R} = i_L\right),\ \text{right switch on} \tag{1.9}$$

Because the switches alternate, and the switching functions must be 0 or 1, these sets of equations can be combined to give

$$V_{\text{in}} - L\frac{di_L}{dt} = q_2 v_C, \quad C\frac{dv_C}{dt} + \frac{v_C}{R} = q_2 i_L \tag{1.10}$$

The combined expressions are simpler and easier to analyze than the original equations.

For control purposes, the average of equations such as (1.10) often proceeds with the replacement of switching functions q with duty ratios d. The discrete time action of a switching function thus will be represented by an average duty cycle parameter. Switching functions, the advantages gained by averaging, and control approaches such as PWM are discussed at length in several chapters in this handbook.

1.5.5 Resolving the Interface Problem Lossless Filter Design

Lossless filters for power electronics applications are sometimes called smoothing filters [9]. In applications in which dc outputs are of interest, such filters are commonly implemented as simple lowpass LC structures. The analysis is facilitated because in most cases the residual output waveform, termed ripple, has a known shape. Filter design for rectifiers or dc-dc converters is a question of choosing storage elements large enough to keep ripple low, but not so large that the whole circuit becomes unwieldy or expensive.

Filter design is more challenging when ac outputs are desired. In some cases, this is again an issue of lowpass filter design. In many applications, lowpass filters are not adequate to meet low noise requirements. In this situation, active filters can be used. In power electronics, the term *active filter* refers to lossless switching converters that actively inject or remove energy moment-by-moment to compensate for distortion. The circuits (discussed elsewhere in this handbook) are not related to the linear active filter op-amp circuits used in analog signal processing. In ac cases, there is a continuing opportunity for innovation in filter design.

1.6 Summary

Power electronics is the study of electronic circuits for the control and conversion of electrical energy. The technology is a critical part of our energy infrastructure, and supports almost all important electrical applications. For power electronics design, we consider only those circuits and devices that, in principle, introduce no loss and can achieve near-perfect reliability. The two key characteristics of high efficiency and high reliability are implemented with switching circuits, supplemented with energy storage. Switching circuits in turn can be organized as switch matrices. This facilitates their analysis and design.

In a power electronic system, the three primary challenges are the hardware problem of implementing a switching matrix, the software problem of deciding how to operate that matrix, and the interface problem of removing unwanted distortion and providing the user with the desired clean power source. The hardware is implemented with a few special types of power semiconductors. These include several types of transistors, especially MOSFETs and IGBTs, and several types of thyristors, especially SCRs and GTOs. The software problem can be represented in terms of switching functions. The frequency, duty ratio, and phase of the switching functions are available for operational purposes. The interface problem is addressed by means of lossless filter circuits. Most often, these are lossless LC passive filters to smooth out ripple or reduce harmonics. More recently, active filter circuits have been applied to make dynamic corrections in power conversion waveforms.

Improvements in devices and advances in control concepts have led to steady improvements in power electronic circuits and systems. This is driving tremendous expansion of their application. Personal computers, for example, would be unwieldy and inefficient without power electronic dc supplies. Portable communication devices and computers would be impractical. High-performance lighting systems, motor controls, and a wide range of industrial controls depend on power electronics. In the near future, we can expect strong growth in automotive applications, in dc power supplies for communication systems, in portable applications, and in high-end converters for advanced microprocessors. During the next generation, we will reach a time when almost all electrical energy is processed through power electronics somewhere in the path from generation to end use.

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2

The Power Diode

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2.1 Diode as a Switch

Among all the static switching devices used in power electronics (PE), the power diode is perhaps the simplest. Its circuit symbol, shown in Fig. 2.1, is a two terminal device, and with terminal A known as the anode and terminal K known as the cathode. If terminal A experiences a higher potential compared to terminal K, the device is said to be forward biased and a forward current (I_F) will flow through the device in the direction as shown. This causes a small voltage drop across the device (<1 V), which under ideal conditions is usually ignored. By contrast, when a diode is reverse biased, it does not conduct and the diode then experiences a small current flowing in the reverse direction called the leakage current. Both forward voltage drop and leakage current are ignored in an ideal diode. In PE applications a diode is usually considered to be an ideal static switch.

The characteristics of a practical diode depart from the ideals of zero forward and infinite reverse impedance, as shown in Fig. 2.2a. In the forward direction, a potential barrier associated with the distribution of charges in the vicinity of the junction, together with other effects, leads to a voltage drop. In the case of silicon this is in the range of 1 V for currents in the normal range. In the reverse direction, within the normal voltage operating range, a very small current flows that is largely independent of the voltage. For practical purposes the static characteristics are often represented as shown in Fig. 2.2b. In Fig. 2.2b the forward characteristic is expressed as a threshold voltage V_O with a linear incremental or slope resistance *r*. The reverse characteristic remains the same over the range of possible leakage currents irrespective of voltage within the normal working range.

2.2 Some Properties of PN Junction

From the forward and reverse-biased condition characteristics, one notices that when the diode is forward biased, current rises rapidly as the voltage is increased. Current in the reverse-biased region is significantly small until the breakdown voltage of the diode is reached. Once the applied voltage is over this limit, the current will increase rapidly to a very high value limited only by an external resistance.

DC Diode parameters. The most important are the following:

- ***Forward voltage*** V_F is the voltage drop of a diode across *A* and *K* at a defined current level when it is forward biased.
- ***Breakdown voltage*** V_B is the voltage drop across the diode at a defined current level when it is beyond reverse-biased level. This is known as avalanche.
- ***Reverse current*** I_R is the current at a particular voltage, and which is below the breakdown voltage.

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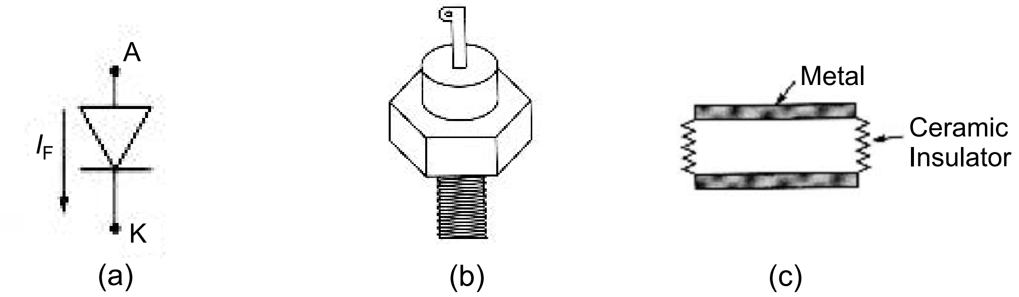


FIGURE 2.1 Power diode: (a) symbol; (b) and (c) types of packaging.

AC Diode parameters. Very common are the following:

- ***Forward recovery time*** t_{FR} is the time required for the diode voltage to drop to a particular value after the forward current starts to flow.
- ***Reverse recovery time*** t_{RR} is the time interval between the application of reverse voltage and the reverse current dropped to a particular value as shown in Fig. 2.2. Parameter t_a is the interval between the zero crossing of the diode current and when it becomes I_{RR}. On the other hand, t_b is the time interval from the maximum reverse recovery current to ≈ 0.25 of I_{rr}. The ratio of the two parameters t_a and t_b is known as the softness factor SF. Diodes with abrupt recovery characteristics are used for high-frequency switching. See Fig. 2.3 for soft and abrupt recovery.

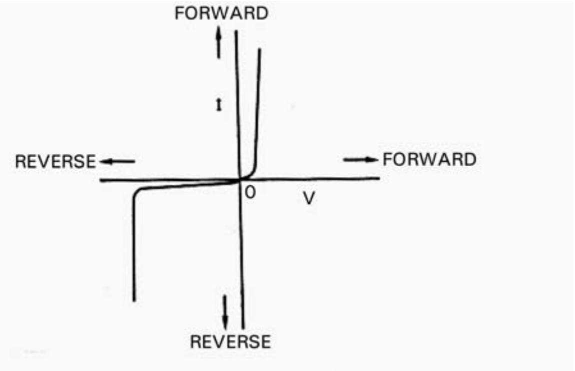


FIGURE 2.2a Typical static characteristic of a power diode (forward and reverse have different scale).

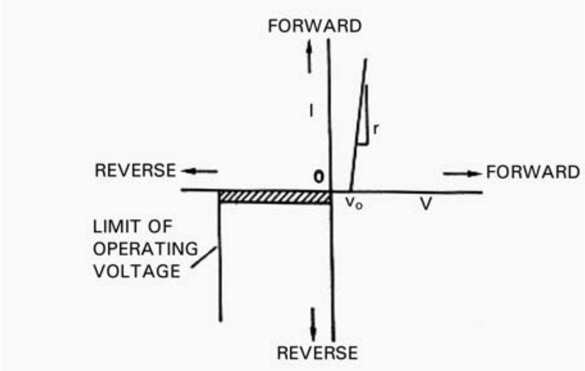


FIGURE 2.2b Practical representation of the static characteristic of a power diode.

In practice, a design engineer frequently needs to calculate reverse recovery time in order to evaluate the possibility of high-frequency switching. As a rule of thumb, the lower t_{rr} is, the faster the diode can be switched [1].

$$t_{rr} = t_a + t_b \tag{2.1}$$

If t_b is negligible compared to t_a (which commonly occurs), then the following expression is valid:

$$t_{rr} = \sqrt{\frac{2Q_{RR}}{di/dt}}$$

from which the reverse recovery current

$$I_{rr} = \sqrt{\frac{di}{dt} 2Q_{RR}}$$

where Q_{RR} is the storage charged, and can be calculated from the area enclosed by the path of the recovery current.

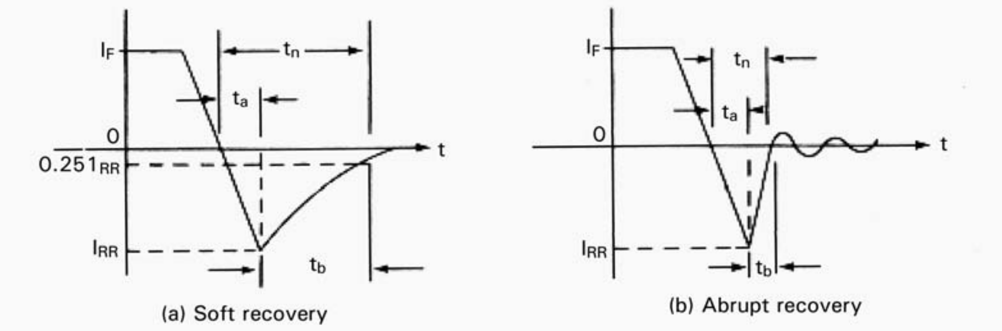
Example 2.1 The manufacturer of a selected diode gives the rate of fall of the diode current $di/dt = 20\,\text{A}/\mu\text{s}$, and a reverse recovery time of $t_{rr} = 5\,\mu\text{s}$. What value of peak reverse current do you expect?

Solution. The peak reverse current is given as:

$$I_{rr} = \sqrt{\frac{di}{dt} 2Q_{RR}}$$

The storage charge Q_{RR} is calculated as $Q_{rr} = \frac{1}{2} di/dt t_{rr}^2 = 1/2 \times 20\ \text{A}/\mu\text{s} \times (5 \times 10^{-6})^2 = 50\ \mu\text{C}$. Hence

$$I_{rr} = \sqrt{20 \frac{a}{\mu s} \times 2 \times 50\ \mu C} = 44.72\ A$$



(a) Soft recovery

(b) Abrupt recovery

FIGURE 2.3 Diode reverse recovery process with various softness factors. (a) Soft recovery; and (b) abrupt recovery.

Diode Capacitance C_D is the net diode capacitance including the junction (C_J) plus package capacitance (C_P).

In high-frequency pulse switching a parameter known as transient thermal resistance is of vital importance because it indicates the instantaneous junction temperature as a function of time under constant input power.

2.3 Common Diode Types

Depending on their applications, diodes can be segregated into the following major divisions:

Small Signal Diode. These are the semiconductor devices used most often in a wide variety of applications. In general purpose applications, they are used as a switch in rectifiers, limiters, capacitors, and in wave shaping. The common diode parameters a designer needs to know include forward voltage, reverse breakdown voltage, reverse leakage current, and recovery time.

Silicon Rectifier Diode. These are the diodes that have high forward-current carrying capability, typically up to several hundred amperes. They usually have a forward resistance of only a fraction of an ohm while their reverse resistance is in the megaohm range. Their primary application is in power conversion, such as for power supplies, UPS, rectifiers/inverinverters etc. In case of current exceeding the rated value, their case temperature will rise. For stud mounted diodes, their thermal resistance is between 0.1 to 1° C/W.

Zener Diode. Its primary applications are in the voltage reference or regulation. However, its ability to maintain a certain voltage depends on its temperature coefficient and impedance. The voltage reference or regulation application of Zener diodes are based on their avalanche properties. In the reverse-biased mode, at a certain voltage the resistance of these devices may suddenly drop. This occurs at the Zener voltage V_X, a parameter the designer knows beforehand.

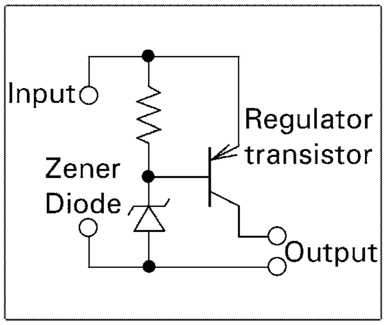


FIGURE 2.4 Voltage regulator with a Zener diode for reference.

Figure 2.4 shows a circuit in which a Zener diode is used to control the reference voltage of a linear power supply. Under normal operating conditions, the transistor will transmit power to the load (output) circuit. The output power level will depend on the transistor base current. A very high base current will impose a large voltage across the Zener and it may attain Zener voltage V_X, at which point it will crush and limit the power supply to the load.

Photodiode. When a semiconductor junction is exposed to light, photons generate hole-electron pairs. When these charges diffuse across the junction, they produce photo current. Hence this device acts as a source of current that increases with the intensity of light.

Light-Emitting Diode (LED). Power diodes used in PE circuits are high-power versions of the commonly used devices employed in analog and digital circuits. They are manufactured in many varieties and ranges. The current rating can be from a few amperes to several hundreds while the voltage rating varies from tens of volts to several thousand volts.

2.4 Typical Diode Ratings

2.4.1 Voltage Ratings

For power diodes, a data sheet will give two voltage ratings. One is the repetitive peak inverse voltage (V_{RRM}) and the other is the nonrepetitive peak inverse voltage. The nonrepetitive voltage (V_{RM}) is the diode's capability to block a reverse voltage that may occur occasionally due to an overvoltage surge. On the other hand, repetitive voltage is applied on the diode in a sustained manner. To understand this, let us look at the circuit in Fig. 2.5a.

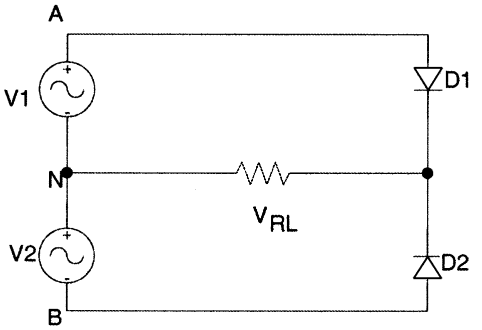


FIGURE 2.5 (a) The circuit.

Example 2.2. Two equal source voltages of 220 V peak and phase-shifted from each other by 180° supply a common load: (a) Show the load voltage; (b) describe when diode $D1$ will experience V_{RRM}; and (c) determine the V_{RRM} magnitude considering a safety factor of 1.5.

Solution. (a)The Input voltages, load voltage, and the voltage across D1 when it is not conducting (V_{RRM}) are shown in Fig. 2.5b.

(b) Diode D1 will experience V_{RRM} when it is not conducting. This happens when the applied voltage V1 across it is in the negative region (from 70 to 80 ms as shown in Fig. 2.5b) and consequently the diode is reverse biased. The actual ideal voltage across it is the peak value of the two input voltages 220 × 2 = 440 V. This is because when $D1$ is not conducting, $D2$ is. Hence, V_{an}, V_{bn} is also applied across it because $D2$ is practically shorted.

(c) The $V_{RRM} = 440$ V is the value under ideal circumstances. In practice, however, higher voltages may occur due to stray circuit inductances and/or transients due to the reverse recovery of the diode. These are hard to estimate. Hence, a design engineer would always use a safety factor to cater to these overvoltages, that is, a diode with a $220 \times 2 \times 1.5 = 660$ V rating.

2.4.2 Current Ratings

Power diodes are usually mounted on a heat sink. This effectively dissipates the heat arising due to continuous conduction. Current ratings are estimated based on temperature rise considerations. The data sheet of a diode normally specifies three different current ratings. These are: (1) the average current; (2) the rms current; and (3) the peak current. A design engineer must ensure that each of these values are never exceeded. To do that, the actual current (average, rms, and peak) in the circuit must be evaluated either by calculation, simulation, or measurement. These values must be checked against the ones given in the data sheet for that selected diode. The calculated values must be less than or equal to the data sheet values. The following example shows this technique.

Example 2.3 The current waveform passing through a diode switch in a switch-mode power-supply application is shown in Fig. 2.6. Find the average, rms and peak currents.

Solution. The current pulse duration is shown to be 0.2 ms within a period of 1 ms and with a peak amplitude of 50 A. Hence the required currents are:

$$I_{\text{average}} = 50 \times \frac{0.2}{1} = 10 \text{ A}$$

$$I_{\text{rms}} = \sqrt{50^2 \times \frac{0.2}{1}} = 22.36 \text{ A}$$

$$I_{\text{rms}} = 50 \text{ A}$$

Sometimes, a surge current rating and its permissible duration are also given in a data sheet. For protection of diodes and other semiconductor devices, a fast acting fuse is required.

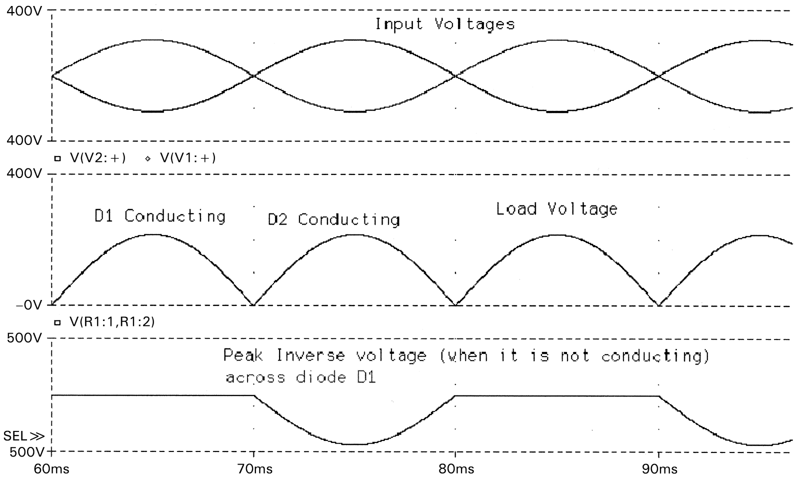


FIGURE 2.5 (b) The waveforms.

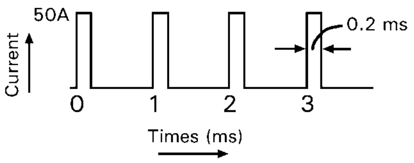


FIGURE 2.6 The current waveform in Example 2.3.

These fuses are selected based on their I^2t rating, which is normally specified in a data sheet for a selected diode.

2.5 Snubber Circuits for Diode

Snubber circuits are essential for diodes used in switching circuits. It can save a diode from overvoltage spikes, which may arise during the reverse recovery process. A very common snubber circuit for a power diode consists of a capacitor and a resistor connected in parallel with the diode as shown in Fig. 2.7.

When the reverse recovery current decreases, the capacitor by virtue of its property will try to retain the voltage across it, which is approximately the voltage across the diode. The resistor, on the other hand, will help to dissipate some of the energy stored in the inductor, which forms the I_{rr} loop. The dv/dt across a diode can be calculated as:

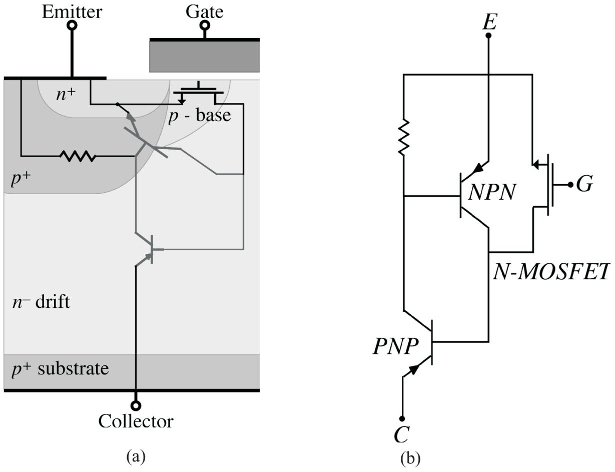
$$\frac{dv}{dt} = \frac{0.632 * V_S}{\tau} = \frac{0.632 * V_S}{R_S * C_S} \tag{2.2}$$

where V_S is the voltage applied across the diode.

Usually the dv/dt rating of a diode is given in manufacturer datasheets. By knowing dv/dt and R_S, one can choose the value of the snubber capacitor C_S. Here R_S can be calculated from the diode reverse recovery current:

$$R_S = \frac{V_S}{I_{rr}} \tag{2.3}$$

The designed dv/dt value must always be equal or lower than the dv/dt value found from the data sheet.



(a) (b)

FIGURE 2.7 A typical snubber circuit.

2.6 Series and Parallel Connection of Power Diodes

For specific applications when the voltage or current rating of a chosen diode is not enough to meet the designed rating, diodes can be connected in series or in parallel. Connecting them in series will give the structure a high voltage rating that may be necessary for high-voltage applications [2]. However, one must ensure that the diodes are properly matched, especially in terms of their reverse recovery properties. Otherwise, during reverse recovery there may be large voltage unbalances between the series-connected diodes. Additionally, due to differences in reverse recovery times, some diodes may recover from the phenomenon earlier than the others, thereby causing them to bear the full reverse voltage. All of these problems can effectively be overcome by connecting a bank of a capacitor and a resistor in parallel with each diodes as shown in Fig. 2.8.

If a selected diode cannot match the required current rating, one may connect several diodes in parallel. In order to ensure equal current sharing, the designer must choose diodes with the same forward voltage drop properties. It is also important to ensure that the diodes are mounted on similar heat sinks and are cooled (if necessary) equally. This will affect the temperatures of the individual diodes, which in turn may change the diode forward characteristics.

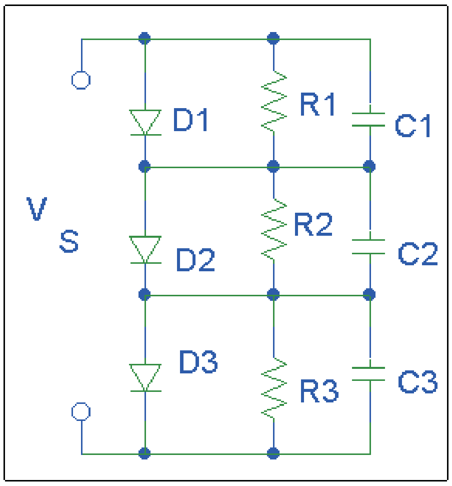


FIGURE 2.8 Series-connected diodes with necessary protection.

Tutorial 2.1 Reverse Recovery and Overvoltages

Figure 2.9 shows a simple switch mode power supply. The switch (1-2) is closed at $t = 0\,\mathrm{S}$. When the switch is open, a freewheeling current $I_F = 20\,\mathrm{A}$ flows through the load (RL), freewheeling diode (DF), and the large load circuit inductance (LL). The diode reverse recovery current is 20 A and it then

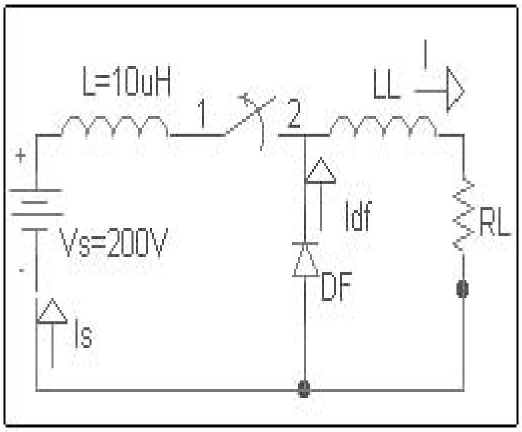


FIGURE 2.9 A simple switch mode power supply with freewheeling diode.

decays to zero at the rate of 10 A/μS. The load is rated at 10 Ω and the forward on-state voltage drop is neglected.

(a) Draw the current waveform during the reverse recovery (I_{rr}) and find its time (t_{rr}).
(b) Calculate the maximum voltage across the diode during this process (I_{rr}).

Solution. (a) A typical current waveform during reverse recovery process is shown in Fig. 2.10 for an ideal diode.

When the switch is closed, the steady-state current is $I_{SS} = 200\ \text{V}/10\ \Omega = 20\ \text{A}$, because under the steady-state condition the inductor is shorted. When the switch is open, the reverse recovery current flows in the right-hand side loop consisting of LL, RL, and DF. The load inductance LL is assumed to be shorted. Hence, when the switch is closed, the loop equation is [3]:

$$V = L\frac{di_S}{dt} \quad \text{from which} \quad \frac{di_S}{dt} = \frac{V}{L} = \frac{200}{10} = 20\ \text{A}/\mu\text{S}$$

At the moment the switch is open, the same current keeps flowing in the right-hand side loop. Hence,

$$\frac{di_d}{dt} = -\frac{di_S}{dt} = -20\ \text{A}/\mu\text{S}$$

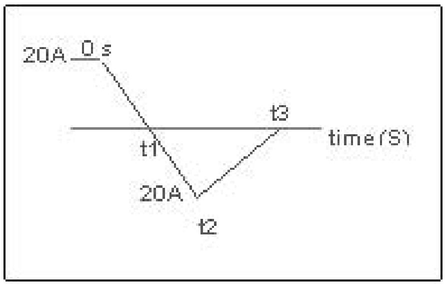


FIGURE 2.10 Current through the freewheeling diode during reverse recovery.

from time zero to time t_1 the current will decay at a rate of 20 A/S and will be zero at $t_1 = 20/20 = 1/\mu$S. The reverse recovery current starts at this point and according to the given condition becomes 20 A at t_2. From this point on, the rate of change remains unchanged at 20 A/μS. Period $t_2 - t_1$ is found:

$$t_2 - t_1 = \frac{20\ A}{20\ \text{A}/\mu\text{S}} = 1\ \mu\text{S}$$

From t_2 to t_3 the current decays to zero at the rate of 20 A/μS. The required time is

$$t_3 - t_2 = \frac{20\ A}{10\ \text{A}/\mu\text{S}} = 2\ \mu\text{S}$$

Hence the actual *reverse recovery time*: $t_{rr} = t_3 - t_1 = (1 + 1 + 2) - 1 = 3\ \mu$S.

(b) The diode experiences the maximum voltage only when the switch is open. This is due to both the source voltage 200 V and the newly formed voltage caused by the change in current through inductor *L*. The voltage across the diode,

$$V_D = -V + L\frac{di_S}{dt} = -200 + (10 \times 10^{-6})(-20 \times 10^6)$$
$$= -400\ \text{V}$$

Tutorial 2.2 Ideal Diode Operation, Mathematical Analysis and PSPICE Modelling

This tutorial illustrates the operation of an ideal diode circuit. Most of the power electronic applications operate at a relatively high voltage and, in such cases, the voltage drop across the power diode is usually small. It is quite often justifiable to use the ideal diode model. An ideal diode has a zero conduction drop when it is forward-biased and has zero current when it is reverse-biased. The equations and the analysis presented here are based on an ideal diode model.

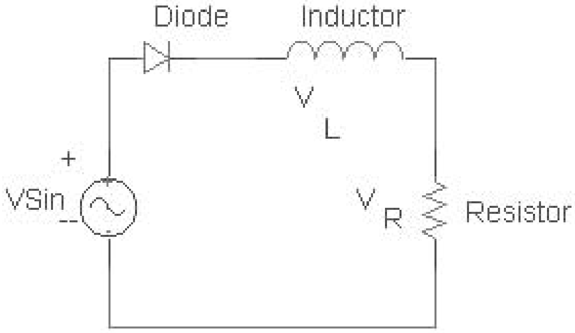


FIGURE 2.11 Circuit diagram.

Circuit Operation A circuit with a single diode and a very common RL load is shown in Fig. 2.11. The source V_S is an alternating sinusoidal source. Suppose $V_S = E_m \sin(\omega t)$. V_S is positive when $0 < wt < \pi$, and is negative when $\pi < \omega t < 2\pi$. When V_S starts to become positive, the diode begins conducting and the positive source keeps the diode in conduction until ωt reaches π radians. At that instant (defined by $\omega t = \pi$ radians), the current through the circuit is not zero and there is some energy stored in the inductor. The voltage across an inductor is positive when the current through it is on the increase and it becomes negative when the current through it tends to fall. When the voltage across the inductor is negative, it is in such a direction as to forward bias the diode. The polarity of voltage across the inductor is as shown in Figs. 2.12 and 2.13.

When V_S changes from a positive to a negative value, there is current through the load at the instant $\omega t = \pi$ radians and the diode continues to conduct until the energy stored in the inductor becomes zero. After that the current tends to flow in the reverse direction and the diode blocks conduction. The entire applied voltage now appears across the diode.

Circuit Analysis The expression for the current through the diode can be obtained from the following mathematical analysis [7]. It is assumed that the current flows for $0 < \omega t < \beta$, where $\beta > \pi$, when the diode conducts, and the driving function for the differential equation is the sinusoidal function defining the source voltage. During the period defined by $\beta < \omega t < 2\pi$, the diode blocks the current and acts as an open switch. For this period, there is no equation defining the behavior of the circuit. For $0 < \omega t < \beta$, Eq. (2.4) applies [7].

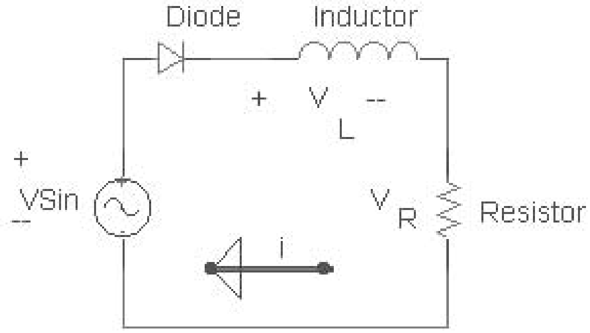


FIGURE 2.12 Current rising, $0 < \omega t < \pi/2$.

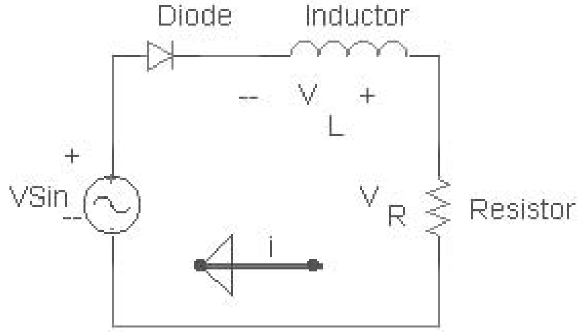


FIGURE 2.13 Current falling, $\pi/2 < \omega t < \pi$.

$$L\frac{di}{dt} + R^* i = E^* \sin(\theta), \text{ where } -0 \leq \theta \leq \beta \tag{2.4}$$

$$L\frac{di}{dt} + R^* i = 0 \tag{2.5}$$

$$\omega L\frac{di}{d\theta} + R^* i = 0 \tag{2.6}$$

$$i(\theta) = A^* e\frac{-R\theta}{\omega L}$$

Assuming a linear differential equation, the solution is found in two parts. The homogeneous equation is defined by Eq. (2.5). It is preferable to express the equation in terms of the angle θ instead of t. As $\theta = \omega t$, then $d\theta = \omega.dt$. Then Eq. (2.5) is converted to Eq. (2.6). Equation (2.7) is the solution to this homogeneous equation and is called the complementary integral.

The value of constant A in the complementary solution is to be calculated. The particular solution is the steady-state response and Eq. (2.8) expresses it. The steady-state response is the current that would flow in steady-state in a circuit that contains only the source, the resistor, and the inductor as shown in the circuit in Fig. 2.11, where the only element missing is the diode. This response can be obtained using the differential equation, the Laplace transform, or the ac sinusoidal circuit analysis. The total solution is the sum of both the complementary and the particular solution. It is shown in Eq. (2.9). The value of A is obtained using the initial condition. As the diode starts conducting at $\omega t = 0$ and the current starts building up from zero, $i(0) = 0$. The value of A is expressed by Eq. (2.10).

Once the value of A is found, the expression for current is known. After evaluating A, current can be evaluated at different values of ωt, starting from $\omega t = \pi$. As wt increases, the current continues to decrease. For some value of ωt, say β, the current would be zero. If $\omega t > \beta$, the current would drop to a negative value. As the diode blocks current in the reverse direction, the diode stops conducting when ωt is reached. Then an expression for the average output voltage can be obtained. Because the average voltage across the inductor has to be zero, the average voltage across the resistor and at the cathode of the diode are the same. This average value can be obtained as shown in Eq. (2.11).

$$i(\theta) = \left(\frac{E}{Z}\right)\sin(\omega t - \alpha) \tag{2.8}$$

where $\alpha = a\tan\left(\frac{\omega l}{R}\right)$, and $Z^2 = R^2 + \omega l^2$

$$i(\theta) = A^{*}e\left(\frac{-R\theta}{\omega l}\right) + \frac{E}{Z}\sin(\theta - \alpha) \tag{2.9}$$

$$A = \left(\frac{E}{Z}\right)\sin(\alpha) \tag{2.10}$$

Hence, the average output voltage:

$$V_{OAVG} = \frac{E}{2\pi}\int_0^{\beta}\sin\theta.d\theta = \frac{E}{2\pi}{*}[1 - \cos(\beta)] \tag{2.11}$$

PSPICE Modelling: For modelling the ideal diode using PSPICE, the circuit used is shown in Fig. 2.14. Here the nodes are numbered. The ac source is connected between nodes 1 and 0. The diode is connected between nodes 1 and 2 and the inductor links nodes 2 and 3. The resistor is connected from 3 to the reference node, that is, node 0.

The PSPICE program in text form is presented here:

```
*Half-wave rectifier with RL load
*An exercise to find the diode current
VIN 1 0 sin(0 100 V 50 Hz)
D1 1 2 Dbreak
L1 2 3 10 mH
R1 3 0 5 Ω
.MODEL Dbreak D(IS=10N N=1 BV=1200 IBV=10E-3
VJ=0.6)
.TRAN 10 μs 100 μs 60 μs 100 μs
.PROBE
.OPTIONS (ABSTOL=1N RELTOL=.01 VNTOL=1MV)
.END
```

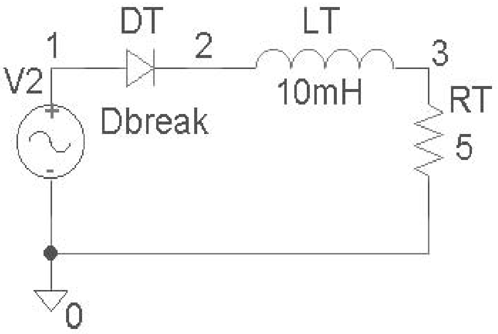


FIGURE 2.14 PSPICE circuit to study the diode R-L circuit.

The diode is characterized using the MODEL statement. The TRAN statement controls the transient operation for a period of 100 ms at an interval of 10 ms. The OPTIONS statement sets limits for tolerances. The output can be viewed on the screen because of the PROBE statement. A snapshot of various voltages/currents are presented in Fig. 2.15.

It is evident from Fig. 2.15 that the current lags the source voltage. This is a typical phenomenon in any inductive circuit and is associated with the energy storage property of the inductor. This property of the inductor causes the current to change slowly, governed by the time constant $\tau = \tan^{-1}(\omega l/R)$. Analytically, this is calculated by the expression in Eq. 2.8.

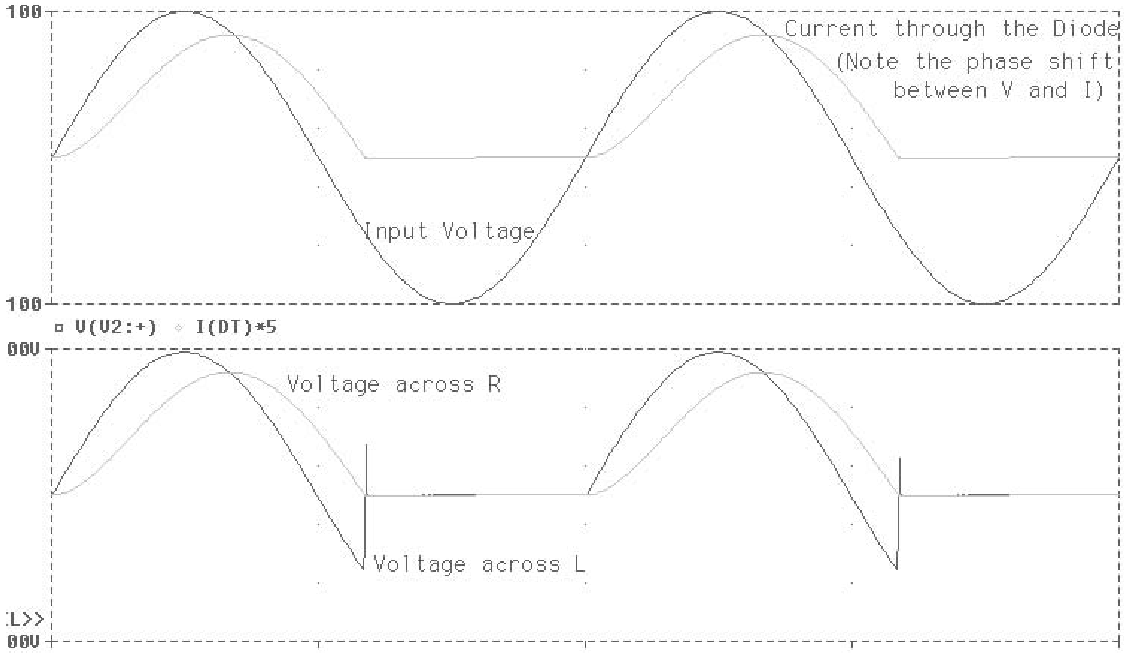


FIGURE 2.15 Voltage/current waveforms at various points in the circuit.

2.7 Typical Applications of Diodes

A. In rectification. Four diodes can be used to fully rectify an ac signal as shown in Fig. 2.16. Apart from other rectifier circuits, this topology does not require an input transformer. However, transformers are used for isolation and protection. The direction of the current is decided by two diodes conducting at any given time. The direction of the current through the load is always the same. This rectifier topology is known as the bridge rectifier.

The average rectifier output voltage

$$V_{\mathrm{dc}} = \frac{2V_m}{\pi}$$

where V_m is the peak input voltage.

The rms rectifier output voltage

$$V_{\mathrm{rms}} = \frac{V_m}{\sqrt{2}}$$

This rectifier is twice as efficient as a single-phase rectifier.

B. For Voltage Clamping. Figure 2.17 shows a voltage clamper. The negative pulse of the input voltage charges the capacitor to its max. value in the direction shown. After charging, the capacitor cannot discharge because it is open circuited by the diode. Hence the output voltage,

$$V_o = V_m + V_i = V_m(1 + \sin(\omega t))$$

The output voltage is clamped between zero and 2 V_m.

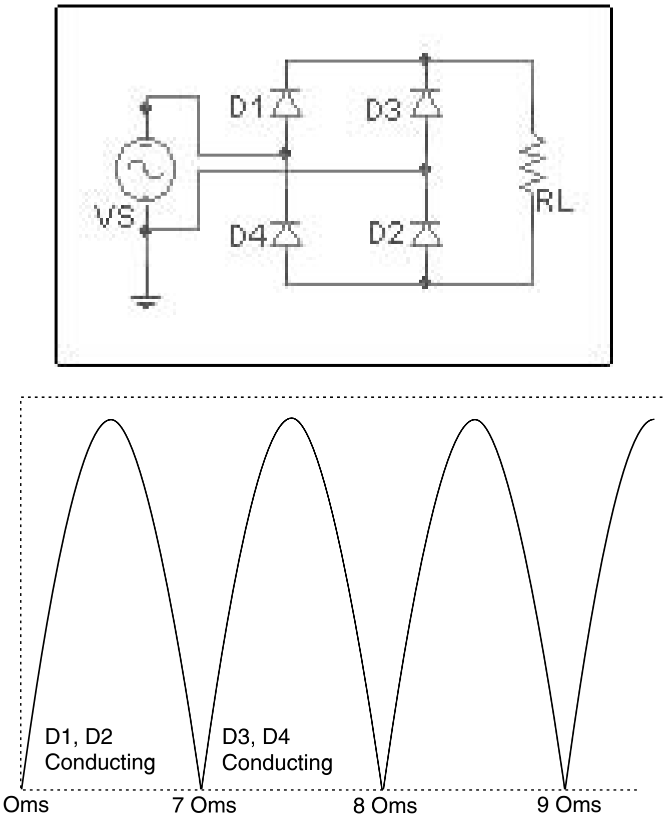


FIGURE 2.16 Full bridge rectifier and its output dc voltage.

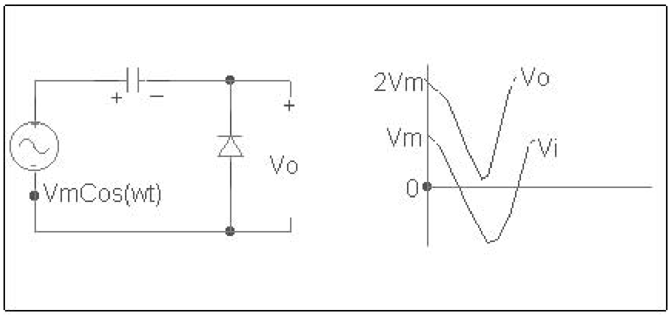


FIGURE 2.17 Voltage clamping with diode.

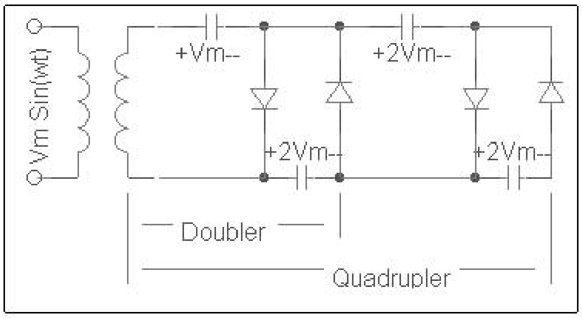


FIGURE 2.18 Voltage doubler and quadrupler circuit.

C. As Voltage Multiplier By connecting diodes in a predetermined manner, an ac signal can be doubled, tripled, and even quadrupled. This is shown in Fig. 2.18. The circuit will yield a dc voltage equal to 2 V_m. The capacitors are alternately charged to the maximum value of the input voltage.

2.8 Standard Datasheet for Diode Selection

In order for a designer to select a diode switch for specific applications, the following Tables and standard test results can be used. A power diode is chosen primarily based on forward current (I_F) and the peak inverse (V_{RRM}) voltage [5]. For example, the designer chose the diode type $V30$ from Table 2.1 because it closely matches his/her calculated values of I_F and V_{RRM} without exceeding those values. However, if for some reason only the V_{RRM} matches but the calculated value of I_F

comes in at a higher figure, one should select diode H14, and so on. A similar concept is used for V_{RRM}.

In addition to the forementioned diode parameters, one should also calculate parameters such as the peak forward voltage, reverse recovery time, case and junction temperatures etc. and check them against the datasheet values. Some of these datasheet values are provided in Table 2.2 for the selected diode *V*30. Figures 2.19–2.21 give the standard experimental relationships between voltages, currents, and power and case temperatures for our selected *V*30 diode. These characteristics help a designer to understand the safe operating range for the diode, and to make a decision as to whether or not a snubber or a heatsink should be used. If one is particularly interested in the actual reverse recovery time measurement, the circuit given in Fig. 2.22 can be constructed and experimented upon.

2.8.1 General-Use Rectifier Diodes

TABLE 2.1 Diode election based on average forward current $I_{F(avg)}$, and peak inverse voltage V_{RRM} [4]

$I_{F(avg)}$ (A)	V_{RRM} (V) Type	50	100	200	300	400	500	600	800	1000	1300	1500
0.4	*V*30	–	–	–	–	–	–	–	yes	yes	yes	yes
1.0	*H*14	–	yes	yes	yes	yes	yes	yes	yes	yes	–	–
1.1	*V*06	–	–	yes	–	yes	–	yes	yes	–	–	–
1.3	*V*03	–	–	yes	–	yes	–	yes	yes	–	–	–
2.5	*U*05	–	yes	yes	–	yes	–	yes	yes	–	–	–
3.0	*U*15	–	yes	yes	–	yes	–	yes	yes	–	–	–

Used with permission, [7].

TABLE 2.2 Details of diode for diode *V*30 selected from Table 2.1

Absolute maximum ratings[a,b]

Item	Type		V30J	V30L	V30M	V30N
Repetitive Peak reverse Voltage	V_{RRM}	V	800	1000	1300	1500
Nonrepetitive Peak Reverse Voltage	V_{RSM}	V	1000	1300	1600	1800
Average Forward Current	$I_{F(AV)}$	A	0.4 (Single-phase, half sine wave 180° conduction TL = 100°C, Lead length = 10 mm)			
Surge(Nonrepetitive) Forward current	I_{FSM}	A	30 (Without PIV, 10 ms conduction, $T_j = 150$°C start)			
I^2t Limit Value	I^2t	A^2s	3.6 (Time = 2 ~ 10 ms, 1 = rms value)			
Operating Junction Temperature	T_j	°C	−50 ~ +150			
Storage Temperature	T_{stg}	°c]	−50 ~ +150			

---

[a] Lead mounting: lead temperature 300°C max. to 3.2 mm from body for 5 s. max.

[b] Mechanical strength: bending 90° × 2 cycles or 180° × 1 cycle, Tensile 2 kg, Twist 90° × 1 cycle.

TABLE 2.3 Characteristics ($T_L = 25$°C)

Item	Symbols	Units	Min.	Typ.	Max.	Test Conditions
Peak Reverse Current	I_{RRM}	μA	–	0.6	10	All class Rated V_{RRM}
Peak Forward Voltage	V_{FM}	V	–	–	1.3	$I_{FM} = 0.4$ Ap, single-phase, half sine wave 1 cycle
Reverse Recovery Time	*trr*	μs	–	3.0	–	$I_F = 22$ mA, $V_R = -15$ V
Steady-State Thermal Impedance	$R_{th(j-a)}$					
	$R_{th(j-1)}$	°C/W	–	–	80 50	Lead length=10 mm

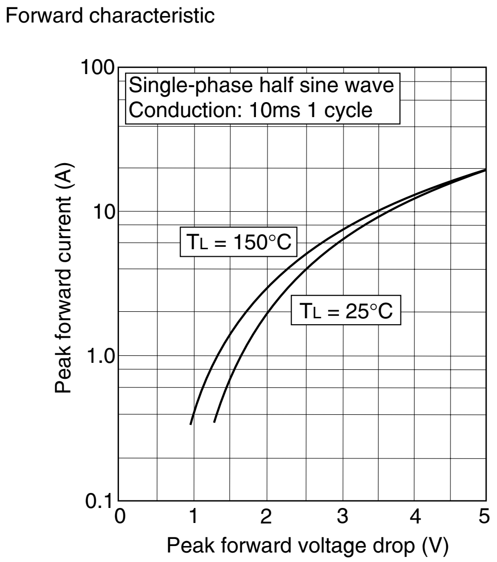


FIGURE 2.19 Variation of peak forward voltage drop with peak forward current.

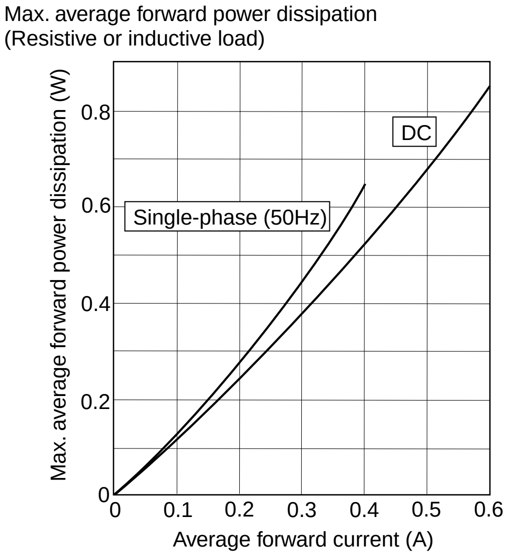


FIGURE 2.20 Variation of maximum forward power dissipation with average forward current.

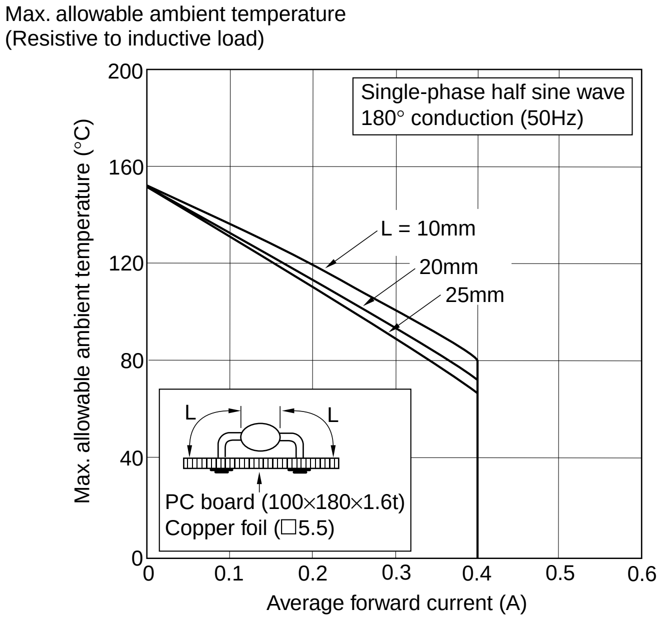


FIGURE 2.21 Maximum allowable case temperature with variation of average forward current.

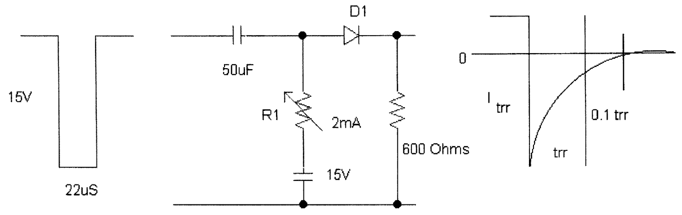


FIGURE 2.22 Reverse recovery time (t_{rr}) measurement.

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3

Thyristors

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3.1 Introduction

Thyristors are usually three-terminal devices with four layers of alternating *p*- and *n*-type material (i.e. three *p*-*n* junctions) in their main power handling section. In contrast to the linear relation that exists between load and control currents in a transistor, the thyristor is bistable. The control terminal of the thyristor, called the gate (G) electrode, may be connected to an integrated and complex structure as part of the device. The other two terminals, anode (A) and cathode (K), handle the large applied potentials (often of both polarities) and conduct the major current through the thyristor. The anode and cathode terminals are connected in series with the load to which power is to be controlled.

Thyristors are used to approximate ideal closed (no voltage drop between anode and cathode) or open (no anode current flow) switches for control of power flow in a circuit. This differs from low-level digital switching circuits that are designed to deliver two distinct small voltage levels while conducting small currents (ideally zero). Power electronic circuits must have the capability of delivering large currents and be able to withstand large externally applied voltages. All thyristor types are controllable in switching from a forward-blocking state (positive potential applied to the anode with respect to the cathode with correspondingly little anode current flow) into a forward-conduction state (large forward anode current flowing with a small anode-cathode potential drop). After switching from a forward-blocking state into the forward-conduction state, most thyristors have the characteristic that the gate signal can be removed and the thyristor will remain in its forward-conduction mode. This property, termed "latching," is an important distinction between thyristors and other types of power electronic devices. Some thyristors are also controllable in switching from forward-conduction back to a forward-blocking state. The particular design of a thyristor will determine its controllability and often its application.

Thyristors are typically used at the highest energy levels in power conditioning circuits because they are designed to handle the largest currents and voltages of any device technology (systems with voltages approximately greater than 1 kV or currents higher than 100 A). Many medium-power circuits (systems operating at <1 kV or 100 A) and particularly low-power circuits (systems operating <100 V or several amperes)

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generally make use of power bipolar transistors, power MOSFETs, or insulated gate bipolar transistors (IGBTs) as the main switching elements because of the relative ease in controlling them. The IGBT technology, however, continues to improve and multiple silicon die are commonly packaged together in a module. These modules are now replacing thyristors in 1–3 kV applications because of easier gate-drive requirements. Power diodes are used throughout all levels of power conditioning circuits and systems for component protection and wave-shaping.

A thyristor used in some ac power circuits (50 or 60 Hz in commercial utilities or 400 Hz in aircraft) to control ac power flow can be made to optimize internal power loss at the expense of switching speed. These thyristors are called phase-control devices because they are generally turned from a forward-blocking into a forward-conducting state at some specified phase angle of the applied sinusoidal anode-cathode voltage waveform. A second class of thyristors is used in association with dc sources or in converting ac power at one amplitude and frequency into ac power at another amplitude and frequency, and must generally switch on and off relatively quickly. A typical application for this second class of thyristors is that of converting a dc voltage or current into an ac voltage or current. A circuit that performs this operation is often called an inverter, and the associated thyristors used are referred to as inverter thyristors.

There are four major types of thyristors: *i*) silicon-controlled rectifier (SCR); *ii*) gate turn-off thyristor (GTO); *iii*) MOS-controlled thyristor (MCT) and its various forms; and *iv*) static induction thyristor (SITh). The MCTs are so-named because many parallel enhancement-mode MOSFET structures of one charge type are integrated into the thyristor for turn-on and many more MOSFETs of the other charge type are integrated into the thyristor for turn-off. These MCTs are currently limited to operation at medium power levels. Other types of integrated MOS-thyristor structures can be operated at high power levels, but these devices are not commonly available or are produced for specific applications. A static induction thyristor (SITh), or field-controlled thyristor (FCTh), has essentially the same construction as a power diode with a gate structure that can pinch-off anode current flow. High-power SIThs have a subsurface gate (buried-gate) structure to allow larger cathode areas to be utilized, and hence larger current densities are possible. The advantage of using MCTs, derivative forms of the MCT, or SIThs is that they are essentially voltage-controlled devices, (e.g., little control current is required for turn-on or turn-off) and, therefore, require simplified control circuits attached to the gate electrode. Detailed discussion of variations of MCTs and SIThs as well as additional references on these devices are discussed by Hudgins [1]. Less important types of thyristors include the Triac (a pair of antiparallel SCRs integrated together to form a bidirectional current switch) and the programmable unijunction transistor (PUT).

Both SCRs and GTOs are designed to operate at all power levels. These devices are primarily controlled using electrical signals (current), although some types are made to be controlled using optical (photons) energy for turn-on. Subclasses of SCRs and GTOs are reverse conducting types and symmetric structures that block applied potentials in the reverse and forward polarities. Other variations of GTOs are the gate-commutated turn-off thyristor (GCT) and the bi-directional controlled thyristor (BCT). Most power converter circuits that incorporate thyristors make use of either SCRs or GTOs, and hence this chapter will focus on these two devices, although the basics of operation are applicable to all thyristor types.

All power electronic devices must be derated (e.g., power dissipation levels, current conduction, voltage blocking, and switching frequency must be reduced) when operating above room temperature (defined as $\approx 25\,^\circ$C). Bipolar-type devices have thermal runaway problems, in that if allowed to conduct unlimited current, these devices will heat up internally, causing more current to flow, thus generating more heat, and so forth until destruction. Devices that exhibit this behavior are pin diodes, bipolar transistors, and thyristors.

Almost all power semiconductor devices are made from silicon (Si), but some limited commercial devices are available using gallium-arsenide (GaAs), and silicon-carbide SiC. The latter two semiconductor material systems will not be directly discussed because of the lack of availability and usage. The physical description and general behavior of thyristors are unimportant to the semiconductor material system used although the discussion and any numbers cited in the chapter will be associated with Si devices.

3.2 Basic Structure and Operation

Figure 3.1 shows a conceptual view of a typical thyristor with the three *p-n* junctions and the external electrodes labeled. Also shown in the figure is the thyristor circuit symbol used in electrical schematics.

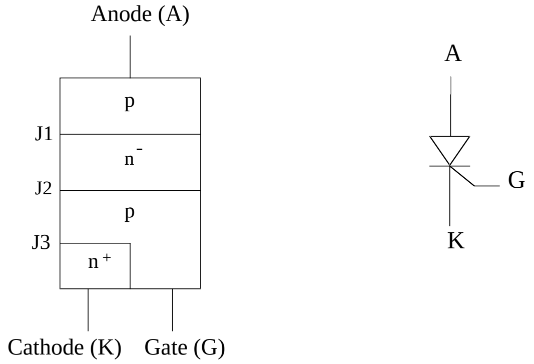

FIGURE 3.1 Simple cross section of a typical thyristor and the associated electrical schematic symbols.

A high-resistivity region, *n*-base, is present in all thyristors. It is this region, the *n*-base and associated junction J_2 of Fig. 3.1, which must support the large applied forward voltages that occur when the switch is in its off- or forward-blocking state (nonconducting). The *n*-base is typically doped with impurity phosphorus atoms at a concentration of $\approx 10^{14}$ cm^{-3}. The *n*-base can be 10s to 100s of μm thick to support large voltages. High-voltage thyristors are generally made by diffusing aluminum or gallium into both surfaces to obtain deep junctions with the *n*-base. The doping profile of the *p*-regions ranges from about 10^{15} to 10^{17} cm^{-3}. These *p*-regions can be up to 10s of μm thick. The cathode region (typically only a few μm thick) is formed by using phosphorus atoms at a doping density of 10^{17} to 10^{18} cm^{-3}.

The higher the forward-blocking voltage rating of the thyristor, the thicker the *n*-base region must be. However increasing the thickness of this high-resistivity region, results in slower turn-on and turn-off (i.e., longer switching times and/or lower frequency of switching cycles because of more stored charge during conduction). For example, a device rated for a forward-blocking voltage of 1 kV will, by its physical construction, switch much more slowly than one rated for 100 V. In addition, the thicker high-resistivity region of the 1 kV device will cause a larger forward voltage drop during conduction than the 100 V device carrying the same current. Impurity atoms, such as platinum or gold, or electron irradiation are used to create charge-carrier recombination sites in the thyristor. The large number of recombination sites reduces the mean carrier lifetime (average time that an electron or hole moves through the Si before recombining with its opposite charge-carrier type). A reduced carrier lifetime shortens the switching times (in particular the turn-off or recovery time) at the expense of increasing the forward conduction drop. There are other effects associated with the relative thickness and layout of the various regions that make up modern thyristors, but the major trade-off between forward-blocking voltage rating and switching times, and between forward-blocking voltage rating and forward-voltage drop during conduction should be kept in mind. In signal-level electronics the analogous trade-off appears as a lowering of amplification (gain) to achieve higher operating frequencies, and is often referred to as the gain-bandwidth product.

The operation of thyristors is as follows. When a positive voltage is applied to the anode (with respect to a cathode), the thyristor is in its forward-blocking state. The center junction J_2 (see Fig. 3.1) is reverse-biased. In this operating mode the gate current is held to zero (open-circuit). In practice, the gate electrode is biased to a small negative voltage (with respect to the cathode) to reverse-bias the GK-junction J_3 and prevent charge-carriers from being injected into the *p*-base. In this condition only thermally generated leakage current flows through the device and can often be approximated as zero in value (the actual value of the leakage current is typically many orders of magnitude lower than the conducted current in the on-state). As long as the forward applied voltage does not exceed the value necessary to cause excessive carrier multiplication in the depletion region around J_2 (avalanche breakdown), the thyristor remains in an off-state (forward-blocking). If the applied voltage exceeds the maximum forward blocking voltage of the thyristor, it will switch to its on-state. However, this mode of turn-on causes nonuniformity in the current flow, is generally destructive, and should be avoided.

When a positive gate current is injected into the device J_3 becomes forward-biased and electrons are injected from the *n*-emitter into the *p*-base. Some of these electrons diffuse across the *p*-base and are collected in the *n*-base. This collected charge causes a change in the bias condition of J_1. The change in bias of J_1 causes holes to be injected from the *p*-emitter into the *n*-base. These holes diffuse across the *n*-base and are collected in the *p*-base. The addition of these collected holes in the *p*-base acts the same as gate current. The entire process is regenerative and will cause the increase in charge carriers until J_2 also becomes forward biased and the thyristor is latched in its on-state (forward-conduction). The regenerative action will take place as long as the gate current is applied in sufficient amount and for a sufficient length of time. This mode of turn-on is considered to be the desired one as it is controlled by the gate signal.

This switching behavior can also be explained in terms of the two-transistor analog shown in Fig. 3.2. The two transistors are regeneratively coupled so that if the sum of their forward current gains (α's) exceeds unity, each drives the other into saturation. Equation 3.1 describes the condition necessary for the thyristor to move from a forward-blocking state into the forward-conduction state. The forward current gain (expressed as the ratio of collector current to emitter current) of the *pnp* transistor is denoted by α_p, and that of the *npn* as α_n. The α's are current dependent and increase slightly as the current increases. The center junction J_2 is reverse-biased under forward applied voltage (positive v_{AK}). The associated electric field in the depletion region around the junction can

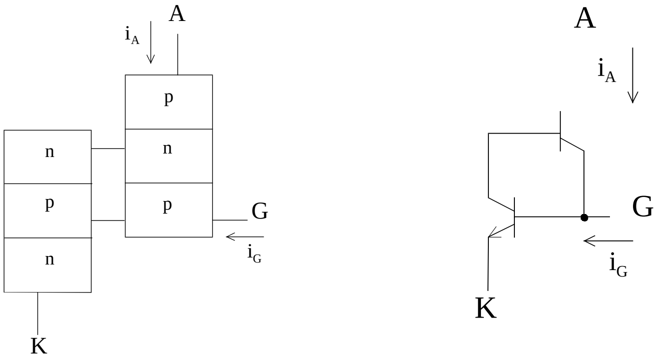

FIGURE 3.2 Two-transistor behavioral model of a thyristor.

result in significant carrier multiplication, denoted as a multiplying factor M on the current components I_{co} and i_G.

$$i_A = \frac{MI_{co} + M\alpha_n i_G}{1 - M(\alpha_n + \alpha_p)} \tag{3.1}$$

In the forward-blocking state, the leakage current I_{co} is small, both α's are small, and their sum is $<$ unity. Gate current increases the current in both transistors, increasing their α's. Collector current in the *npn* transistor acts as base current for the *pnp*, and analogously, the collector current of the *pnp* acts as base current driving the *npn* transistor. When the sum of the two α's equals unity, the thyristor switches to its on-state (latches). This condition can also be reached, without any gate current, by increasing the forward applied voltage so that carrier multiplication ($M \gg 1$) at J_2 increases the internal leakage current, thus increasing the two α's. A third way to increase the α's is by increasing the device (junction) temperature. Increasing the temperature causes a corresponding increase in the leakage current I_{co} to the point where latching can occur. The typical manifestation of this temperature dependence is an effective lowering of the maximum blocking voltage that can be sustained by the thyristor.

Another way to cause a thyristor to switch from forward-blocking to forward-conduction exists. Under a forward-applied voltage, J_2 is reverse-biased while the other two junctions are forward-biased in the blocking mode. The reverse-biased junction of J_2 is the dominant capacitance of the three and determines the displacement current that flows. If the rate of increase in the applied v_{AK} is sufficient (dv_{AK}/dt), it will cause a significant displacement current through the J_2 capacitance. This displacement current can initiate switching similar to that of an externally applied gate current. This dynamic phenomenon is inherent in all thyristors and causes there to be a limit (dv/dt) to the time rate of applied v_{AK} that can be placed on the device to avoid uncontrolled switching. Alterations to the basic thyristor structure can be produced that increase the dv/dt limit and will be discussed in Section 3.4.

Once the thyristor has moved into forward conduction, any applied gate current is superfluous. The thyristor is latched, and for SCRs, cannot be returned to a blocking mode by using the gate terminal. Anode current must be commutated away from the SCR for a sufficient time to allow stored charge in the device to recombine. Only after this recovery time has occurred can a forward voltage be reapplied (below the dv/dt limit of course) and the SCR again be operated in a forward-blocking mode. If the forward voltage is reapplied before sufficient recovery time has elapsed, the SCR will move back into forward-conduction. For GTOs, a large applied reverse gate current (typically in the range of 10–50 of the anode current) applied for a sufficient time can remove enough charge near the GK junction to cause it to turn off, thus interrupting base current to the *pnp* transistor and causing thyristor turn-off. This is similar in principle to using negative base current to quickly turn off a traditional transistor.

3.3 Static Characteristics

3.3.1 Current-Voltage Curves for Thyristors

A plot of the anode current (i_A) as a function of anode-cathode voltage (v_{AK}) is shown in Fig. 3.3. The forward-blocking mode is shown as the low-current portion of the graph (solid curve around operating point "1"). With zero gate current and positive v_{AK} the forward characteristic in the off- or blocking-state is determined by the center junction J_2, which is reverse-biased. At operating point "1," very little current flows (I_{co} only) through the device. However, if the applied voltage exceeds the forward-blocking voltage, the thyristor switches to its on- or conducting-state (shown as operating point "2) because of carrier multiplication (M in Eq. 1). The effect of gate current is to lower the blocking voltage at which switching takes place. The thyristor moves rapidly along the negatively sloped portion of the curve until it reaches a stable operating point determined by the external circuit (point "2). The portion of the graph indicating forward conduction shows the large values of i_A that may be conducted at relatively low values of v_{AK}, similar to a power diode.

As the thyristor moves from forward-blocking to forward-conduction, the external circuit must allow sufficient anode current to flow to keep the device latched. The minimum anode current that will cause the device to remain in forward-conduction as it switches from forward-blocking is called the

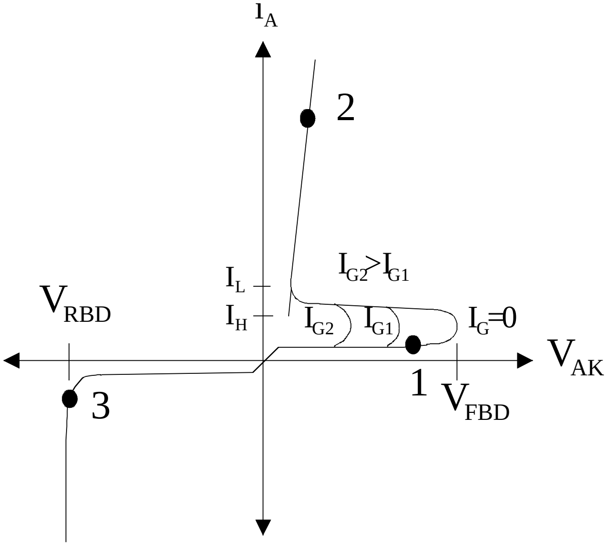

FIGURE 3.3 Static characteristic *i-v* curve typical of thyristors.

latching current I_L. If the thyristor is already in forward-conduction and the anode current is reduced, the device can move its operating mode from forward-conduction back to forward-blocking. The minimum value of anode current necessary to keep the device in forward-conduction after it has been operating at a high anode current value is called the holding current I_H. The holding current value is lower than the latching current value as indicated in Fig. 3.3.

The reverse thyristor characteristic, quadrant III of Fig. 3.3, is determined by the outer two junctions (J_1 and J_3), which are reverse-biased in this operating mode (applied v_{AK} is negative). Symmetric thyristors are designed so that J_1 will reach reverse breakdown due to carrier multiplication at an applied reverse potential near the forward breakdown value (operating point "3" in Fig. 3.3). The forward- and reverse-blocking junctions are usually fabricated at the same time with a very long diffusion process (10 to 50 h) at high temperatures ($>$ 1200 °C). This process produces symmetric blocking properties. Wafer-edge termination processing causes the forward-blocking capability to be reduced to ≈90% of the reverse-blocking capability. Edge termination is discussed in what follows. Asymmetric devices are made to optimize forward-conduction and turn-off properties, and as such reach reverse breakdown at much lower voltages than those applied in the forward direction. This is accomplished by designing the asymmetric thyristor with a much thinner *n*-base than is used in symmetric structures. The thin *n*-base leads to improved properties such as lower forward drop and shorter switching times. Asymmetric devices are generally used in applications when only forward voltages (positive v_{AK}) are to be applied (including many inverter designs).

The form of the gate-to-cathode *VI* characteristic of SCRs and GTOs is similar to that of a diode. With positive gate bias, the gate-cathode junction is forward-biased and permits the flow of a large current in the presence of a low voltage drop. When negative gate voltage is applied to an SCR, the gate-cathode junction is reverse-biased and prevents the flow of current until avalanche breakdown voltage is reached. In a GTO, a negative gate voltage is applied to provide a low impedance path for anode current to flow out of the device instead of out of the cathode. In this way the cathode region (base-emitter junction of the equivalent *npn* transistor) turns off, thus pulling the equivalent *npn* transistor out of conduction. This causes the entire thyristor to return to its blocking state. The problem with the GTO is that the gate-drive circuitry is typically required to sink ≈10% of the anode current in order to achieve turn-off.

3.3.2 Edge and Surface Terminations

Thyristors are often made with planar diffusion technology to create the anode region. Formation of these regions creates cylindrical curvature of the metallurgical gate-cathode junction. Under reverse bias, the curvature of the associated depletion region results in electric field crowding along the curved section of the p^+-diffused region. The field crowding seriously reduces the breakdown potential below that expected for the bulk semiconductor. A floating field ring, an extra p^+-diffused region with no electrical connection at the surface, is often added to modify the electric field profile and thus reduce it to a value below or at the field strength in the bulk. An illustration of a single floating field ring is shown in Fig. 3.4. The spacing *W* between the main anode region and the field ring is critical. Multiple rings can also be employed to further modify the electric field in high-voltage rated thyristors.

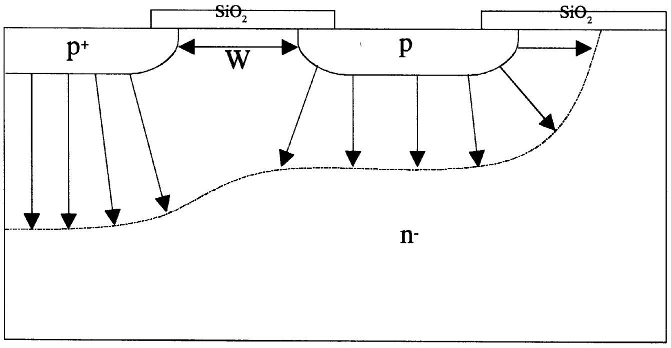

FIGURE 3.4 Cross section showing a floating field ring to decrease the electric field intensity near the curved portion of the main anode region (leftmost p^+-region).

Another common method for altering the electric field at the surface is to use a field plate as shown in cross section in Fig. 3.5. By forcing the potential over the oxide to be the same as at the surface of the p^+-region, the depletion region can be extended so that the electric field intensity is reduced near the curved portion of the diffused p^+-region. A common practice is to use field plates with floating field rings to obtain optimum breakdown performance.

High-voltage thyristors are made from single wafers of Si and must have edge terminations other than floating field rings or field plates to promote bulk breakdown and limit

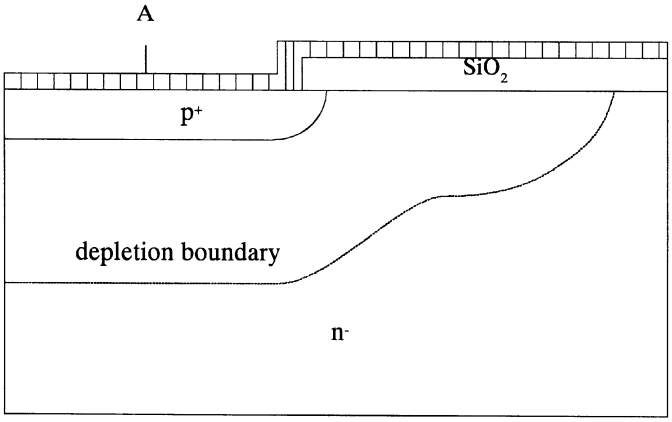

FIGURE 3.5 Cross section showing a field plate used to reduce the electric field intensity near the curved portion of the p^+-region (anode).

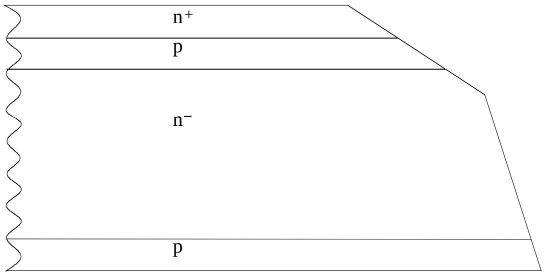

FIGURE 3.6 Cross section of a thyristor showing the negative bevel (upper pn^-- and pn^+-junctions) and positive bevel (lower pn^--junction) used for edge termination of large-area devices.

leakage current at the surface. Controlled bevel angles can be created using lapping and polishing techniques during production of large-area thyristors. Two types of bevel junctions can be created: *i*) a positive bevel defined as one in which the junction area decreases when moving from the highly doped to the lightly doped side of the depletion region; and *ii*) a negative bevel defined as one in which the junction area increases when moving from the highly doped to the lightly doped side of the depletion region. In practice, the negative bevel must be lapped at an extremely shallow angle to reduce the surface field below the field intensity in the bulk. All positive bevel angles between 0 and 90° result in a lower surface field than in the bulk. Figure 3.6 shows the use of a positive bevel for the J_1 junction and a shallow negative bevel for the J_2 and J_3 junctions on a thyristor cross section to make maximum use of the Si area for conduction and still reduce the surface electric field. Further details of the use of beveling, field plates, and field rings can be found in Ghandi [2] and Baliga [3].

3.3.3 Packaging

Thyristors are available in a wide variety of packages, from small plastic ones for low-power (i.e., TO-247), to stud-mount packages for medium-power, to press-pack (also called flat-pack) for the highest power devices. The press-packs must be mounted under pressure to obtain proper electrical and thermal contact between the device and the external metal electrodes. Special force-calibrated clamps are made for this purpose. Large-area thyristors cannot be directly attached to the large copper pole-piece of the press-pack because of the difference in the coefficient of thermal expansion (CTE), hence the use of a pressure contact for both anode and cathode.

Many medium-power thyristors are appearing in modules where a half- or full-bridge (and associated anti-parallel diodes) is put together in one package.

A power module package should have five characteristics:

i) electrical isolation of the baseplate from the semiconductor;
ii) good thermal performance;
iii) good electrical performance;
iv) long life/high reliability; and
v) low cost.

Electrical isolation of the baseplate from the semiconductor is necessary in order to contain both halves of a phase leg in one package as well as for convenience (modules switching to different phases can be mounted on one heat sink) and safety (heat sinks can be held at ground potential).

Thermal performance is measured by the maximum temperature rise in the Si die at a given power dissipation level with a fixed heat sink temperature. The lower the die temperature, the better the package. A package with a low thermal resistance from junction-to-sink can operate at higher power densities for the same temperature rise or lower temperatures for the same power dissipation than a more thermally resistive package. While maintaining low device temperature is generally preferable, temperature variation affects majority carrier and bipolar devices differently. Roughly speaking, in a bipolar device such as a thyristor, switching losses increase and conduction losses decrease with increasing temperature. In a majority carrier device, conduction losses increase with increasing temperature. The thermal conductivity of typical materials used in thyristor packages is shown in Table 3.1.

Electrical performance refers primarily to the stray inductance in series with the die, as well as the capability of mounting a low-inductance bus to the terminals. Another problem is the minimization of capacitive crosstalk from one switch to another, which can cause an abnormal on-state condition by charging the gate of an off-state switch, or from a switch to any circuitry in the package as would be found in a hybrid power module. Capacitive coupling is a major cause of electromagnetic interference (EMI). As the stray inductance of the module and the bus sets a minimum switching loss for the device because the switch must absorb the stored inductive energy, it is very important to minimize

TABLE 3.1 Thermal conductivity of thyristor package materials

Material	Thermal Conductivity (W/m · K) at 300 K
Silicon	150
Copper (baseplate and pole pieces)	390–400
AlN substrate	170
Al_2O_3 (Alumina)	28
Aluminum (Al)	220
Tungsten (W)	167
Molybdenum (Mo)	138
Metal matrix composites (MMC)	170
Thermal grease (heatsink compound)	0.75
60/40 Solder (Pb/Sn eutectic)	50
95/5 Solder (Pb/Sn high temperature)	35

inductance within the module. Reducing the parasitic inductance reduces the high-frequency ringing during transients that is another cause of radiated electromagnetic interference, as since stray inductance can cause large peak voltages during switching transients, minimizing it helps to maintain the device within its safe operating area.

Long life and high reliability are primarily attained through minimization of thermal cycling, minimization of ambient temperature, and proper design of the transistor stack. Thermal cycling fatigues material interfaces because of coefficient of thermal expansion (CTE) mismatch between dissimilar materials. As the materials undergo temperature variation, they expand and contract at different rates, which stresses the interface between the layers and can cause interface deterioration (e.g., cracking of solder layers or wire debonding). Chemical degradation processes such as dendrite growth and impurity migration are accelerated with increasing temperature, so keeping the absolute temperature of the device low and minimizing the temperature changes to which it is subject are important. Typical CTE values for common package materials are given in Table 3.2.

Low cost is achieved in a variety of ways. Both manufacturing and material costs must be taken into account when designing a power module. Materials that are difficult to machine or form, even if they are relatively cheap in raw form, molybdenum, for example, should be avoided. Manufacturing processes that lower yield also drive up costs. In addition, a part that is very reliable can reduce future costs by reducing the need for repair and replacement.

The basic half-bridge module has three power terminals: plus, minus, and phase. Advanced modules differ from traditional high-power commercial modules in several ways. The baseplate is metallized aluminum nitride (AIN) ceramic rather than the typical 0.25″-thick, nickel-plated copper baseplate with a soldered metallized ceramic substrate for electrical isolation. This AlN baseplate stack provides a low thermal resistance from die to heat sink. The copper terminal power buses are attached by solder to the devices in a wirebond-free, low-inductance, low-resistance, device-interconnect configuration. The balance of the assembly is typical for module manufacturing with attachment of shells, use of dielectric gels, and with hard epoxies and adhesives to seal the finished module. An example of an advanced module is shown in Fig. 3.7. Details of the thermal performance of modules and advanced modules can be found in Beker *et al.* [4] and Godbold *et al.* [5].

TABLE 3.2 CTE for thyristor package materials

Material	CTE (μm/m · K) at 300 K
Silicon	4.1
Copper (baseplate and pole pieces)	17
AlN substrate	4.5
Al_2O_3 (Alumina)	6.5
Tungsten (W)	4.6
Molybdenum (Mo)	4.9
Aluminum (Al)	23
Metal matrix composites (MMC)	5–20
60/40 Solder (Pb/Sn eutectic)	25

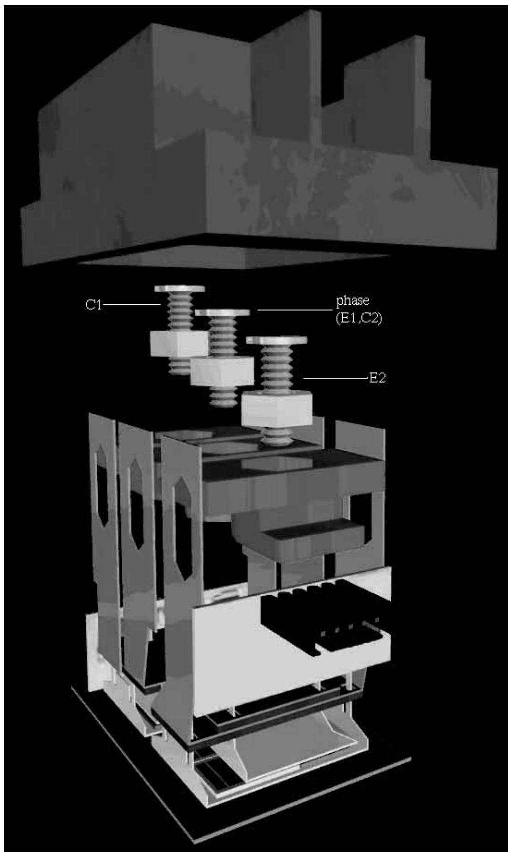

FIGURE 3.7 Advanced module cut-away showing contacts without using wirebonds.

3.4 Dynamic Switching Characteristics

The time rate of rise of both anode current (*di/dt*) during turn-on and anode-cathode voltage (*dv/dt*) during turn-off is an important parameter to control for ensuring proper and reliable operation. All thyristors have maximum limits for *di/dt* and *dv/dt* that must not be exceeded. Devices capable of conducting large currents in the on-state are necessarily made with large-surface areas through which the current flows. During turn-on, localized areas (near the gate region) of a device begin to conduct current. The initial turn-on of an SCR is shown in Fig. 3.8. The cross section illustrates how injected gate current flows to the nearest cathode region, causing this portion of the *npn* transistor to begin conducting. The *pnp* transistor then follows the *npn* into conduction such that

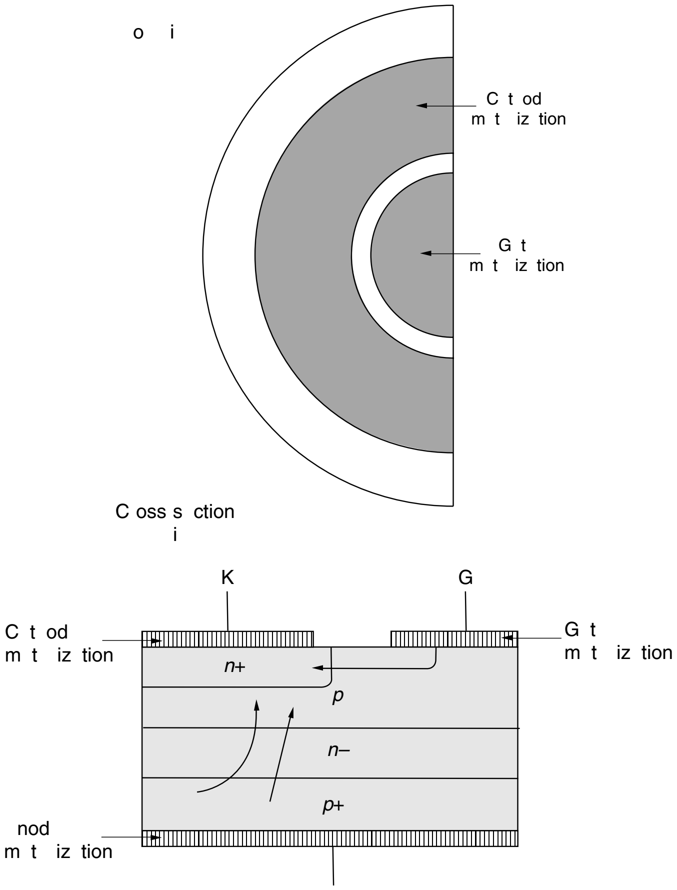

FIGURE 3.8 Top view and associated cross section of gate-cathode periphery showing initial turn-on region in a center-fired thyristor.

anode current begins flowing only in a small portion of the cathode region. If the local current density becomes too large (in excess of several thousand amperes per square centimeter), then self-heating will damage the device. Sufficient time (referred to as plasma spreading time) must be allowed for the entire cathode area to begin conducting before the localized currents become too high. This phenomenon results in a maximum allowable rate of rise of anode current in a thyristor and is referred to as a *di*/*dt* limit. In many high-frequency applications, the entire cathode region is never fully in conduction. Prevention of *di*/*dt* failure can be accomplished if the rate of increase of the conduction area exceeds the *di*/*dt* rate such that the internal junction temperature does not exceed a specified critical temperature (typically ≈350 °C). This critical temperature decreases as the blocking voltage increases. Adding series inductance to the thyristor to limit *di*/*dt* below its maximum usually causes circuit design problems.

Another way to increase the *di*/*dt* rating of a device is to increase the amount of gate-cathode periphery. Inverter SCRs

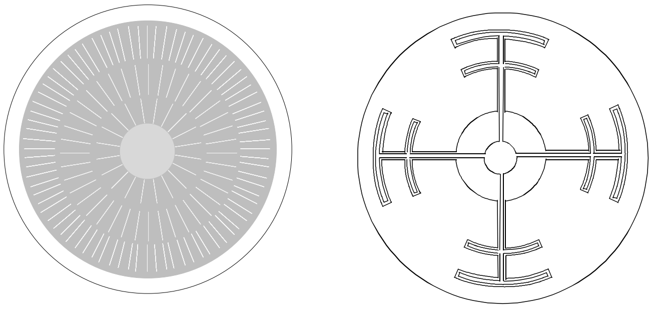

FIGURE 3.9 Top view of typical interdigitated gate-cathode patterns used for thyristors.

(so named because of their use in high-frequency power converter circuits that convert dc to ac invert) are designed so that there is a large amount of gate edge adjacent to a significant amount of cathode edge. A top surface view of two typical gate-cathode patterns, found in large thyristors is shown in Fig. 3.9. An inverter SCR often has a stated maximum *di*/*dt* limit of ≈2000 A/μs. This value has been shown to be conservative [6], and by using excessive gate current under certain operating conditions, an inverter SCR can be operated reliably at 10,000 to 20,000 A/μs.

A GTO takes the interdigitation of the gate and cathode to the extreme (Fig. 3.9, left). In Fig. 3.10 a cross section of a GTO shows the amount of interdigitation. A GTO often has cathode islands that are formed by etching the Si. A metal plate can be placed on the top to connect the individual cathodes into a large arrangement of electrically parallel cathodes. The gate metallization is placed so that the gate surrounding each cathode is electrically in parallel as well. This construction not only allows high *di*/*dt* values to be reached, as in an inverter SCR, but also provides the capability to turn off the anode current by shunting it away from the individual cathodes and out the gate electrode upon reverse-biasing of the gate. During turn-off, current is decreasing while voltage across the device is increasing. If the forward voltage becomes too high while sufficient current is still flowing, then the device will drop back into its conduction mode instead of

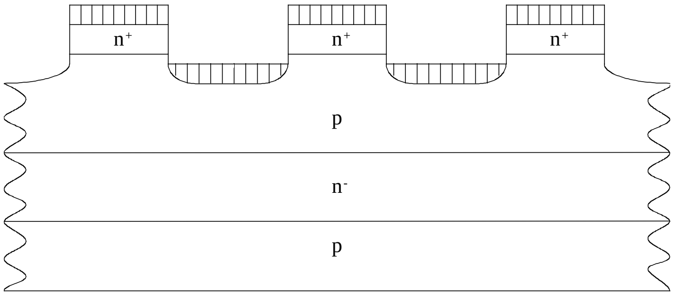

FIGURE 3.10 Cross section of a GTO showing the cathode islands and interdigitation with the gate (*p*-base).

completing its turn-off cycle. Also, during turn-off, the power dissipation can become excessive if the current and voltage are simultaneously too large. Both of these turn-off problems can damage the device as well as other portions of the circuit.

Another switching problem that occurs is associated primarily with thyristors, although other power electronic devices suffer some degradation of performance from the same problem. This problem occurs because thyristors can self-trigger into a forward-conduction mode from a forward-blocking mode if the rate of rise of forward anode-cathode voltage is too large. This triggering method is due to displacement current through the associated junction capacitances (capacitance at J_2 dominates because it is reverse-biased under forward applied voltage). The displacement current contributes to the leakage current I_{co}, shown in Eq. (1). Therefore SCRs and GTOs have a maximum dv/dt rating that should not be exceeded (typical values are 100 to 1000 V/μs). Switching into a reverse-conducting state from a reverse-blocking state due to an applied reverse dv/dt, is not possible because the values of the reverse α's of the equivalent transistors can never be made large enough to cause the necessary feedback (latching) effect. An external capacitor is often placed between the anode and cathode of the thyristor to help control the dv/dt experienced. Capacitors and other components that are used to form such protection circuits, known as snubbers, are used with all power semiconductor devices.

3.4.1 Cathode Shorts

As the temperature in the thyristor increases > 25 °C, the minority carrier lifetime and the corresponding diffusion lengths in the n- and p-bases increase. This leads to an increase in the α's of the equivalent transistors. Discussion of the details of the minority carrier diffusion length and its role in determining the current gain factor α can be found in Sze [7]. Referring to Eq. (1), it is seen that a lower applied bias will give a carrier multiplication factor M, sufficient to switch the device from forward-blocking into conduction because of this increase of the α's with increasing temperature. Placing a shunt resistor in parallel with the base-emitter junction of the equivalent npn transistor (shown in Fig. 3.11) will result in an effective current gain α_{neff} that is lower than α_n, as given by Eq. (2), where v_{GK} is the applied gate-cathode voltage, R_s is the equivalent lumped value for the distributed current shunting structure, and the remaining factors form the appropriate current factor based on the applied bias and characteristics of the gate-cathode junction. The shunt current path is implemented by providing intermittent shorts, called cathode shorts, between the p-base (gate) region and the n^+-emitter (cathode) region in the thyristor as illustrated in Fig. 3.12. The lumped shunt resistance value is in the range of 1 to 15 Ω as measured from gate to cathode.

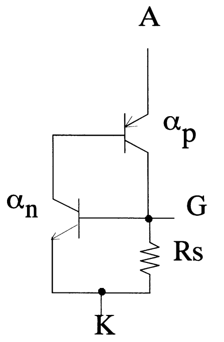

FIGURE 3.11 Two-transistor equivalent circuit showing the addition of a resistive shunt path for anode current.

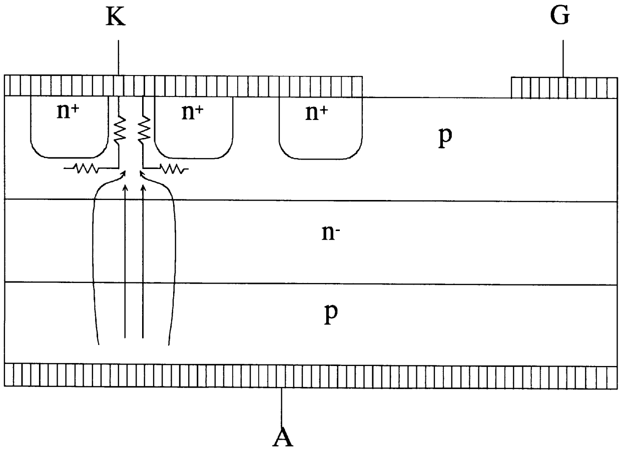

FIGURE 3.12 Cross section showing cathode shorts and the resulting resistive shunt path for anode current.

$$\alpha_{n_{\text{eff}}} = \alpha_n \left(\frac{1}{1 + v_{GK} \alpha_n / R_S i_0 e^{q v_{GK}/kT}} \right) \tag{3.2}$$

Low values of anode current (e.g., those associated with an increase in temperature under forward-blocking conditions) will flow through the shunt path to the cathode contact, bypassing the n^+-emitter and keeping the device out of its forward-conduction mode. As the anode current becomes large, the potential drop across the shunt resistance will be sufficient to forward bias the gate-cathode junction J_3 and bring the thyristor into forward conduction. The cathode shorts also provide a path for displacement current to flow without forward biasing J_3. Both the dv/dt rating of the thyristor and the forward blocking characteristics are improved by using cathode shorts. However, the shorts do, cause a lowering of cathode current handling capability because of the loss of some of the cathode area (n^+-region) to the shorting pattern, an increase in the necessary gate current to obtain switching from forward-blocking to forward-conduction, and an increased complexity in manufacturing the thyristor. The loss of cathode area due to the shorting-structure is from 5 to 20 , depending on the type of thyristor. By careful design of the cathode short windows to the p-base, the holding current can be made lower than the latching current. This is important

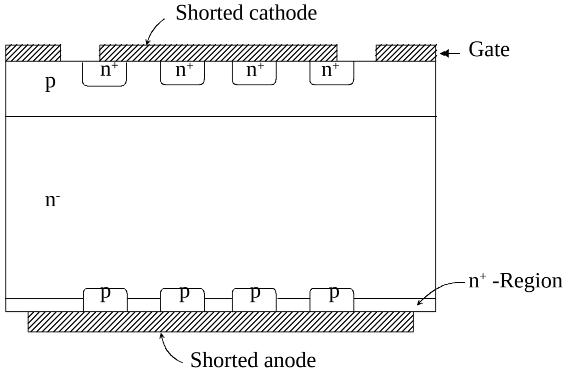

FIGURE 3.13 Cross section showing integrated cathode and anode shorts.

so that the thyristor will remain in forward conduction when used with varying load impedances.

3.4.2 Anode Shorts

A further increase in forward-blocking capability can be obtained by introducing anode shorts (reduces α_p in a similar manner that cathode shorts reduce α_n) along with the cathode shorts. An illustration of this is provided in Fig. 3.13. In this structure, both J_1 and J_3 are shorted (anode and cathode shorts) so that the forward-blocking capability of the thyristor is completely determined by the avalanche breakdown characteristics of J_2. Anode shorts will result in the complete loss of reverse-blocking capability and is only for thyristors used in asymmetric circuit applications.

3.4.3 Amplifying Gate

The cathode-shorting structure will reduce the gate sensitivity dramatically. To increase this sensitivity and yet retain the benefits of the cathode-shorts, a structure called an amplifying gate (or regenerative gate) is used, as shown in Fig. 3.14 (and Fig. 3.9, right). When the gate current (1) is injected into the p-base through the pilot-gate contact, electrons are injected into the p-base by the n^+-emitter with a given emitter injection efficiency. These electrons traverse through the p-base (time taken for this process is called the transit time) and accumulate near the depletion region. This negative charge accumulation leads to injection of holes from the anode. The device then turns-on after a certain delay, dictated by the p-base transit time, and the pilot anode current (2 on the figure) begins to flow through a small region near the pilot-gate contact as shown in Fig. 3.14.

This flow of pilot anode current corresponds to the initial sharp rise in the anode current waveform (phase I), as shown in Fig. 3.15. The device switching then goes into phase II, during which the anode current remains fairly constant, suggesting that the resistance of the region has reached its lower limit. This is due to the fact that the pilot anode current (2) takes a finite time to traverse through the p-base laterally and become the gate current for the main cathode area. The n^+-emitters start to inject electrons which traverse the p-base vertically and after a certain finite time (transit time of the p-base) reach the depletion region. The total time taken by the lateral traversal of pilot anode current and the electron transit time across the p-base is the reason for observing this characteristic phase II interval. The width of the phase II interval is comparable to the switching delay, suggesting that the p-base transit time is of primary importance. Once the main cathode region turns on, the resistance of the device decreases and the anode current begins to rise again (transition from phase II to phase III). From this time onward in the switching cycle, the plasma spreading velocity will dictate the rate at which the conduction area will increase. The current density during phase I and phase II can be quite large, leading to a considerable increase in the local temperature and device failure. The detailed effect of the amplifying gate on the anode current rise will be noticed only at high levels of di/dt (in the range of 1000 A/μs). It can be concluded that the amplifying gate will increase gate sensitivity at the expense of some di/dt capability, as demonstrated by Sankaran *et al.* (8). This

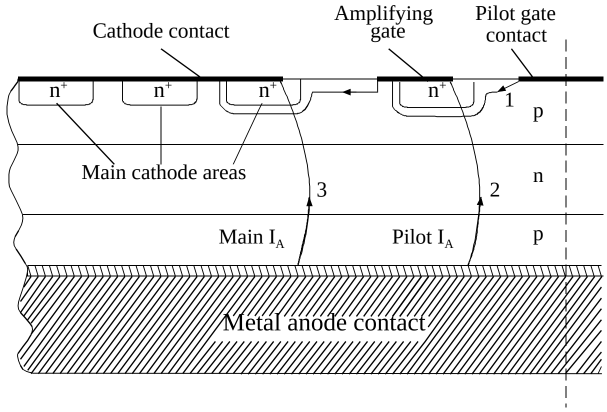

FIGURE 3.14 Cross section showing the amplifying gate structure in a thyristor.

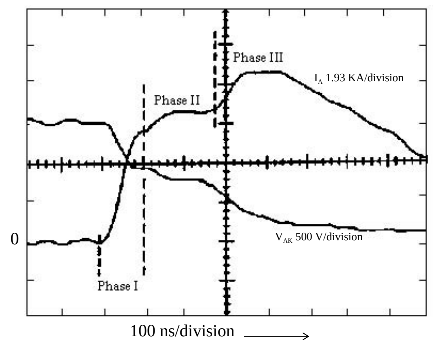

FIGURE 3.15 Turn-on waveforms showing the effect of the amplifying gate in the anode current rise.

lowering of di/dt capability can be somewhat offset by an increase in gate-cathode interdigitation as previously discussed.

3.4.4 Temperature Dependencies

The forward blocking voltage of an SCR has been shown to be reduced from 1350 V at 25 °C to 950 V at −175 °C in a near linear fashion [8]. Above 25 °C, the forward-blocking capability is again reduced due to changes in the minority carrier lifetime. Several dominant physical parameters associated with semiconductor devices are sensitive to temperature variations, causing their dependent device characteristics to change dramatically. The most important of these parameters are: *i*) the minority carrier lifetimes (which control the high-level injection lifetimes); *ii*) the hole and electron mobilities; *iii*) the impact ionization collision cross sections; and *iv*) the free-carrier concentrations (primarily the ionized impurity-atom concentration). Almost all of the impurity atoms are ionized at temperatures >0 °C, and so further discussion of the temperature effects on ionization is not relevant for normal operation. The detailed discussion of these physical parameters is beyond the scope of this chapter but references listed for those interested in pursuing relevant information about temperature effects.

It is well known that charge carrier recombination events are more efficient at lower temperatures. This shows up as a larger potential drop during forward conduction and a shorter recovery time during turn-off. A plot of the anode current during turn-off, at various temperatures, for a typical GTO is shown in Fig. 3.16.

An approximate relation between the temperature and the forward drop across the *n*-base of a thyristor is discussed in detail by Herlet [10] and Hudgins *et al.* [11]. The junction potential drops in the device, the temperature dependence of the bandgap energy, along with the *n*-base potential drop, a temperature-dependent equation relating anode current density J_A, and the applied anode-cathode voltage V_{AK} are also given in Reference [11]. Data from measurements at forward current densities $\approx 100\ \mathrm{A/cm^2}$ on a GTO rated for 1-kV symmetric blocking have forward voltage drops of 1.7 V at −50 °C to 1.8 V at 150 °C.

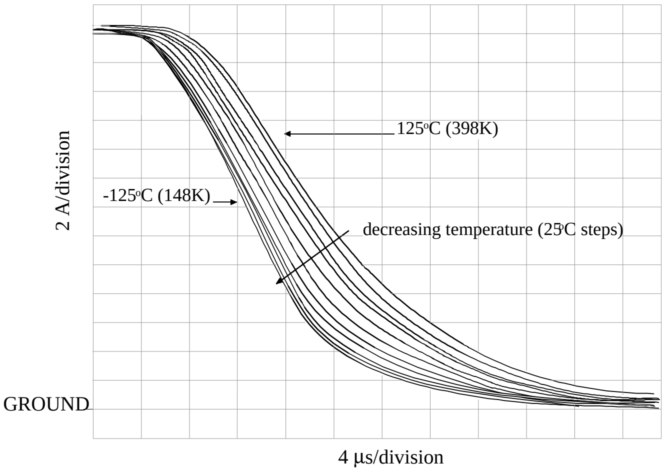

FIGURE 3.16 Temperature effect on the anode current tail during turn-off.

3.5 Thyristor Parameters

Understanding of a thyristor's maximum ratings and electrical characteristics is required for proper application. Use of a manufacturer's data sheet is essential for good design practice. *Ratings* are maximum or minimum values that set limits on device capability. A measure of device performance under specified operating conditions is a *characteristic* of the device. A summary of some of the maximum ratings that must be considered when choosing a thyristor for a given application is provided in Table 3.3. Thyristor types shown in parentheses indicate a maximum rating unique to that device. Both forward and reverse repetitive and nonrepetitive voltage ratings must be considered, and a properly rated device must be chosen so that the maximum voltage ratings are never exceeded. In most cases, either forward or reverse voltage transients in excess of the nonrepetitive maximum ratings result in destruction of the device. The maximum rms or

TABLE 3.3 Thyristor maximum ratings specified by manufacturers

Symbol	Description
V_{RRM}	Peak repetitive reverse voltage
V_{RMS}	Peak nonrepetitive reverse voltage (transient)
$V_{\mathrm{R(DC)}}$	DC reverse blocking voltage
V_{DRM}	Peak repetitive forward off-state voltage
V_{DSM}	Peak nonrepetitive forward off-state voltage (transient)
$V_{\mathrm{D(DC)}}$	DC forward blocking voltage
$I_{\mathrm{T(RMS)}}$, $I_{\mathrm{F(RMS)}}$	RMS forward on-state current
$I_{\mathrm{T(AV)}}$, $I_{\mathrm{F(AV)}}$	Average forward on-state current at specified case or junction temperature
I_{TMS}, $I_{\mathrm{F(TSM)}}$	Peak one-cycle surge on-state current (values specified at 60 and 50 Hz)
I_{TGQ} (GTO)	Peak controllable current
I^2t	Nonrepetitive pulse overcurrent capability (8.3 ms)
P_T	Maximum power dissipation
di/dt	Critical rate of rise of on-state current at specified junction temperature, gate current, and forward blocking voltage
$P_{\mathrm{GM}}/(P_{\mathrm{FGM}}$ for GTO)	Peak gate power dissipation (reverse)
P_{RGM}(GTO)	Peak gate power dissipation (reverse)
$P_{\mathrm{G(AV)}}$	Average gate power dissipation
V_{FGM}	Peak forward gate voltage
V_{RGM}	Peak reverse gate voltage
I_{FGM}	Peak forward gate current
I_{RGM} (GTO)	Peak reverse gate current
T_{STG}	Storage temperature
T_j	Junction operating temperature
V_{RMS}	Voltage isolation (modules)

average current ratings given are usually those that cause the junction to reach its maximum rated temperature. Because the maximum current will depend upon the current waveform and upon thermal conditions external to the device, the rating is usually shown as a function of case temperature and conduction angle. The peak single half-cycle surge-current rating must be considered, and in applications where the thyristor must be protected from damage by overloads, a fuse with an I^2t rating smaller than the maximum rated value for the device must be used. Maximum ratings for both forward and reverse gate voltage, current, and power also must not be exceeded.

The maximum rated operating junction temperature T_J must not be exceeded, as device performance, in particular voltage-blocking capability, will be degraded. Junction temperature cannot be measured directly but must be calculated from a knowledge of steady-state thermal resistance $R_{\Theta(J-C)}$, and the average power dissipation. For transients or surges, the transient thermal impedance ($Z_{\Theta(J-C)}$ curve must be used (provided in manufacturer's data sheets). The maximum average power dissipation P_T is related to the maximum rated operating junction temperature and the case temperature by the steady-state thermal resistance. In general, both maximum dissipation and its derating with increasing case temperature are provided.

The number and type of thyristor characteristics specified varies widely from one manufacturer to another. Some characteristics are given only as typical values of minima or maxima, while many characteristics are displayed graphically. Table 3.4 summarizes some of the typical characteristics provided as maximum values. The maximum value means that the manufacturer guarantees that the device will not exceed the value given under the specified operating or switching conditions. A minimum value means that the manufacturer guarantees that the device will perform at least as good as the characteristic given under the specified operating or switching conditions. Thyristor types shown in parentheses indicate a characteristic unique to that device. Gate conditions of both voltage and current to ensure either nontriggered or triggered device operation are included. The turn-on and turn-off transients of the thyristor are characterized by switching times like the turn-off time listed in Table 3.4. The turn-on transient can be divided into three intervals: *i*) gate-delay interval; *ii*) turn-on of initial area; and *iii*) spreading interval. The gate-delay interval is simply the time between application of a turn-on pulse at the gate and the time the initial cathode area turns on. This delay decreases with increasing gate drive current and is of the order of a few microseconds. The second interval, the time required for turn-on of the initial area, is quite short, typically < 1 μs. In general, the initial area turned on is a small percentage of the total useful device area. After the initial area turns on, conduction spreads (spreading interval or plasma spreading time) throughout the device in tens of microseconds for high-speed devices or thyristors. The plasma spreading time may take up to hundreds of microseconds in large-area phase-control devices.

TABLE 3.4 Typical thyristor characteristic maximums and minimum specified by manufacturers

Symbol	Description
V_{TM}, V_{FM}	Maximum on-state voltage drop (at specified junction temperature and forward current)
I_{DRM}	Maximum forward off-state current (at specified junction temperature and forward voltage)
I_{RRM}	Maximum reverse off-state current (at specified junction temperature and reverse voltage)
dv/dt	Minimum critical rate of rise of off-state voltage at specified junction temperature and forward-blocking voltage level
V_{GT}	Maximum gate trigger voltage (at specified temperature and forward applied voltage)
V_{GD}, V_{GDM}	Maximum gate nontrigger voltage (at specified temperature and forward applied voltage)
I_{GT}	Maximum gate trigger current (at specified temperature and forward applied voltage)
T_{gt} (GTO)	Maximum turn-on time (under specified switching conditions)
T_q	Maximum turn-off time (under specified switching conditions)
t_D	Maximum turn-on delay time (for specified test)
$R_{\Theta(\mathrm{J-C})}$	Maximum junction-to-case thermal resistance
$R_{\Theta(\mathrm{C-S})}$	Maximum case-to-sink thermal resistance (interface lubricated)

Table 3.5 lists many of the thyristor parameters that appear either as listed values or as information on graphs. The definition of each parameter and the test conditions under which they are measured are given in the table as well.

3.6 Types of Thyristors

In recent years, most development effort has gone into both continued integration of the gating and control electronics into thyristor modules and the use of MOS technology to create gate structures integrated into the thyristor itself. Many variations of this theme are being developed and some technologies should rise above the others in the years to come. Further details concerning most of the following discussion of thyristor types can be found in Reference [1].

3.6.1 SCRs and GTOs

The highest power handling devices continue to be bipolar thyristors. High-powered thyristors are large diameter devices, some well in excess of 100 mm, and as such have a limitation on the rate of rise of anode current, a di/dt rating. The depletion capacitances around the *pn* junctions, in particular the center junction, limit the rate of rise in forward voltage that can be applied even after all the stored charge, introduced

TABLE 3.5 Symbols and definitions of major thyristor parameters

R_θ	Thermal Resistance	Specifies the degree of temperature rise per unit of power, measuring junction temperature from a specified external point. Defined when junction power dissipation results in steady-state thermal flow.
$R_{\theta(J-A)}$	Junction-to-ambient thermal resistance	The steady-state thermal resistance between the junction and ambient.
$R_{\theta(J-C)}$	Junction-to-case thermal resistance	The steady-state thermal resistance between the junction and case surface.
$R_{\theta(J-S)}$	Junction-to-sink thermal resistance	The steady-state thermal resistance between the junction and the heat sink mounting surface.
$R_{\theta(C-S)}$	Contact thermal resistance	The steady-state thermal resistance between the surface of the case and the heat sink mounting surface.
Z_θ	Transient thermal impedance	The change of temperature difference between two specified points or regions at the end of a time interval divided by the step function change in power dissipation at the beginning of the same interval causing the change of temperature difference.
$Z_{\theta(J-A)}$	Junction-to-ambient transient thermal impedance	The transient thermal impedance between the junction and ambient.
$Z_{\theta(J-C)}$	Junction-to-case transient thermal impedance	The transient thermal impedance between the junction and the case surface.
$Z_{\theta(J-S)}$	Junction-to-sink transient thermal impedance	The transient thermal impedance between the junction and the heat sink mounting surface.
T_A	Ambient temperature	It is the temperature of the surrounding atmosphere of a device when natural or forced-air cooling is used, and is not influenced by heat dissipation of the device.
T_S	Sink temperature	The temperature at a specified point on the device heat sink.
T_C	Case temperature	The temperature at a specified point on the device case.
T_J	Junction temperature	The device junction temperature rating. Specifies the maximum and minimum allowable operation temperatures.
T_{STG}	Storage temperature	Specifies the maximum and minimum allowable storage temperatures (with no electrical connections).
V_{RRM}	Peak reverse blocking voltage	Within the rated junction temperature range, and with the gate terminal open-circuited, specifies the repetitive peak reverse anode to cathode voltage applicable on each cycle.
V_{RSM}	Transient peak reverse blocking voltage	Within the rated junction temperature range, and with the gate terminal open-circuited, specifies the nonrepetitive peak reverse anode to cathode voltage applicable for a time width equivalent to < 5 ms.
$V_{R(\mathrm{DC})}$ SCR Only	DC Reverse blocking voltage	Within the rated junction temperature range, and with the gate terminal open-circuited, specifies the maximum value for dc anode to cathode voltage applicable in the reverse direction.
V_{DRM}	Peak forward blocking voltage	Within the rated junction temperature range, and with the gate terminal open-circuited (SCR), or with a specified reverse voltage between the gate and cathode (GTO), specifies the repetitive peak off-state anode to cathode voltage applicable on each cycle. This does not apply for transient off-state voltage application.
V_{DSM}	Transient peak forward blocking voltage	Within the rated junction temperature range, and with the gate terminal open-circuited (SCR), or with a specified reverse voltage between the gate and cathode (GTO), specifies the nonrepetitive off-state anode to cathode voltage applicable for a time width equivalent to < 5 ms. This gives the maximum instantaneous value for nonrepetitive transient off-state voltage.
$V_{D(\mathrm{DC})}$	DC Forward blocking voltage	Within the rated junction temperature range, and with the gate terminal open-circuited (SCR), or with a specified reverse voltage between the gate and cathode (GTO), specifies the maximum value for dc anode to cathode voltage applicable in the forward direction.
dv/dt	Critical rate-of-rise of off-state voltage $dv/dt = (0.632\ V_D)/\tau$ V_D is specified off-state voltage τ is time constant for exponential	At the maximum rated junction temperature range, and with the gate terminal open-circuited (SCR), or with a specified reverse voltage between the gate and cathode (GTO), this specifies the maximum rate-of-rise of off-state voltage that will not drive the device from an off-state to an on-state when an exponential off-state voltage of specified amplitude is applied to the device.
V_{TM}	Peak on-state voltage	At specified junction temperature, and when on-state current (50 or 60 Hz, half sine wave of specified peak amplitude) is applied to the device, indicates peak-value for the resulting voltage drop.
$I_{T(\mathrm{RMS})}$	RMS on-state current	At specified case temperature, indicates the rms value for on-state current that can be continuously applied to the device.
$I_{T(\mathrm{AV})}$	Average on-state current	At specified case temperature, and with the device connected to a resistive or inductive load, indicates the average value for forward-current (sine half wave, commercial frequency) that can be continuously applied to the device.
I_{TSM}	Peak on-state current	Within the rated junction temperature range, indicates the peak-value for non-repetitive on-state current (sine half wave, 50 or 60 Hz). This value indicated for one cycle, or as a function of a number of cycles.

(continued)

TABLE 3.5 (Continued)

I^2t	Current-squared time	The maximum, on-state, nonrepetitive short-time thermal capacity of the device and is helpful in selecting a fuse or providing a coordinated protection scheme of the device in the equipment. This rating is intended specifically for operation less than one half cycle of a 180° (degree) conduction angle sinusoidal waveform. The off-state blocking capability cannot be guaranteed at values near the maximum I^2t.
di/dt	Critical rate-of-rise of on-state current	At specified case temperature, specified off-state voltage, specified gate conditions, and at a frequency of <60 Hz, indicates the maximum rate-of-rise of on-state current which the thyristor will withstand when switching from an off-state to an on-state, when using recommended gate drive.
I_{RRM}	Peak reverse leakage current	At maximum rated junction temperature, indicates the peak value for reverse-current flow when a voltage (sine half wave, 50 or 60 Hz, and having a peak value as specified for repetitive peak reverse-voltage rating) is applied in a reverse direction to the device.
I_{DRM}	Peak forward leakage current	At maximum rated junction temperature, indicates the peak-value for off-state-current flow when a voltage (sine half wave, 50 or 60 Hz, and having a peak value for repetitive off-state voltage rating) is applied in a forward direction to the device. For a GTO, a reverse voltage between the gate and cathode is specified.
P_{GM} (SCR)	Peak gate power dissipation	Within the rated junction temperature range, indicates the peak value for maximum allowable power dissipation over a specified time period, when the device is in forward conduction between the gate and cathode.
P_{GFM} (GTO)	Peak gate forward power dissipation	
$P_{G(\mathrm{AV})}$	Average gate power dissipation	Within the rated junction temperature range, indicates the average value for maximum allowable power dissipation when the device is forward-conducting between the gate and cathode.
P_{GRM} GTO Only	Peak gate reverse power dissipation	Within the rated junction temperature range, indicates the peak value for maximum allowable power dissipation in the reverse direction between the gate and cathode, over a specified time period.
$P_{GR(\mathrm{AV})}$ GTO only	Average gate reverse power dissipation	Within the rated junction temperature range, indicates the average value for maximum allowable power dissipation in the reverse direction between the gate and cathode.
I_{GFM}	Peak forward gate current	Within the rated junction temperature range, indicates the peak value for forward-current flow between the gate and cathode.
I_{GRM} GTO Only	Peak reverse gate current	Within the rated junction temperature range, indicates peak value for reverse-current that can be conducted between the gate and cathode.
V_{GRM}	Peak reverse gate voltage	Within the rated junction temperature range, indicates the peak value for reverse-voltage applied between the gate and cathode.
V_{GFM}	Peak forward gate voltage	Within the rated junction temperature range, indicates the peak value for forward-voltage applied between the gate and cathode.
I_{GT}	Gate current to trigger	At a junction temperature of 25 °C, and with a specified off-voltage, and a specified load resistance, indicates the minimum gate dc current required to switch the thyristor from an off-state to an on-state.
V_{GT}	Gate voltage to trigger	At a junction temperature of 25 °C, and with a specified off-state voltage, and a specified load resistance, indicates the minimum dc gate voltage required to switch the thyristor from an off-state to an on-state.
V_{GDM} SCR Only	Nontriggering gate voltage	At maximum rated junction temperature, and with a specified off-state voltage applied to the device, indicates the maximum dc gate voltage that will not switch the device from an off-state to an on-state.
I_{TGO} GTO Only	Gate controlled turn-off current	Under specified conditions, indicates the instantaneous value for on-current usable in gate control, specified immediately prior to device turn-off.
t_{on} SCR Only	Turn-on time	At specified junction temperature, and with a peak repetitive off-state voltage of half-rated value, followed by device turn-on using specified gate current, and when specified on-state current of specified *di/dt* flows, indicated as the time required for the applied off-state voltage to drop to 10 of its initial value after gate current application. *Delay time* is the term used to define the time required for applied voltage to drop to 90 of its initial value following gate-current application. The time required for the voltage level to drop from 90 to 10 of its initial value is referred to as rise time. The sum of both of these defines turn-on time.
T_q SCR Only	Turn-off Time	Specified at maximum rated junction temperature. Device set up to conduct on-state current, followed by applying specified reverse anode-cathode voltage to quench on-state current, and then increasing the anode-cathode voltage at a specified rate-of-rise as determined by circuit conditions controlling the point where the specified off-state voltage is reached. Turn-off time defines the minimum time which the device will hold its off-state, starting from the time on-state current reached zero until the time forward voltage is again applied (i.e., applied anode-cathode voltage becomes positive again).
t_{gt} GTO Only	Turn-on time	When applying forward-current to the gate, indicates the time required to switch the device from an off-state to an on-state.
t_{qt} GTO Only	Turn-off time	When applying reverse-current to the gate, indicates the time required to switch the device from an on-state to an off-state.

during conduction, is removed. The associated displacement current under application of forward voltage during the thyristor blocking state sets a dv/dt limit. Some effort in improving the voltage hold-off capability and overvoltage protection of conventional silicon-controlled rectifiers (SCRs) is underway by incorporating a lateral high-resistivity region to help dissipate the energy during break-over. Most effort, though, is being directed toward further development of high-performance gate turn-off (GTO) thyristors because of their controllability and to a lesser extent in optically triggered structures that feature gate circuit isolation.

High-voltage GTO thyristors with symmetric blocking capability require thick *n*-base regions to support the high electric field. The addition of an n^+-buffer layer next to the p^+-anode allows high voltage blocking and a low forward voltage drop during conduction because of the thinner *n*-base required. Cylindrical anode shorts have been incorporated to facilitate excess carrier removal from the *n*-base during turn-off and still retain high blocking capability. This device structure can control 200 A, operating at 900 Hz, with a 6-kV hold-off. Some of the design trade-offs between the *n*-base width and turn-off energy losses in these structures been determined. A similar GTO incorporating an n^+-buffer layer and a *pin* structure has been fabricated that can control up to 1 kA (at a forward drop of 4 V) with a forward blocking capability of 8 kV. A reverse-conducting GTO has been fabricated that can block 6 kV in the forward direction, interrupt a peak current of 3 kA, and has a turn-off gain of ≈ 5.

A modified GTO structure, called a gate commutated thyristor (GCT), has been designed and manufactured that commutates all of the cathode current away from the cathode region and diverts it out the gate contact. The GCT is similar to a GTO in structure except that it has a low-loss *n*-buffer region between the *n*-base and *p*-emitter. The GCT device package is designed to result in very low parasitic inductance and is integrated with a specially designed gate-drive circuit. The specially designed gate drive and ring-gate package circuit allow the GCT to be operated without a snubber circuit and switch with higher anode di/dt, than a similar GTO. At blocking voltages of 4.5 kV and higher the GCT seems to provide better performance than a conventional GTO. The speed at which the cathode current is diverted to the gate (di_{GQ}/dt) is directly related to the peak snubberless turn-off capability of the GCT. The gate drive circuit can sink current for turn-off at di_{GQ}/dt values > 7000 A/μs. This hard gate drive results in a low charge storage time of ≈ 1 μs. Low storage time and fail-short mode make the GCT attractive for high-voltage series applications.

3.6.2 MOS-Controlled Thyristors, MCT

The corresponding equivalent circuit of the *p*-type MCT unit cell is provided in Fig. 3.17. When the MCT is in its forward blocking state and a negative gate-anode voltage is applied, an inversion layer is formed in the *n*-doped material that allows holes to flow laterally from the *p*-emitter (*p*-channel FET source) through the channel to the *p*-base (*p*-channel FET drain). This hole flow is the base current for the *npn* transistor. The *n*-emitter then injects electrons, which are collected in the *n*-base, causing the *p*-emitter to inject holes into the *n*-base so that the *pnp* transistor is turned on and latches the MCT. The MCT is brought out of conduction by applying a positive gate-anode voltage. This signal creates an inversion layer that diverts electrons in the *n*-base away from the *p*-emitter and into the heavily doped *n*-region at the anode. This *n*-channel FET current amounts to a diversion of the *pnp* transistor base current so that its base-emitter junction turns off. Holes are then no longer available for collection by the *p*-base. The elimination of this hole current (*npn* transistor base current) causes the *npn* transistor to turn off. The remaining stored charge recombines and returns the MCT to its blocking state. The seeming variability in fabrication of the turn-off FET structure continues to limit the performance of MCTs, particularly current interruption capability, although these devices can handle 2 to 5 times the conduction current density of IGBTs. Numerical modeling and experimental verification of the modeling have shown the sensitivity that an ensemble of cells has to current filamentation during turn-off. All MCT device designs center around the problem of current interrup-

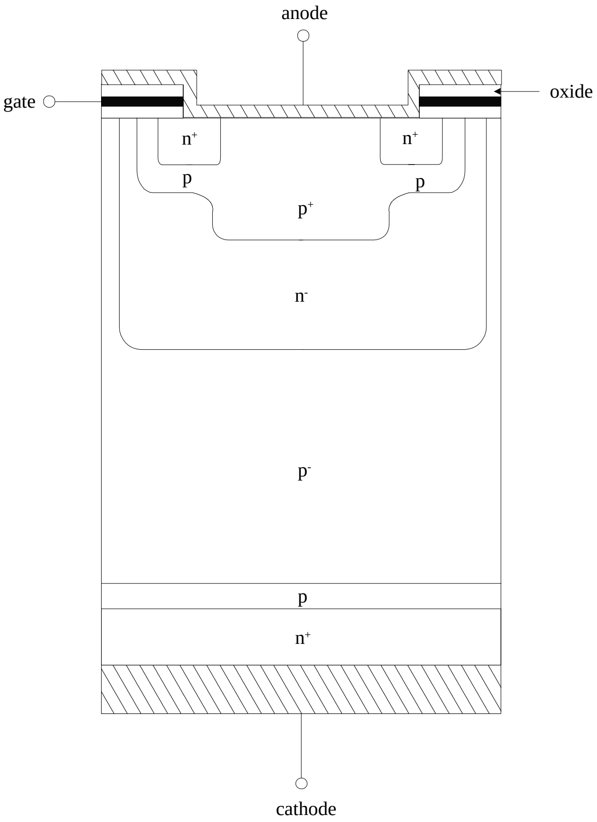

FIGURE 3.17 Cross section of unit-cell of a *p*-type MCT.

tion capability. Both turn-on, which is relatively simple, by comparison, and conduction properties approach the one-dimensional (1D) thyristor limit.

Early generations of MCTs had >50,000 cells connected in parallel. Newer devices have >200,000 cells, with a total active area of 0.38 cm^2. These devices are rated for 1000 V and a peak controllable current of 75 A. All of the cells contain an *n*-channel FET structure to turn off, and 4 have the *p*-channel FET structure to turn the device on. The latest version of the "standard" MCT is a diffusion–doped (instead of the usual epitaxial growth) device with an active area of 1 cm^2. They are rated for 3000-V forward blocking, have a forward drop of 2.5 V at 100 A, and are capable of interrupting around 300 A with a recovery time of 5 μs. Three of these high-voltage devices have been placed in a series array that operates at 5-kV blocking and interrupts 150 A. Other MCTs have been designed to withstand 2.5 kV with a turn-off capability of several kiloamperes per square centimeter per unit cell. Turn-off simulations have been performed for high-voltage MCTs as well as discussion of lateral device designs. A thorough analysis of the interaction of field plates and guard rings in punch-through and non-punch-through structures, for achieving high-voltage planar junctions has also been performed.

Trench- or buried-gate technology has contributed to the reduction of the $R_{\mathrm{on}} \times$ Area product in power MOSFETs by a factor of three or more compared to surface gate devices. An MCT that uses this technology, called a depletion-mode thyristor (DMT), was designed. The cross section of the device and a simple equivalent circuit are shown in Fig. 3.18. The depletion region formed between the trench-gate fingers, by applying a negative gate-cathode voltage, diverts current away from the n^+-emitter (cathode) of the thyristor structure to the collector of a *pnp* transistor structure (also at the cathode) through a lateral resistance (the *p*-base of the thyristor). This current diversion turns off the equivalent *npn* transistor of the thyristor structure, thus depriving the thyristor's *pnp* transistor of any base current and which results in complete turn-off of the device. Depletion mode thyristors were produced that had forward-blocking ratings of 500 V, 1.1 V forward drop at 200 A/cm^2 (a similar IGBT had a forward drop of 2 V at the same current density), and could control a maximum current density of 5000 A/cm^2. A similar device is the base resistance controlled thyristor (BRT). Here, a *p*-channel MOSFET is integrated into the *n*-drift region of the MCT, and is used to modulate the lateral *p*-base resistance of the thyristor, causing the holding current to increase above the conduction value, thus achieving turn-off. Some BRTs were fabricated with 600-V blocking capability and an active area of 1.3 mm^2 (315 cells). These devices operate in an "IGBT" mode until the current is large enough to cause the thyristor structure to latch. The forward drop was 1.24 V at 300 A/cm^2, about the same as a similarly fabricated thyristor.

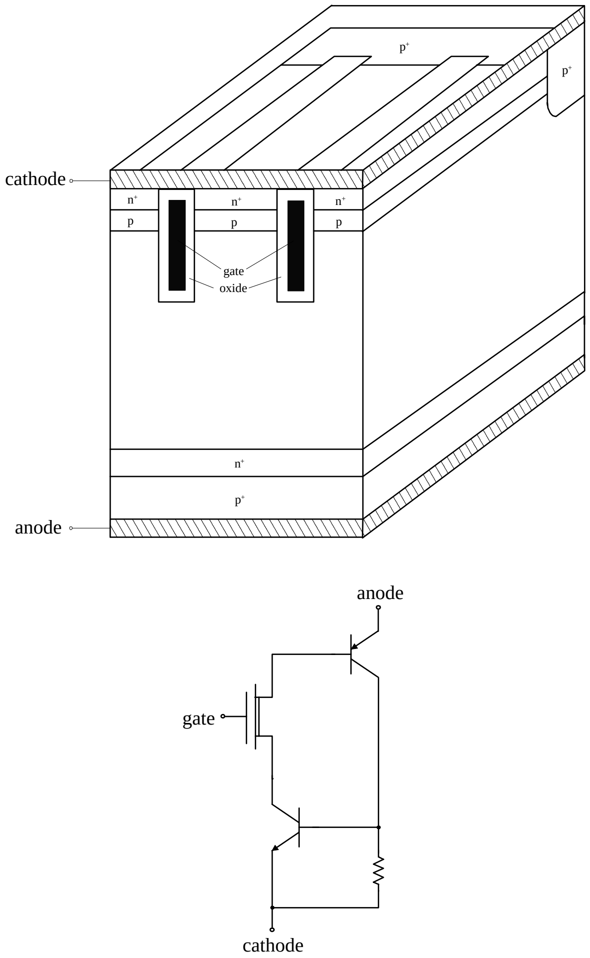

FIGURE 3.18 Cross section and equivalent circuit for a depletion-mode thyristor (DMT).

Another new MCT structure has been demonstrated. Called an emitter switched thyristor (EST), it uses an integrated lateral MOSFET to connect a floating thyristor *n*-emitter region to an n^+-thyristor cathode region, as shown in Fig. 3.19. The lateral MOS structure is such that it can initially turn on the thyristor's *pnp* transistor. When enough anode current flows, the *p*-base-*n*-floating-emitter junction injects carriers and the thyristor latches (the EST moves from an IGBT-like operating mode to a latched thyristor mode). All thyristor current flows through the lateral MOSFET so that it can control the thyristor current. The gate can lose control if the thyristor current becomes excessive so that the parallel parasitic thyristor latches. The ESTs were designed for 600-V forward-blocking and can interrupt 1000 A/cm^2 per unit cell with a turn-off time ≈7 μs. Integrating an IGBT into a thyristor structure has been proposed. This device, called an IGBT-triggered thyristor (ITT), is similar in structure and operation to the EST. Two-dimensional (2D) simulations comparing switching of an inductive load and conduction performance of the ITT to a conventional IGBT have indicated

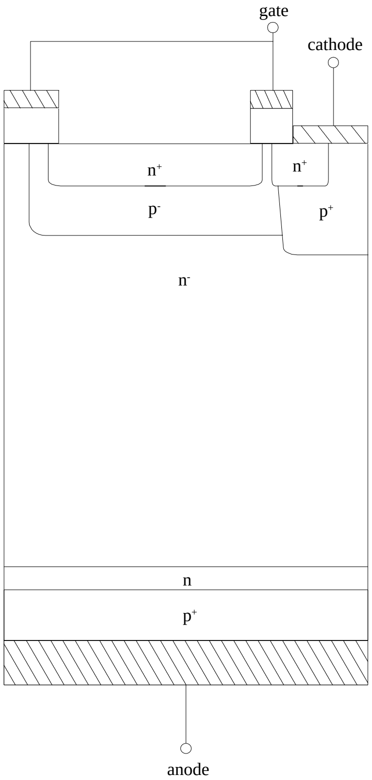

FIGURE 3.19 Cross section of a unit-cell of an emitter switched thyristor (EST).

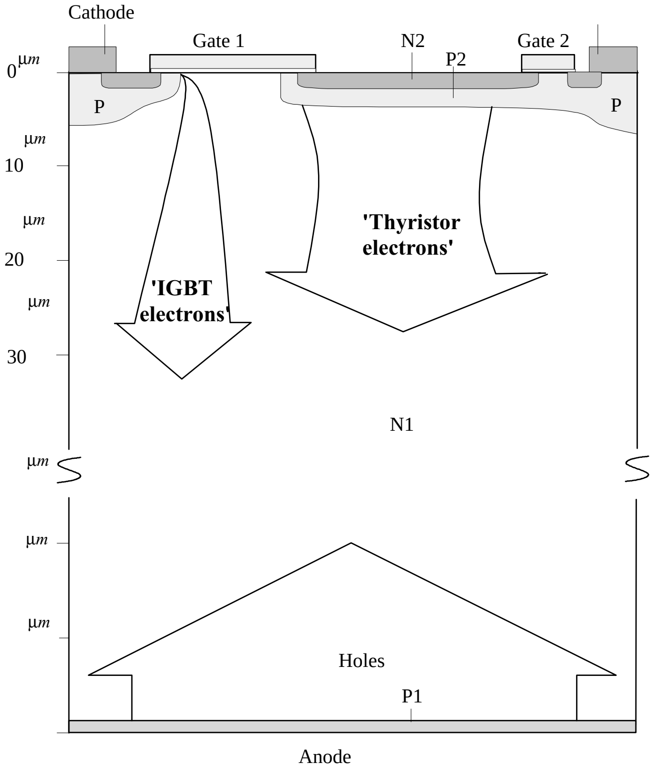

FIGURE 3.20 Cross-section of a unit-cell of a dual gate emitter switched thyristor (DG-EST).

that the ITT has a lower forward drop (0.5 V lower at 100 A/cm^2) with only a slightly increased turn-off time: 0.19 μs for the ITT and 0.16 μs for the IGBT.

The best designed EST is the dual gate emitter switched thyristor (DG-EST) [12]. The structure is shown in Fig. 3.20. The leftmost gate controls the IGBT current, as indicated in the figure. The rightmost gate forms the MOS channel in series with the thyristor current. The second gate determines whether the thyristor section is in or out. Switching as an IGBT has considerable advantages in terms of controllability, particularly in practical circuits.

There are a number of important features in the DG-EST. The IGBT section, creating the "IGBT electrons" is similar to a conventional modern IGBT design. The good shorting essential to latch-up free operation can be identified by the deep *p*-well along with the cathode metallization. The thyristor structure is unlike that of typical discrete thyristor devices in that the junctions are very shallow, in order to make them compatible with IGBT processing. However, similarities to conventional thyristors exist in that the N2 region must be heavily doped for good electron injection efficiency. Further, in common with conventional thyristors, the P2 region is shorted. Here, the shorting would appear excessive, except that the *p*-doping is carefully controlled to give a lateral resistance, and unwanted turn-on is not possible as the N2 emitter is separately controlled by its own lateral MOS channel.

The DG-EST is intended to be switched in IGBT mode, so as to exploit the controllability and snubberless capabilities of an IGBT. Thus, the lateral MOS channel is only turned on after the voltage across the device has started falling. At turn-off, the lateral MOS channel is turned off a short time before the IGBT section starts to switch. As the lateral MOS only turns off into the IGBT on-state, it needs only a low blocking voltage. Therefore, it can be a good quality lateral device that introduces a low additional voltage in the on-state.

3.6.3 Static Induction Thyristors

A static induction thyristor (SITh) or field controlled thyristor (FCTh) has a cross section similar to that shown in Fig. 3.21. Other SITh configurations have surface gate structures. The device is essentially a *pin* diode with a gate structure that can pinch-off anode current flow. Large area devices are generally the buried-gate type because larger cathode areas and, hence, larger current densities are possible. Planar gate devices have been fabricated with blocking capabilities of up to 1.2 kV and conduction currents of 200 A, while step-gate (trench-gate) structures have been produced that are able to block up to 4 kV and conduct 400 A. Similar devices with a "Verigrid"

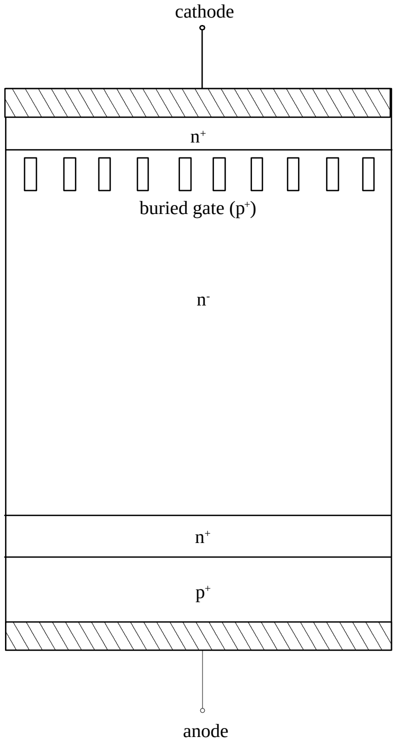

FIGURE 3.21 Cross section of a static induction thyristor (SITh) or field-controlled thyristor (FCT).

structure have been demonstrated that can block 2 kV and conduct 200 A, with claims of up to 3.5-kV blocking and 200-A conduction. Buried gate devices that block 2.5 kV and conduct 300 A have also been fabricated.

3.6.4 Optically Triggered Thyristors

Optically gated thyristors have traditionally been used in power utility applications where series stacks of devices are necessary to achieve the high voltages required. Isolation between gate drive circuits for circuits such as static VAR compensators and high-voltage dc to ac inverters have driven the development of this class of devices. One of the most recent devices can block 6 kV forward and reverse, conduct 2.5 kA average current, and maintains a di/dt capability of 300 A/μs, and a dv/dt capability of 3000 V/μs, with a required trigger power of 10 mW. An integrated light-triggered and light-quenched static induction thyristor has been produced that can block 1.2 kV and conduct up to 20 A (at a forward drop of 2.5 V). This device is an integration of a normally off, buried-gate static induction photothyristor and a normally off, *p*-channel Darlington surface-gate static induction phototransistor. The optical trigger and quenching power required is <5 and 0.2 mW, respectively.

3.6.5 Bidirectional Control Thyristor

The Bidirectional control thyristor (BCT) is an integrated assembly of two antiparallel thyristors on one Si wafer. The intended application for this switch is in VAR compensators, static switches, soft starters, and motor drives. These devices are rated at up to 6.5 kV blocking. Cross talk between the two halves has been minimized. A cross section of the BCT is shown in Fig. 3.22. Note that each surface has a cathode and an anode (opposite devices). The small gate-cathode periphery necessarily restricts the BCT to low-frequency applications because of its di/dt limit.

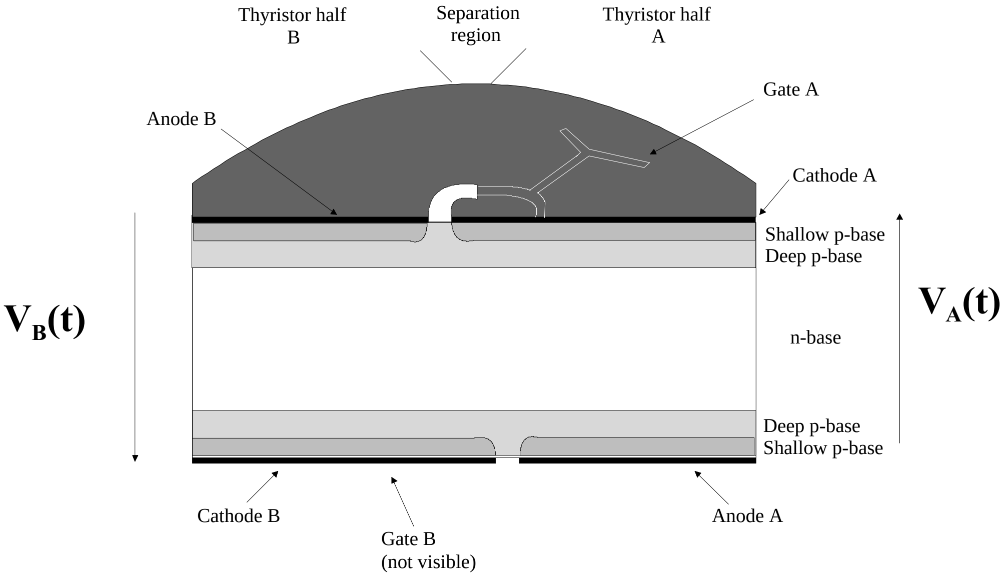

FIGURE 3.22 Cross section of a bidirectional control thyristor (BCT).

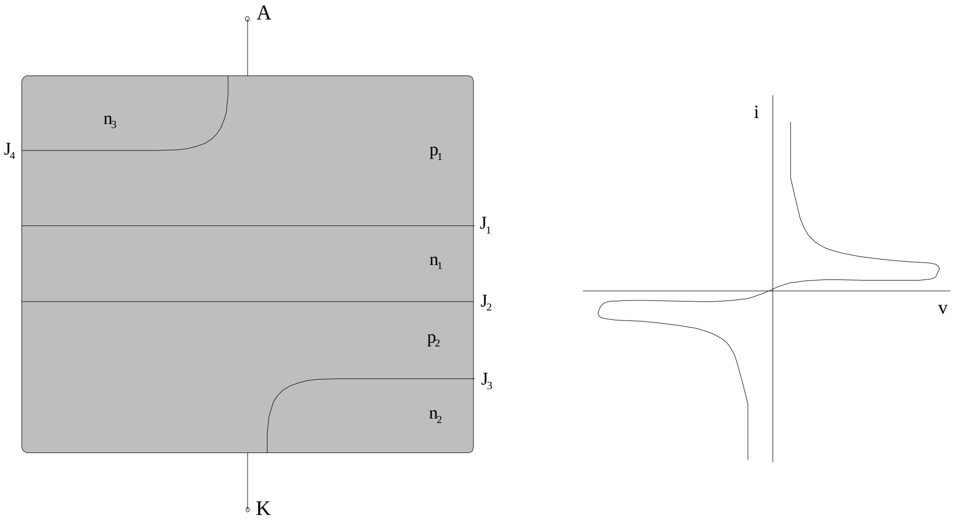

FIGURE 3.23 Cross section and *iv* plot of a Triac.

A low-power device similar to the BCT, but in existence for many years, is the Triac. A simplified cross section of a Triac is shown in Fig. 3.23. A positive voltage applied to the anode with respect to the cathode forward-biases J_1, while reverse-biasing J_2; J_4, and J_3 are shorted by the metal contacts. When J_2 is biased to breakdown, a lateral current flows in the p_2-region. This lateral flow forward-biases the edge of J_3, causing carrier injection. The result is that the device switches into its thyristor mode and latches. Applying a reverse voltage causes the opposite behavior at each junction, but with the same result. Figure 3.23 also shows the *iv* plot for a Triac. The addition of a gate connection allows the breakover to be controlled at a lower forward voltage.

3.7 Gate Drive Requirements

3.7.1 Snubber Circuits

To protect a thyristor, from a large di/dt during turn-on and a large dv/dt during turn-off, a snubber circuit is needed. A general snubber topology is shown in Figure 3.24. The turn-on snubber is made by inductance L_1 (often L_1 is stray inductance only). This protects the thyristor from a large di/dt during the turn-on process. The auxiliary circuit made by R_1 and D_1 allows the discharging of L_1 when the thyristor is turned off. The turn-off snubber is made by resistor R_2 and capacitance C_2. This circuit protects a GTO from large dv/dt during the turn-off process. The auxiliary circuit made by D_2 and R_2 allows the discharging of C_2 when the thyristor is turned on. The circuit of capacitance C_2 and inductance L_1 also limits the value of dv/dt across the thyristor during forward blocking. In addition, L_1 protects the thyristor from reverse over-currents.

3.7.2 Gate Circuits

It is possible to turn on a thyristor by injecting a current pulse into its gate. This process is known as gating the thyristor. The most important restrictions are on the maximum peak and duration of the gate pulse current. In order to allow a safe turn-on commutation, the current pulse should be high

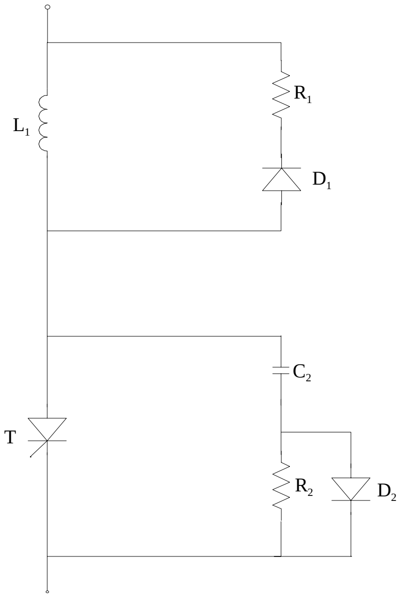

FIGURE 3.24 Turn-on (top elements) and turn-off (bottom elements) snubber circuits for thyristors.

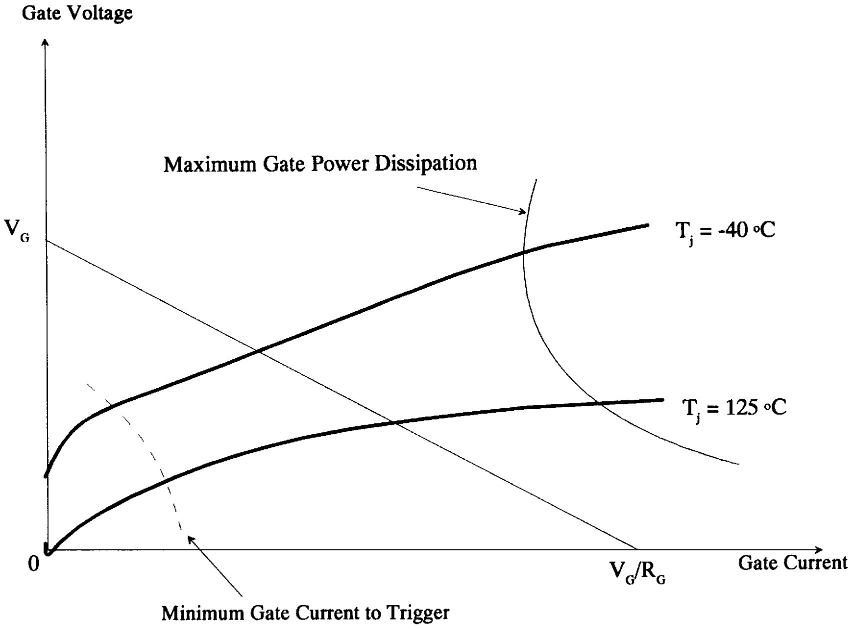

FIGURE 3.25 Gate *i-v* curve for a typical thyristor.

enough and, in order to avoid an unwanted turn-off immediately after the turn-on, it should last for a sufficient time. In estimating how large the gate current pulse should be to ensure device turn on, the gate current-voltage characteristic, which is given with the device data sheet, must be used. An example of this kind of data sheet is shown in Fig. 3.25.

In Fig. 3.25 are shown the gate current-voltage characteristics for the maximum and minimum operating temperatures. The dashed line represents the minimum gate current and corresponding gate voltage needed to ensure that the thyristor will be triggered at various operating temperatures. It is also known as the locus of minimum firing points. On the data sheet it is possible to find a line representing the maximum operating power of the thyristor gating internal circuit. The straight line, between V_G and V_G/R_G, represents the current voltage characteristic of the equivalent trigger circuit. If the equivalent trigger circuit line intercepts the two gate current-voltage characteristics for the maximum and minimum operating temperatures after they intercept the dashed line and before they intercept the maximum operating power line, then the trigger circuit is able to turn on the thyristor at any operating temperature without destroying or damaging the device.

Another feature of the gating process that should be analyzed is the fast turn-on required for these devices. In order to allow a fast turn-on, and correspondingly large anode di/dt during the turn-on process, a large gate current pulse is supplied during the initial turn-on phase with a large di_G/dt. The gate current is kept on, at lower value, for some time after the thyristor is turned on in order to avoid unwanted turn-off of the device. A shaped gate current waveform of this type is shown in Fig. 3.26.

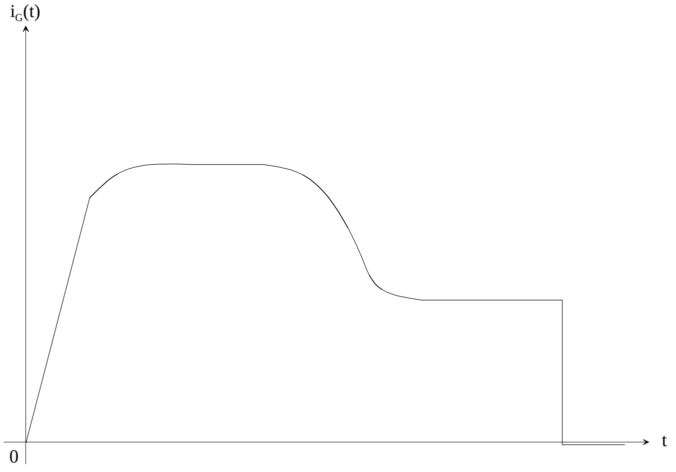

FIGURE 3.26 Gate current waveform showing large initial current followed by a suitable back-porch value.

In order to keep the power and control circuits electrically unconnected, the gate signal generator and the gate of the thyristor are often connected through a transformer. There is a transformer winding for each thyristor; this way, unwanted short-circuits between devices are avoided. A general block diagram of a thyristor gate-trigger circuit is shown in Fig. 3.27. This application is for a standard bridge configuration often used in power converters.

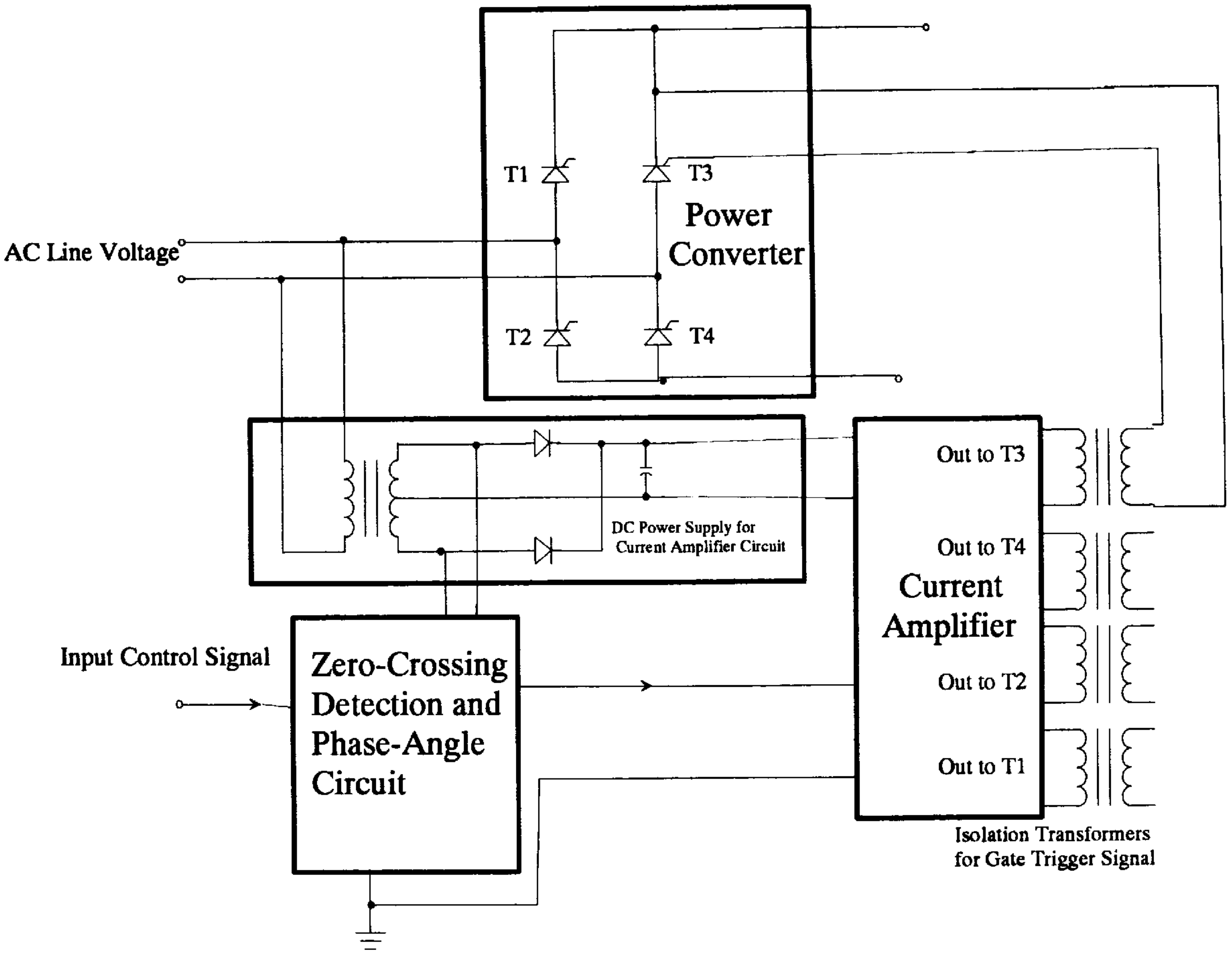
AC Line Voltage
T1
T2
T3
T4
Power Converter
DC Power Supply for Current Amplifier Circuit
Input Control Signal
Zero-Crossing Detection and Phase-Angle Circuit
Out to T3
Out to T4
Current Amplifier
Out to T2
Out to T1
Isolation Transformers for Gate Trigger Signal

FIGURE 3.27 Block diagram of a transformer-isolated gate drive circuit.

Another problem can arise if the trigger circuit produces just one pulse and there exists an RL-type load. For example, if the circuit is a single-phase controlled bridge, the load is only resistive, and then delay angle between the load current and voltage across is 0°. If the load is an RL-type, the load current will reach zero after the voltage across it does. It could happen that a thyristor is triggered before the opposite one is turned off, and because of the short time of the current pulse, it becomes impossible to control the bridge in the desired way. A possible solution to this problem could be the generation of a longer current pulse. Because of the presence of the transformer, a solution like the one just described is not possible. An alternative solution can be the generation of a series of short pulses that last as long as a long single pulse. A single short pulse, a single long pulse, and a series of short pulses are shown in Fig. 3.28.

There are many gate trigger circuits that use optical isolation between the logic-level electronics and a drive stage (typically MOSFETs) configured in a push-pull output. The dc power supply voltage for the drive stage is provided through transformer isolation. Many device manufacturers supply drive circuits available on PC boards or diagrams of suggested circuits.

3.8 PSpice Model

Circuit simulators such as Spice and PSpice are widely used as tools in the design of power systems. For this purpose equivalent circuit models for thyristors have been developed. A variety of models have been proposed with varying degrees of complexity and accuracy. Many times the simple two-transistor model described in Section 3.2 is used in PSpice. This simple structure, however, cannot create the appropriate negative-differential-resistance (*ndr*) behavior as the thyristor moves from forward-blocking to forward-conduction. A

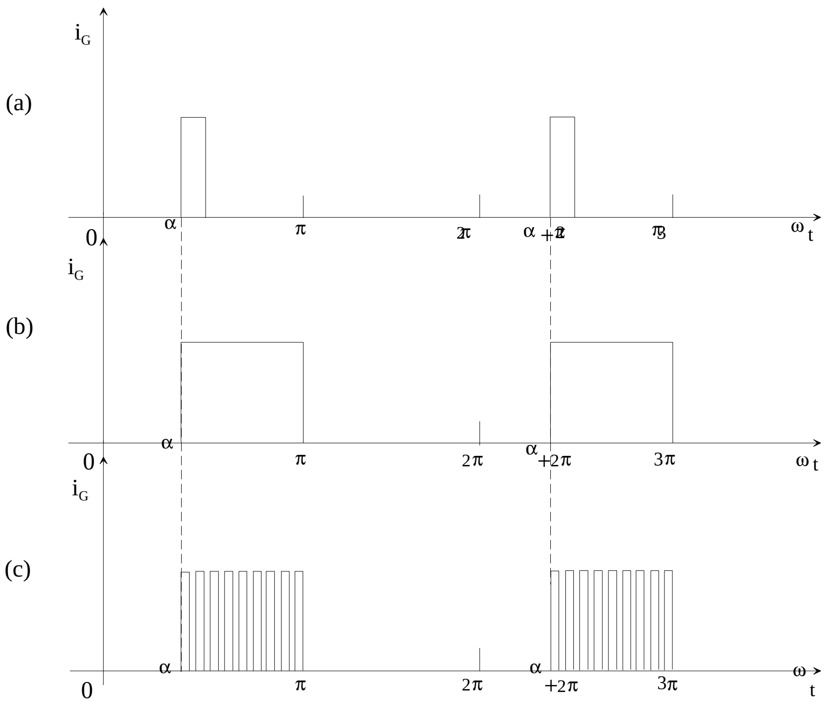

FIGURE 3.28 Gate pulses used as an alternative to one long current pulse.

PSpice model for a GTO developed by Tsay *et. al.* [13] captures many of the behaviors of thyristors. This model creates device characteristics such as the static I-V curve shown in Fig. 3.3, dynamic characteristics such as turn-on and turn-off times, device failure modes such as current crowding due to excessive di/dt at turn-on, and spurious turn-on due to excessive dv/dt at turn-off, thermal effects, and so on. Specifically, three resistors are added to the two-transistor model to create the appropriate behavior.

The proposed two-transistor, three-resistor model ($2T$-$3R$) is shown in Fig. 3.29. This circuit exhibits the desired NDR behavior. Given the static I-V characteristics for an SCR or GTO, it is possible to obtain similar curves from the model by choosing appropriate values for the three resistors and for the forward current gains α_p and α_n of the two transistors. The process of curve-fitting can be simplified by keeping in mind that resistor R_1 tends to affect the negative slope of the I-V characteristic, resistor R_2 tends to affect the value of the holding current I_H, and resistor R_3 tends to affect the value of the forward breakdown voltage V_{FBD}. When modeling thyristors with cathode or anode shorts, as described in Section 3.4, the presence of these shorts determines the values of R_1 and R_2, respectively. In the case of a GTO an important device characteristic is the so-called turn-off gain $K_{\text{off}} = I_A/|I_G|$, that is, the ratio of the anode current to the negative gate current required to turn off the device. An approximate formula relating the turn-off gain to the α's of the two transistors is given in what follows:

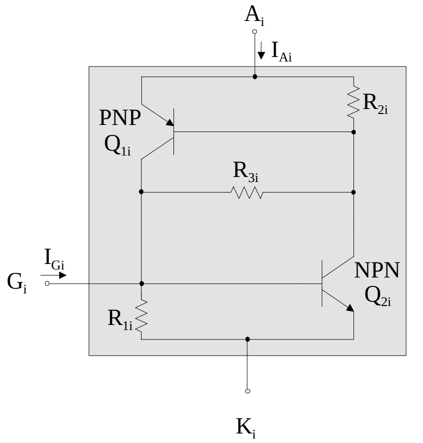

FIGURE 3.29 A two-transistor, three-resistor model for SCRs and GTOs.

$$K_{\text{off}} = \frac{\alpha_n}{\alpha_n + \alpha_p - 1} \tag{3.3}$$

The ability of this model to predict dynamic effects depends on the dynamics included in the transistor models. If transistor junction capacitances are included, it is possible to model the dv/dt limit of the thyristor. Too high a value of dv_{AK}/dt will cause significant current to flow through the J_2 junction capacitance. This current acts like a gate current and can turn on the device.

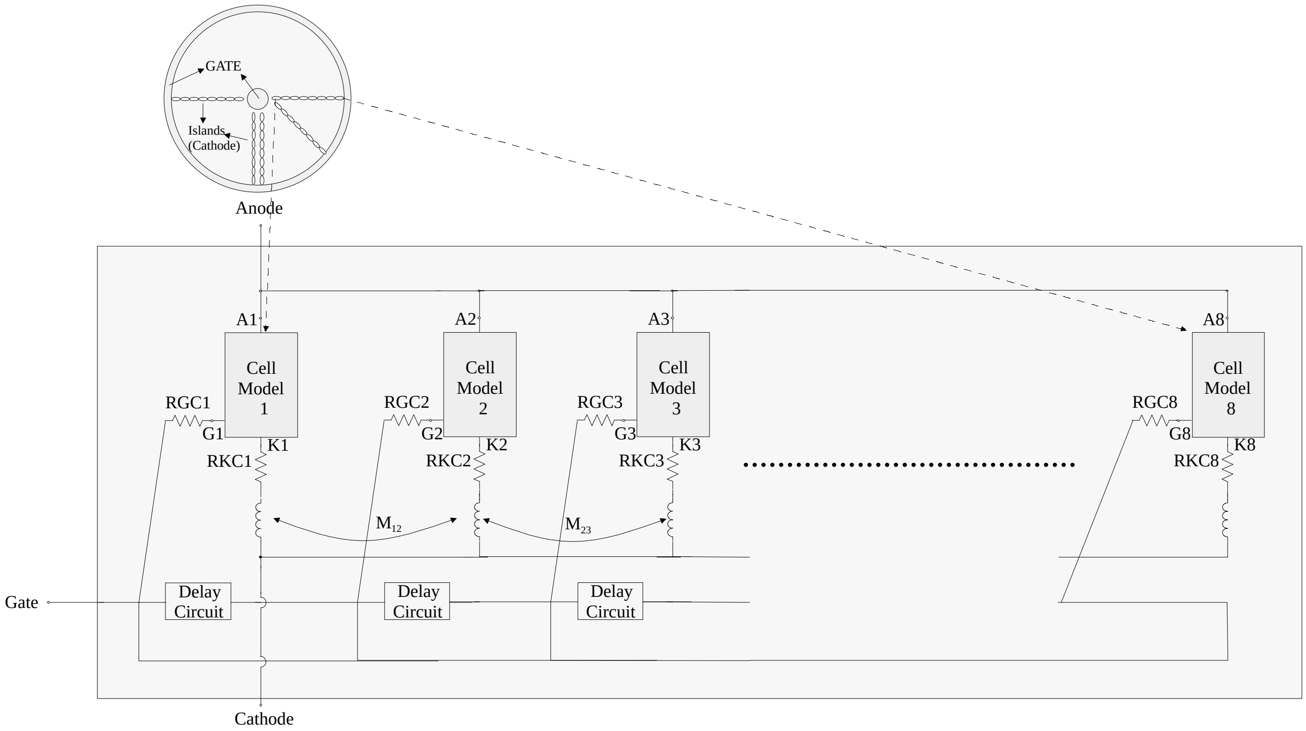
GATE
Islands
(Cathode)
Anode
A1
A2
A3
A8
Cell Model 1
Cell Model 2
Cell Model 3
Cell Model 8
RGC1
RGC2
RGC3
RGC8
G1
G2
G3
G8
K1
K2
K3
K8
RKC1
RKC2
RKC3
RKC8
M_{12}
M_{23}
Gate
Delay Circuit
Delay Circuit
Delay Circuit
Cathode

FIGURE 3.30 Thyristor multicell circuit model containing eight cells.

This model does not accurately represent spatial effects such as current crowding at *turn-on* (the di/dt limit), when only part of the device is conducting, and, in the case of a GTO, current crowding at *turn-off*, when current is extracted from the gate to turn off the device. Current crowding is caused by the location of the gate connection with respect to the conducting area of the thyristor and by the magnetic field generated by the changing conduction current. Gate-contact and cathode-contact resistance can be included for each cell as well. To model these effects, Tsay *et al.* [13] propose a multicell circuit model, in which the device is discretized in a number of conducting cells, each having the structure of Fig. 3.30. This model, shown in Fig. 3.31, takes into account the mutual inductive coupling, the delay in the gate turn-off signal due to positions of the cells relative to the gate connection, and nonuniform gate- and cathode-contact resistance. In particular, the *RC* delay circuits (series *R* with a shunt *C* tied to the cathode node) model the time delays between the gate triggering signals due to the position of the cell with respect to the gate connection; coupled inductors, *M*'s, model magnetic coupling between cells; resistors, R_{KC}'s, model nonuniform contact resistance; resistors, R_{GC}'s, model gate contact resistances. The various circuit elements in the model can be estimated from device geometry and measured electrical characteristics. The choice of the number of cells is

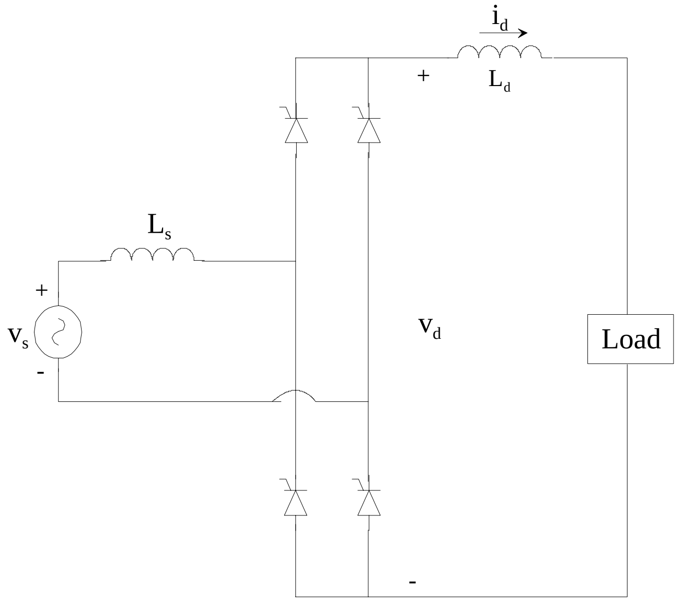
i_d
+
L_d
L_s
+
v_s
-
V_d
Load
-

FIGURE 3.31 Single-phase controlled rectifier circuit.

TABLE 3.6 Element values for each cell of a multicell GTO model

Model Component	Symbol	Vaue
Delay resistor	R	1 μΩ
Delay capacitor	C	1 nF
Mutual coupling inductance	M	10 nH
Gate contact resistance	R_{GC}	1 mΩ
Cathode contact resistance	R_{KC}	1 mΩ

a trade-off between accuracy and complexity. An example of the values of the RC delay network, R_{GC}'s, R_{KC}'s, M's is given in Table 3.6.

3. Applications

The most important application of thyristors is for line-frequency, phase-controlled rectifiers. This family includes several topologies, of which one of the most important is used to construct high voltage dc (HVDC) transmission systems. A single-phase controlled rectifier is shown in Fig. 3.31.

The presence of thyristors makes the average output voltage controllable by appropriate gating of the thyristors. If the gate signals to the thyristors were continuously applied, the thyristors in Fig. 3.31 behave as diodes. If no gate currents are supplied they behave as open circuits. Gate current can be applied any time (phase delay) after the forward voltage becomes positive. Using this phase-control feature it is possible to produce an average output voltage less than the average output voltage obtained from an uncontrolled rectifier.

3. .1 Direct current-Alternating current Utility Inverters

Three-phase converters can be made in different ways, according to the system in which they are employed. The basic circuit used to construct these topologies is shown in Fig. 3.32.

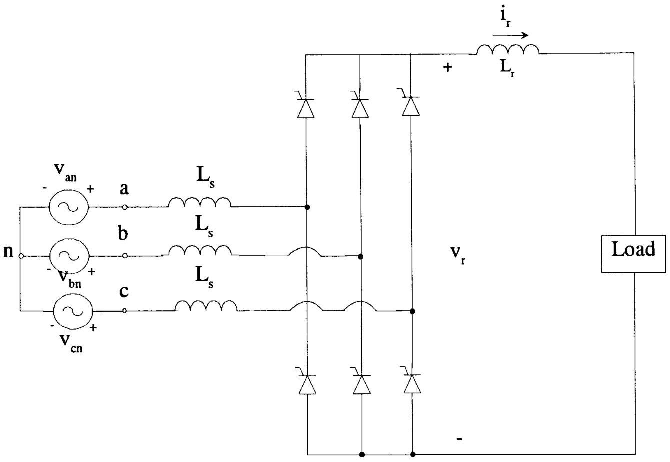
i_r
+
L_r
V_{an}
- +
a
L_s
b
L_s
n
V_{bn}
c
L_s
V_{cn}
v_r
Load
-

FIGURE 3.32 A 3-phase controlled bridge circuit used as a basic topology for many converter systems.

The thyristors in the circuit of Fig. 3.32 are used in the same way they were used in single-phase circuits but necessarily with more complex control. Starting from this basic configuration, it is possible to construct more complex circuits in order to obtain high-voltage or high-current outputs, or just to reduce the output ripple by constructing a multiphase converter. One of the most important systems using the topology shown in Fig. 3.32 as a basic circuit is the HVDC system represented in Fig. 3.33. This system is made by two converters, a transmission line, and two ac systems. Each converter terminal is made of two poles. Each pole is made by connecting two 6-pulse line-frequency converters through

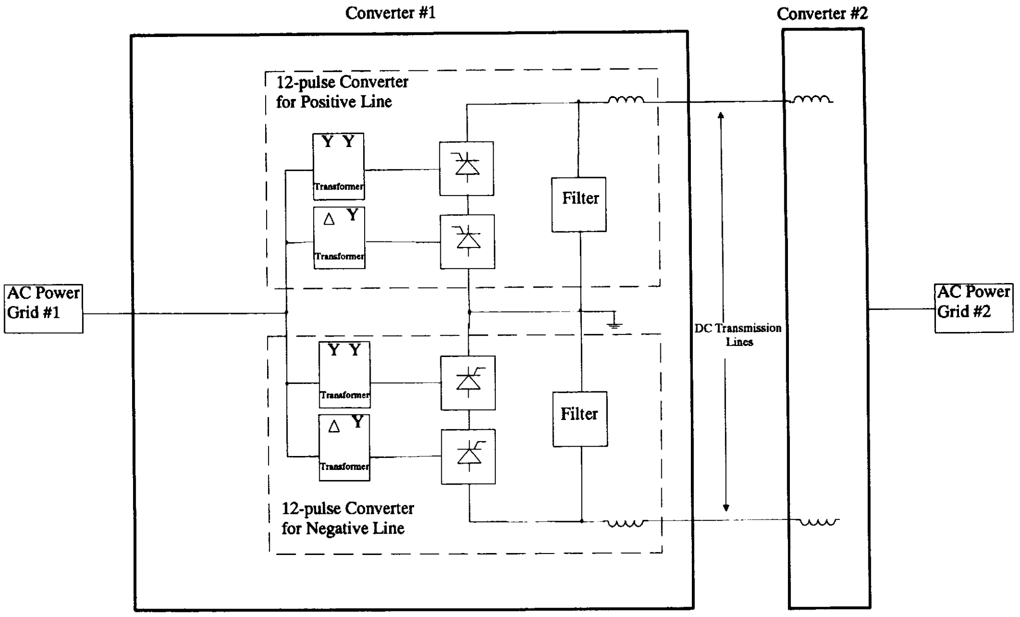
Converter #1
Converter #2
12-pulse Converter for Positive Line
Y Y
Transformer
Δ Y
Transformer
Filter
AC Power Grid #1
AC Power Grid #2
DC Transmission Lines
Y Y
Transformer
Δ Y
Transformer
Filter
12-pulse Converter for Negative Line

FIGURE 3.33 A high-voltage dc (HVDC) transmission system.

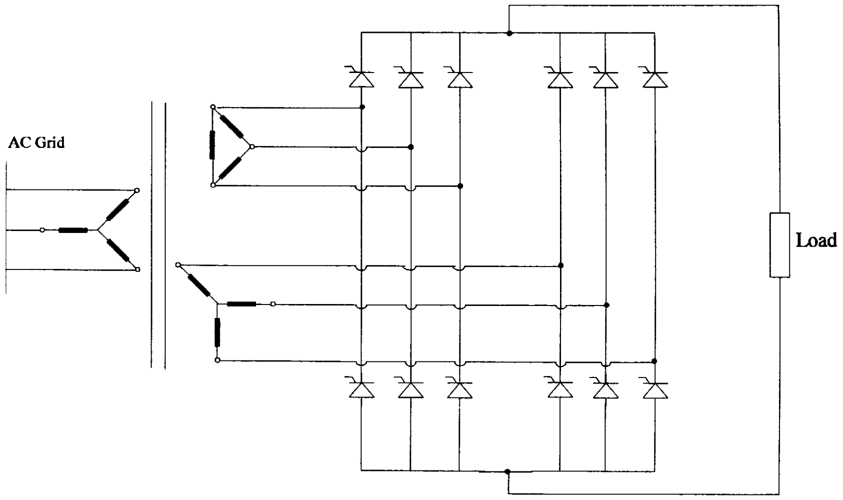

FIGURE 3.34 Parallel connection of two 6-pulse converters for high-current applications.

Δ-Y and Y-Y transformers in order to obtain a 12-pulse converter and a reduced output ripple. The filters are required to reduce the current harmonic generated by the converter. Thyristors are required in order to reduce the voltage amplitude to the ac voltage amplitude level by appropriate switching action.

When a large amount of current and relatively low voltage is required, it is possible to connect, using a specially designed inductor, two 6-pulse line-frequency converters connected through Δ-Y and Y-Y transformers. This topology is shown in Fig. 3.34.

3. .2 Motor Control

Another important application of thyristors is in motor control circuits. They are used to construct the first stage of an electric motor drive in order to vary the amplitude of the voltage waveform across the windings of the electrical motor as it is shown in Fig. 3.35.

An electronic controller controls the gate current of these thyristors. The rectifier and inverter sections can be thyristor circuits. A controlled rectifier is used in conjunction with a square wave or pulse-width modulated (PWM) voltage source inverter (VSI) to create the speed-torque controller system. Figure 3.36 shows a square-wave or PWM VSI with a controlled rectifier on the input side. The switch block inverter is made of thyristors (usually GTOs) for high power. Low-power motor controllers often use IGBT inverters.

In motor control, thyristors are also used in current-source inverter (CSI) topologies. When the motor is controlled by a CSI, a controlled rectifier is also needed on the input side. Figure 3.37 shows a typical CSI inverter.

Diodes, capacitors, and the motor leakage inductance make a forced commutation circuit. These circuits are needed to force the current through the thyristors to zero, in order to turn them off if using SCRs. This is not needed when using GTOs. This inverter topology does not need any additional circuitry to provide the regenerative braking (energy recovery when slowing the motor). To allow bidirectional power flow,

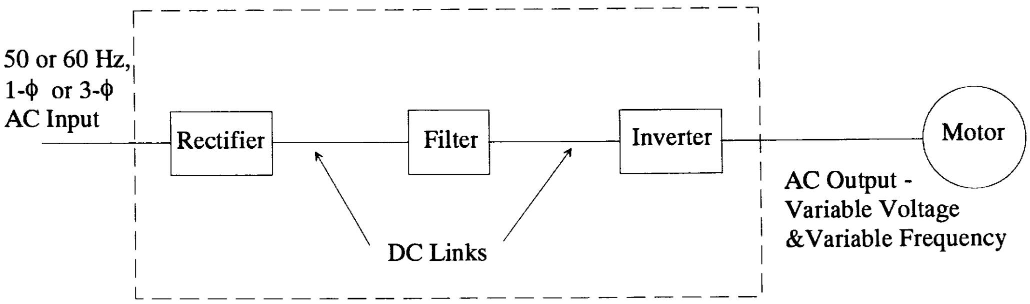

FIGURE 3.35 Variable frequency converter for motor control.

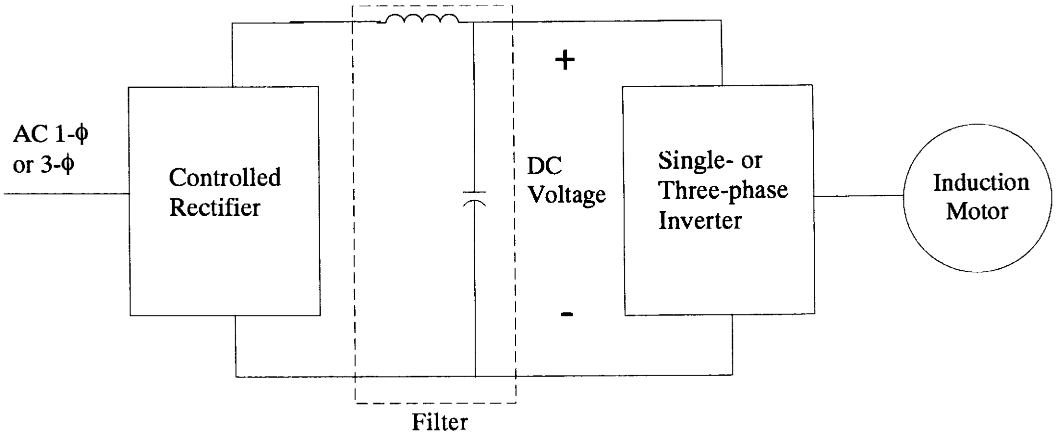

FIGURE 3.36 Pulsewidth modulated or square-wave inverter with a controlled rectifier input.

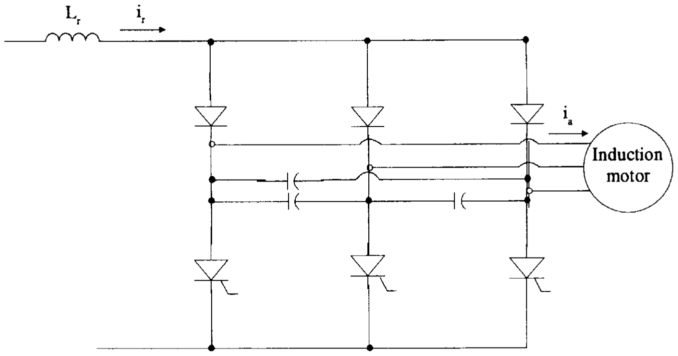

FIGURE 3.37 Current-source inverter on the output section of a motor drive system using capacitors for power factor correction.

then to allow regenerative braking, two back-to-back connected line-frequency thyristor converters used to be employed in the past. Use of antiparallel GTOs with symmetric blocking capability or diodes in series with each asymmetric GTO reduces the number of power devices needed, but greatly increases the control complexity.

3. .3 VAR Compensators and Static Switching Systems

Thyristors are also used to switch capacitors (TSC) or inductors (TCI) in order to control the reactive power in the system. An example of these circuits is shown in Fig. 3.38. These circuits act as a static VAR (volts-amps reactive) controller. The topology represented on the left-hand side of Fig. 3.38 is called a thyristor-controlled inductor (TCI) and it acts as a variable inductor where the inductive VAR supplied can be varied quickly. Because the system may require either inductive or capacitive VAR, it is possible to connect a bank of capacitors in parallel with a TCI. The topology shown on the right-hand side of Fig. 3.38 is called a thyristor-switched capacitor (TSC). Capacitors can be switched out by blocking the gate pulse of all thyristors in the circuit. The problem of this topology is the voltage across the capacitors at the thyristor turn-off. At turn-on the thyristor must be gated at the instant of the maximum ac voltage to avoid large overcurrents.

A less important application of thyristors is as a static transfer switch, used to improve the reliability of uninterruptible power supplies (UPS) as shown in Fig. 3.39. There are two modes of using the thyristors. The first leaves the load permanently connected to the UPS system and in case of emergency disconnects the load from the UPS and connects it directly to the power line. The second mode is opposite to the first one. Under normal conditions the load is permanently connected to the power line, and in event of a line outage, the load is disconnected from the power line and connected to the UPS system.

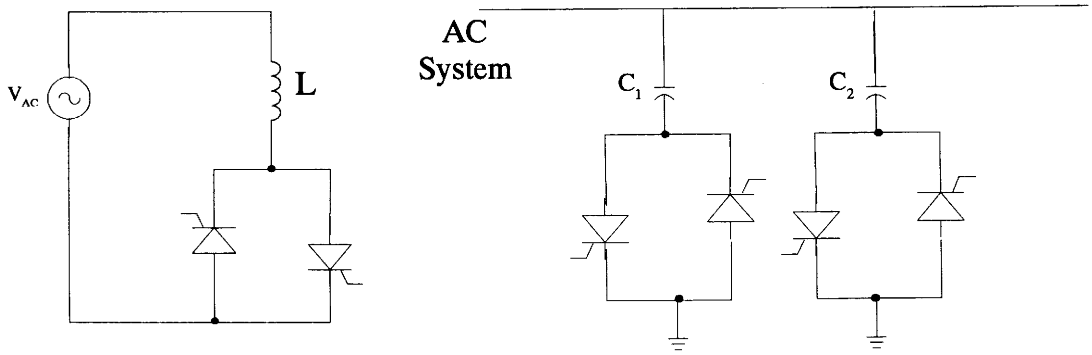

FIGURE 3.38 Per phase thyristor-controlled inductor (TCI) and thyristor-switched capacitor (TSC) system.

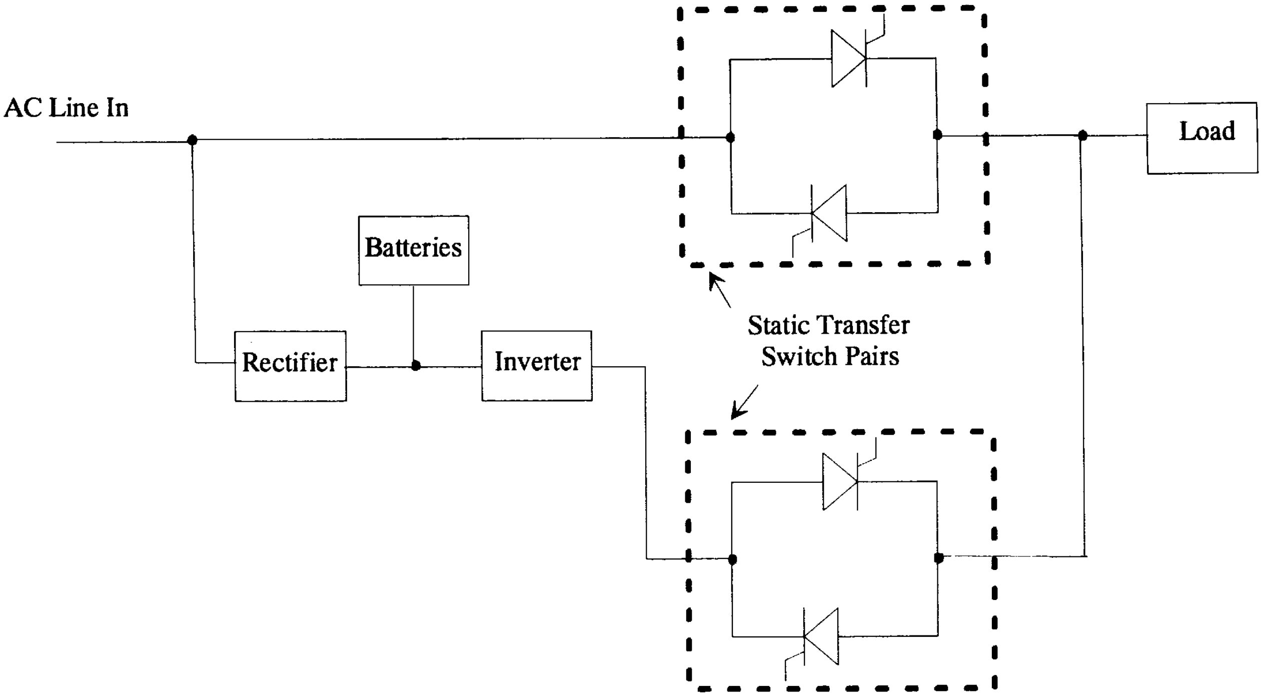

FIGURE 3.39 Static transfer switch used in a UPS system.

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4

ate Turn ff Th ristors

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4.1 Introduction

A gate turn-off thyristor (known as a GTO) is a three-terminal power semiconductor device that belongs to a thyristor family with a four-layer structure. They also belong to a group of power semiconductor devices that have the ability to fully control on and off states via the control terminal (gate). The design, development, and operation of the GTO is easier to understand if we compare it to the conventional thyristor. Like a conventional thyristor, applying a positive gate signal to its gate terminal can turn on a GTO. Unlike a standard thyristor, a GTO is designed to turn off by applying a negative gate signal.

There are two types of GTOs: asymmetrical and symmetrical. The asymmetrical GTOs are the most common type on the market. This type is normally used with an antiparallel diode and hence high reverse-blocking capability is not available. Reverse conducting is accomplished with an antiparallel diode integrated onto the same silicon wafer. The symmetrical GTOs have equal forward- and reverse-blocking capability.

4.2 Basic Structure and Operation

The symbol for a GTO is shown in Fig. 4.1a. A high degree of interdigitation is required in GTOs in order to achieve efficient turn-off. The most common design employs the cathode area separated into multiple segments (cathode fingers) and arranged in concentric rings around the device center. The internal structure is shown in Fig. 4.1b. A common contact disk pressed against the cathode fingers connects the fingers together. It is important that all the fingers turn off simultaneously, otherwise the current may be concentrated into fewer fingers, with damage due to overheating more likely.

The high level of gate interdigitation also results in a fast turn-on speed and high *di*/*dt* performance of GTOs. The most remote part of a cathode region is no more than 0.16 mm from a gate edge and hence the entire GTO can conduct within ≈ 5 µs with sufficient gate drive and the turn-on losses can be reduced. However, interdigitation reduces the available emitter area and therefore the low-frequency average current rating is less than for a standard thyristor with an equivalent diameter.

The basic structure of a GTO, a four-layer *p*-*n*-*p*-*n* semiconductor device, is very similar in construction to a thyristor. It has several design features that allow it to be turned on and off by reversing the polarity of the gate signal. The most important differences are that the GTO has long narrow emitter fingers surrounded by gate electrodes and no cathode shorts.

The turn-on mode is similar to that of a standard thyristor. The injection of the hole current from the gate forward biases the cathode *p*-base junction, causing electron emission from the cathode. These electrons flow to the anode and induce hole injection by the anode emitter. The injection of holes and electrons into the base regions continues until charge multiplication effects bring the GTO into conduction. This is shown in Fig. 4.2a. As with a conventional thyristor, only the area of cathode adjacent to the gate electrode is turned on initially and the remaining area is brought into conduction by plasma spreading. However, unlike the thyristor, the GTO consists of many narrow cathode elements, heavily interdigitated with the gate electrode, and therefore the initial turned-on area is very large and the time required for plasma spreading is small.

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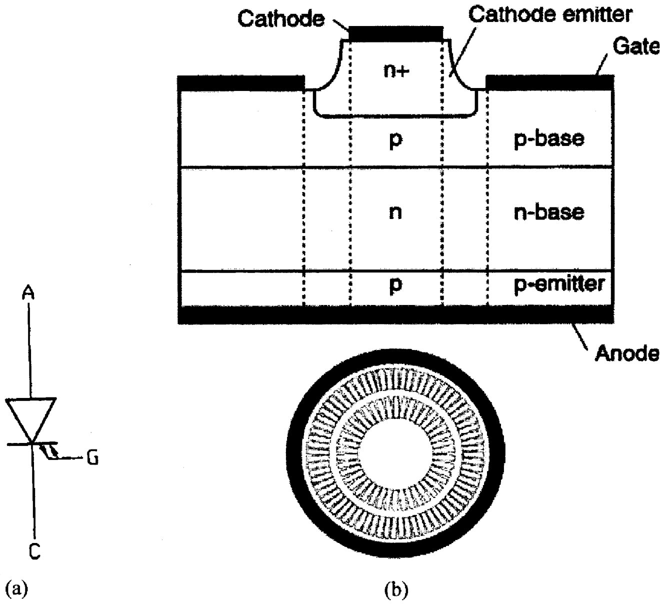


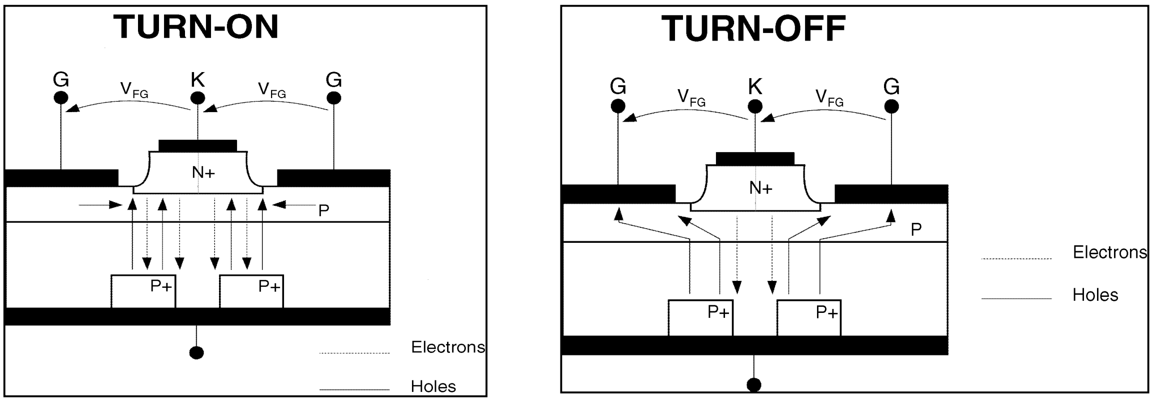
(a) (b)

FIGURE 4.1 GTO structure: (a) GTO symbol; (b) GTO structure.

Therefore, the GTO is brought into conduction very rapidly and can withstand a high turn-on *di*/*dt*.

In order to turn off a GTO, the gate is reversed-biased with respect to the cathode and holes from the anode are extracted from the *p*-base. This is shown in Fig. 4.2b. As a result, a voltage drop is developed in the *p*-base region, which eventually reverse biases the gate cathode junction and cuts off the injection of electrons. As the hole extraction continues, the *p*-base is further depleted, thereby squeezing the remaining conduction area. The anode current then flows through the areas most remote from the gate contacts, forming high current density filaments. This is the most crucial phase of the turn-off process in GTOs because high-density filaments lead to localized heating, which can cause device failure unless these filaments are extinguished quickly. An application of higher negative gate voltage may aid in extinguishing the filaments rapidly. However, the breakdown voltage of the gate-cathode junction limits this method.

When the excess carrier concentration is low enough for carrier multiplication to cease and the device reverts to the forward blocking condition. Although the cathode current has stopped flowing at this point, anode-to-gate current supplied by the carriers from an *n*-base region-stored charge continues to flow. This is observed as a tail current that decays exponentially as the remaining charge concentration is reduced by a recombination process. The presence of this tail current with the combination of high GTO off-state voltage produces substantial power losses. During this transition period, the



(a) (b)

FIGURE 4.2 (a) Turn-on; and (b) turn-off of GTOs.

electric field in the *n*-base region is grossly distorted due to the presence of the charge carriers and may result in premature avalanche breakdown. The resulting impact ionization can cause device failure. This phenomenon is known as "dynamic avalanche." The device regains its steady-state blocking characteristics when the tail current diminishes to leakage current level.

4.3 GTO Thyristor Models

A one-dimensional two-transistor GTO model is shown in Fig. 4.3. The device is expected to yield the turn-off gain *g* given by:

$$A_g = \frac{I_A}{I_G} = \frac{\alpha_{npn}}{\alpha_{pnp} + \alpha_{npn} - 1} \tag{4.1}$$

where I_A is the anode current and I_G the gate current at turn-off, and α_{npn} and α_{pnp} are the common-base current gains in the *n-p-n* and *p-n-p* transistor sections of the device. For a nonshorted device, the charge is drawn from the anode and regenerative action commences, but the device does not latch on (remain on when the gate current is removed) until

$$\alpha_{npn} + \alpha_{pnp} \geq 1 \tag{4.2}$$

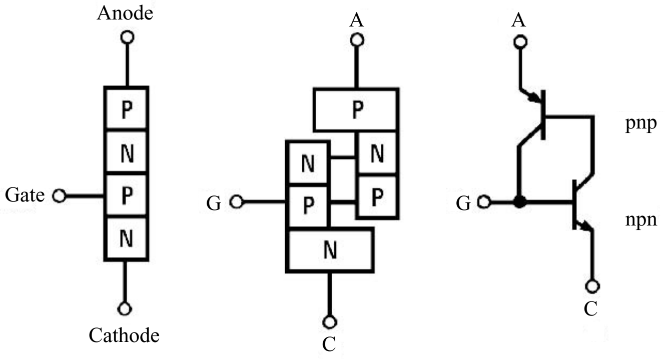


FIGURE 4.3 Two-transistor model representing the GTO thyristor.

This process takes only a short time for the current and the current gains to increase enough to satisfy Eq. (4.2). For anode-shorted devices, the mechanism is similar but the anode short impairs the turn-on process by providing a base–emitter short, thus reducing the *p-n-p* transistor gain, which is shown in Fig. 4.4. The composite *p-n-p* gain of the emitter-shorted structure is given as follows:

$$\alpha_{pnp}(\text{composite}) = \alpha_{pnp}\left(\frac{1 - V_{be}}{R_{\text{Sanode}}}\right) \tag{4.3}$$

where V_{be} = emitter base voltage (generally 0.6 V for injection of carriers) and R_S is the anode-short resistance. The anode emitter injects when the voltage around it exceeds 0.06 V, and therefore the collector current of the *n-p-n* transistor flowing through the anode shorts influences turn-on. The GTO remains in a transistor state if the load circuit limits the current through the shorts.

4.4 Static Characteristics

4.4.1 On-State Characteristics

In the on-state, the GTO operates in a similar manner to the thyristor. If the anode current remains above the holding current level then positive gate drive may be reduced to zero and the GTO will remain in conduction. However, as a result of the turn-off ability of the GTO, it does possess a higher holding current level than the standard thyristor and, in addition, the cathode of the GTO thyristor is subdivided into small finger elements to assist turn-off. Thus, if the GTO thyristor anode current transiently dips below the holding current level, localized regions of the device may turn off,

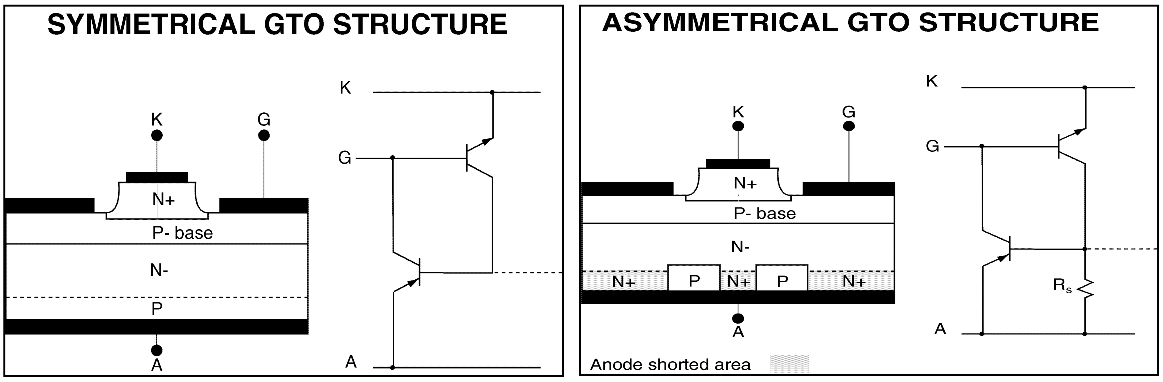


FIGURE 4.4 Two-transistor models of GTO structures.

thus forcing a high anode current back into the GTO at a high rate of rise of anode current after this partial turn-off. This situation could be potentially destructive. Therefore, it is recommended that the positive gate drive not be removed during conduction but held at a value $I_{G(ON)}$ where $I_{G(ON)}$ is greater than the maximum critical trigger current (I_{GT}) over the expected operating temperature range of the GTO thyristor.

Figure 4.5 shows the typical on-state *v-I* characteristics for a 4000-A, 4500-V GTO from the Dynex range of GTOs [1] at junction temperatures of 25 and 125 °C. The curves can be approximated to a straight line of the form:

$$V_{TM} = V_0 + IR_0 \tag{4.4}$$

where V_0 = voltage intercept and it models the voltage across the cathode and anode forward-biased junctions, and R_0 =on-state resistance. When average and RMS values of on-state current (I_{TAV}, I_{TRMS}) are known, then the on-state power dissipation P_{ON} can be determined using V_0 and R_0. That is,

$$P_{ON} = V_0 I_{TAV} + R_0 I^2_{TRMS} \tag{4.5}$$

14.4.2 Off-State Characteristics

Unlike the standard thyristor, the GTO does not include cathode emitter shorts to prevent nongated turn-on effects due to *dv/dt*-induced forward-biased leakage current. In the off-state of the GTO, steps should therefore be taken to prevent such potentially dangerous triggering. This can be accomplished by either connecting the recommended value of resistance between gate and cathode (R_{GK}) or maintaining a small reverse bias on the gate contact ($V_{RG} = -2$ V). This will prevent the cathode emitter from becoming forward-biased and will therefore sustain the GTO thyristor in the off state.

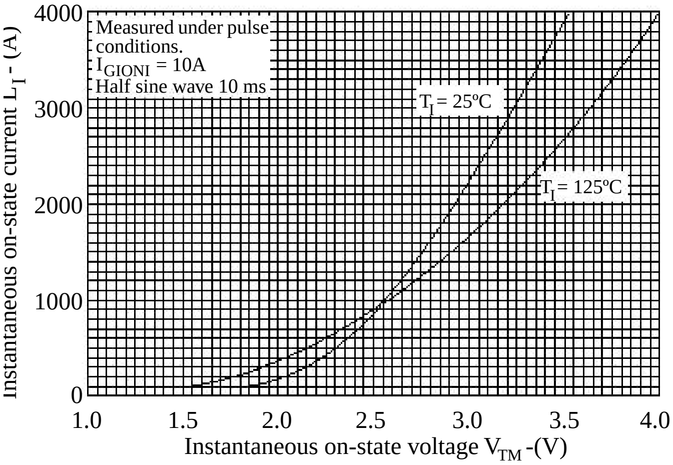


FIGURE 4.5 V-I Characteristics of GTO (see the data sheet in Reference 1). GTO gate characteristic information reproduced by kind permission of Dynex Semiconductor.

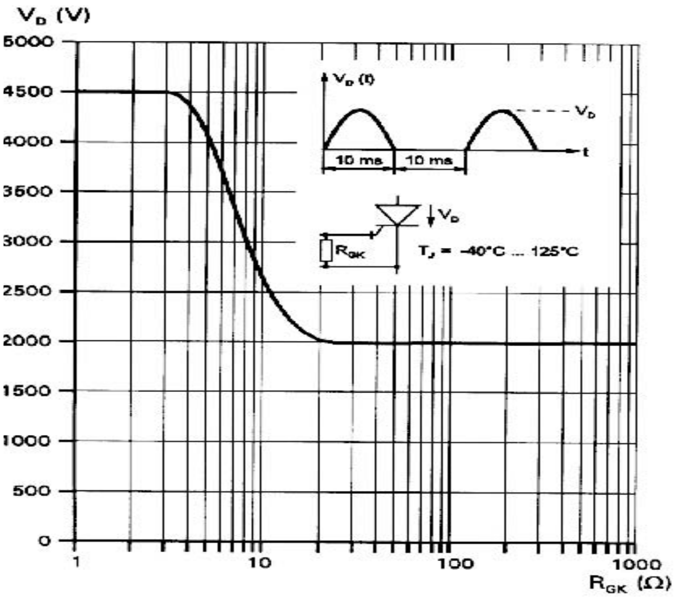


FIGURE 4.6 GTO blocking voltage vs R_{GK} (see the data sheet in Reference 1). GTO gate characteristic information reproduced by kind permission of Dynex Semiconductor.

The peak off-state voltage is a function of resistance R_{GK}. This is shown in Fig. 4.6. Under ordinary operating conditions, GTOs are biased with a negative gate voltage of ≈ -15 V supplied from the gate drive unit during the off-state interval. Nevertheless, provision of R_{GK} may be a desirable design practice in the event the gate-drive failure for any reason ($R_{GK} < 1.5\Omega$ is recommended for a large GTO). Here R_{GK} dissipates energy and hence adds to the system losses.

4.4.3 Rate of Rise of Off-State Voltage dv_T/dt

The rate of rise of off-state voltage (dv_D/dt) depends on the resistance R_{GK} connected between the gate and the cathode and the reverse bias applied between the gate and the cathode. This relationship is shown in Fig. 4.7.

1.4.4 Gate Triggering Characteristics

The gate trigger current (I_{GT}) and the gate trigger voltage (V_{GT}) are both dependent on junction temperature T_j as shown in Fig. 4.8. During the conduction state of the GTO a certain value of gate current must be supplied and this value should be larger than the I_{GT} at the lowest junction temperature at which the GTO operates. In dynamic conditions the specified I_{GT} is not sufficient to trigger the GTO switching from higher voltage and high *di/dt*. In practice, a much higher peak gate current I_{GM} (on the order of 10 times I_{GT}) at T_j min is recommended to obtain good turn-on performance.

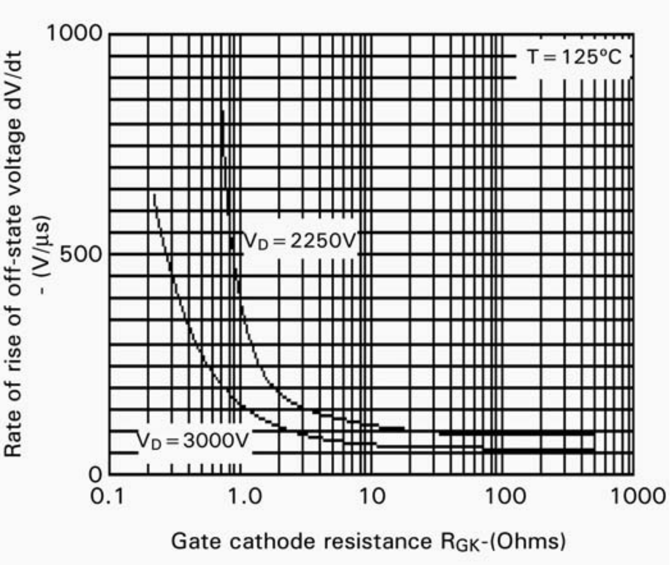


FIGURE 4.7 dv_D/dt vs R_{GK} (see the data sheet in Reference 1). GTO gate characteristic information reproduced by kind permission of Dynex Semiconductor.

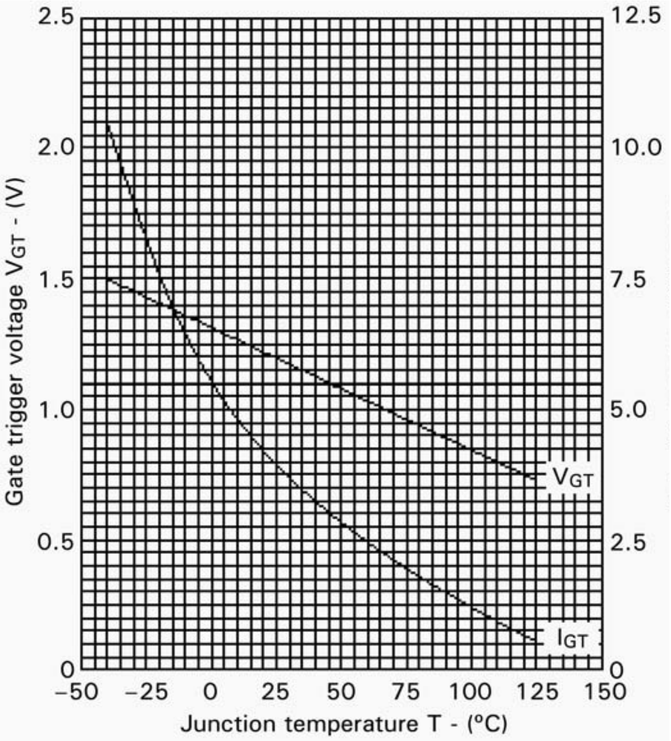


FIGURE 4.8 GTO trigger characteristics (see the data sheet in Reference 1).

4.5 Switching Phases

The switching process of a GTO thyristor goes through four operating phases: (a) turn-on; (b) on-state; (c) turn-off; and (d) off-state.

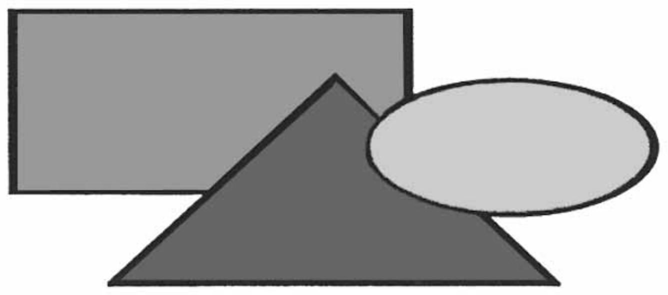


FIGURE 4.9 A typical turn-on gate pulse (see the data sheet in Reference 2). Courtesy of Westcode.

Turn-on: A GTO has a highly interdigited gate structure with no regenerative gate. Thus it requires a large initial gate trigger pulse. A typical turn-on gate pulse and its important parameters are shown in Fig. 4.9. Minimum and maximum values of I_{GM} can be derived from the device data sheet. A value of di_g/dt positioned against turn-on time is given under the device characteristics found on the data sheet [2]. The rate of rise of gate current di_g/dt will affect the device turn-on losses. The duration of the I_{GM} pulse should not be less than half the minimum for time given in data sheet ratings. A longer period will be required if the anode current di/dt is low such that I_{GM} is maintained until a sufficient level of anode current is established.

On-state: Once the GTO is turned on, forward gate current must be continued for the entire conduction period. Otherwise, the device will not remain in conduction during the on-state period. If large negative di/dt or anode current reversal occurs in the circuit during the on-state, then higher values of I_G may be required. However, much lower values of I_G are required when the device has heated up.

Turn-off: The turn-off performance of a GTO is greatly influenced by the characteristics of the gate turn-off circuit. Thus the characteristics of the turn-off circuit must match with the device requirements. Fig. 4.10 shows the typical anode and gate currents during the turn-off. The gate turn-off process involves the extraction of the gate charge, the gate avalanche period, and the anode current decay. The amount of charge extraction is a device parameter and its value is not affected significantly by the external circuit conditions. The initial peak turn-off current and turn-off time, which are important parameters of the turning-off process, depend on the external circuit components. The device data sheet gives typical values for I_{GQ}.

The turn-off circuit arrangement of a GTO is shown in Fig. 4.11. The turn-off current gain of a GTO is low, typically 6 to 15. Thus, for a GTO with a turn-off gain of 10, it will require a turn-off gate current of 10 A to turn-off an on-state

FIGURE 4.10 Anode and gate currents during turn-off (see the data sheet in Reference 2). Courtesy of Westcode.

FIGURE 4.12 Gate-cathode resistance, R_{GK} (see the data sheet in Reference 2). Courtesy of Westcode.

of 100 A. A charged capacitor C is normally used to provide the required turn-off gate current. Inductor L limits the turn-off di/dt of the gate current through the circuit formed by R_1, R_2, SW_1, and L. The gate circuit supply voltage V_{GS} should be selected to give the required value of V_{GQ}. The values of R_1 and R_2 should also be minimized.

Off-state period: During the off-state period, which begins after the fall of the tail current to zero, the gate should ideally remain reverse-biased. This reverse bias ensures maximum blocking capability and dv/dt rejection. The reverse bias can be obtained either by keeping SW_1 closed during the whole off-state period or via a higher impedance circuit SW_2 and R_3 provided a minimum negative voltage exits. This higher impedance circuit SW_2 and R_3 must sink the gate leakage current.

In case of a failure of the auxiliary supplies for the gate turn-off circuit, the gate may be in reverse-biased condition and the GTO may not be able to block the voltage. To ensure that the blocking voltage of the device is maintained, a minimum gate-cathode resistance (R_{GK}) should be applied as shown in Fig. 4.12. The value of R_{GK} for a given line voltage can be derived from the data sheet.

FIGURE 4.11 Turn-off circuit (see the data sheet in Reference 2). Courtesy of Westcode.

4.6 SPICE GTO Model

A GTO may be modeled with two transistors as shown in Fig. 4.3. However, a GTO model [3] consisting of two thyristors, which are connected in parallel, yield improved on-state, turn-on and turn-off characteristics. This is shown in Fig. 4.13 with four transistors.

When the anode to cathode voltage V_{AK} is positive and there is no gate voltage, the GTO model will be in the off state like a standard thyristor. If a positive voltage (V_{AK}) is applied to the anode with respect to the cathode and no gate pulse is applied, $I_{B1} = I_{B2} = 0$ and, therefore, $I_{C1} = I_{C2} = 0$. Thus, no anode current will flow and $I_A = I_K = 0$.

When a small voltage is applied to the gate, then I_{B2} is nonzero and, therefore, both $I_{C1} = I_{C2} = 0$ are nonzero. Thus the internal circuit will conduct and there will be a current flow from the anode to the cathode.

When a negative gate pulse is applied to the GTO model, the p-n-p junction near to the cathode will behave as a diode.

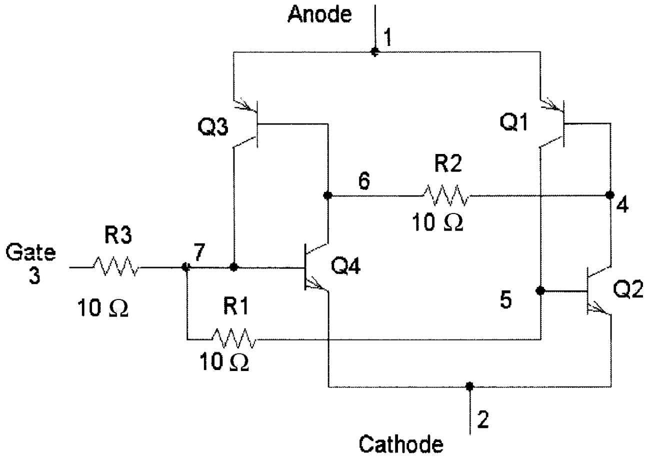


FIGURE 4.13 Four-transistor GTO model. Courtesy of Westcode.

The diode will be reverse biased because the gate voltage is negative to the cathode. Therefore, the GTO will stop conduction.

When the anode-to-cathode voltage is negative, that is, the anode voltage is negative with respect to the cathode, the GTO model will act like a reverse-biased diode. This is because the *p-n-p* transistor will see a negative voltage at the emitter and the *n-p-n* transistor will see a positive voltage at the emitter. Therefore both transistors will be in the off state and hence the GTO will not conduct. The SPICE subcircuit description of the GTO model will be as follows:

4.7 Applications

Gate turn-off thyristors have many applications, including motor drives, induction heating [4], distribution lines [5], pulsed power [6], and flexible ac transmission systems [7].

```
.SUBCIRCUIT   1              2        3      ; GTO Subcircuit definition
*Terminal           anode    cathode  gate
Q1    5   4   1     DMOD1             p-n-p  ; p-n-p transistor with model DMOD1
Q3    7   6   1     DMOD1             p-n-p
Q2    4   5   2     DMOD2             n-p-n  ; p-n-p transistor with model DMOD2
Q4    6   7   2     DMOD2             n-p-n
R1    7   5   10 Ω
R2    6   4   10 Ω
R3    3   7   10 Ω
.MODEL    DMOD1                       p-n-p  ; Model statement for a p-n-p transistor
.MODEL    DMOD2                       n-p-n  ; Model statement for an n-p-n transistor
.ENDS                                 ; End of subcircuit definition
```

Acknowledgment

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5

Power Bipolar Transistors

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5.1 Introduction

The first transistor was created in 1948 by a team of physicists at the Bell Telephone Laboratories and soon became a semiconductor device of major importance. Before the transistor, amplification was achieved only with vacuum tubes. Although there are now integrated circuits with millions of transistors, flow and control of electrical energy still require single transistors. Therefore, power semiconductor switches constitute the heart of modern power electronics. Such devices should have larger voltage and current ratings, instant turn-on and turn-off characteristics, very low voltage drop when fully on, zero leakage current in blocking condition, enough ruggedness to switch highly inductive loads, which are measured in terms of safe operating area (SOA) and ES/b (reverse-biased second breakdown), high-temperature and radiation-withstand capabilities and high reliability. The right combination of such features restricts device suitability to only certain applications. Figure 5.1 depicts those voltage and current ranges, in terms of frequency, at which where the most common power semiconductors devices can operate.

The figure actually gives an overall picture of where power semiconductors are typically applied in industries: High voltage and current ratings permit applications in large motor drives, induction heating, renewable energy inverters, HVDC converters, and static VAR compensators and active filters. By contrast, low-voltage and high-frequency applications that include switching mode power supplies, resonant converters and motion control systems and low-frequency with high-current and voltage devices are restricted to cycloconverter-fed and multimegawatt drives [1].

Power-*npn* or *pnp* bipolar transistors used to be the traditional components for driving several of these industrial applications. However, insulated-gate bipolar-transistor (IGBT) and metal-oxide-semiconductor field-effect transition (MOSFET) technology have progressed so much that they are now viable replacements for the bipolar types. Bipolar-*npn* or *pnp* transistors still have performance areas in which they still may be used; for example, they have lower saturation voltages over their operating temperature range, but they are considerably slower, exhibiting long turn-on and turn-off times. When a bipolar transistor is used in a totem-pole circuit, the most difficult design aspects to overcome are the base drive circuitry, i.e. the required circuit for driving the base. Although bipolar transistors have lower input capacitance than those of MOSFETs and IGBTs, they are current driven. Thus, the drive circuitry must generate high and prolonged input currents.

The high input impedance of the IGBT is an advantage over its bipolar counterpart. However, input capacitance is also high. As a result, the drive circuitry must rapidly charge and discharge the input capacitor of the IGBT during the transition time. The IGBT low-saturation voltage performance is analogous to bipolar power-transistor performance, even over the operating-temperature range. The IGBT requires a $-5/+10$ V gate-emitter voltage transition to ensure reliable output switching.

The MOSFET gate and IGBT are similar in many areas of operation. For instance, both devices have high input impedance, are voltage-driven, and use less silicon than the

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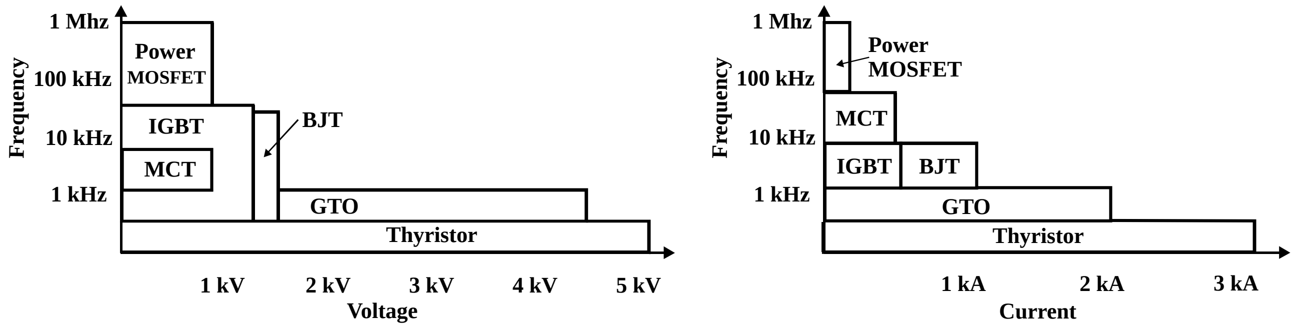


(a) (b)

FIGURE 5.1 Power semiconductor operating regions. (a) voltage vs frequency; and (b) current vs frequency.

bipolar power transistor to achieve the same drive performance. Additionally, the MOSFET gate has high input capacitance, which places the same requirements on the gate-drive circuitry as the IGBT employed at that stage. The IGBTs outperform MOSFETs when it comes to conduction loss vs supply-voltage rating. The saturation voltage of MOSFETs is considerably higher and less stable over temperature than that of IGBTs. For these reasons, the insulated-gate bipolar transistor took the place of bipolar junction transistors in several applications during the 1980s. Although the IGBT is a cross between the bipolar and MOSFET transistor, with the output switching and conduction characteristics of a bipolar transistor, but voltage-controlled like a MOSFET, the early IGBT versions were prone to latch up, which had been largely eliminated by the 1980s. Another characteristic with some IGBT types is the negative temperature coefficient, which can lead to thermal runaway and makes the paralleling of devices hard to achieve. Currently, this problem is being addressed in the latest generations of IGBTs.

It is very clear that a categorization based on voltage and switching frequency provides two key parameters for determining whether a MOSFET or an IGBT is the better device in an application. However, there are still difficulties in selecting a component for use in the crossover region, which includes voltages of 250 to 1000 V and frequencies of 20 to 100 kHz. At voltages <500 V, the BJT has been entirely replaced by MOSFET in power applications and has also been displaced at higher voltages, where new designs use IGBTs. Most regular industrial needs are in the range of 1–2 kV blocking voltages, 200–500 ampere conduction currents, and with switching speeds of 10–100 ns. Although in the last few years, new high voltage projects displaced BJTs towards IGBT, and it is expected that there will be a decline in the number of new power system designs that incorporate bipolar junction transistors, some applications for BJTs remain; in addition the huge built-up history of equipment installed in industries makes the bipolar junction transistor a good device.

5.2 Basic Structure and Operation

The bipolar junction transistor (BJT) consists of a three-region structure of *n*-type and *p*-type semiconductor materials; it can be constructed as *npn* as well as *pnp*. Figure 5.2 shows the physical structure of a planar *npn* bipolar junction transistor. The operation is closely related to that of a junction diode where in normal conditions the *pn* junction between the base and collector is forward-biased ($v_{BE} > 0$), causing electrons to be injected from the emitter into the base. As the base region is thin, the electrons travel across it and arrive at the reverse-biased base-collector junction ($v_{BC} < 0$), where there is an electric field (depletion region). Upon arrival at this junction the electrons are pulled across the depletion region and drawn into the collector. These electrons flow through the collector region and out the collector contact. Because electrons are negative carriers, their motion constitutes positive current flowing into the external collector terminal. Even though the forward-biased base-emitter junction injects holes from base to emitter, the holes do not contribute to the collector current but result in a net current flow component into the base from the external base terminal. Therefore, the emitter current is composed of these two components: electrons destined to be

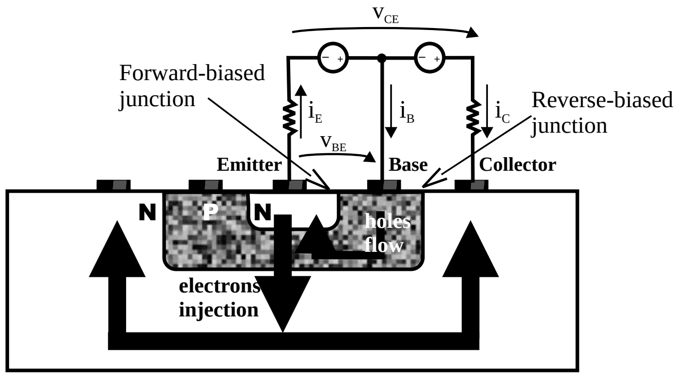


FIGURE 5.2 Structure of a planar bipolar junction transistor.

injected across the base-emitter junction, and holes injected from the base into the emitter. The emitter current is exponentially related to the base-emitter voltage by the equation:

$$i_E = i_{E0}\left(e\frac{v_{BE}}{\eta \cdot v_T} - 1\right) \tag{5.1}$$

where i_E is the saturation current of the base-emitter junction and which is a function of the doping levels, temperature and the area of the base-emitter junction, V_T is the thermal voltage Kt/q and η is the emission coefficient. The electron current arriving at the collector junction can be expressed as a fraction α of the total current crossing the base-emitter junction

$$i_C = \alpha i_E \tag{5.2}$$

Because the transistor is a three-terminals device, i_E is equal to $i_C + i_B$, hence the base current can be expressed as the remaining fraction,

$$i_B = (1 - \alpha) i_E \tag{5.3}$$

The collector and base currents are thus related by the ratio

$$\frac{i_c}{i_B} = \frac{\alpha}{1 - \alpha} = \beta \tag{5.4}$$

The values of α and β for a given transistor depend primarily on the doping densities in the base, collector and emitter regions, as well as on the device geometry. Recombination and temperature also affect the values for both parameters. A power transistor requires a large blocking voltage in the off state and a high current capability in the on state; a vertically oriented four-layer structure as shown in Fig. 5.3 is preferable because it maximizes the cross-sectional area through which the current flows, enhancing the on-state resistance and power dissipation in the device [2]. There is an intermediate collector region with moderate doping, and the emitter region is controlled so as to have a homogeneous electrical field.

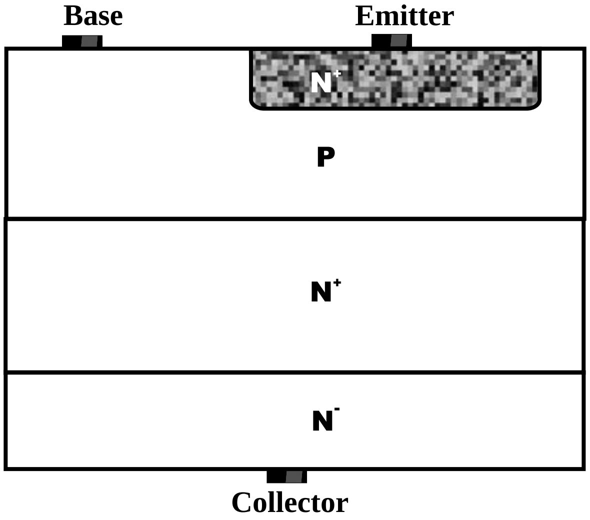


FIGURE 5.3 Power transistor vertical structure.

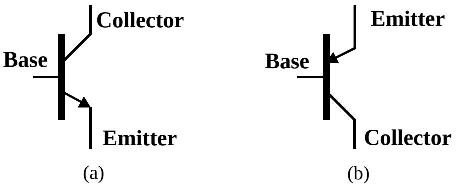


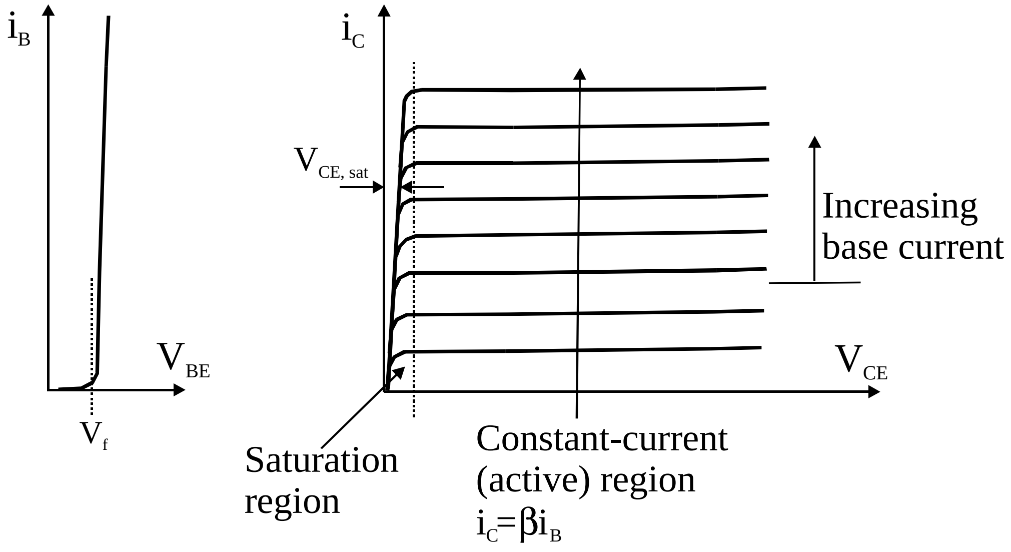
FIGURE 5.4 Circuit symbols (a) NPN transistor; and (b) PNP transistor.

Optimization of doping and base thickness are required to achieve high breakdown voltage and amplification capabilities. Power transistors have their emitters and bases interleaved to reduce parasitic ohmic resistance in the base current path, which also improves the device for second breakdown failure. The transistor is usually designed to maximize the emitter periphery per unit area of silicon, in order to achieve the highest current gain at a specific current level. In order to ensure those transistors have the greatest possible safety margin, they are designed to be able to dissipate substantial power and, thus, have low thermal resistance. It is for this reason, among others, that the chip area must be large and that the emitter periphery per unit area is sometimes not optimized. Most transistor manufacturers use aluminum metallization because it has many attractive advantages, among them easier application via vapor deposition and easier definition with photolithography. A major problem with aluminum is that only a thin layer can be applied by normal vapor-deposition techniques. Thus, when high currents are applied along the emitter fingers, a voltage drop occurs along them, and the injection efficiency on the portions of the periphery that are farthest from the emitter contact is reduced. This limits the amount of current each finger can conduct. If copper metallization is substituted for aluminum, then it is possible to lower the resistance from the emitter contact to the operating regions of the transistors (the emitter periphery).

From a circuit point of view, Eqs. (5.1)–(5.4) are used to relate the variables of the BJT input port (formed by base (B) and emitter (E)) to the output port (collector (C) and emitter (E)). The circuit symbols are shown in Fig. 5.4. Most of power electronics applications use NPN transistors because electrons move faster than holes, and therefore, NPN transistors have considerable faster commutation times.

5.3 Static Characteristics

Device static ratings determine the maximum allowable limits of current, voltage, and power dissipation. The absolute voltage limit mechanism is concerned with the avalanche in



(a) (b)

FIGURE 5.5 Family of current-voltage characteristic curves. (a) base-emitter input port; and (b) collector-emitter output port.

terms of preventing thermal runaway. Forward current ratings are specified at which the junction temperature does not exceed a rated value so as to prevent leads and contacts from being evaporated. Power dissipated in a semiconductor device produces a temperature rise and is related to thermal resistance. A family of voltage-current characteristic curves is shown in Fig. 5.5. Figure 5.5a shows the base current i_B plotted as a function of the base-emitter voltage v_{BE} and Fig. 5.5b depicts the collector current i_C as a function of the collector-emitter voltage V_{CE}, with i_B as the controlling variable.

Figure 5.5 shows several curves distinguished from each other by the value of the base current. The active region is defined where flat, horizontal portions of voltage-current curves show "constant" i_C current, because the collector current does not change significantly with v_{CE} for a given i_B. Those portions are used only for small signal transistors operating as linear amplifiers. On the other hand, switching power electronics systems require transistors to operate in either the saturation region where v_{CE} is small or in the cutoff region where the current is zero and the voltage is upheld by the device. A small base current drives the flow of a much larger current between collector and emitter; such gain (called beta Eq. (5.4)) depends upon temperature, V_{CE} and I_C. Figure 5.6 shows current gain increase with increased collector voltage; gain falls off at both high and low current levels.

High voltage BJTs typically have low current gain, and hence Darlington-connected devices, as indicated in Fig. 5.7 are commonly used. Considering gains β_1 and β_2 for each one of these transistors, the Darlington connection will have an increased gain of $\beta_1 + \beta_2 + \beta_1\beta_2$ and diode D1 speeds up the turn-off process by allowing the base driver to remove the stored charge on the transistor bases.

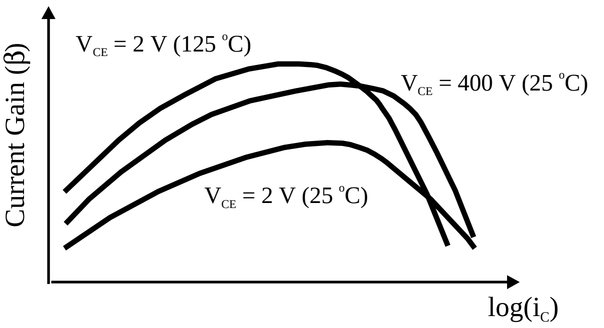


FIGURE 5.6 Current gain depends on temperature V_{CE} and I_C.

Vertical-structure power transistors have an additional region of operation called quasi-saturation, indicated in the characteristics curve of Fig. 5.8. Such a feature is a consequence of the lightly doped collector drift region where the collector base junction supports a low reverse bias. If the transistor enters the hard-saturation region the on-state power dissipation is minimized; there is, however, a tradeoff in quasi-saturation the stored charges are smaller. At high

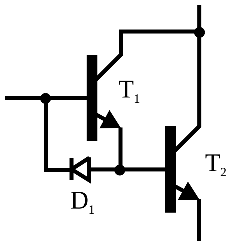


FIGURE 5.7 Darlington-connected BJTs.

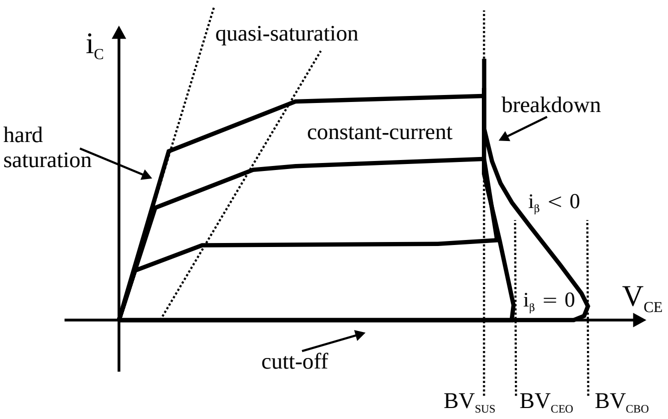


FIGURE 5.8 Voltage-current characteristics for a vertical power transistor.

collector currents beta gain decreases with increased temperature and with quasi-saturation operation such negative feedback allows careful device paralleling. Two mechanisms at the microelectronic level determine the fall-off in beta, namely conductivity modulation and emitter crowding. One can note that there is a region called primary breakdown due to conventional avalanche of the C-B junction and the attendant large flow of current. Here BV_{SUS}, the limit for primary breakdown, is the maximum collector-emitter voltage that can be sustained across the transistor when it is carrying high collector current. The BV_{SUS} is lower than BV_{CEO} or BV_{CBO}, both of which measure the transistor's voltage standoff capability when the base current is zero or negative. The bipolar transistor has another potential failure mode called second breakdown, which shows as a precipitous drop in the collector-emitter voltage at large currents. Because the power dissipation is not uniformly spread over the device but is, instead, rather concentrated on regions, this serves to make the local gradient of temperature rise very quickly. Such thermal runaway brings hot spots that can eventually melt and recrystallize the silicon, thereby resulting in device destruction. The key to avoiding second breakdown is to: (1) keep power dissipation under control; (2) use a controlled rate of change of base current during turn-off; (3) use protective snubber circuitry; and (4) position the switching trajectory within the safe operating area (SOA) boundaries.

In order to describe the maximum values of current and voltage to which the BJT should be subjected, two diagrams are used: the forward-bias safe operating area (FBSOA) given in Fig. 5.9 and the reverse-bias safe operating area (RBSOA) shown in Fig. 5.10. In the FBSOA current I_{CM} is the maximum current of the device and there is a boundary defining the maximum thermal dissipation and a margin defining the second breakdown limitation. These regions are expanded for switching mode operation. Inductive load generates a higher peak energy at turn-off than does its resistive counterpart. It is then possible to have a secondary breakdown failure if RBSOA is exceeded. A reverse base current helps the internal operation leading to an expanded region RBSOA. The RBSOA curve shows that for voltages below V_{CEO} the safe area is independent of reverse bias voltage V_{EB} and is only limited by the device collector current, whereas above V_{CEO} the collector current must be under control, dependent upon the applied reverse-bias voltage; in addition, temperature effects derate the safe operating area. The ability of a transistor to switch high currents reliably is thus determined by its peak power-handling capabilities. This ability is dependent upon both the transistor's current and thermal density throughout the active region. In order to optimize the safe operating area (SOA) capability, both current- and thermal density must be low. In general, it is the hot spots occurring at the weakest area of the transistor that will cause a device to fail due to second breakdown phenomena. Although a wide base width will limit the current density across the base region, good heat sinking directly under the collector will enable the transistor to withstand high peak power. When the power and heat are spread over a large silicon area, all of these destructive tendencies are held to a minimum, and the transistor will have the highest SOA capability.

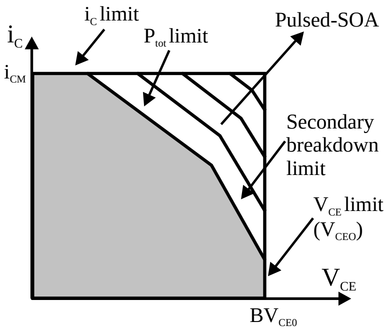


FIGURE 5.9 Forward-bias safe operating area (FBSOA).

When the transistor is on, one can ignore the base current losses and calculate power dissipation on the on state (conduction losses) with Eq. (5.5). Hard saturation minimizes collector-emitter voltage, which decreases on-state losses.

$$P_{ON} = I_C V_{CE(sat)} \tag{5.5}$$

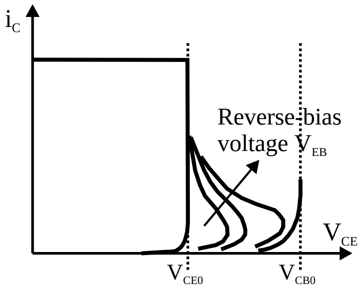


FIGURE 5.10 Reverse-bias safe operating area (RBSOA).

5.4 Dynamic Switching Characteristics

Switching characteristics are important in defining device velocity during change from conduction (on) to blocking (off) states. Such transition velocity is of paramount importance because most of the losses are due to high frequency switching. Figure 5.11 shows typical waveforms for a resistive load. Index "r" refers to the rising time (from 10 to 90 of maximum value); for example t_{ri} is the current rise time and depends upon base current. The falling time is indexed by "f"; the parameter t_{fi} is the current falling time, that is, when the transistor is blocking such time corresponds to crossing from the saturation to the cutoff state. In order to improve t_{fi}, the base current for blocking must be negative and the device must be kept in quasi-saturation so as to minimize stored charges. The delay time is denoted by t_d, corresponding to the time to discharge the capacitance of junction base-emitter, which time can be reduced with a larger current base with high slope. Storage time (t_s) is a very important parameter for BJT transistors, it is the time required to neutralize the carriers stored in the collector and the base. Storage time and switching losses are key points when dealing with bipolar power transistors. Switching losses occur at both turn-on and turn-off. For high-frequency operation the rising and falling times for voltage and current transitions play an important role as indicated by Fig. 5.12.

A typical inductive load transition is indicated in Fig. 5.13. The figure indicates a turn-off transition. Current and voltage are interchanged at turn-on and an approximation based upon straight line switching intervals (resistive load) gives the switching losses calculated using Eq. (5.6).

$$P_S = \frac{V_S I_M}{2}\tau f_s \tag{5.6}$$

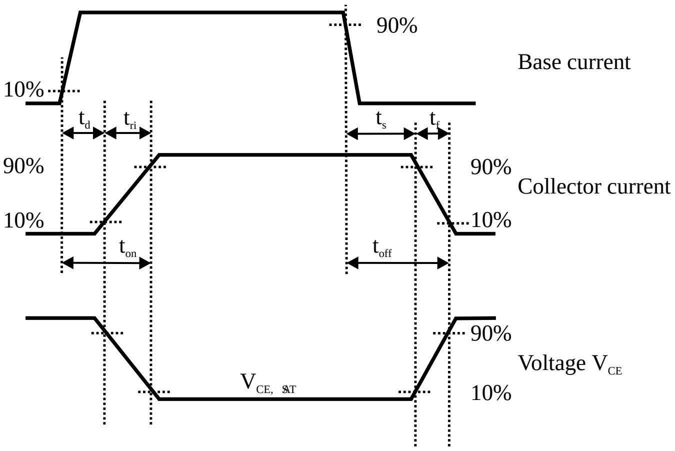


FIGURE 5.11 Resistive load dynamic response.

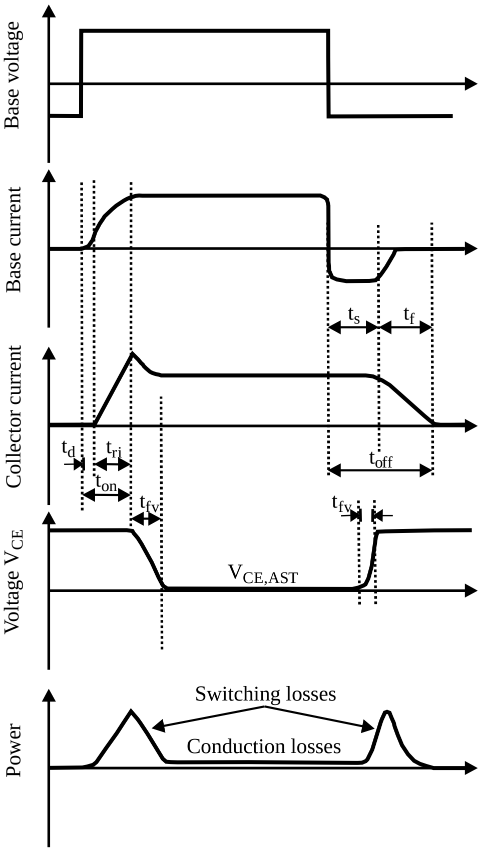


FIGURE 5.12 Inductive load switching characteristics.

where τ is the duration of the switching interval and V_S and I_M are the maximum voltage and current levels as shown in Fig. 5.14.

Most advantageous operation is achieved when fast transitions are optimized. Such a requirement minimizes switching losses. Therefore, a good bipolar drive circuit influences significantly the transistor performance. A base drive circuit should provide a high forward base drive current (I_{B1}) as indicated in Fig. 5.14 if power semiconductor turn-on is to be ensured quickly. Base drive current should keep the BJT fully saturated so as to minimize forward conduction losses, but a level I_{B2} would maintain the transistor in quasi-saturation, which avoids an excess of charges in the base. Controllable

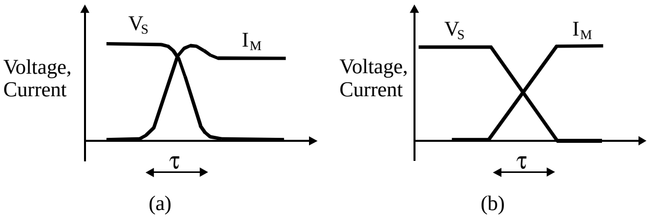


FIGURE 5.13 Turn-off voltage and current switching transition. (a) inductive load; and (b) resistive load.

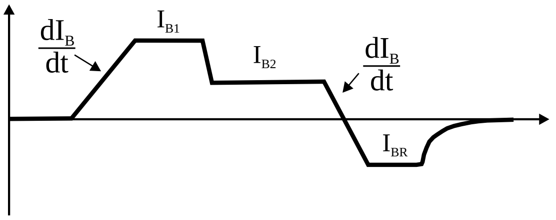


FIGURE 5.14 Recommended base current for BJT driving.

slope and reverse current I_{BR} sweep out stored charges in the transistor base, speeding up device turn-off.

5.5 Transistor Base Drive Applications

A plethora of circuits has been suggested to command transistors successfully for operation in power electronics switching systems [3]. Such base drive circuits try to satisfy the following requirements: supply the right collector current; adapt the base current to the collector current; and extract a reverse current from base to speed up device blocking. A good base driver reduces the commutation times and total losses, thus increasing efficiency and operating frequency. Depending upon the grounding requirements between the control and the power circuits, the base drive might be either an isolated or nonisolated type. Figure 5.15 shows a nonisolated circuit. When T_1 is switched on, T_2 is driven and diode D_1 is forward-biased, which provides a reverse bias and keeps T_3 off. The base current I_B is positive and saturates the power transistor T_P. When T_1 is switched off, T_3 switches on due to the negative path provided by R_3 and $-$VCC, providing a negative current for switching off the power transistor T_P.

When a negative power supply is not provided for the base drive, a simple circuit like Fig. 5.16 can be used in low-power applications (stepper motors, small dc-dc converters, relays, pulsed circuits). When the input signal is high T_1 switches on and a positive current goes to T_P, thus keeping the capacitor charged with the Zener voltage; and when the input signal falls, T_2 provides a path for the discharge of the capacitor, which imposes a pulsed negative current from the base-emitter junction of T_P.

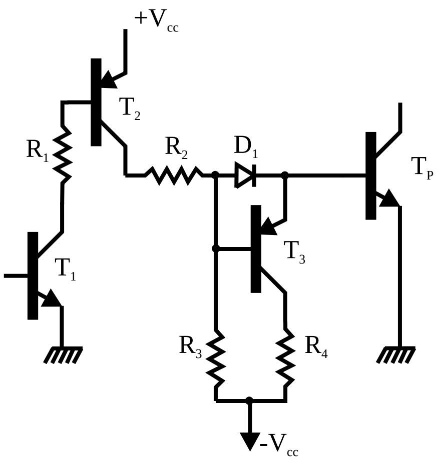


FIGURE 5.15 Nonisolated base driver.

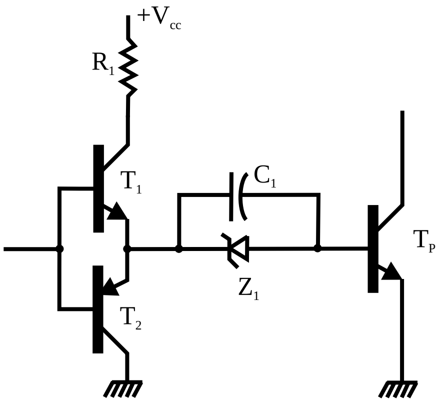


FIGURE 5.16 Base command without negative power supply.

A combination of large reverse base drive and antisaturation techniques may be used to reduce storage time to almost zero. A circuit called Baker's clamp may be employed as illustrated in Fig. 5.17. When the transistor is on its base it is two diode drops below the input. Assuming that diodes D_2 and D_3 have a forward bias voltage of $\approx$0.7 V, then the base will be 1.4 V below the input terminal. Due to diode D_1 the collector is one diode drop, or 0.7 V below the input. Therefore, the collector will always be more positive than the base by 0.7 V, staying out of saturation; further because collector voltage increases the gain β also increases slightly. Diode D_4 provides a negative path for the reverse base current. The input base current can be supplied by a driver circuit similar to the one discussed in Fig. 5.15.

Several situations require ground isolation, off-line operation, and floating transistor topology. In addition, safety needs may require an isolated base drive circuit. Numerous circuits have been demonstrated in switching power supplies to isolated topologies, usually integrating base drive requirements with their power transformers. Isolated base drive

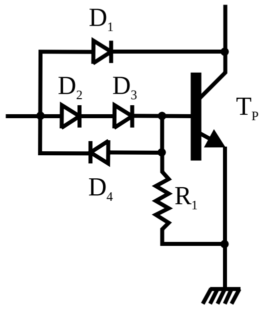


FIGURE 5.17 Antisaturation diodes (Baker clamps) improve power transistor storage time.

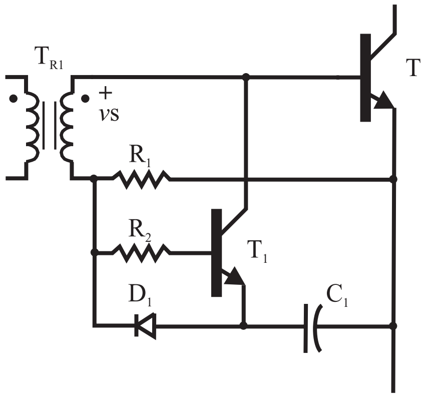


FIGURE 5.18 Isolated base drive circuit.

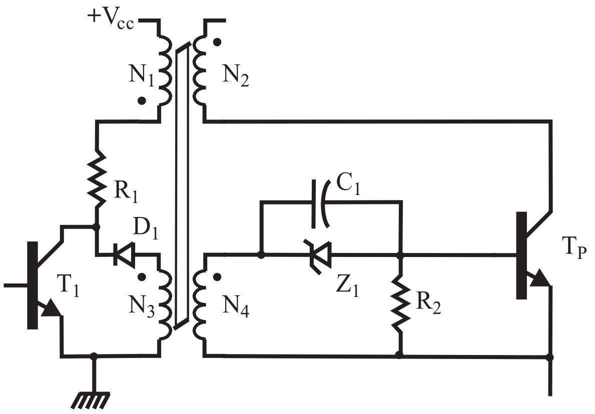


FIGURE 5.20 Proportional base drive circuit.

circuits may provide either constant current or proportional current excitation. A very popular base drive circuit for floating switching transistor is shown in Fig. 5.18. When a positive voltage is impressed on the secondary winding (V_S) of T_{R1}, a positive current flows into the base of the power transistor T_P and it switches on (resistor R_1 limits the base current). Capacitor C_1 is charged by ($V_S - V_{D1} - V_{\mathrm{BE}}$) and T_1 is kept blocked because diode D_1 reverse biases the T_1 base-emitter. When V_S is zipped off, the capacitor voltage V_C brings the emitter of T_1 to a negative potential in respect to its base. Therefore, T_1 is excited so as to switch on and start pulling a reverse current from the T_P base. Another very effective circuit is shown in Fig. 5.19 with a minimum number of components. The base transformer has a tertiary winding, which uses the energy stored in the transformer to generate the reverse base current during the turn-off command. Other configurations are also possible by adding to the isolated circuits the Baker clamp diodes, or Zener diodes with paralleled capacitors.

Sophisticated isolated base drive circuits can be used to provide proportional base drive currents where it is possible to control the value of β; by keeping it constant for all collector currents shorter storage time results. Figure 5.20 shows one possible way to realize a proportional base drive circuit. When transistor T_1 turns on, the transformer T_{R1} is in negative saturation and power transistor T_P is off. During the time that T_1 is on a current flows through winding N_1, limited by resistor R_1, storing energy in the transformer and holding it at saturation. When transistor T_1 turns off, the energy stored in N_1 is transferred to winding N_4, pulling the core from negative to positive saturation. Windings N_2 and N_4 will withstand as a current source, transistor T_P will stay on, and gain β will be imposed by the turns ratio given by:

$$\beta = \frac{N_4}{N_2} \tag{5.7}$$

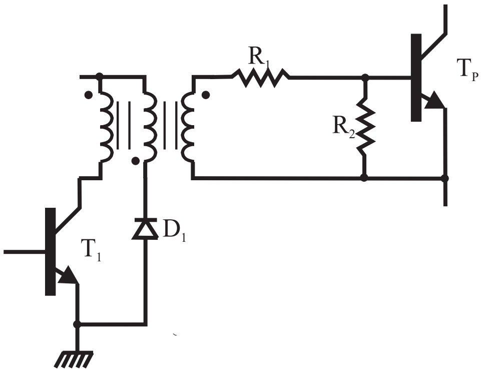


FIGURE 5.19 Transformer coupled base drive with tertiary winding transformer.

To use the proportional drive given in Fig. 5.20 careful design of the transformer must be done in order to have the flux balanced, which will then keep the core under saturation. Transistor gain must be somewhat higher than the value imposed by the transformer turns ratio, which requires cautious device matching.

The most critical portion of the switching cycle occurs during transistor turn-off because normally reverse-base current is made very large in order to minimize storage time and such a condition may avalanche the base-emitter junction and lead to destruction. There are two options to prevent this from happening: turning off the transistor at low values of collector-emitter voltage (which is not practical in most of the applications), or reducing collector current with rising collector voltage, implemented by RC protective networks called snubbers. Therefore, an RC snubber network can be used to divert the collector current during the turn-off, which then improves the reverse bias safe operating area; in addition, the snubber circuit dissipates a fair amount of switching power and this relieves the transistor. Figure 5.21 shows a turn-off snubber network; when the power transistor is off capacitor C is charged through diode $D1$. Such collector current flows temporarily into the capacitor as the collector-voltage rises; as the power transistor turns on, the capacitor discharges through the resistor R back into the transistor.

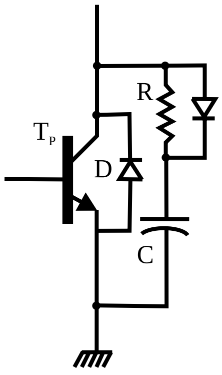


FIGURE 5.21 Turn-off snubber network.

It is not possible to fully develop all aspects of simulation of BJT circuits. Before giving an example, some comments are necessary regarding modeling and simulation of bipolar junction transistor circuits. There are several types of commercial circuit simulation programs available on the market, extending from a set of functional elements (passive components, voltage controlled and current sources, semiconductors) which can be used to model devices, to other programs that have the possibility of implementing algorithm relationships. Those streams are called subcircuit (building auxiliary circuits around a SPICE primitive) and mathematical (deriving models from internal device physics) methods. Simulators can solve circuit equations exactly, giving models for the nonlinear transistors, and predict the analog behavior of the node voltages and currents in continuous time. They are costly in computer time and such programs have not been written normally to serve the needs of power electronic circuit design but rather they are used to design low-power and low-voltage electronic circuits. Therefore, one has to decide which approach should be taken for incorporating BJT power transistor modeling, and a trade-off between accuracy and simplicity must be considered. If precise transistor modeling is required, subcircuit-oriented programs should be used. On the other hand, when simulation of complex power electronic system structures or novel power electronic topologies are devised, switch modeling should be rather simple, (which can be accomplished by taking into consideration fundamental switching operations) and a mathematically oriented simulation program should be used.

5.6 SPICE Simulation of Bipolar Junction Transistors

A general-purpose circuit program that can be applied to simulate electronic and electrical circuits and predict circuit behavior, SPICE was originally developed at the Electronics Research Laboratory of the University of California, Berkeley (1975). The name stands for simulation program for integrated circuits emphasis. A circuit must be specified in terms of element names, element values, nodes, variable parameters, and sources. Several types of circuit analysis are possible using SPICE:

- nonlinear dc analysis calculates dc transference;
- nonlinear transient analysis calculates signals as a function of time;
- linear ac analysis computes a Bode plot of output as a function of frequency;
- noise analysis;
- sensitivity analysis;
- distortion analysis;
- Fourier analysis; and
- Monte-Carlo analysis.

PSpice is a commercial version which has analog and digital libraries of standard components such as operational amplifiers, digital gates, and flip-flops. This makes it a useful tool for a wide range of analog and digital applications. An input file, called source file, consists of three parts: (1) data statements, with description of the components and the interconnections; (2) control statements, which tell SPICE what type of analysis to perform on the circuit; and (3) output statements, with specifications of which outputs are to be printed or plotted. Two other statements are required the title statement and the end statement. The title statement is the first line and can contain any information, while the end statement is always .END. This statement must be a line by itself, followed by carriage return. In addition, there are also comment statements, which must begin with an aterisk ( ) and are ignored by SPICE. There are several model equations for bipolar junction transistors.

The SPICE system has built-in models for semiconductor devices, and the user only needs to specify the pertinent model parameter values. The model for the BJT is based on the integral-charge model of Gummel and Poon [4]. However, if the Gummel-Poon parameters are not specified, the model reduces to the piecewise-linear Ebers-Moll model as depicted in Fig. 5.22. In either case, charge-storage effects, ohmic resistances, and a current-dependent output conductance may be included. The forward gain characteristics are defined by the parameters IS and BF, the reverse characteristics by IS and BR. Three ohmic resistances RB, RC, and RE are also included. The two diodes are modelled by voltage sources and experimental Shockley equations can be transformed into logarithmic ones. A set of device model parameters is defined on a separate MODEL card and assigned a unique model name. The device element cards in SPICe then reference the model name. This scheme lessens the need to specify all of the model parameters on each device element card. Parameter values are defined by appending the parameter name, as given here for each model type, followed by an equal sign and the parameter value. Model parameters not given a value are assigned the default values given here for each model type.

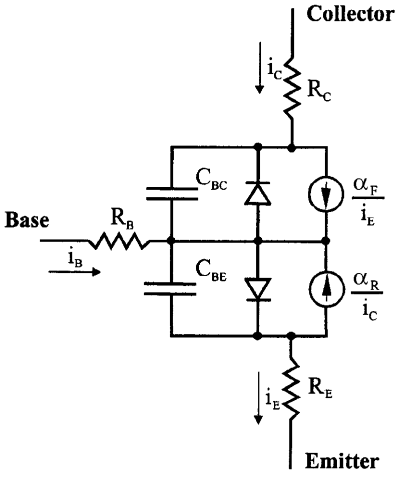


FIGURE 5.22 Ebers-Moll transistor model.

As an example, the model parameters for the 2N2222A NPN transistor are given in what follows:

```
.MODEL Q2N222A NPN (IS=14.34F XTI=3
  EG=1.11 VAF=74.03 BF=255.9
NE=1.307 ISE=14.34F IKF=.2847 XTB=1.5
  BR=6.092 NC=2 ISC=0 IKR=0
RC=1 CJC=7.306P MJC=.3416 VJC=.75 FC=.5
  CJE=22.01P MJE=.377
VJE=.75 TR=46.91N TF=4.11.1P ITF=.6
  VTF=1.7 XTF=3 RB=10)
```

Figure 5.23 shows a BJT buck chopper. The dc input voltage is 12 V, load resistance R is 5 Ω, filter inductance L is 145.8 μH and the filter capacitance C is 200 μF. The chopping frequency is 25 kHz and the duty cycle of the chopper is 42 as indicated by the control voltage statement (V_G). The listing that follows plots the instantaneous load current (I_O), the input current (I_S), the diode voltage (V_D), the output voltage (V_C) and calculates the Fourier coefficients of the input current (I_S). This listing for the careful reader as it provides more details and enhancements that are useful when SPICE is chosen for simulations as shown below.

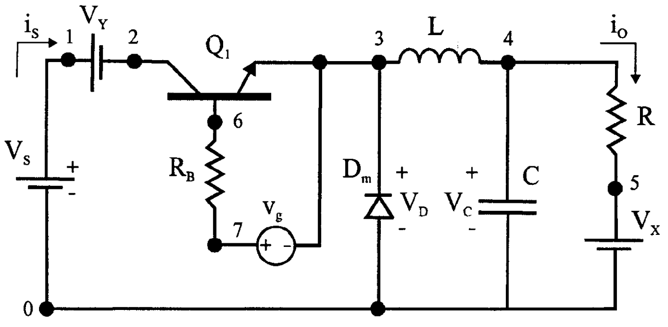


FIGURE 5.23 BJT buck chopper.

5.7 BJT Applications

Bipolar junction power transistors are applied to a variety of power electronic functions, switching mode power supplies, dc motor inverters, PWM inverters [5], and many other functions too numerous to name. To conclude, three applications are illustrated.

A flyback converter is given in Fig. 5.24. The switching transistor is required to withstand peak collector voltage at turn-off and peak collector currents at turn-on. In order to limit the collector voltage to a safe value, the duty cycle must

```
*SOURCE
VS   1    0    DC   12V
VY   1    2    DC   0V            ;Voltage source to measure input current
VG   7    3    PULSE 0V  30V  0.1NS  0/Ins  16.7US  4OUS)
*CIRCUIT
RB   7    6    250                ;Transistor base resistance
R    5    0    5
L    3    4    145.8UH
C    5    0    200UF IC=3V        ;Initial voltage
VX   4    5    DC    0V           ;Source to inductor current
DM   0    3    DMOD               ;Freewheeling diode
.MODEL DMOD D(IS=2.22E-15 BV=1200V DJO=O TT=O)
Q1   2    6    3    3    2N6546 ;BJT switch
.MODEL 2N6546 NPN (IS=6.83E-14 BF=13 CJE=1PF CJC=607.3PF TF=26.5NS)
*ANALYSIS
.TRAN   2US 2.1MS  2MS UIC        ;Transient analysis
.PROBE                             ;Graphics post-processor
.OPTIONS ABSTOL=1.OON RELTOL=0.01 VNTOL=0.1 ITL5=40000
.FOUR   25KHZ I(VY)               ;Fourier analysis
.END
```

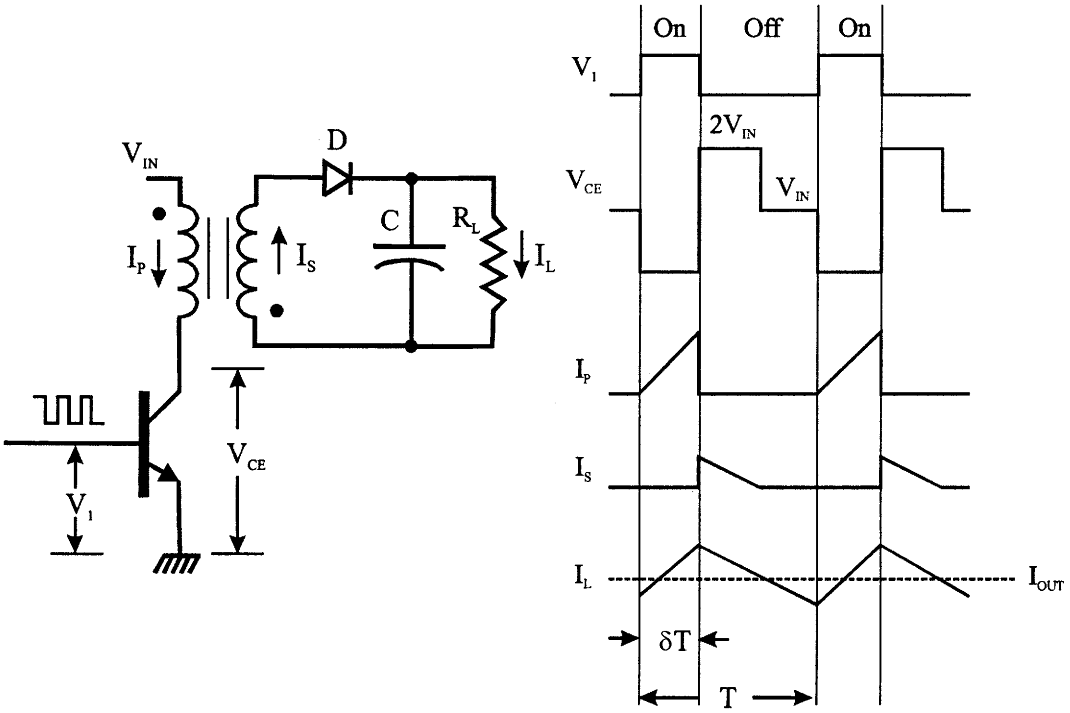

On
Off
On
V_1
V_{IN}
D
C
R_L
I_P
I_S
I_L
V_{CE}
V_1
$2V_{IN}$
V_{IN}
I_P
I_S
I_L
I_{OUT}
δT
T

FIGURE 5.24 Flyback converter.

be kept relatively low, normally <50%, that is, $\delta < 0.5$. In practice, the duty-cycle is taken at ≈0.4, which limits the peak collector. A second design factor the transistor must meet is the working collector current at turn-on, dependent on the primary transformer-choke peak current, the primary-to-secondary turns ratio, and the output load current. When the transistor turns on, the primary current builds up in the primary winding and thus stores energy, as the transistor turns off, the diode at the secondary winding is forward biasing, which releases the stored energy into the output capacitor and

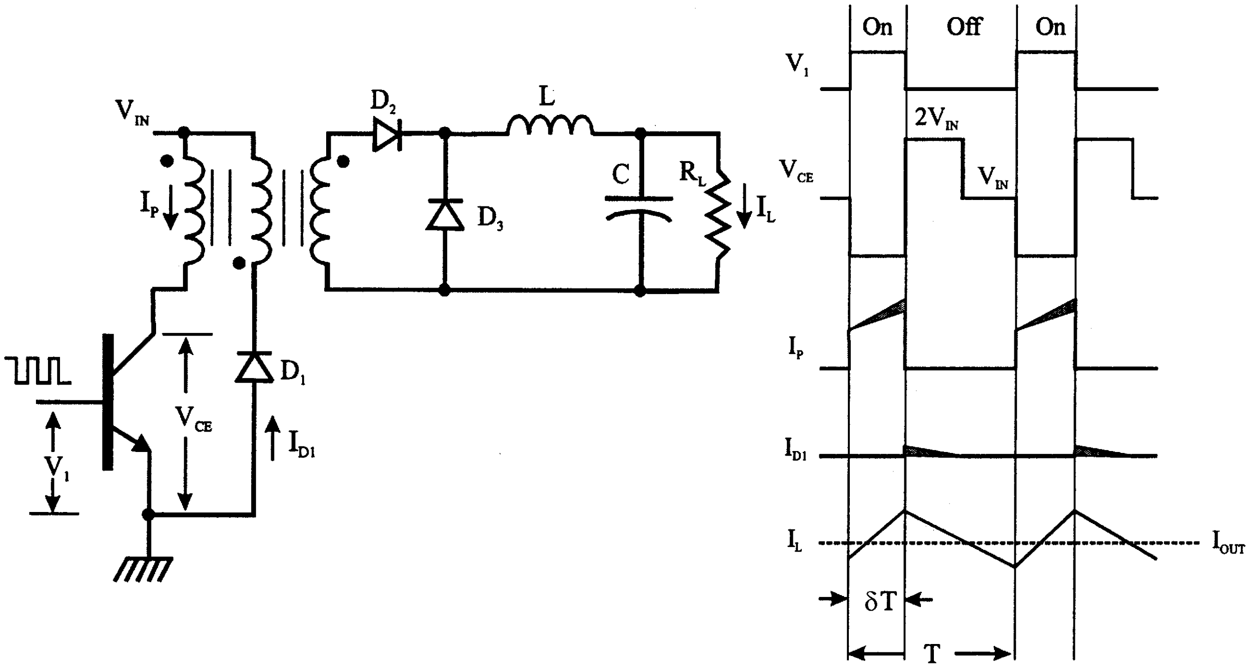

On
Off
On
V_1
V_{IN}
D_2
L
D_3
C
R_L
I_L
I_P
D_1
I_{D1}
V_{CE}
V_1
$2V_{IN}$
V_{IN}
I_P
I_{D1}
I_L
I_{OUT}
δT
T

FIGURE 5.25 Isolated forward converter.

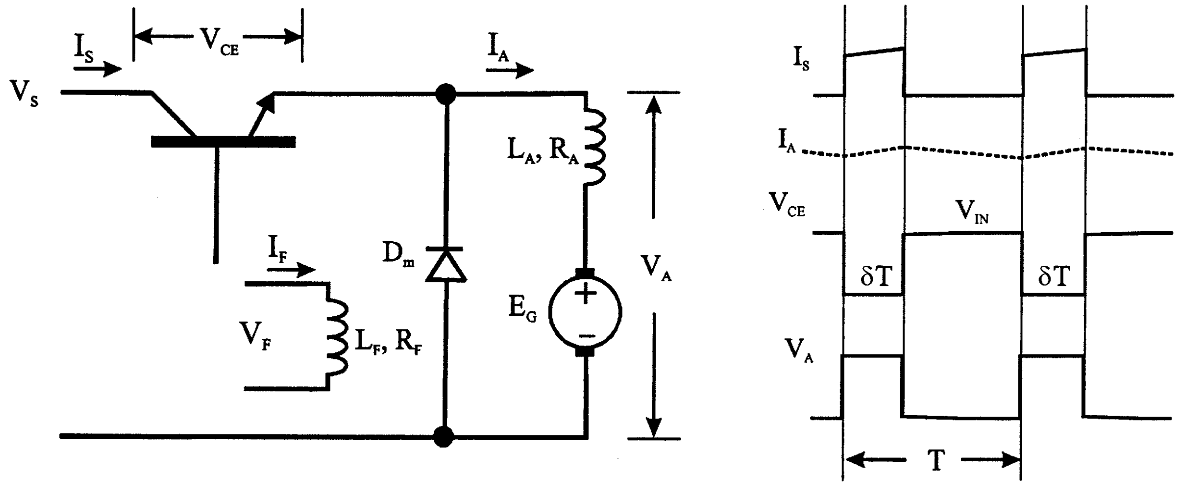


FIGURE 5.26 Chopper-fed dc drive.

load. Such a transformer operating as a coupled inductor is actually defined as a transformer-choke. The transformer-choke of the flyback converter must be designed carefully so as to avoid saturation because the operation is unidirectional on the B-H characteristic curve. Therefore, a core with a relatively large volume and air gap must be used. An advantage of the flyback circuit is the simplicity by which a multiple output switching power supply may be realized. This is because the isolation element acts as a common choke to all outputs and thus only a diode and a capacitor are needed for an extra output voltage.

Figure 5.25 shows the basic forward converter and its associated waveforms. The isolation element in the forward converter is a pure transformer that should not store energy and, therefore, a second inductive element L is required at the output for proper and efficient energy transfer. Notice that the primary and secondary windings of the transformer have the same polarity, that is, the dots are at the same winding ends. When the transistor turns on, current builds up in the primary winding. Because of the same polarity of the transformer secondary winding, such energy is forward transferred to the output and also stores in inductor L through diode $D2$, which is forward-biased. When the transistor turns off, the transformer winding voltage reverses, back-biasing diode $D2$, and the flywheel diode $D3$ is forward-biased, conducting currents in the output loop and delivering energy to the load through inductor L. The tertiary winding and diode D provide transformer demagnetisation by returning the transformer magnetic energy into the output dc bus. It should be noted that the duty cycle of the switch b must be kept $<50\%$ so that when the transformer voltage is clamped through the tertiary winding, the integral of the volt-seconds between the input voltage and the clamping level balances to zero. Duty cycles $>50\%$, that is, $\delta > 0.5$, will upset the volt-seconds balance, driving the transformer into saturation, which in turn produces high collector current spikes that may destroy the switching transistor. Although the clamping action of the tertiary winding and the diode limit the transistor peak collector voltage to the dc input, care must be taken during construction to couple the tertiary winding tightly to the primary (bifilar wound) to eliminate voltage spikes caused by leakage inductance.

Chopper drives are connected between a fixed-voltage dc source and a dc motor to vary the armature voltage. In addition to armature voltage control, a dc chopper can provide regenerative braking of the motors and will return energy back to the supply. This energy-saving feature is desirable for transportation systems such as mass rapid transit ones (MRT) and chopper drives are also used in battery electric vehicles. A dc motor can be operated in one of the four quadrants by controlling the armature of field voltages (or currents). It is often required that the armature or field terminals be reversed in order to operate the motor in the desired quadrant. Figure 5.26 shows a circuit arrangement of a chopper-fed dc separately excited motor. This is a one-quadrant drive and the waveforms for the armature voltage, load current, and input current are also shown. By varying the duty cycle, the power flow to the motor (and speed) can be controlled.

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6

The Power MOSFET

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6.1 Introduction

This chapter gives an overview of power MOSFET semiconductor switching devices. Detailed discussion of the physical structure, fabrication and physical behavior of the device and packaging is beyond the scope of this chapter. The emphasis here will be on the terminal *i-v* switching characteristics of the available device, turn-on and turn-off switching characteristics, PSpice modeling and its current voltage and switching limits. Even though, most of today's available semiconductor power devices are made of silicon or germanium materials, other materials such as gallium arsenide, diamond and silicon carbide are currently being tested.

One of the main contributions that led to the growth of the power electronics field has been the unprecedented advancement in semiconductor technology, especially with respect to switching speed and power handling capabilities. The area of power electronics started by the introduction of the silicon controlled rectifier (SCR) in 1958. Since then, the field has grown in parallel with the growth of the power semiconductor device technology. In fact, the history of power electronics is very much connected to the development of switching devices and it emerged as a separate discipline when high-power and MOSFET devices were introduced in the 1960s and 1970s. Since then, the introduction of new devices has been accompanied by dramatic improvement in power rating and switching performance. Because of their functional importance, drive complexity, fragility, and cost, the power electronic design engineer must be equipped with a thorough understanding of the device operation, limitation, drawbacks, and related reliability and efficiency issues.

In the 1980s, the development of power semiconductor devices took an important turn when new process technology was developed that allowed integration of MOS and bipolar junction transistor (BJT) technologies on the same chip. Thus far, two devices using this new technology have been introduced: insulated bipolar transition (IGBT) and MOS-controlled thyristor (MCT). Many integrated circuit (IC) processing methods as well as equipment have been adapted for the development of power devices. However, unlike microelectronic ICs, which process information, power device ICs process power and so their packaging and processing techniques are quite different. Power semiconductor devices represent the "heart" of modern power electronics, with two major desirable characteristics of power semiconductor devices guiding their development:

1. switching speed (turn-on and turn-off times); and
2. power handling capabilities (voltage blocking and current carrying capabilities).

Improvements in both semiconductor processing technology and manufacturing and packaging techniques have allowed power semiconductor development for high-voltage and high current ratings and fast turn-on and turn-off characteristics.

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Today, switching devices are manufactured with amazing power handling capabilities and switching speeds as will be shown later. The availability of different devices with different switching speeds, power handling capabilities, size, cost etc., makes it possible to cover many power electronics applications. As a result, trade-offs are made when it comes to selecting power devices.

6.2 The Need for Switching in Power Electronic Circuits

As already stated, the heart of any power electronic circuit is its semiconductor-switching network. The question arises here as to whether we have to use switches to perform electrical power conversion from the source to the load. The answer, of course, is no, as there are many circuits that can perform energy conversion without switches, including linear regulators and power amplifiers. However, the need to use semiconductor devices to perform conversion functions is very much related to converter efficiency. In power electronic circuits, the semiconductor devices are generally operated as switches, that is, either in the on-state or the off-state. This is unlike the case for power amplifiers and linear regulators where semiconductor devices operate in the linear mode. As a result, a very large amount of energy is lost within the power circuit before the processed energy reaches the output. Semiconductor switching devices are used in power electronic circuits because of their ability to control and manipulate very large amounts of power from the input to the output with a relatively very low power dissipation in the switching device. Their use helps to create a very highly efficient power electronic system.

Efficiency is considered an important figure of merit and has significant implications for overall system performance. Low efficiency power systems, large amounts of power are dissipated in the form of heat, which results in one or more of the following implications:

1. Cost of energy increases due to increased consumption.
2. Additional design complications might be imposed, especially regarding the design of device heat sinks.
3. Additional components such as heat sinks increase cost, size and weight of the system, resulting in low-power density.
4. High-power dissipation forces the switch to operate at low switching frequency, resulting in limited bandwidth, slow response, and most important, the size and weight of magnetic components (inductors and transformers) and capacitors remain large. Therefore, it is always desired to operate switches at very high frequencies. However, we will show later that as the switching frequency increases, the average switching power dissipation increases. Hence, a trade-off must be made between reduced size, weight and cost of components versus reduced switching power dissipation, which means inexpensive low switching frequency devices.
5. Reduced component and device reliability.

For more than 30 years, it has been shown that switching (mechanical or electrical) is the best possible way to achieve high efficiency. However, unlike mechanical switches, electronic switches are far more superior because of their speed and power handling capabilities as well as reliability.

We should note that the advantages of using switches do not come without a cost. Because of the nature of switch currents and voltages (square waveforms), high-order harmonics are normally generated in the system. To reduce these harmonics, additional input and output filters are normally added to the system. Moreover, depending on the device type and power electronic circuit topology used, driver circuit control and circuit protection can significantly increase both the complexity of the system and its cost.

Example 6.1. The purpose of this example is to investigate the efficiency of four different power circuits whose functions are to take in power from 24-V dc source and deliver a 12-V dc output to a 6-Ω resistive load. In other words, these circuits serve as a dc transformer with a ratio of 2:1. The four circuits shown in Fig. 6.1a,b,c,d represent the voltage divider circuit, Zener regulator, transistor linear regulator, and switching circuit, respectively. The objective is to calculate the efficiency of these four power electronic circuits.

Solution 6.1. *Voltage divider dc regulator:* The first circuit, the simplest, forms a voltage divider with $R = R_L = 6\ \Omega$ and $V_o = 12$ V. The efficiency defined as the ratio of the average load power P_L to the average input power, P_{in}

$$\begin{aligned}\eta &= \frac{P_L}{P_{\text{in}}}\% \\ &= \frac{R_L}{R_L + R}\% = 50\%\end{aligned}$$

In fact, efficiency is simply V_o/V_{in} . As the output voltage becomes smaller, the efficiency decreases proportionally.

Zener dc Regulator: Since the desired output is 12 V, we select a Zener diode with Zener breakdown $V_Z = 12$ V. Assume the Zener diode has the *i-v* characteristic shown in Fig. 6.1(e); as $R_L = 6\ \Omega$, the load current I_L, is 2 A. Then we calculate R for $I_Z = 0.2$ A (10 of the load current). This results in $R = 5.27\ \Omega$. The input power is $P_{\text{in}} = 2.2\ \text{A} \times 24\ \text{V} = 52.8$ W and the output power is

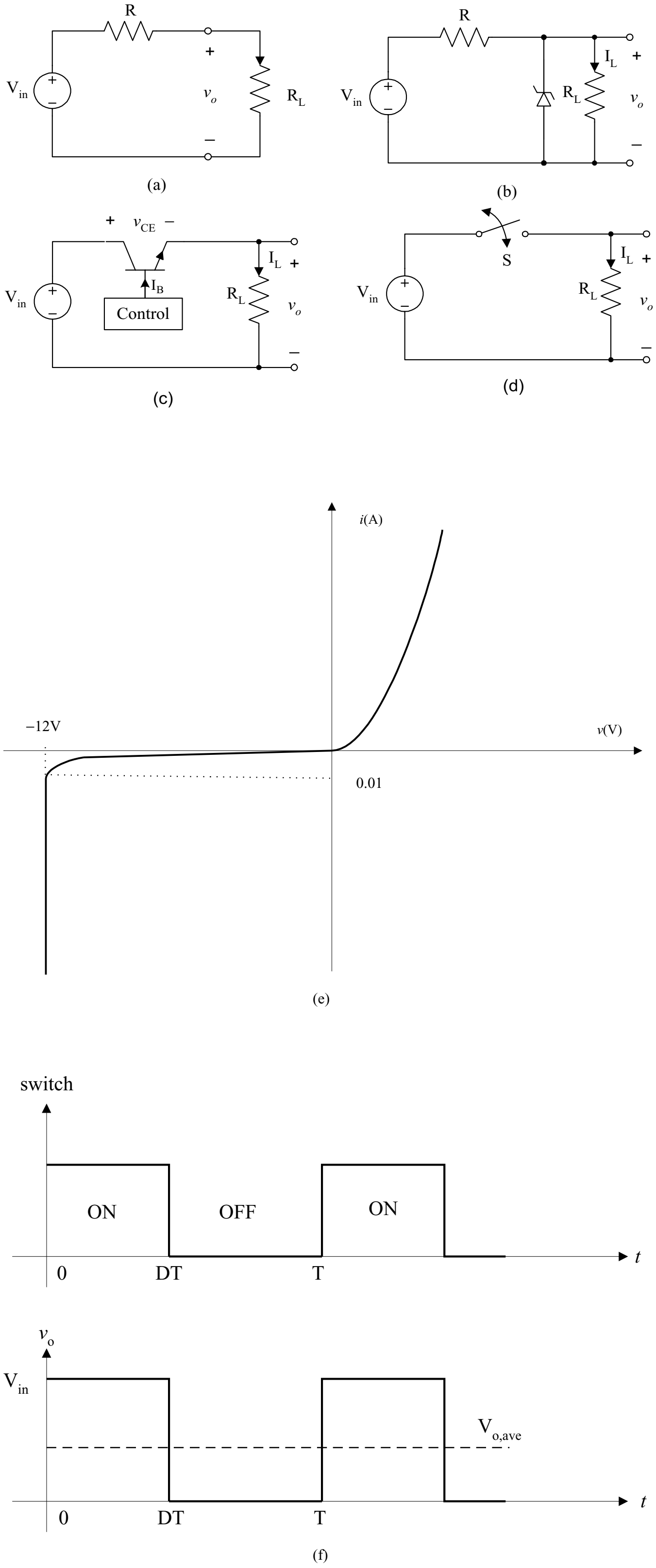


FIGURE 6.1 (a) Voltage divider; (b) Zener regulator; (c) transistor regulator; (d) switching circuit; (e) *i-v* Zener diode characteristics and (f) switching and output waveforms.

$P_{out} = 24$ W. The efficiency of the circuit is given by

$$\eta = \frac{24\text{ W}}{52.8\text{ W}}\% \\ = 45.5\%$$

Transistor dc Regulator: It is clear from Fig. 6.1c that for $V_o = 12$ V, the collector emitter voltage must by ≈ 12 V. Hence, the control circuit must provide base current I_B to put the transistor in the active mode with $V_{CE} \approx 12$ V. As the load current is 2 A, then collector current is approximately 2 A (assume small I_B). The total power dissipated in the transistor can be approximated by the following equation:

$$P_{diss} = V_{CE}I_C + V_{BE}I_B \\ \approx V_{CE}I_C \approx 12 \times 2 = 24\text{ W}$$

Therefore, the efficiency of the circuit is 50 .

Switching dc Regulator: Let us consider the switching circuit of Fig. 6.1d by assuming the switch is ideal and is periodically turned on and off in Fig. 6.1f. The output voltage waveform is shown in Fig. 6.1f. Although the output voltage is not constant or pure dc, its average value is given by

$$V_{o,\text{ave}} = \frac{1}{T}\int_o^{T_o} V_{\text{in}}dt = V_{\text{in}}D$$

where D is the duty ratio and it equals the ratio of the on-time to the switching period. For $V_{o,\text{ave}} = 12$ V, we set $D = 0.5$, that is, the switch has a duty cycle of 0.5 or 50 . Here the average output power is 48 W and the average input power is also 48 W, resulting in 100 efficiency This is of course because we assumed that the switch is ideal. However, if we assume that a BJT switch is used in forementioned circuit with $V_{CE,\text{sat}} = 1$ V and I_B is small, then the average power loss across the switch is approximately 2 W, which creates an overall efficiency of 96 . Of course, the switching circuit given in this example is over simplified because the switch requires additional driving circuitry that was not shown, and which also dissipates some of the power. However, the example illustrates that higher efficiency can be obtained by switching to a power electronic circuit as compared to the efficiency obtained from a linear power electronic circuit. Further, the difference between the linear circuit in Fig. 6.1b and 6.1c and the switched circuit of Fig. 6.1d is that the power delivered to the load in the latter case pulsates between zero and 96 W. If the application calls for constant power delivery with little output voltage ripple, then an LC filter must be added to smooth out the output voltage.

A final observation is required on what is known as load and line regulation. Line regulation is defined as the ratio between the change in output voltage ΔV_o, with respect to the change in the input voltage ΔV_{in}. These are very important parameters in power electronics because the dc input voltage is obtained from a rectified line voltage that normally changes by ±20%. Therefore, any off-line power electronics circuit must have a limited or specified range of line regulation. If we assume that the input voltage in Fig. 6.1a,b is changed by 2 V, that is $\Delta V_{\text{in}} = 2$ V, and with R_L unchanged, the corresponding change in the output voltage ΔV_o is 1 V and 0.55 V, respectively. This is considered very poor line regulation. Figure 6.1c,d have much better line and load regulations because the closed-loop control compensates for the line and load variations.

6.3 General Switching Characteristics

6.3.1 The Ideal Switch

It is always desirable to have power switches perform as close as possible to the ideal case. For a semiconductor device to operate as an ideal switch, it must possess the following features:

1. no limit on the amount of current (known as forward or reverse current) the device can carry when in the conduction state (on-state);
2. No limit on the amount of device-voltage ((known as forward- or reverse-blocking voltage) when the device is in the nonconduction state off-state;
3. zero on-state voltage drop when in the conduction state;
4. infinite off-state resistance, that is, zero leakage current when in the nonconduction state; and
5. no limit on the operating speed of the device when a state is changed, that is, zero rise and fall times.

The switching waveforms for an ideal switch are shown in Fig. 6.2, where i_{sw} and v_{sw} are the current through and the voltage across the switch, respectively.

During switching and conduction periods the power loss is zero, resulting in a 100 efficiency; with no switching delays, an infinite operating frequency can be achieved. In short, an ideal switch has infinite speed, unlimited power handling capabilities, and 100 efficiency. It must be noted that it is not surprising to find semiconductor-switching devices that for all practical purposes can almost perform as ideal switches for number of applications.

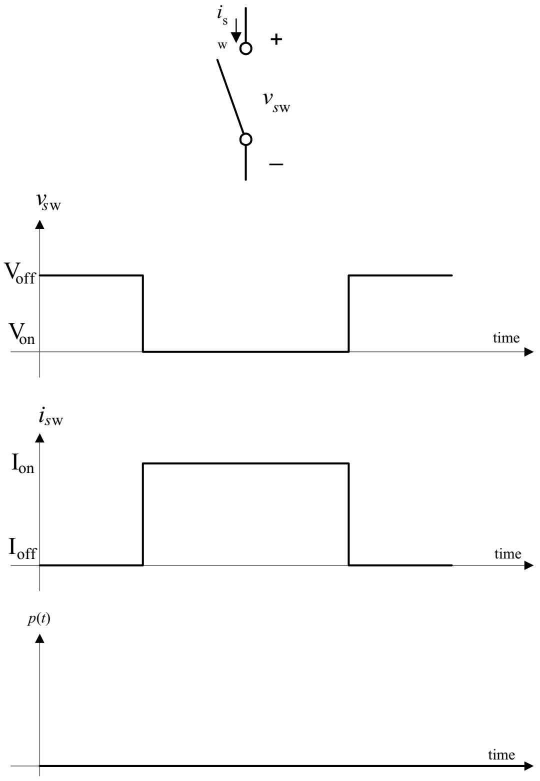


FIGURE 6.2 Ideal switching current, voltage and power waveforms.

6.3.2 The Practical Switch

The practical switch has the following switching and conduction characteristics:

1. Limited power handling capabilities, that is, limited conduction current when the switch is in the on-state, and limited blocking voltage when the switch is in the off-state.
2. Limited switching speed caused by the finite turn-on and turn-off times. This limits the maximum operating frequency of the device.
3. Finite on-state and off-state resistances, that is, forward voltage drop exists when in the on-state, and reverse current flow (leakage) exists when in the off-state.
4. Because of characteristics 2 and 3, the practical switch experiences power losses in the on- and off-states (known as conduction loss), and during switching transitions (known as switching loss).

The typical switching waveforms of a practical switch are shown in Fig. 6.3a.

The average switching power and conduction power losses can be evaluated from these waveforms. We should point out that the exact practical switching waveforms vary from one device to another device, but Fig. 6.3a gives a reasonably good representation, Moreover, other issues such as temperature dependence, power gain, surge capacity, and over-voltage capacity must be considered when addressing specific devices for specific applications. A useful plot that illustrates how switching takes place from on to off and vice versa is what is called *switching trajectory*, which is simply a plot of i_{sw} vs v_{sw}.

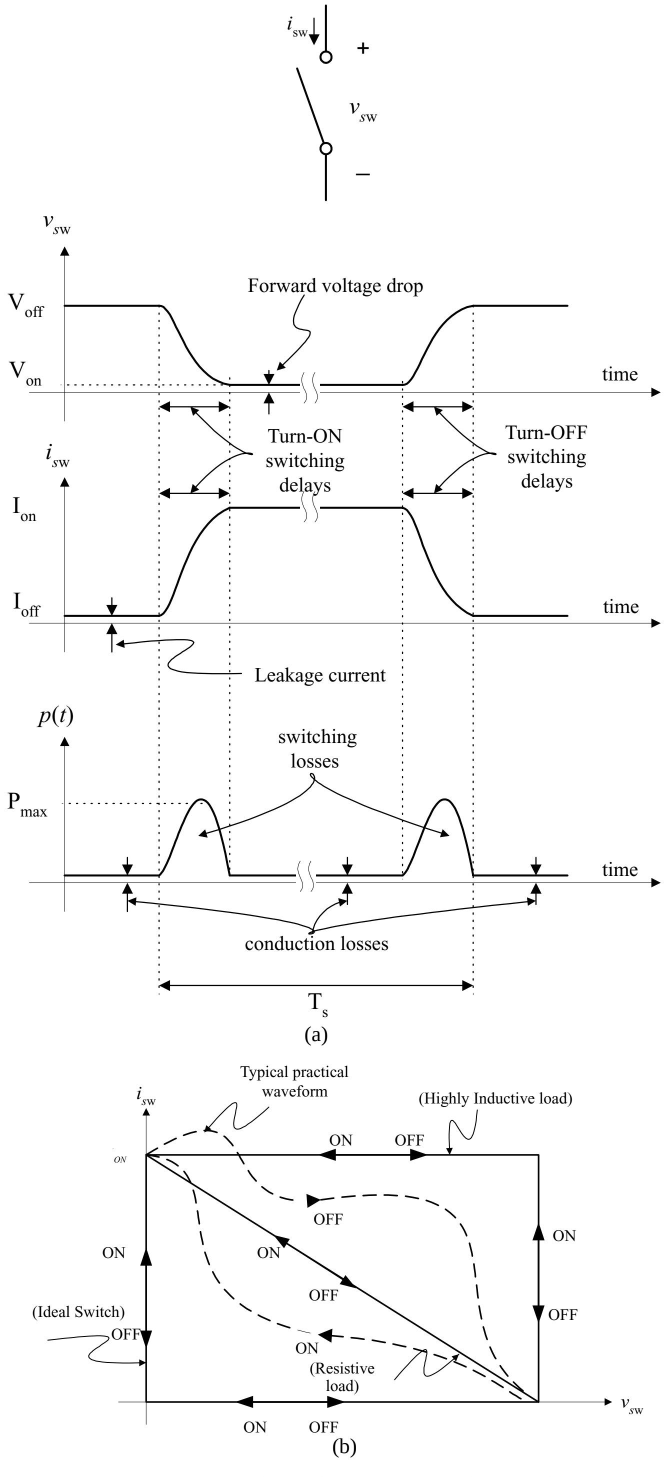

i_{sw}
+
v_{sw}
–
v_{sw}
V_{off}
Forward voltage drop
V_{on}
time
Turn-ON switching delays
Turn-OFF switching delays
i_{sw}
I_{on}
I_{off}
time
Leakage current
$p(t)$
switching losses
P_{max}
time
conduction losses
T_s
(a)
Typical practical waveform
(Highly Inductive load)
i_{sw}
ON
OFF
(Ideal Switch)
(Resistive load)
v_{sw}
(b)

FIGURE 6.3 (a) Practical switching current, voltage and power waveforms; and (b) switching trajectory.

Figure 3(b) shows several switching trajectories for the ideal and practical cases under resistive loads.

EXAMPLE 6.2. Consider a linear approximation of Fig. 6.3a as shown in Fig. 6.4a: (a) give a possible circuit implementation using a power switch whose switching waveforms are shown in Fig. 6.4a; (b) derive the expressions for the instantaneous switching and conduction power losses and sketch them; (c) determine the total average power dissipated in the circuit during one switching frequency; and (d) determine the maximum power.

SOLUTION 6.2. (a) First let us assume that the turn-on time t_{on} and turn-off time t_{off}, the conduction voltage V_{ON}, and the leakage current I_{OFF}, are part of the switching characteristics of the switching device and have nothing to do with circuit topology.

When the switch is off, the blocking voltage across the switch is V_{OFF}, which can be represented as a dc voltage source of value V_{OFF} reflected somehow across the switch during the off-state. When the switch is on, the current through the switch equals I_{ON}, and hence a dc current is needed in series with the switch when it is in the on-state. This suggests that when the switch turns off again, the current in series with the switch must be diverted somewhere else (this process is known as

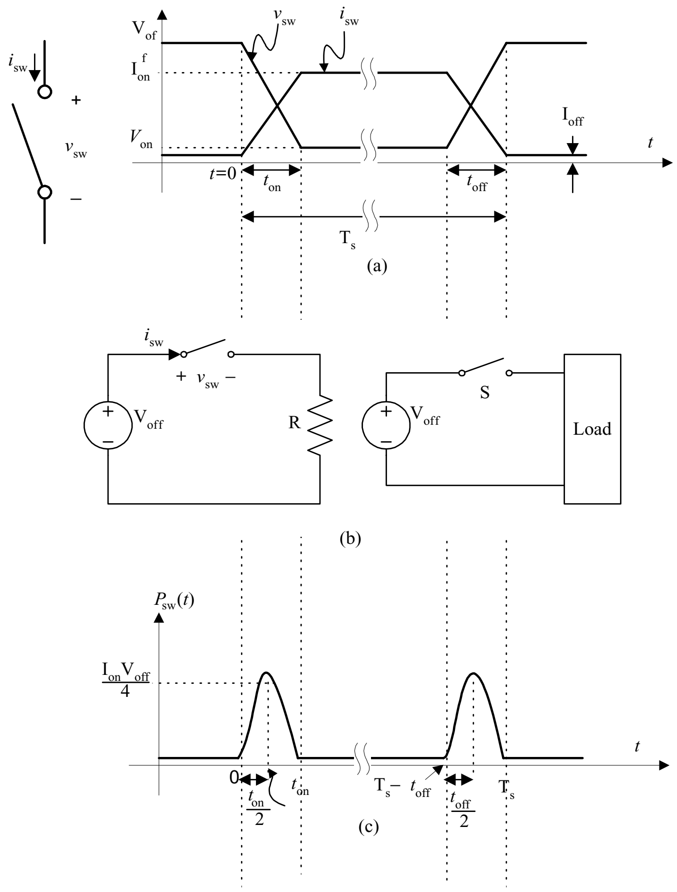

i_{sw}
+
v_{sw}
–
V_{off}
I_{on}
V_{on}
v_{sw}
i_{sw}
I_{off}
t
$t=0$
t_{on}
t_{off}
T_s
(a)
i_{sw}
+ v_{sw} –
V_{off}
R
S
Load
(b)
$P_{sw}(t)$
$\frac{I_{on}V_{off}}{4}$
t
0
$\frac{t_{on}}{2}$
t_{on}
$T_s - t_{off}$
$\frac{t_{off}}{2}$
T_s
(c)

FIGURE 6.4 Linear approximation of typical current and voltage switching waveforms.

commutation). As a result, a second switch is needed to carry the main current from the switch being investigated when it is switched off. However, as i_{sw} and v_{sw} are linearly related as shown in Fig. 6.4, a resistor will do the trick and a second switch is not needed. Figure 6.4 shows a one-switch implementation with S the switch and R the switched-load.

(b) The instantaneous current and voltage waveforms during the transition and conduction times are given as follows:

$$i_{sw}(t) = \begin{cases} \dfrac{t}{t_{ON}}(I_{ON} - I_{OFF}) + I_{OFF} & 0 \le t \le t_{ON} \\ I_{ON} & t_{ON} \le t \le T_s - t_{OFF} \\ -\dfrac{t - T_s}{t_{off}}(I_{ON} - I_{OFF}) + I_{OFF} & \\ & T_s - t_{OFF} \le t \le T_s \end{cases}$$

$$V_{sw}(t) = \begin{cases} -\dfrac{V_{OFF} - V_{ON}}{t_{ON}}(t - t_{ON}) + V_{ON} & \\ & 0 \le t \le t_{ON} \\ V_{ON} & t_{ON} \le t \le T_s - t_{OFF} \\ \dfrac{V_{OFF} - V_{ON}}{t_{OFF}}(t - (T_s - t_{OFF})) + V_{ON} & \\ & T_s - t_{OFF} \le t \le T_s \end{cases}$$

It can be shown that if we assume $I_{ON} \gg I_{OFF}$ and $V_{OFF} \gg V_{ON}$, then the instantaneous power $p(t) = i_{sw}v_{sw}$ can be given as follows:

$$p(t) = \begin{cases} -\dfrac{V_{OFF}I_{ON}}{t_{ON}^2}(t - t_{ON})t & 0 \le t \le t_{ON} \\ V_{ON}I_{ON} & t_{ON} \le t \le T_s - t_{OFF} \\ -\dfrac{V_{OFF}I_{ON}}{t^2}(t = (T_s - t_{OFF}))(t - T_s) & \\ & T_s - t_{OFF} \le t \le T_s \end{cases}$$

Figure 6.4(c) shows a plot of the instantaneous power where the maximum power during turn-on and turn-off is $V_{OFF}I_{ON}/4$.

(c) The total average dissipated power is given by

$$P_{ave} = \frac{1}{T_s}\int_0^{T_s} p(t)dt = \frac{1}{T_s}\left[\int_0^{t_{ON}} -\frac{V_{OFF}I_{ON}}{t_{ON}^2}(t - t_{ON})t\, dt + \int_{t_{ON}}^{T_s - t_{OFF}} V_{ON}I_{ON}\, dt + \int_{T_s - t_{OFF}}^{T_s} -\frac{V_{OFF}I_{ON}}{t_{OFF}^2}(t - (T_s - t_{OFF}))(t - T_s)dt\right]$$

The evaluation of the preceding integral gives

$$P_{ave} = \frac{V_{OFF}I_{ON}}{T_s}\left(\frac{t_{ON} + t_{OFF}}{6}\right) + \frac{V_{ON}I_{ON}}{T_s}(T_s - t_{OFF} - t_{ON})$$

The first expression represents the total switching loss and the second represents the total conduction loss over one switching cycle. We notice that as frequency increases, average power increases linearly. In addition, power dissipation increases with an increase in the forward conduction current and the reverse-blocking voltage.

(d) The maximum power occurs at the time when the first derivative of $p(t)$ during switching is set to zero, that is,

$$\left.\frac{dp(t)}{dt}\right|_{t=t_{max}} = 0$$

Solving the preceding equation for t_{max}, we obtain values at turn-on and turn-off, respectively,

$$t_{max} = \frac{t_{rise}}{2}$$

$$t_{max} = T - \frac{T_{fall}}{2}$$

Solving for maximum power, we obtain

$$P_{max} = \frac{V_{off}I_{on}}{4}$$

6.4 The Power MOSFET

Unlike the bipolar junction transistor (BJT), the MOSFET device belongs to the *unipolar device family, because it uses only the majority carriers in conduction.* The development of metal-oxide-semiconductor (MOS) technology for microelectronic circuits opened the way for development of the power metal oxide semiconductor field effect transistor (MOSFET) device in 1975. Selecting the most appropriate device for a given application is not an easy task because it requires knowledge about the device characteristics, their unique features, innovation, and engineering design experience. Unlike low-power (signal devices), high-power devices are more complicated in structure, driver design, and their operational *i-v* characteristics are difficult to understand. This knowledge is very important for power electronics engineers when designing circuits that will make these devices close to ideal. The device symbol for a *p*- and *n*-channel enhancement and depletion types are shown in Fig. 6.5. Figure 6.6 shows the *i-v* characteristics for the *n*-channel enhancement-type MOSFET. It is the fastest power switching device, with switching frequency >MHz, and with voltage power ratings up to 600 V and current rating as high as 40 A. Regions of operations for MOSFET will be studied.

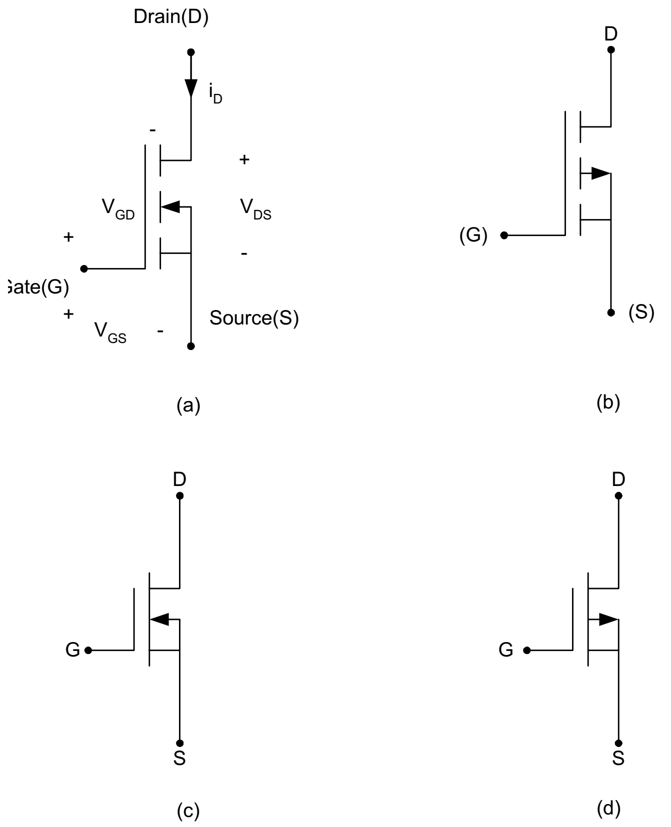


FIGURE 6.5 Device symbols: (a) n-channel enhancement-mode; (b) p-channel enhancement-mode; (c) n-channel depletion-mode; and (d) p-channel depletion-mode.

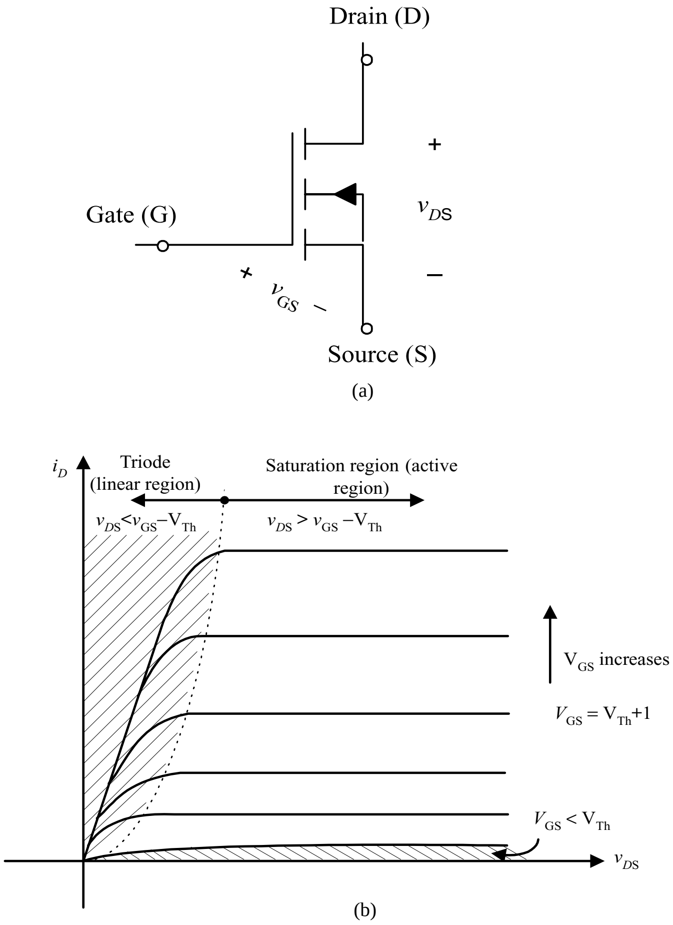


FIGURE 6.6 (a) The n-channel enhancement-mode MOSFET; and (b) its i_D vs v_{DS} characteristics.

6.5 MOSFET Structure

Unlike the lateral channel MOSFET devices used in much of the IC technology in which the gate, source and drain terminals are located at the same surface of the silicon wafer, power MOSFETs use vertical channel structure in order to increase the device power rating [1]. In the vertical channel structure, the source and drain are on opposite side of the silicon wafer. Figure 6.7a shows a vertical cross-sectional view for a power MOSFET. Figure 6.7b shows a more simplified representation. There are several discrete types of the vertical structure power MOSFET available commercially today, including V-MOSFET, U-MOSFET, D-MOSFET, and S-MOSFET [1, 2]. The p-n junction between the p-base (also referred to as body or bulk region) and the n-drift region provide the forward voltage blocking capabilities. The source metal contact is connected directly to the p-base region through a break in the n^+-source region in order to allow for a fixed potential to the p-base region during normal device operation. When the gate and source terminal are set to the same potential ($V_{\mathrm{GS}} = 0$), no channel is established in the p-base region, that is, the channel region remains unmodulated. The lower doping in the n-drift region is needed in order to achieve higher drain voltage blocking capabilities. For the drain-source current I_D to flow, a conductive path must be established between the n^+- and n^--regions through the p-base diffusion region.

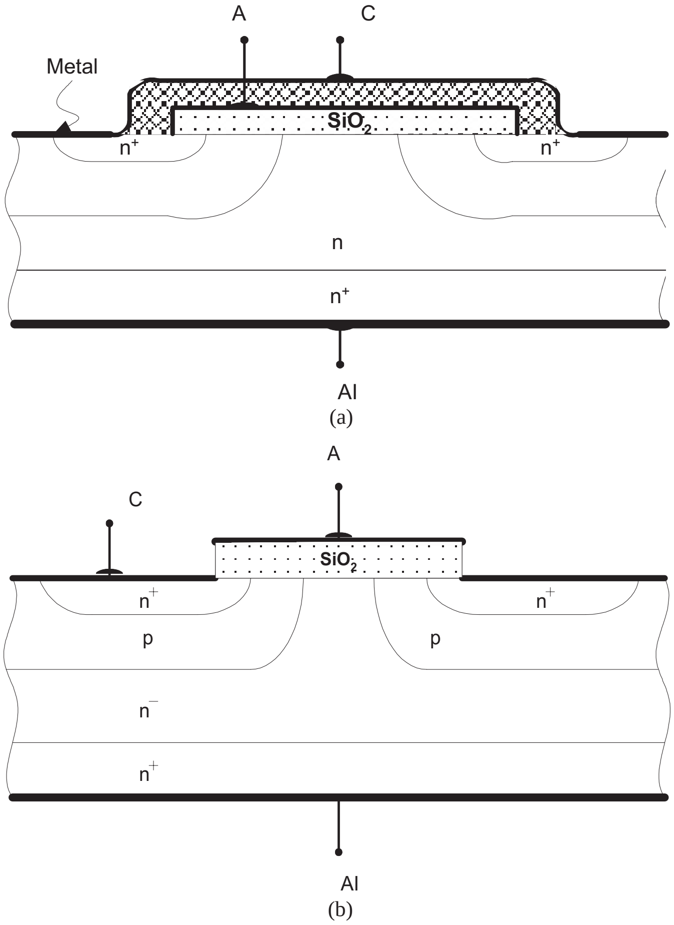
6.5.1 On-State Resistance

When the MOSFET is in the on-state (triode region), the channel of the device behaves like a constant resistance $R_{\mathrm{DS(on)}}$ that is linearly proportional to the change between v_{DS} and i_{D} as given by the following relation:

$$R_{\mathrm{DS(on)}} = \frac{\partial v_{\mathrm{DS}}}{\partial i_D}\Big|_{v_{\mathrm{GS=Constant}}} \tag{6.1}$$

The total conduction (on-state) power loss for a given MOSFET with forward current I_D and on-resistance $R_{\mathrm{DS(on)}}$ is given by

$$P_{\mathrm{on,diss}} = I_D^2 R_{\mathrm{DS(on)}} \tag{6.2}$$



(a)

(b)

FIGURE 6.7 (a) Vertical cross-sectional view for a power MOSFET; and (b) simplified representation.

The value of $R_{DS(on)}$ can be significant and varies between tens of milliohms and a few ohms for low-voltage and high-voltage MOSFETS, respectively. The on-state resistance is an important data sheet parameter, because it determines the forward voltage drop across the device and its total power losses.

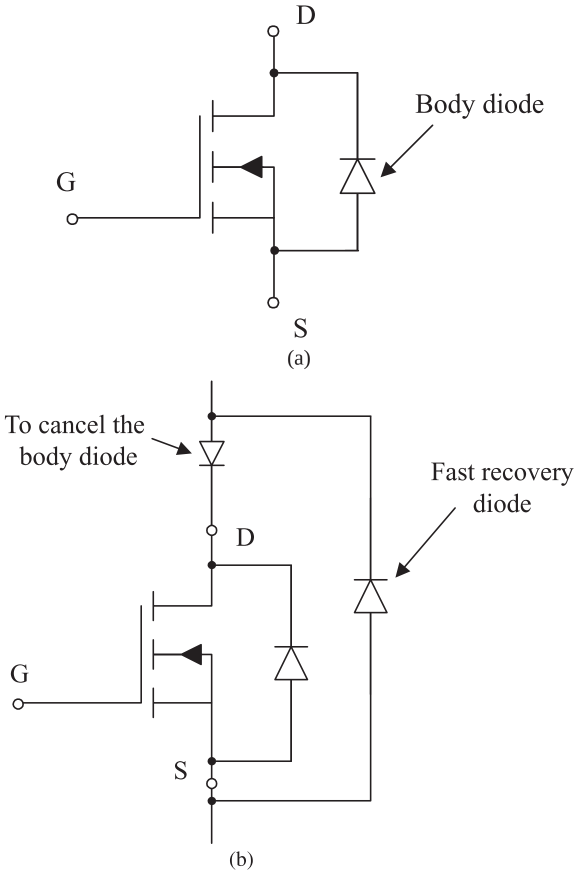
Unlike the current-controlled bipolar device, which requires base current to allow the current to flow in the collector, the power MOSFET device is a voltage-controlled unipolar device and requires only a small amount of input (gate) current. As a result, it requires less drive power than the BJT. However, it is a nonlatching current like the BJT, that is, a gate source voltage must be maintained. Moreover, as only majority carriers contribute to the current flow, MOSFETs surpass all other devices in switching speed, which switching speeds can exceed a few megahertz. Comparing the BJT and the MOSFET, the BJT has greater power handling capabilities and smaller switching speed, while the MOSFET device has less power handling capabilities and relatively fast switching speed. The MOSFET device has a higher on-state resistor than the bipolar transistor. Another difference is that the BJT parameters are more sensitive to junction temperature when compared to the MOSFET and, unlike the BJT, MOSFET devices do not suffer from second breakdown voltages and sharing current in parallel devices is possible.

6.5.2 Internal Body Diode

The modern power MOSFET has an internal diode called a body diode connected between the source and the drain as shown in Fig. 6.8a. This diode provides a reverse direction for the drain current, allowing a bidirectional switch implementation. Even though the MOSFET body diode has adequate current and switching speed ratings, in some power electronic applications that require the use of ultra-fast diodes, an external fast recovery diode is added in antiparallel fashion after blocking the body diode by a slow recovery diode as shown in Fig. 6.8b.

6.5.3 Internal Capacitors

Another important parameter that affect the MOSFET switching behavior are the parasitic capacitances between the device's three terminals, namely, gate-to-source, C_{gs}, gate-to-drain C_{gd} and drain-to-source (C_{ds}) capacitances as shown in Fig. 6.9a. The values of these capacitances are nonlinear and a function



(a)

(b)

FIGURE 6.8 (a) MOSFET internal body diode; and (b) implementation of a fast body diode.

of device structure, geometry, and bias voltages. During turn-on, capacitors C_{gd} and C_{gs} must be charged through the gate, hence, the design of the gate control circuit must take into consideration the variation in these capacitances. The largest variation occurs in the gate-to-drain capacitance as the drain-to-gate voltage varies. The MOSFET parasitic capacitance is given in terms of the device data sheet parameters C_{iss}, C_{oss}, and C_{rss} as follows:

$$C_{gd} = C_{rss}$$
$$C_{gs} = C_{iss} - C_{rss}$$
$$C_{ds} = C_{oss} - C_{rss}$$

where C_{rss} is the small-signal reverse transfer capacitance; C_{iss} is the small-signal input capacitance with the drain and source terminals shorted; and C_{oss} is the small-signal output capacitance with the gate and source terminals shorted.

The MOSFET capacitances C_{gs}, C_{gd} and C_{ds} are nonlinear and a function of the dc bias voltage. The variations in C_{oss} and C_{iss} are significant as the drain-to-source voltage and the gate-to-source voltage each cross zero. The objective of the drive circuit is to charge and discharge the gate-to-source and gate-to-drain parasitic capacitances to turn on and off the device, respectively.

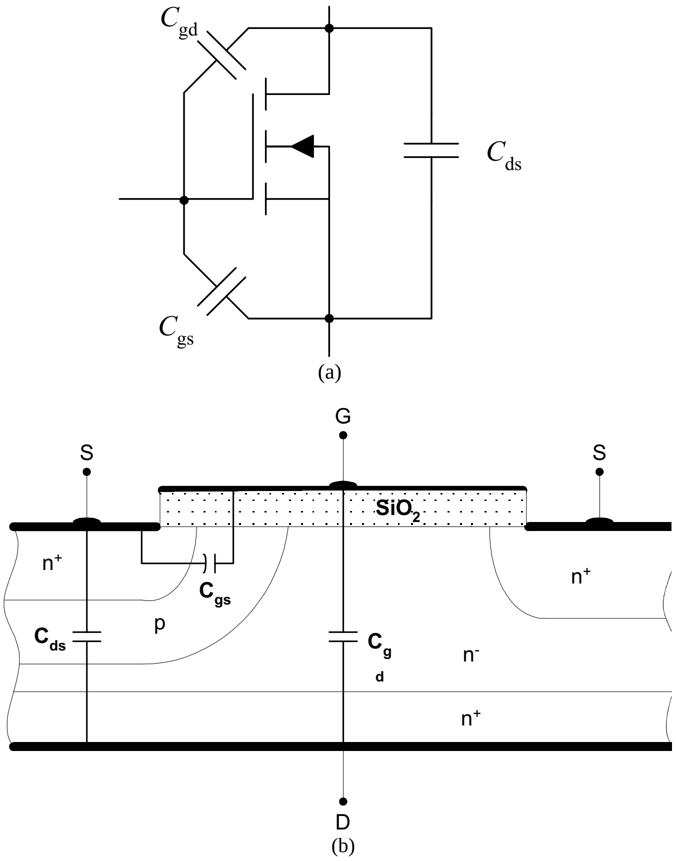


FIGURE 6.9 (a) Equivalent MOSFET representation including junction capacitances; and (b) representation of this physical location.

In power electronics, the aim is to use power-switching devices that operate at higher and higher frequencies. Hence, the size and weight of output transformers, inductors, and filter capacitors will decrease. As a result, MOSFETs are now used extensively in power supply design that requires high switching frequencies, including switching and resonant mode power supplies and brushless dc motor drives. Because of its large conduction losses, its power rating is limited to a few kilowatts. Because of its many advantages over BJT devices, modern MOSFET devices have received high market acceptance.

6.6 MOSFET Regions of Operation

Most MOSFET devices used in power electronics applications are of the *n*-channel, enhancement type, like that shown in Fig. 6.6a. For the MOSFET to carry drain current, a channel between the drain and the source must be created. This occurs when the gate-to-source voltage exceeds the device threshold voltage V_{Th}. For $v_{GS} > V_{Th}$, the device can be either in the triode region, which is also called “constant resistance” region, or in the saturation region, depending on the value of v_{DS}. For given v_{GS}, with small v_{DS} ($v_{DS} < v_{GS} - V_{Th}$), the device operates in the triode region (saturation region in the BJT), and for larger v_{DS} ($v_{DS} > v_{GS} - V_{Th}$), the device enters the saturation region (active region in the BJT). For $v_{GS} < V_{Th}$, the device turns off, with drain current almost equal to zero. Under both regions of operation, the gate current is almost zero. This is why the MOSFET is known as a voltage-driven device and, therefore, requires simple gate control circuit.

The characteristic curves in Fig. 6.6b show that there are three distinct regions of operation labeled as triode region, saturation region, and cut-off region. When used as a switching device, only triode and cut-off regions are used, whereas, when it is used as an amplifier, the MOSFET must operate in the saturation region, which corresponds to the active region in the BJT.

The device operates in the cut-off region (off-state) when $v_{GS} < v_{Th}$, resulting in no induced channel. In order to operate the MOSFET in either the triode or saturation region, a channel must first be induced. This can be accomplished by applying gate-to-source voltage that exceeds v_{Th}, that is,

$$v_{GS} > V_{Th}$$

Once the channel is induced, the MOSFET can operate in either the triode region (when the channel is continuous with no pinch-off, resulting in drain current proportional to the channel resistance) or the saturation region (the channel pinches off, resulting in constant I_D). The gate-to-drain bias voltage (v_{GD}) determines whether the induced channel enters pinch-off or not. This is subject to the following restriction.

For a triode mode of operation, we have

$$v_{\mathrm{GD}} > V_{\mathrm{Th}}$$
$$v_{\mathrm{GD}} < V_{\mathrm{Th}}$$

And for the saturation region of operation, pinch-off occurs when $v_{\mathrm{GD}} = V_{\mathrm{Th}}$.

In terms v_{DS}, the preceding inequalities may be expressed as follows.

1. For triode region of operation

$$v_{\mathrm{DS}} < v_{\mathrm{GS}} - V_{\mathrm{Th}} \quad \text{and} \quad v_{\mathrm{GS}} > V_{\mathrm{Th}} \tag{6.3}$$

2. For saturation region of operation

$$v_{\mathrm{DS}} > v_{\mathrm{GS}} - V_{\mathrm{Th}} \quad \text{and} \quad v_{\mathrm{GS}} > V_{\mathrm{Th}} \tag{6.4}$$

3. For cut-off region of operation

$$v_{\mathrm{GS}} < V_{\mathrm{Th}} \tag{6.5}$$

It can be shown that drain current i_D can be mathematically approximated as follows:

$$i_D = K[2(v_{\mathrm{GS}} - V_{\mathrm{Th}})v_{\mathrm{DS}} - v_{\mathrm{DS}}^2] \quad \textit{triode region} \tag{6.6}$$
$$i_D = K(v_{\mathrm{GS}} - V_{\mathrm{Th}})^2 \quad \textit{saturation region} \tag{6.7}$$

where

$$K = \tfrac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)$$

and μ_n is the electron mobility; C_{OX} is the oxide capacitance per unit area; L is the length of the channel; and W is the width of the channel.

Typical values for these parameters are given in the PSpice model that will be discussed later. At the boundary between the saturation (active) and triode regions, we have

$$v_{\mathrm{DS}} = v_{\mathrm{GS}} - V_{\mathrm{Th}} \tag{6.8}$$

which results in the following equation for i_D:

$$i_D = kv_{\mathrm{DS}}^2 \tag{6.9}$$

The input transfer characteristics curve for i_D vs v_{GS} is when the device is operating in the saturation region shown in Fig. 6.10.

The large signal equivalent circuit model for an n-channel enhancement-type MOSFET operating in the saturation mode is shown in Fig. 6.11. The drain current is represented by a current source as the function of V_{TH} and v_{GS}.

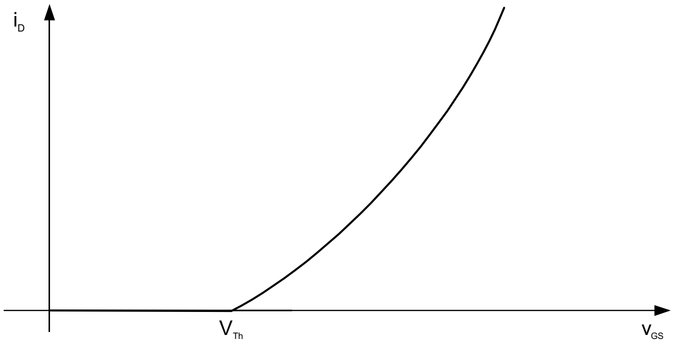


FIGURE 6.10 Input transfer characteristics for a MOSFET device when operating in the saturation region.

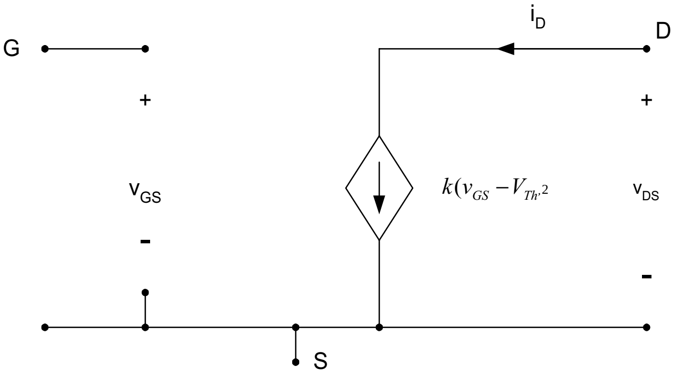


FIGURE 6.11 Large signal equivalent circuit model.

If after the channel is pinched-off, we assume that the drain-source current will no longer be constant but rather depends on the value of v_{DS} as shown in Fig. 6.12, then the increased value of v_{DS} cause a reduced channel length, resulting in a phenomenon known as channel-length modulation [3, 4]. If the $v_{\mathrm{DS}} - i_{\mathrm{D}}$ lines are extended as shown in Fig. 6.12, they all intercept the v_{DS}-axis at a single point labeled $-1/\lambda$, where λ is

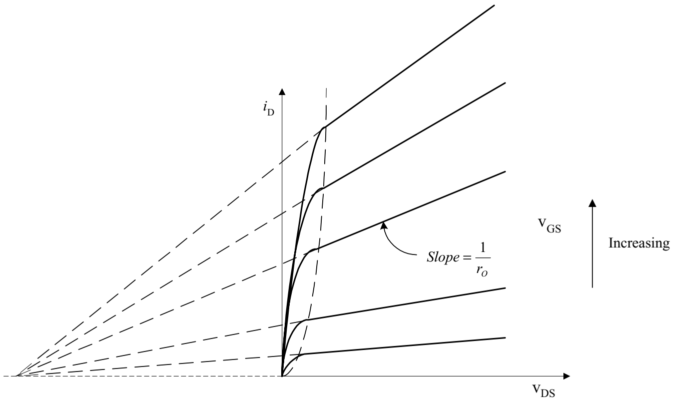


FIGURE 6.12 The MOSFET characteristics curve including output resistance.

a positive constant MOSFET parameter. The term $(1 + \lambda v_{DS})$ is added to the i_D equation in order to account for the increase in i_D due to the channel-length modulation. Here i_D is given by

$$i_D = k(v_{GS} - V_{Th})^2(1 + \lambda v_{DS}) \qquad \textit{saturation region} \qquad (6.10)$$

From the definition of the r_0 given in Eq. 6.11, it is easy to show that the MOSFET output resistance can be expressed as follows:

$$r_0 = \frac{1}{\lambda k(v_{GS} - V_{Th})} \qquad (6.11)$$

If we assume that the MOSFET is operating under small signal condition, that is, the variation in v_{GS} on i_D vs v_{GS} is in the neighborhood of the dc operating point Q at i_D and v_{GS} as shown in Fig. 6.13. As a result, the i_D current source can be represented by the product of the slope g_m and v_{GS} as shown in Fig. 6.14.

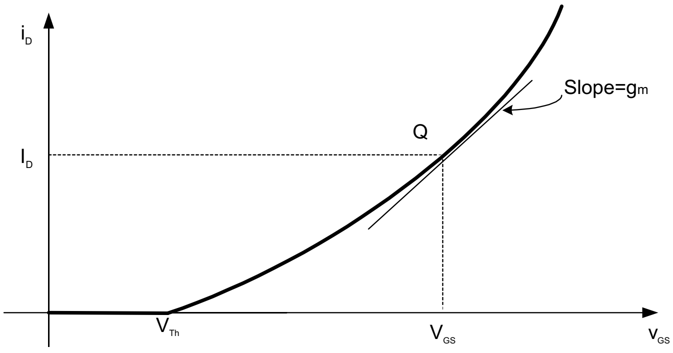


FIGURE 6.13 Linearized i_D vs v_{GS} curve with operating dc point (Q).

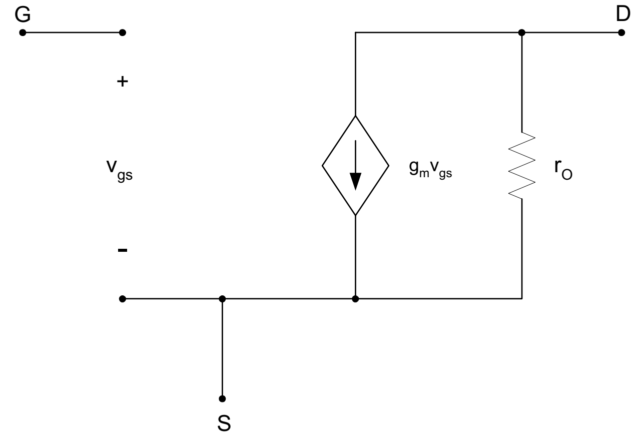


FIGURE 6.14 Small signal equivalent circuit including MOSFET output resistance.

6.6.1 MOSFET Switching Characteristics

Because the MOSFET is a majority carrier transport device, it is inherently capable of high frequency operation [5–8]. However, the MOSFET has two limitations:

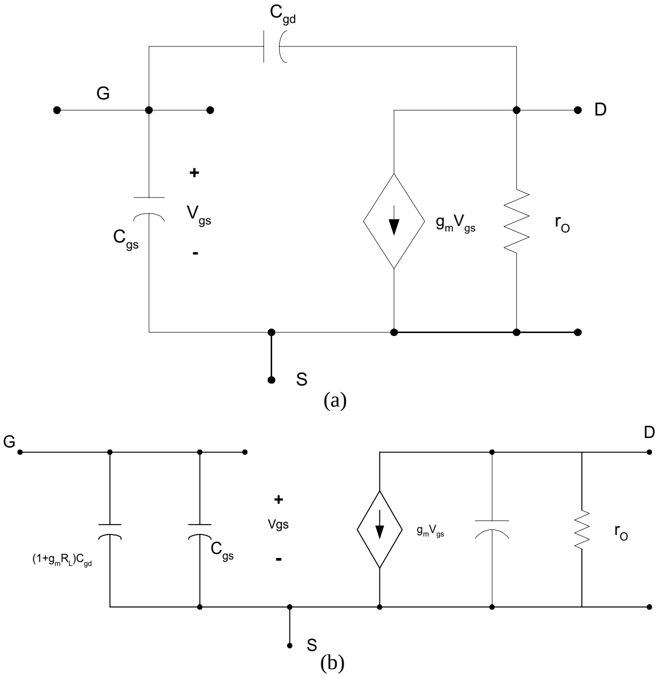
1. high input gate capacitances; and
2. transient/delay due to carrier transport through the drift region.

As stated earlier, the input capacitance consists of two components: the gate-to-source and gate-to-drain capacitances. The input capacitances can be expressed in terms of the device junction capacitances by applying the Miller theorem to Fig. 6.15a. Using the Miller theorem, the total input capacitance C_{in}, seen between the gate-to source, is given by

$$C_{in} = C_{gs} + (1 + g_m R_L)C_{gd} \qquad (6.12)$$

The frequency responses of the MOSFET circuit are limited by the charging and discharging times of C_{in}. The Miller effect is inherent in any feedback transistor circuit with resistive load that exhibits a feedback capacitance from the input and output. The objective is to reduce the feedback gate-to-drain resistance. The output capacitance between the drain-to-source C_{ds} does not affect the turn-on and turn-off MOSFET switching characteristics. Figure 6.16 shows how C_{gd} and C_{gs} vary under increased drain-source v_{Ds} voltage.

In power electronics applications, power MOSFET are operated at high frequencies in order to reduce the size of



(a)

(b)

FIGURE 6.15 (a) Small signal model including parasitic capacitances. (b) Equivalent circuit using Miller theorem.

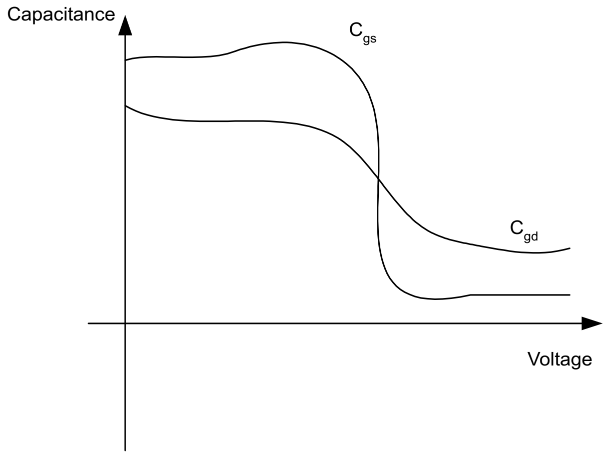


FIGURE 6.16 Variation of C_{gd} and C_{gs} as a function of v_{DS}.

the magnetic components. In order to reduce the switching losses, power MOSFET are maintained in either the on-state (conduction state) or the off-state (forward-blocking) state.

It is important we understand internal device behavior, which leads to an understanind of the parameters that govern the device transition from the on-state and off-states. To investigate the on- and off-switching characteristics, we consider the simple power electronic circuit shown in Fig. 6.17a under inductive load. The flyback diode D is used to pick up the load current when the switch is off. To simplify the analysis we will assume the load inductance is a large enough L_0 that the current through it is constant as shown in Fig. 6.17b.

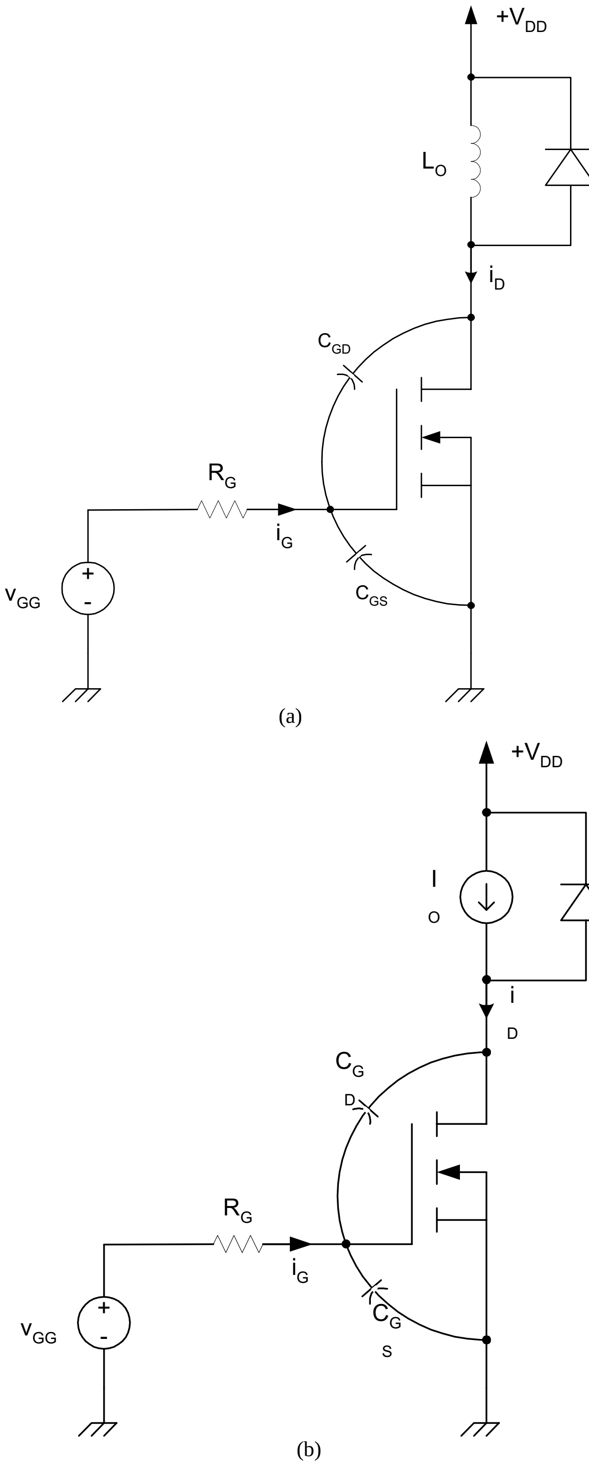
6.6.2 Turn-On Characteristics

Let us assume initially that the device is off and that the load current I_0, flows through D as shown in Fig. 6.18a, $v_{GG} = 0$. The voltage $v_{DS} = V_{DD}$ and $i_G = i_D$. At $t = t_0$, the voltage v_{GG} is applied as shown in Fig. 6.19a. The voltage across C_{GS} starts charging through R_G. The gate-source voltage, v_{GS} controls the flow of the drain-to-source current i_D. Let us assume that for $t_0 \leq t < t_1$, $v_{GS} < V_{Th}$, that is, the MOSFET remains in the cut-off region with $i_D = 0$, regardless of v_{DS}. The time interval $(t_2 1, t_0)$ represents the delay turn-on time needed to change C_{GS} from zero to V_{Th}. The expression for the time interval $\Delta t_{10} = t_1 - t_0$ can be obtained as shown next.

The gate current is given by

$$\begin{aligned} i_G &= \frac{v_{GG} - v_{GS}}{R_G} \\ &= i_{c_{GS}} + i_{c_{GD}} \\ &= C_{GS}\frac{dv_{GS}}{dt} - C_{GD}\frac{d(v_G - v_D)}{dt} \end{aligned} \tag{6.13}$$

where v_G and v_D are gate-to-ground and drain-to-ground voltages, respectively. As we have $v_G = v_{GS}$, $v_D = +V_{DD}$,



(a)

(b)

FIGURE 6.17 (a) Simplified equivalent circuit used to study turn-on and turn-off characteristics of the MOSFET; and (b) simplified equivalent circuit.

then i_G is given by

$$i_G = C_{GS}\frac{dv_{GS}}{dt} + C_{GD}\frac{dv_{GS}}{dt} = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt} \tag{6.14}$$

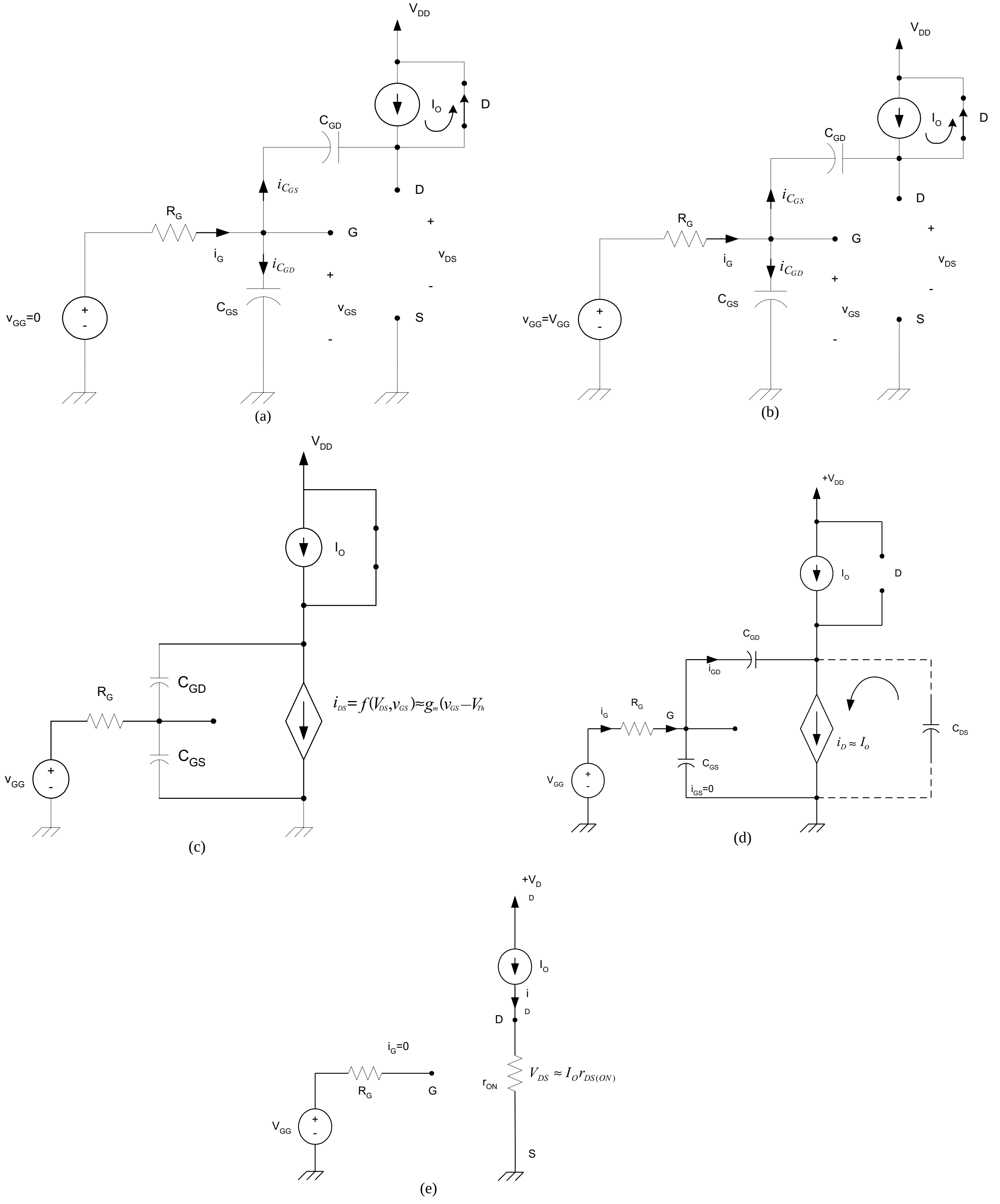

V_DD
C_GD
I_O
D
i_CGS
D
R_G
G
+
v_DS
-
i_G
i_CGD
+
C_GS
v_GS
S
v_GG=0
+
-
-
(a)
V_DD
C_GD
I_O
D
i_CGS
D
R_G
G
+
v_DS
-
i_G
i_CGD
+
C_GS
v_GS
S
v_GG=V_GG
+
-
-
(b)
V_DD
I_O
R_G
C_GD
C_GS
i_DS=f(V_DS,v_GS)≈g_m(v_GS−V_Th
v_GG
+
-
(c)
+V_DD
I_O
D
C_GD
i_GD
R_G
i_G
G
i_D ≈ I_o
C_DS
C_GS
V_GG
+
-
i_GS=0
(d)
+V_D
D
I_O
i
D
D
i_G=0
R_G
G
r_ON
V_DS ≈ I_O r_DS(ON)
V_GG
+
-
S
(e)

FIGURE 6.18 Equivalent modes: (a) MOSFET is in the off-state for $t < t_o$, $v_{GG} = 0$, $v_{DS} = V_{DD}$, $i_G = 0$, $i_D = 0$; (b) MOSFET is in the off-state with $v_{GS} < V_{Th}$ for $t_1 > t > t_0$; (c) $v_{GS} > V_{Th}$, $i_D < I_0$ for $t_1 < t < t_2$; (d) $v_{GS} > V_{Th}$, $i_D = I_0$ for $t_2 \le t < t_3$; and (e) $v_{GS} > V_{Th}$, $i_0 = I_0$, $t > t_3$ the device is fully on.

From Eqs. (13) and (14), we obtain,

$$\therefore \frac{V_{GG} - v_{GS}}{R_G} = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt} \tag{6.15}$$

Solving Eq. (6.15) for $v_{GS}(t)$ for $t > t_0$ with $v_{GS}(t_0) = 0$, we obtain,

$$v_{GS}(t) = V_{GG}(1 - e^{(t-t_0)/\tau}) \tag{6.16}$$

where

$$\tau = R_G(C_{GS} + C_{GD})$$

The gate current i_G is given by

$$\begin{aligned} i_G &= \frac{v_{GG} - v_{GS}}{R_G} \\ i_G &= \frac{V_{GG}}{R_G} e^{-(t-t_0)/\tau} \end{aligned} \tag{6.17}$$

As long as $v_{GS} < V_{Th}$, i_D remains zero. At $t - t_1$, v_{GS} reaches V_{Th}, causing the MOSFET to start conducting. Waveforms for i_G and v_{GS} are shown in Fig. 6.19. The time interval $(t_1 - t_0)$ is given by

$$\Delta t_{10} = t_1 - t_0 = -\tau \ln\left(1 - \frac{V_{Th}}{V_{GG}}\right)$$

Δt_{10} represents the first delay interval in the turn-on process.

For $t > t_1$ with $v_{GS} > V_{Th}$, the device starts conducting and its drain current is given as a function of v_{GS} and V_{Th}. In fact, i_D starts flowing exponentially from zero as shown in Fig. 6.19d. Assume the input transfer characteristics for the MOSFET are limited as shown in Fig. 6.20 with the slope of g_m given by

$$g_m = \frac{\dfrac{\partial i_D}{\partial v_{GS}}}{I_D} = \frac{2\sqrt{i_{DSS} I_d}}{V_{Th}} \tag{6.18}$$

The drain current can be approximated as follows:

$$i_D(t) = g_m(v_{GS} - V_{Th}) \tag{6.19}$$

As long as $i_D(t) < I_0$, D remains on and $v_{DS} = V_{DD}$ are as shown in Fig. 6.18c.

The equation for $v_{GS}(t)$ remains the same as in Eq. (6.16), hence, Eq. (6.19) results in $i_D(t)$ given by

$$i_D(t) = g_m(V_{GG} - V_{Th}) - g_m V_{GG} e^{-(t-t_1)/\tau} \tag{6.20}$$

The gate current continues to decrease exponentially as shown in Fig. 6.19. At $t = t_2$, i_D reaches its maximum value of I_0, turning D off. The time interval $\Delta t_{21} = (t_2 - t_1)$ is obtained from Eq. (20) by setting $i_D(t_2) = I_0$.

$$\Delta t_{21} = \tau Ln \frac{g_m V_{GG}}{gm(V_{GG} - V_{Th}) - I_0} \tag{6.21}$$

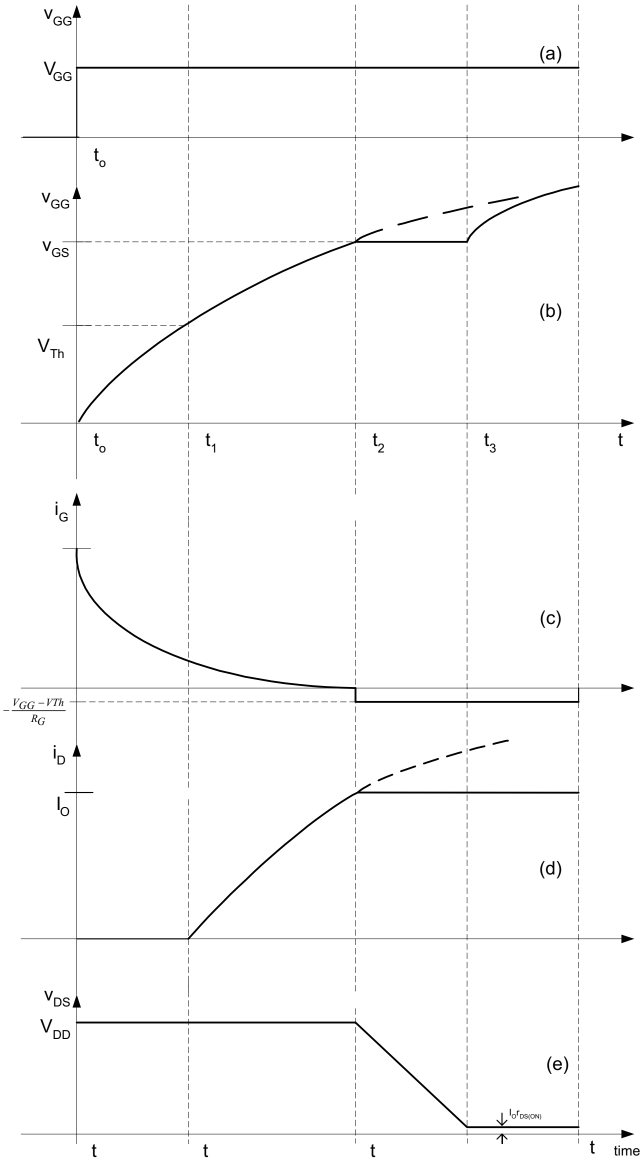


FIGURE 6.19 Turn-on waveform switching.

For $t > t_2$ the diode turns off and $i_D \approx I_0$ is as shown in Fig. 6.18d. As the drain-current is nearly a constant, then the gate-source voltage is also constant according to the input transfer characteristic of the MOSFET, that is,

$$i_D = g_m(v_{GS} - V_{Th}) \approx I_0 \tag{6.22}$$

Hence,

$$v_{GS}(t) = \frac{I_0}{g_m} + V_{Th} \tag{6.23}$$

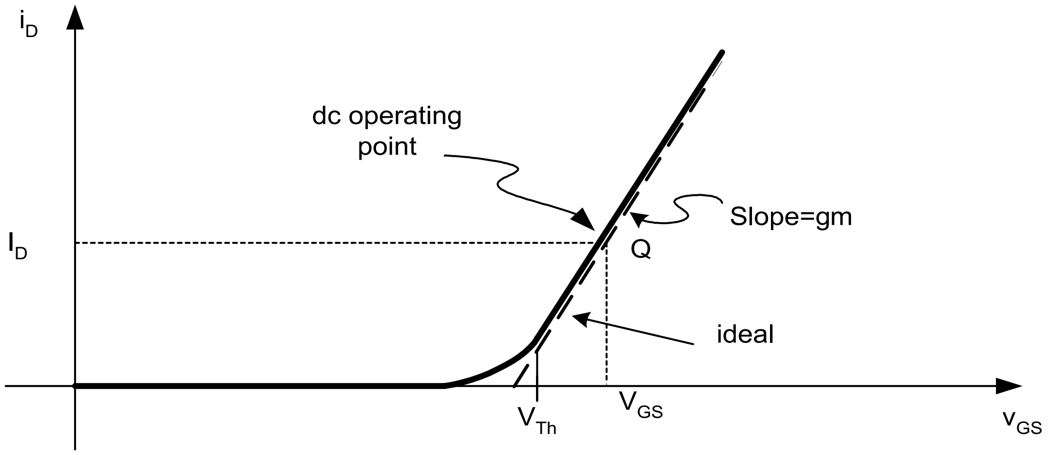


FIGURE 6.20 Input transfer characteristics.

At $t = t_2$, $i_G(t)$ is given by

$$i_G(t_2) = \frac{V_{GG} - v_{GS}(t_2)}{V_{Th}} = \frac{V_{GG} - \frac{I_0}{g_m} - V_{Th}}{V_{Th}} \tag{6.24}$$

As the time constant τ is very small, it is safe to assume that $v_{GS}(t_2)$ reaches its maximum, that is,

$$v_{GS}(t_2) \approx V_{GG}$$

and

$$i_G(t_2) \approx 0$$

For $t_2 \leq t < t_3$, the diode turns off the load current I_0 and (drain current i_D) starts discharging the drain-to-source capacitance.

As v_{GS} is constant, the entire gate current flows through C_{GD}, which results in the following relation,

$$\begin{aligned} i_G(t) &= i_{C_{GD}} \\ &= C_{GD} \frac{d(v_G - v_D)}{dt} \end{aligned}$$

With v_G constant and $v_s = 0$, we have

$$\begin{aligned} i_G(t) &= -C_{GD} \frac{dv_{DS}}{dt} \\ &= -\frac{V_{GG} - V_{Th}}{R_G} \end{aligned}$$

Solving for $v_{DS}(t)$ for $t > t_2$, with $v_{DS}(t_2) = V_{DD}$, we obtain

$$v_{DS}(t) = -\frac{V_{GG} - V_{Th}}{R_G C_{GD}}(t - t_2) + V_{DD} \qquad \text{for } t > t_2 \tag{6.25}$$

This is a linear discharge of C_{GD} as shown in Fig. 6.19e.

The time interval $\Delta t_{32} = (t_3 - t_2)$ is determined by assuming that at $t = t_3$, the drain-to-source voltage reaches its minimum value determined by its on-resistance, $v_{DS(ON)}$ that is, $v_{DS(ON)}$ is given by

$$v_{DS(ON)} \approx I_0 r_{DS(ON)} = \text{constant}$$

For $t > t_3$, the gate current continues to charge C_{GD} and as v_{DS} is constant, v_{GS} starts charging at the same rate as in interval $t_0 \leq t < t_1$, that is,

$$v_{GS}(t) = V_{GG}(1 - e^{-(t-t_3)/\tau})$$

The gate voltage continues to increase exponentially until $t = t_3$, when it reaches V_{GG}, at which $i_G = 0$ and the device fully turns on as shown in Fig. 6.18e.

We have equivalent circuit model when the MOSFET is completely turned on for $t > t_1$. At this time, capacitors C_{GS} and C_{GD} are charged with V_{GG} and $(I_0 r_{DS(ON)} - V_{GG})$, respectively.

The time interval $\Delta t_{32} = (t_3 - t_2)$ is obtained by evaluating v_{DS} at $t = t_3$ as follows:

$$\begin{aligned} v_{DS}(t_3) &= -\frac{V_{GG} - V_{Th}}{R_G C_{GD}}(t_3 - t_2) + V_{DD} \\ &= I_O r_{DS(ON)} \end{aligned} \tag{6.26}$$

Hence, $\Delta t_{32} = (t_3 - t_2)$ is given by

$$\Delta t_{32} = t_3 - t_2 = R_G C_{GD} \frac{(V_{DD} - I_D r_{DS(ON)})}{V_{GG} - V_{Th}} \tag{6.27}$$

The total delay in turning on the MOSFET is given by

$$t_{ON} = \Delta t_{10} + \Delta t_{21} + \Delta t_{32} \tag{6.28}$$

Notice that the MOSFET sustains high voltage and current simultaneously during intervals Δt_{21} and Δt_{32}. This results in large power dissipation during turn-on, which contributes to overall switching losses. The smaller the R_G, the smaller Δt_{21} and Δt_{32} become.

6.6.3 Turn-off Characteristics

To study the turn-off characteristic of the MOSFET, we will consider Fig. 6.17b again by assuming the MOSFET is on and in steady state at $t > t_0$ with the equivalent circuit of Fig. 6.18(e). Therefore, at $t = t_0$ we have the following initial conditions:

$$
\begin{aligned}
v_{DS}(t_0) &= I_D r_{DS(ON)} \\
v_{GS}(t_0) &= V_{GG} \\
t_{DS}(t_0) &= I_0 \\
i_G(t_0) &= 0 \\
v_{C_{GS}}(t_0) &= V_{GG} \\
v_{C_{GD}}(t_0) &= V_{GG} - I_0 r_{DS(ON)}
\end{aligned}
\tag{6.29}
$$

At $t = t_0$, the gate voltage $v_{GG}(t)$ is reduced to zero as shown in Fig. 6.21a. The equivalent circuit at $t > t_0$ is shown in Fig. 6.22a.

We assume that the drain-to-source remains constant while C_{GS} and C_{GD} are discharging through R_G as governed by the following relations,

$$
\begin{aligned}
i_G &= \frac{-v_G}{R_G} = i_{C_{GS}} + i_{C_{GD}} \\
&= C_{GS}\frac{dv_{GS}}{dt} + C_{GD}\frac{dv_{GD}}{dt}
\end{aligned}
$$

As v_{DS} is assumed constant, then i_G becomes

$$
\begin{aligned}
i_G &= \frac{-v_{GS}}{R_G} \\
&= (C_{GS} + C_{GD})\frac{dv_{GS}}{dt}
\end{aligned}
\tag{6.30}
$$

Hence, evaluating for v_{GS} for $t \geq t_0$, we obtain

$$
v_{GS}(t) = v_{GS}(t_0)e^{-(t-t_0)/\tau}
\tag{6.31}
$$

Where

$$
\begin{aligned}
v_{GS}(t_0) &= v_{GG} \\
\tau &= (C_{GS} + C_{GD})R_G
\end{aligned}
$$

As v_{GS} continues to decrease exponentially, drawing current from C_{GD}, it will reach a constant value at which drain current is fixed, that is, $I_D = I_0$. From the input transfer characteristics, the value of v_{GS}, at which $I_D = I_0$, is given by

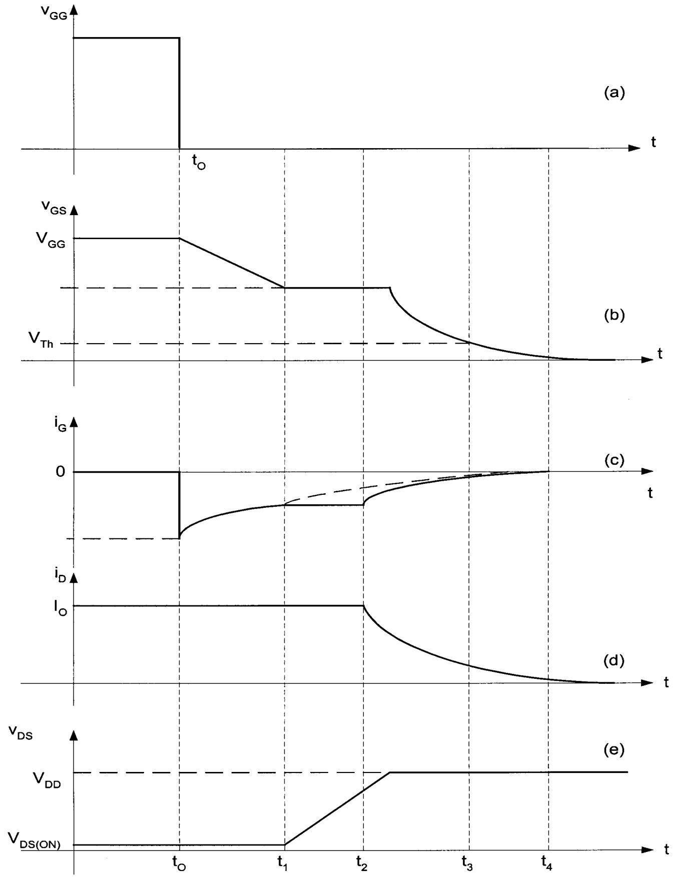


FIGURE 6.21 Turn-on switching waveforms.

$$
v_{GS} = \frac{I_0}{g_m} + V_{Th}
\tag{6.32}
$$

The time interval $\Delta t_{10} = t_1 - t_0$ can be obtained easily by setting Eq. (6.31) to Eq. (6.32) at $t = t_1$. The gate current during the $t_2 \leq t < t_1$ is given by

$$
i_G = -\frac{V_{GG}}{R_G} - e^{-(t-t_0)/\tau}
\tag{6.33}
$$

Because for $t_2 - t_1$ the gate-to-source voltage is constant and equals $v_{GS}(t_1 = I_0/g_m + V_{Th}$ as shown in Fig. 6.21b, then the entire gate current is being drawn from C_{GD} and

$$
\begin{aligned}
i_G &= C_{GD}\frac{dv_{GD}}{dt} = C_{GD}\frac{d(v_{GS} - v_{DS})}{dt} = -C_{GD}\frac{dv_{DS}}{dt} \\
&= \frac{v_{GS}(t_1)}{R_G} = \frac{1}{R_G}\left(\frac{I_0}{g_m} + V_{Th}\right)
\end{aligned}
$$

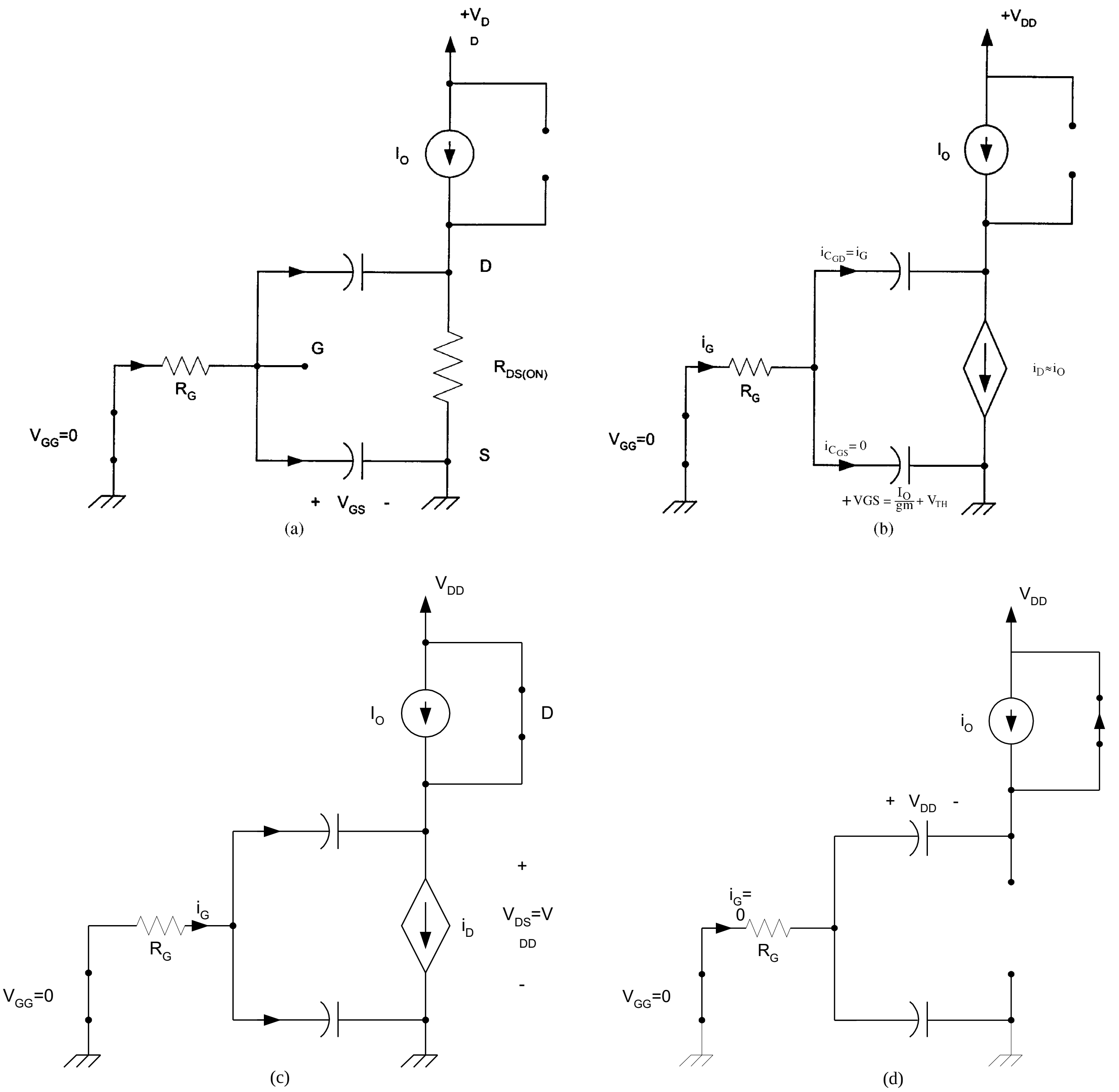

+V_D
D
I_O
D
G
R_DS(ON)
R_G
V_GG=0
S
+ V_GS -
(a)
+V_DD
I_O
i_CGD=i_G
i_G
R_G
i_D≈i_O
V_GG=0
i_CGS=0
+VGS = IO/gm + VTH
(b)
V_DD
I_O
D
i_G
R_G
i_D
+
V_DS=V_DD
-
V_GG=0
(c)
V_DD
i_O
+ V_DD -
i_G=0
R_G
V_GG=0
(d)

FIGURE 6.22 Equivalent circuits: (a) $t_0 \le t < t_1$; (b) $t_1 \le t < t_2$; (c) $t_2 \le t < t_3$; and (d) $t_3 \le t < t_4$.

Assuming i_G constant at its initial value at $t = t_1$, that is,

$$i_G = \frac{v_{\mathrm{GS}}(t_1)}{R_G} = \frac{1}{R_G}\left(\frac{I_0}{g_m} + V_{\mathrm{Th}}\right)$$

Integrating both sides of the preceding equation from t_1 to t with $v_{\mathrm{DS}}(t_1) = -v_{\mathrm{DS(ON)}}$, we obtain

$$v_{\mathrm{DS}}(t) = v_{\mathrm{DS(ON)}} + \frac{1}{R_G C_{\mathrm{GD}}}\left(\frac{I_0}{g_m} + V_{\mathrm{Th}}\right)(t - t_1) \tag{6.34}$$

hence v_{DS} charges linearly until it reaches V_{DD}.

At $t = t_2$, the drain-to-source voltage becomes equal to V_{DD}, forcing D to turn-on as shown in Fig. 6.22c.

The drain-to-source current is obtained from the transfer characteristics and given by

$$i_{\mathrm{DS}}(t) = g_m(v_{\mathrm{GS}} - V_{\mathrm{Th}})$$

Where $v_{\mathrm{GS}}(t)$ is obtained from the following equation:

$$i_G = -\frac{v_{\mathrm{GS}}}{R_G} = (C_{\mathrm{GS}} + C_{\mathrm{GD}})\frac{dv_{\mathrm{GS}}}{dt} \tag{6.35}$$

Integrating both sides from t_2 to t with $v_{GS}(t_2) = I_0/g_m + V_{Th}$, we obtain the following expression for $v_{GS}(t)$,

$$v_{GS}(t) = \left(\frac{I_0}{g_m} + V_{Th}\right) e^{-(t-t_2)/\tau} \tag{6.36}$$

Hence the gate current and drain-to-source current are given by,

$$i_G(t) = \frac{-1}{R_G}\left(\frac{I_0}{g_m} + V_{Th}\right) e^{-(t-t_2)/\tau} \tag{6.37}$$

$$i_{DS}(t) = g_m V_{Th}(e^{-(t-t_2)/\tau} - 1) + I_0 e^{-(t-t_2)/\tau} \tag{6.38}$$

The time interval between $t_2 \le t < t_3$ is obtained by evaluating $v_{GS}(t_3) = V_{Th}$, at which the drain current becomes approximately zero and the MOSFET turn-off. As a result, we have

$$\begin{aligned} v_{GS}(t_3) &= V_{Th} \\ &= \left(\frac{I_0}{g_m} + V_{Th}\right) e^{-(t_3-t_2)/\tau} \end{aligned}$$

Solving for $\Delta t_{32} = t_3 - t_2$, we obtain

$$\Delta t_{32} = t_3 - t_2 = \tau \ln\left(1 + \frac{I_0}{V_{Th} g_m}\right) \tag{6.39}$$

For $t > t_3$, the gate voltage continues to decrease exponentially to zero, at which the gate current becomes zero and C_{GD} charges to $-V_{DD}$. Between t_3 and t_4, I_D discharges to zero as shown in the equivalent circuit Fig. 6.22d.

The total turn-off time for the MOSFET is given by

$$\begin{aligned} t_{off} &= \Delta t_{10} + \Delta t_{21} + \Delta t_{32} + \Delta t_{43} \\ &\approx \Delta t_{21} + \Delta t_{32} \end{aligned} \tag{6.40}$$

The time interval that most affects the power dissipation are Δt_{21} and Δt_{32}. It is clear that in order to reduce the MOSFET t_{on} and t_{off} times, the gate-drain capacitance must be reduced. Readers are encouraged to see the reference by Baliga [1] for detailed discussion on the turn-on and turn-off characteristics of the MOSFET and to explore various fabrication methods.

6.6.4 Safe Operation Area

The safe operation area (SOA) of a device provides the current and voltage limits the device must be able to handle to avoid destructive failure. Typical SOA for a MOSFET device is shown in Fig. 6.23. The maximum current limit while the device is on is determined by the maximum power dissipation,

$$P_{diss,ON} = I_{DS(ON)} R_{DS(ON)} \tag{6.41}$$

As the drain-source voltage starts increasing, the device starts leaving the on-state and enters the saturation (linear) region. During the transition time the device exhibits large voltage and current simultaneously. At higher drain-source voltage values that approach the avalanche breakdown it is observed that power MOSFET suffers from a second breakdown phenomenon. The second breakdown occurs when the MOSFET is in the blocking state (off) and a further increase in v_{DS} will cause a sudden drop in the blocking voltage. The source of this phenomenon in MOSFET is caused by the presence of a parasitic n-type bipolar transistor as shown in Fig. 6.24.

The inherent presence of the body diode in the MOSFET structure makes the device attractive for applications in which bidirectional current flow is needed in the power switches.

Today's commercial MOSFET devices have excellent high operating temperatures. The effect of temperature is more prominent on the on-state resistance as shown in Fig. 6.25.

As the on-state resistance increases, the conduction losses also increase. This large $v_{DS(OW)}$ limits the use of the MOSFET

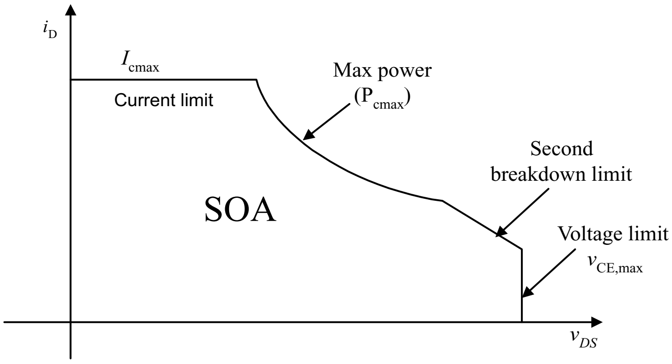


FIGURE 6.23 Safe operation area (SOA) for MOSFET.

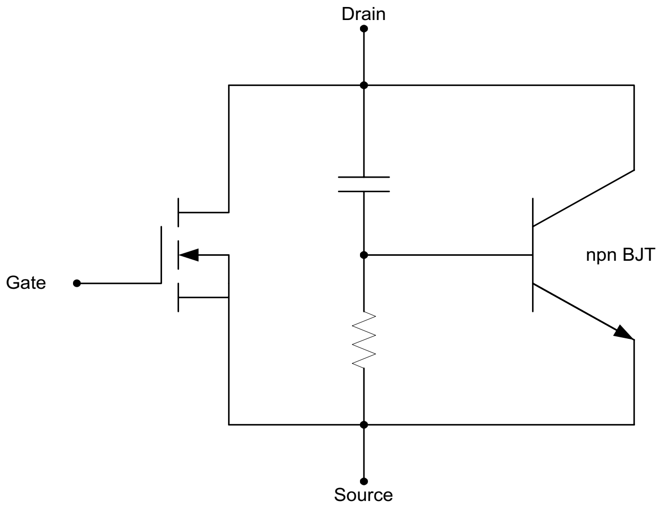


FIGURE 6.24 MOSFET equivalent circuit including the parasitic BJT.

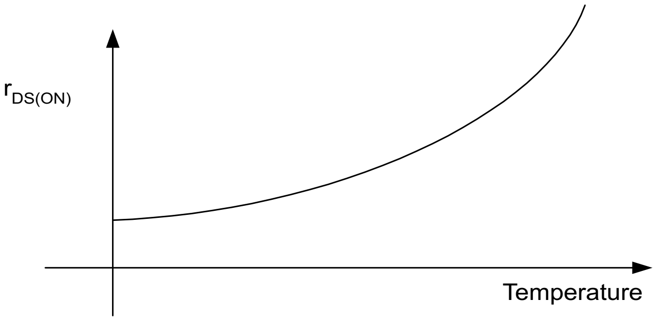


FIGURE 6.25 The on-state resistance as a fraction of temperature.

in high-voltage applications. The use of silicon carbide instead of silicon has reduced $v_{DS(OW)}$ many fold.

As the device technology keeps improving, especially in terms of improved switch speeds and increased power handling capabilities, it is expected that the MOSFET will continue to replace BJTs in all types of power electronics systems.

6.7 MOSFET PSPICE Model

The PSPICE simulation package has been used widely by electrical engineers as an essential software tool for circuit design. With the increasing number of devices available in the market place, PSPICE allows for accurate extraction and understanding of various device parameters and their varied effects on the overall design prior to their fabrication. Today's PSPICE library is rich with numerous commercial MOSFET models. This section will give a brief overview of how the MOSFET model is implemented in PSPICE. A brief overview of the PSPICE modeling of the MOSFET device will be given here.

6.7.1 Static Model

There are four different types of MOSFET models that are also known as *levels*. The simplest MOSFET model is called the LEVEL1 model and is shown in Fig. 6.26. [9, 10].

The LEVEL2 model uses the same parameters as LEVEL1, but it provides a better model for Ids by computing the model coefficients KP, VTO, LAMBDA, PHI, and GAMMA directly from the geometrical, physical and technological parameters [10]. LEVEL3 is used to model the short-channel devices and LEVEL4 represents the Berkeley short-channel IGFET model (BSIM-model).

For the triode regions, $v_{GS} > V_{Th}$, $v_{DS} < v_{GS}$, and $v_{DS} < v_{GS} - V_{Th}$, the drain current is given by

$$i_D = \frac{K_P}{2} \frac{W}{L - 2X_{j_l}} \left(v_{GS} - v_{Th} - \frac{v_{DS}}{2} \right) v_{DS}(1 + \lambda v_{DS}) \qquad (6.41)$$

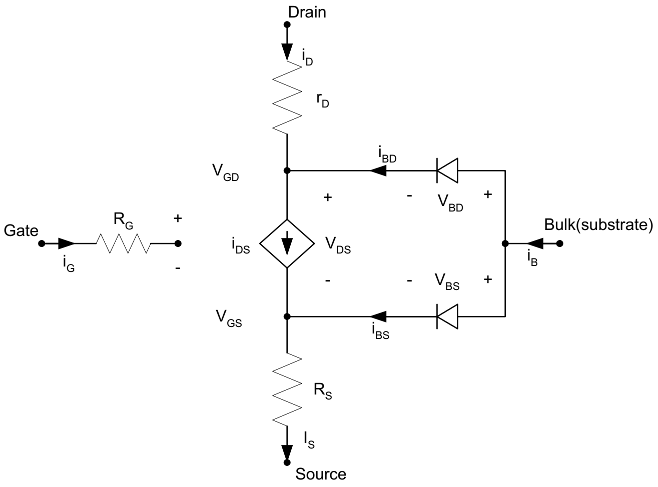


FIGURE 6.26 Spice L1 MOSFET static model.

In the saturation (linear) region, where $v_{GS} > V_{Th}$ and $v_{DS} > v_{GS} - V_{Th}$, the drain current is given by

$$I_D = \frac{K_P}{2} \frac{W}{L - 2X_{j_l}} (V_{GS} - V_{Th})^2 (1 + \lambda V_{DS}) \qquad (6.42)$$

Where K_P is the transconductance and X_{jl} is the lateral diffusion.

The threshold voltage V_{Th} is given by

$$V_{Th} = V_{T0} + \partial \left(\sqrt{2\phi_p - V_{BS}} - \sqrt{2\phi_p} \right) \qquad (6.43)$$

where, V_{T0} is the zero-bias threshold voltage; δ is the body-effect parameter; and ϕ_p is the surface inversion potential.

Typically, $X_{ij} \ll L$ and $\lambda \approx 0$.

The term $(1 + \lambda V_{DS})$ is included in the model as an empirical connection to model the effect of the output conductance when the MOSFET is operating in the triode region. Lambda is known as the channel-length modulation parameter.

When the bulk and source terminals are connected together, that is, $V_{BS} = 0$, the device threshold voltage equals the zero-bias threshold voltage,

$$V_{Tn} = V_{T0}$$

where V_{T0} is positive for the *n*-channel enhancement mode devices and negative for the depletion mode *n*-channel devices.

The parameters K_P, V_{T0}, δ, ϕ are electrical parameters that can be either specified directly in the MODEL statement under the PSPICE keywords KP, VTO, GAMMA and PHI, respectively, as shown in Table 6.1. These parameters can also be calculated when the geometrical and physical parameters. The two-substrate currents that flow from the bulk to the source

I_{BS} and from the bulk to the drain I_{BD} are simply diode currents and are given by

$$I_{BS} = I_{SS}\left(e^{-\frac{V_{BS}}{V_T}} - 1\right) \tag{6.44}$$

$$I_{BD} = I_{DS}\left(e^{-\frac{V_{BD}}{V_T}} - 1\right) \tag{6.45}$$

Where I_{SS} and I_{DS} are the substrate source and substrate drain saturation currents. These currents are considered equal and given as I_S in the MODEL statement with a default value of 10^{-14} A. Where the equation symbols and their corresponding PSpice parameter names are shown in Table 6.1.

In PSpice, a MOSFET device is described by two statements, with first statement starting with the letter M and the second statement starting with .Model, which defines the model used in the first statement. The following syntax is used:

```
M<device_name> <Drain_node_number>
Gate_node_number>
<Source_node_number> <Substrate_node
number> <Model_name> *
[<param_1>=<value_1>
<param_2>=<value_>....]  .MODEL
<Model_name> <type_name>
[ (<param_1>=<value_1>
<param_2>=<value_2> .....]
```

Where the starting letter "M" in `M<devic_name>` statement indicates that the device is a MOSFET and `<device_name>` is a user specified label for the given device, the `<Model_name>` is one of the hundreds of device models specified in the PSpice library; and `<model_name>` or the same name specified in the device name statement `<type_name>`, is either NMOS of PMOS, depending on whether the device is *n*- or *p*-channel MOS, respectively. An optional list of parameter types and their values follows. Length L and width W and other parameters can be specified in the `M<device_name>`, in the .MODEL or .OPTION statements. A user may select not to include any value, and PSpice will use the specified default values in the model. For normal operation (physical construction of the MOS devices), the source and bulk substrate nodes must be connected together. In all the PSpice library files, default parameter values for L, W, AS, AD, PS, PD, NRD, and NDS are included, and a user then should not specify such values in the device "M" statement or in the OPTION statement.

The power MOSFET device PSpice models include relatively complete static and dynamic device characteristics given in the manufacturing data sheet. In general, the following effects are specified in a given PSpice model: dc transfer curves, on-resistance, switching delays, gate dive characteristics, and reverse-mode "body-diode" operation. The device characteristics that are not included in the model are noise, latch-ups, maximum voltage, and power ratings. Please see OrCAD Library Files.

Example 6.3. Let us consider an example that uses IRF MOSFET and connected as shown in Fig. 6.27.

It was decided that the device should have a blocking voltage (V_{DSS}) of 600 V and drain current i_d of 3.6 A. The device selected is IRF CC30 with case TO220. This device is listed in the PSpice library under model number IRFBC30 as follows:

```
*Library of Power MOSFET Models *Copyright
OrCAD, Inc. 1998 All Rights Reserved. *
*$Revision: 1.24 $ *$Author: Rperez $
*$Date: 19 October 1998 10:22:26 $ * .
Model IRFBC30 NMOS NMOS
```

The PSpice code for the MOS device labeled S1 used in Fig. 6.27 is given by

```
MS1 3 5 0 0 IRFBC30 .MODEL IRFBC30
.Model IRFBC30 NMOS(Level=3 Gamma=0
Delta=0 Eta=0 Theta=0 Kappa=0.2
Vmax=0 Xj=0 + Tox=100n Uo=600 Phi=.6
Rs=5.002m Kp=20.43u W=.35 L=2u
Vto=3.625 + Rd=1.851 Rds=2.667MEG
Cbd=790.1p Pb=.8 Mj=.5 Fc=.5
Cgso=1.64n + Cgdo=123.9p Rg=1.052
Is=720.2p N=1 Tt=685) * Int'l Rectifier
pid=IRFCC30 case=TO220
```

6.7.2 Large Signal Model

The equivalent circuit of Fig. 6.28 includes five device parasitic capacitances. The capacitors C_{GB}, C_{GS}, and C_{GD}, represent the charge-storage effect between the gate terminal and the bulk, source and drain terminals, respectively. These are nonlinear two-terminal capacitors expressed as functions of W, L Cox, V_{GS}, V_{T0}, V_{DS}, and C_{GB0}, C_{GSO}, C_{GDO}. Capacitors C_{GB0}, C_{GS0}, and C_{GD0} outside the channel region, are known as overlap capacitances that exist between the gate electrode and the other three terminals, respectively. Table 6.2 shows the list of MOSFET capacitance parameters and their default values. Notice that the PSpice overlap capacitor keywords (C_{GB0}, C_{GSO}, C_{GDO}) are proportional either to the MOSFET width or length of the channel as follows:

$$\begin{aligned} C_{GBO} &= C_{GBO}/\mathrm{L} \\ C_{GSO} &= C_{GSO}/\mathrm{W} \\ C_{GDO} &= C_{GDO}/W \end{aligned} \tag{6.46}$$

In the triode region, where $v_{GS} > v_{DS} - V_{Th}$, the terminal capacitors are given by,

$$\begin{aligned} C_{GS} &= L_W C_{oX}\left[1 - \left(\frac{v_{GS} - v_{DS} - V_{Th}}{2(v_{GS} - V_{Th}) - V_{DS}}\right)^2\right] + \ C_{GS0}. \\ C_{GD} &= L_W C_{oX}\left[1 - \left(\frac{v_{GS} - V_{Th}}{2(v_{GS} - V_{Th}(-v_{DS}}\right)^2\right] + \ C_{GDO}. \\ C_{GB} &= C_{GB0}L \end{aligned} \tag{6.47}$$

TABLE 6.1 PSPICE MOSFET parameters

(a) Device dc and parasitic parameters

Symbol	Name	Description	Default	Units
Level	LEVEL	Model type (1, 2, 3, or 4)	1	
V_{TO}	VTO	Zero-bias threshold voltage	0	V
λ	LAMDA	Channel-length modulation[1,2a]	0	v-1
γ	GAMMA	Body-effect (bulk) threshold parameter	0	$v^{-1/2}$
Φ_ρ	PHI	Surface inversion potential	0.6	V
η	ETA	Static feedback[3]	0	
κ	KAPPA	Saturation field factor[3]	0.2	
μ_0	UO	Surface mobility	600	cm^2/V-s
Is	IS	Bulk saturation current	10^{-14}	A
Js	JS	Bulk saturation current/area	0	A/m^2
J_{SSW}	JSSW	Bulk saturation current/length	0	A/m
N	N	Bulk emission coefficient n	1	
P_B	PB	Bulk junction voltage	0.8	V
P_{BSW}	PBSW	Bulk sidewall diffusion voltage	PB	V
R_D	RD	Drain resistance	0	Ω
R_S	RS	Source resistance	0	Ω
R_G	RG	Gate resistance	0	Ω
R_B	RB	Bulk resistance	0	Ω
R_{ds}	RDS	Drain-source shunt resistance	α	Ω
R_{sh}	RSH	Drain and source diffusion sheet resistance	0	Ω/m^2

(b) Device process and dimensional parameters

Symbol	Name	Description	Default	Units
N_{sub}	NSUB	Substrate doping density	None	cm^{-3}
W	W	Channel width	DEFW	m
L	L	Channel length	DEFL	m
W_D	WD	Lateral diffusion width	0	m
X_{jl}	LD	Lateral diffusion length	0	m
Kp	KP	Transconductance coefficient	20×10^{-6}	A/v^2
t_{0X}	TOX	Oxide thickness	10^{-7}	m
N_{SS}	NSS	Surface-state density	None	cm^{-2}
N_{FS}	NFS	Fast surface-state density	0	cm^{-2}
N_A	NSUB	Substrate doping	0	cm^{-3}
T_{PG}	TPG	Gate material +1 Opposite of substrate −1 Same as substrate 0 Aluminum	1	
X_j	XJ	Metallurgical junction depth[2,3]	0	m
μ_0	UO	Surface mobility	600	cm^2/V-s
U_c	UCRIT	Mobility degradation critical field[2]	10^4	V/cm
U_e	UEXP	Mobility degradation exponent[2]	0	
U_t	VMAX	Maximum drift velocity of carriers[2]	0	m/s
N_{eff}	NEFF	Channel charge coefficient[2]	1	
δ	DELTA	Width effect on threshold 2,3	0	
θ	THETA	Mobility modulation[3]	0	

(c) Device capacitance parameters

Symbol	Name	Description	Default	Units
C_{BD}	CBD	Bulk-drain zero-bias capacitance	0	F
C_{BS}	CBS	Bulk-source zero-bias capacitance	0	F
C_j	CJ	Bulk zero-bias bottom capacitance	0	F/m^2
C_{jsw}	CJSW	Bulk zero-bias perimeter capacitance/length	0	F/m
M_j	MJ	Bulk bottom grading coefficient	0.5	
M_{jsw}	MJSW	Bulk sidewall grading coefficient	0.33	
F_C	FC	Bulk forward-bias capacitance coefficient	0.5	
C_{GSO}	CGSO	Gate-source overlap capacitance/channel width	0	F/m
XCGDO	CGDO	Gate-drain overlap capacitance/channel width	0	F/m
C_{GBO}	CGBO	Gate-bulk overlap capacitance/channel length	0	F/m
X_{QC}	XQC	Fraction of channel charge that associates with drain[1,2]	0	
K_F	KF	Flicker noise coefficient	0	
α_F	AF	Flicker noise exponent	0	

[a] All superscript numbers in the Description column indicate that this/these parameter(s) are available in this/these level number(s), otherwise it/they are available in all levels.

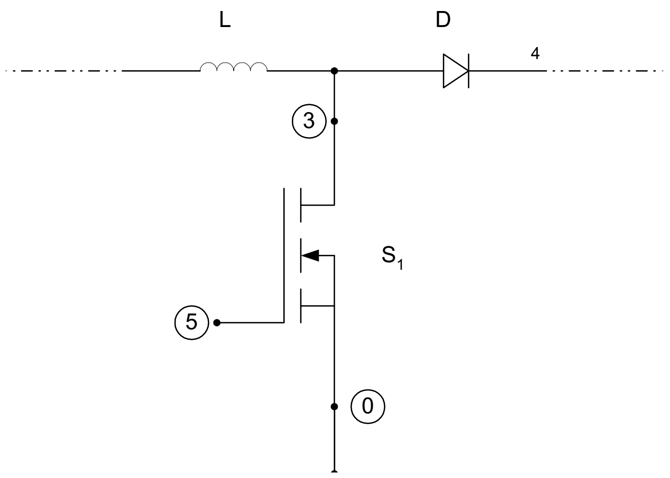


FIGURE 6.27 Example of a power electronic circuit that uses a power MOSFET.

In the saturation (linear) region we have

$$\begin{aligned} C_{GS} &= \tfrac{2}{3} L_W C_{oX} + C_{GSO} \\ C_{GB} &= C_{GB0} L \\ C_{GD} &= C_{GD0} \end{aligned} \tag{6.48}$$

Where C_{oX} is the per-unit-area oxide capacitance given by

$$C_{oX} = \frac{K_{oX} E_0}{T_{oX}}$$

where K_{oX} is the oxide relative dielectric constant, E_0 denotes the free-space dielectric constant as equal to 8.854×10^{-12} F/m; and T_{oX} is the oxide thickness layer as given by data in Table 6.1.

Finally, the diffusion and junction region capacitances between the bulk-to-channel (drain and source) are modeled by C_{BD} and C_{BS} across the two diodes. Because for almost all power MOSFETS, the bulk and source terminals are connected together and at zero potential, diodes D_{BD} and D_{BS} do not have forward bias, thereby resulting in very small conductance values, that is, small diffusion capacitances. The small signal model for MOSFET devices is given in Fig. 6.29.

> **Example** 6.4. Figure 6.30a shows an example of a soft-switching power factor connection circuit that has two MOSFET. Its PSPICE simulation waveforms are shown in Fig. 6.30b.

Table 6.2 shows the PSPICE code for Fig. 6.30a.

6.8 Comparison of Power Devices

As stated earlier, the power electronic range is very wide, from hundreds of milliwatts to hundreds of megawatts and thus it is very difficult to find a single switching device type to cover all power electronic applications. Today's available power devices have tremendous power and frequency rating range, as well as diversity. Their forward current ratings range from a few amperes to a few kiloamperes, their blocking voltage rating

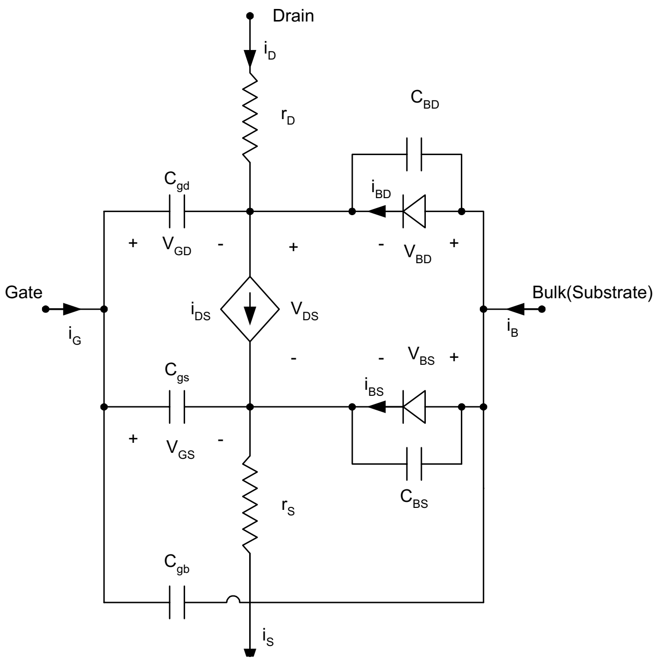


FIGURE 6.28 Large-signal model for the *n*-channel MOSFET.

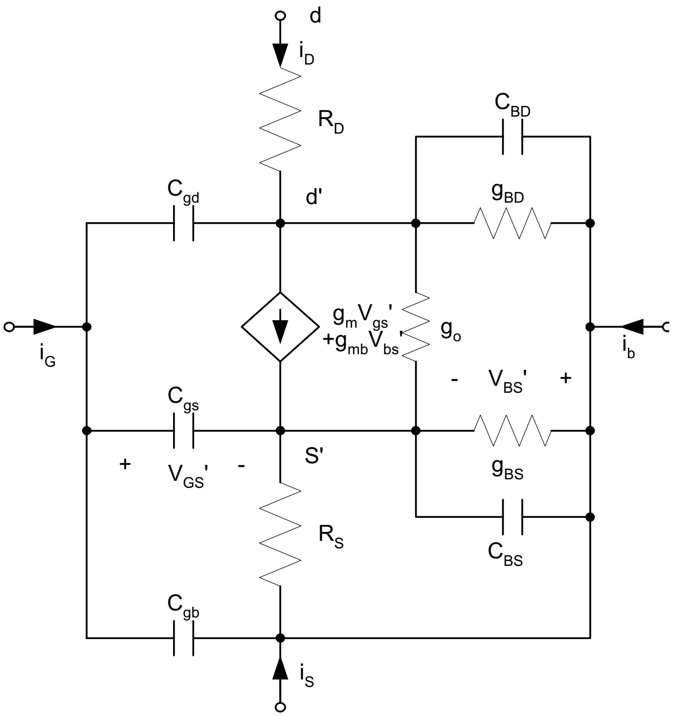


FIGURE 6.29 Small signal equivalent circuit model for MOSFET.

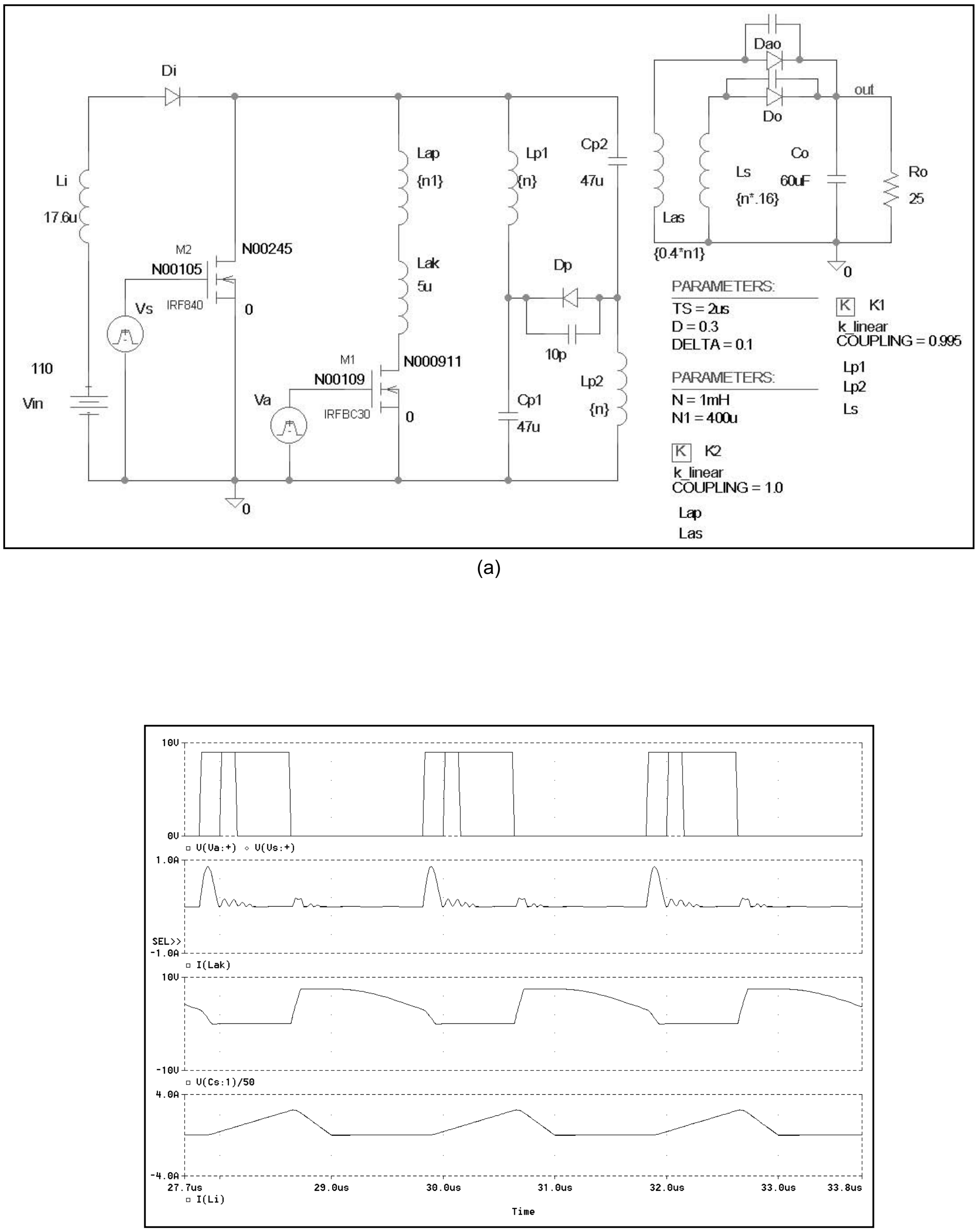
TABLE 6.2 PSPICE MOSFET capacitance parameters and their default values for Figure 6.30a

```
* source ZVT-ZCS
```

```
D_Do        N00111 OUT Dbreak
V_Vs        N00105 9 DC 0 AC 0 PULSE 0.9.0.0.0 {D*Ts} {Ts}
L_Ls        0 N00111 {n*.16}
Kn_K1       L_Lp1 L_Lp2 L_Ls 0.995
C_Co        OUT 0 70uF IC=50
V_Vin       N00103 0 110
L_Li        N00103 N00099 17.6u IC=0
V_Va        N-109 0 DC 0 AC 0 PULSE 0 9 {-Delta*Ts/1.1} 0 0 {2.0*Delta*Ts}
{Ts}
D_Dp        N00121 N00169 Dbreak
C_C7        N00111 OUT 30p
R_Ro        OUT 0 25
C_C8        N00143 OUT 10p
D_Dao       N00143 OUT Dbreak
D_Di        N00099 N00245 Dbreak
L_Lp2       N00121 0 {n} IC=0
C_C9        N00169 N00121 10p
L_Las       N00143 0 {0.4*n1}
Kn_K2       L_Lap L_Las 1.0
L_Lp1       N00245 N00169 {n} IC=0
L_Lap       N00245 N000791 {n1}
C_Cp2       N00245 N00121 47u IC=170
C_Cp1       N00169 0 47u IC=170
L_Lak       N000791 N000911 5u IC=0
M_M1        N000911 N00109 0 0 IRFBC30
M_M2        N00245 N00105 0 0 IRF840
.PARAM D=0.3 DELTA=0.1 N1=400u N=1mH TS=2us
```

```
 **** MOSFET MODEL PARAMETERS

             IRFBC30             IRF840
             NMOS                NMOS
  LEVEL      3                   3
      L      2.000000-06         2.000000-06
      W      .35                 .68
    VTO      3.625               3.879
     KP      20.430000E-06       20.850000E-06
  GAMMA      0                   0
    PHI      .6                  .6
 LAMBDA      0                   0
     RD      1.851               .6703
     RS      5.002000E-03        6.382000E-03
     RG      1.052               .6038
    RDS      2.667000E+06        2.222000E+06
     IS      720.200000E-12      56.030000E-12
     JS      0                   0
     PB      .8                  .8
   PBSW      .8                  .8
    CBD      790.100000E-12      1.415000E-09
     CJ      0                   0
   CJSW      0                   0
     TT      685.000000E-09      710.000000E-09
   CGSO      1.640000E-09        1.625000E-09
   CGDO      123.900000E-12      133.400000E-12
   CGBO      0                   0
    TOX      100.000000E-09      100.000000E-09
     XJ      0                   0
  UCRIT      10.000000E+03       10.000000E+03
  DELTA      0                   0
    ETA      0                   0
 DIOMOD      1                   1
    VFB      0                   0
   LETA      0                   0
   WETA      0                   0
     U0      0                   0
   TEMP      0                   0
    VDD      0                   0
  XPART      0                   0
```


Di
Li
17.6u
110
Vin
Vs
M2
N00105
IRF840
N00245
0
Va
M1
N00109
IRFBC30
N000911
0
Lap
{n1}
Lak
5u
Lp1
{n}
Cp2
47u
Dp
10p
Cp1
47u
Lp2
{n}
Dao
Do
out
Las
{0.4*n1}
Ls
{n*.16}
Co
60uF
Ro
25
0
PARAMETERS:
TS = 2us
D = 0.3
DELTA = 0.1
PARAMETERS:
N = 1mH
N1 = 400u
K K1
k_linear
COUPLING = 0.995
Lp1
Lp2
Ls
K K2
k_linear
COUPLING = 1.0
Lap
Las
10V
0V
U(Va:+) U(Vs:+)
1.0A
SEL>>
-1.0A
I(Lak)
10V
-10V
U(Cs:1)/50
4.0A
-4.0A
27.7us
29.0us
30.0us
31.0us
32.0us
33.0us
33.8us
I(Li)
Time

(a)

(b)

FIGURE 6.30 (a) Example of power electronic circuit; and (b) PSpice simulation waveforms.

ranges from a few volts to a few kilovolts, and the switching frequency ranges from a few hundred hertz to a few mega hertz (see Table 6.3). This table compares the available power semiconductor devices. We only give relative comparison because there is no straightforward technique that can rank these devices. As we compile this table, devices are still being developed very rapidly with higher current, voltage ratings, and switching frequency. Finally, Fig. 6.31 shows a plot of frequency versus power, illustrating the power and frequency ratings of available power devices.

6. uture Trends in Power Devices

It is expected that improvement in power handling capabilities and increasing frequency of operation of power devices will

TABLE 6.3 Comparison of power semiconductor devices

Device type	Year made available	Rated voltage	Rated current	Rated frequency	Rated power	Forward voltage
Thyristor (SCR)	1957	6 kV	3.5 kA	500 Hz	100's MW	1.5–2.5 V
Triac	1958	1 k V	100 A	500 Hz	100's kW	1.5–2 V
GTO	1962	4.5 kV	3 k A	2 kHz	10's MW	3–4 V
BJT (Darlington)	1960 s	1.2 kV	800 A	10 kHz	1 MW	1.5–3 V
MOSFET	1976	500 V	50 A	1 MHz	100 kW	3-4 V
IGBT	1983	1.2 kV	400 A	20 kHz	100's kW	3–4 V
SIT		1.2 kV	300 A	100 kHz	10's kW	10–20 V
SITH	19	1.5 kV	300 A	10 kHz	10's kW	2–4 V
MCT	1988	3 kV	2 kV	20–100 kHz	10's MW	1–2 V

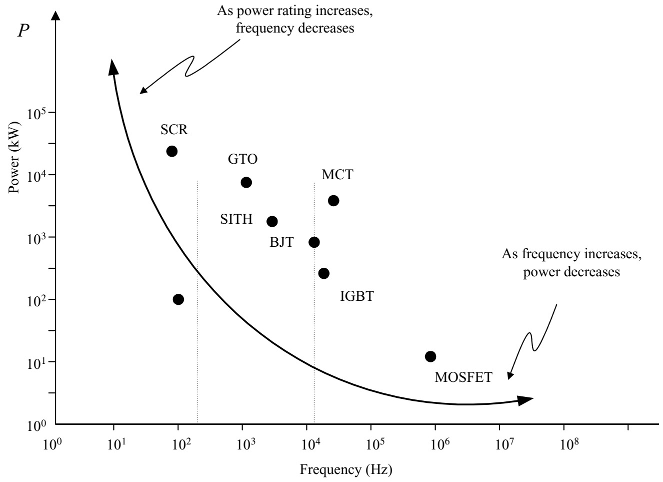


FIGURE 6.31 Power vs frequency for different power devices.

continue to drive the research and development in semiconductor technology. From power MOSFET to power MOS-IGBT and to power MOS-controlled thyristors, power rating has consistently increased by factor of 5 from one type to another. Major research activities will focus on obtaining new device structures based on MOS-BJT technology integration so as to rapidly increase power ratings. It is expected that the power MOS-BJT technology will capture more than 90 of the total power transistor market.

The continuing development of power semiconductor technology has resulted in power systems with driver circuit, logic and control, device protection and switching devices being designed and fabricated on a single chip. Such power IC modules are called "smart power" devices. For example, some of today's power supplies are available as ICs for use in low-power applications. No doubt the development of smart power devices will continue in the near future, addressing more power electronic applications.

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7

Insulated Gate Bipolar Transistor

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7.1 Introduction

The insulated gate bipolar transistor (IGBT), which was introduced in the early 1980s, has become a successful device because of its superior characteristics. The IGBT is a three-terminal power semiconductor switch used to control electrical energy and many new applications would not be economically feasible without IGBTs. Prior to the advent of the IGBT, power bipolar junction transistors (BJTs) and power metal oxide field effect transistors (MOSFETs) were widely used in low to medium power and high-frequency applications, where the speed of gate turn-off thyristors was not adequate. Power BJTs have good on-state characteristics but long switching times especially at turn-off. They are current-controlled devices with small current gain because of high-level injection effects and wide basewidth required to prevent reach-through breakdown for high blocking voltage capability. Therefore, they require complex base-drive circuits to provide the base current during on-state, which increases the power loss in the control electrode.

On the other hand, power MOSFETs are voltage-controlled devices, which require very small current during the switching period and hence have simple gate-drive requirements. Power MOSFETs are majority carrier devices, which exhibit very high switching speeds. However, the unipolar nature of the power MOSFETs causes inferior conduction characteristics as the voltage rating is increased above 200 V. Therefore, their on-state resistance increases with increasing breakdown voltage. Furthermore, as the voltage rating increases, the inherent body diode shows inferior reverse recovery characteristics, which leads to higher switching losses.

In order to improve the power device performance it is advantageous to have the low on-state resistance of power BJTs with an insulated gate input similar to that of a power MOSFET. The Darlington configuration of the two devices shown in Fig. 7.1 has superior characteristics as compared to the two discrete devices. This hybrid device could be gated in the same way as a power MOSFET with low on-state resistance because most of the output current is handled by the BJT. Because of the low current gain of BJT, a MOSFET of equal size is required as a driver. A more powerful approach to obtain the maximum benefits of the MOS gate control and bipolar current conduction is to integrate the physics of MOSFET and BJT within the same semiconductor region. This concept gave rise to the commercially available IGBTs with superior on-state

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characteristics, good switching speed and excellent safe operating area. Compared to power MOSFETs the absence of the integral body diode can be considered as an advantage or disadvantage depending on the switching speed and current requirements. An external fast-recovery diode or a diode in the same package can be used for specific applications. The IGBTs are replacing MOSFETs in high-voltage applications with lower conduction losses. They have on-state voltage and current density comparable to a power BJT with higher switching frequency. Although they exhibit fast turn-on, their turn-off is slower than a MOSFET because of current fall time. Also, IGBTs have considerably less silicon area than similar rated power MOSFETs. Therefore, by replacing power MOSFETs with IGBTs, the efficiency is improved and cost is reduced. Additionally, IGBT is known as a conductivity-modulated FET (COMFET), insulated gate transistor (IGT), and bipolar-mode MOSFET.

As soft-switching topologies offer numerous advantages over the hard-switching topologies, their use is increasing in the industry. By use of soft-switching techniques IGBTs can operate at frequencies up to hundreds of kilohertz. However, IGBTs behave differently under soft-switching condition compared to their behavior under hard-switching conditions. Therefore, the device trade-offs involved in soft-switching circuits are different than those in the hard-switching case. Application of IGBTs in high-power converters subjects them to high-transient electrical stress such as short-circuit and turn-off under clamped inductive load, and therefore robustness of IGBTs under stress conditions is an important requirement. Traditionally, there has been limited interaction between device manufacturers and power electronic circuit designers. Therefore, the shortcomings of device reliability are observed only after the devices are used in actual circuits. This significantly slows down the process of power electronic system optimization. However, the development time can be significantly reduced if all issues of device performance and reliability are taken into consideration at the design stage. As high stress conditions are quite frequent in circuit applications, it is extremely cost efficient and pertinent to model the IGBT performance under these conditions. However, development of the model can follow only after the physics of device operation under stress conditions imposed by the circuit is properly understood. Physically based process and device simulations are a quick and cheap way of optimizing the IGBT. The emergence of mixed-mode circuit simulators in which semiconductor carrier dynamics is optimized within the constraints of circuit level switching is a key design tool for this task.

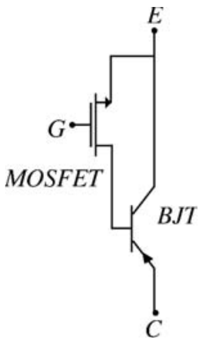
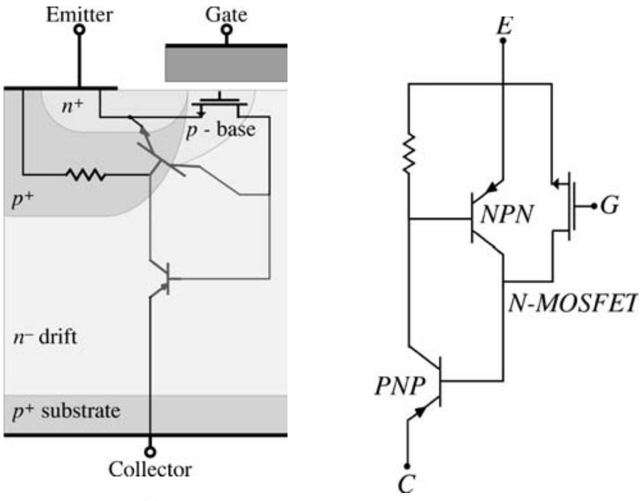


FIGURE 7.1 Hybrid Darlington configuration of MOSFET and BJT.

7.2 Basic Structure and Operation

The vertical cross section of a half cell of one of the parallel cells of an *n*-channel IGBT shown in Fig. 7.2 is similar to that of a double-diffused power MOSFET (DMOS) except for a p^+-layer at the bottom. This layer forms the IGBT collector and a *pn*-junction with n^--drift region, where conductivity modulation occurs by injecting minority carriers into the drain drift region of the vertical MOSFET. Therefore, the current density is much greater than a power MOSFET and the forward voltage drop is reduced. The p^+-substrate, n^--drift layer and p^+-emitter constitute a BJT with a wide base region and hence small current gain. The device operation can be explained by a BJT with its base current controlled by the voltage applied to the MOS gate. For simplicity, it is assumed that the emitter terminal is connected to the ground potential. By applying a negative voltage to the collector, the *pn*-junction between the p^+-substrate and the n^--drift region is reverse-biased, which prevents any current flow and the device is in its reverse blocking state. If the gate terminal is kept at ground potential but a positive potential is applied to the collector, the *pn*-junction between the *p*-base and n^--drift region is reverse-biased. This prevents any current flow and the device is in its



(a) (b)

FIGURE 7.2 The IGBT (a) half-cell vertical cross section and (b) equivalent circuit model.

forward blocking state until the open-base breakdown of the *pnp*-transistor is reached.

When a positive potential is applied to the gate and exceeds the threshold voltage required to invert the MOS region under the gate, an *n*-channel is formed, which provides a path for electrons to flow into the n^--drift region. The *pn*-junction between the p^+-substrate and n^--drift region is forward-biased and holes are injected into the drift region. The electrons in the drift region recombine with these holes to maintain space-charge neutrality and the remaining holes are collected at the emitter, causing a vertical current flow between the emitter and collector. For small values of collector potential and a gate voltage larger than the threshold voltage, the on-state characteristics can be defined by a wide-base power BJT. As the current density increases, the injected carrier density exceeds the low doping of the base region and becomes much larger than the background doping. This conductivity modulation decreases the resistance of the drift region and therefore IGBT has a much greater current density than a power MOSFET with reduced forward-voltage drop. The base-collector junction of the *pnp*-BJT cannot be forward-biased and therefore this transistor will not operate in saturation. However, when the potential drop across the inversion layer becomes comparable to the difference between the gate voltage and threshold voltage, channel pinch-off occurs. The pinch-off limits the electron current and as a result the holes injected from the p^+-layer. Therefore, base current saturation causes the collector current to saturate.

Typical forward characteristics of an IGBT as a function of gate potential and IGBT transfer characteristics are shown in Fig. 7.3. The transfer characteristics of IGBT and MOSFET are similar. The IGBT is in the off-state if the gate-emitter potential is below the threshold voltage. For gate voltages greater than the threshold voltage the transfer curve is linear over most of the drain-current range. Gate oxide breakdown and the maximum IGBT drain current limit the maximum gate-emitter voltage.

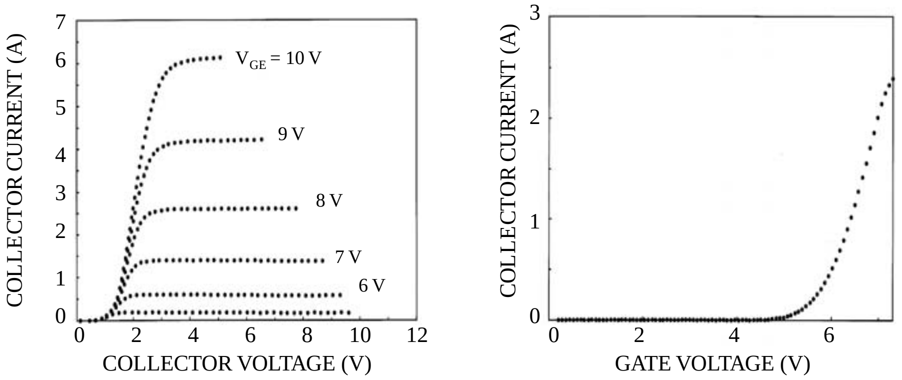


FIGURE 7.3 The IGBT (a) forward- and (b) transfer characteristics.

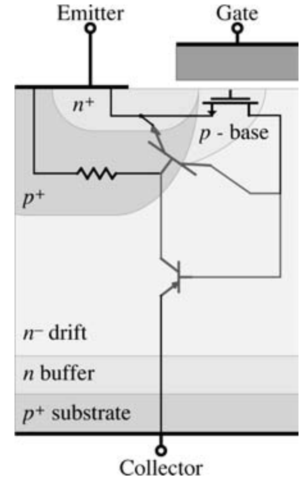


FIGURE 7.4 Punch-through (PT) IGBT.

To turn off the IGBT, the gate is shorted to the emitter to remove the MOS channel and the base current of the *pnp* transistor. The collector current is suddenly reduced because the electron current from the channel is removed. Then the excess carriers in the n^--drift region decay by electron-hole recombination, which causes a gradual collector current decay. In order to keep the on-state voltage drop low, the excess carrier lifetime must be kept large. Therefore, similar to the other minority carrier devices, there is a trade-off between on-state losses and faster turn-off switching times. In the punch-through (PT) IGBT structure of Fig. 7.4 the switching time is reduced by use of a heavily doped *n* buffer layer in the drift region near the collector. Because of much higher doping density in the buffer layer the injection efficiency of the collector junction and the minority carrier lifetime in the base region is reduced. The smaller excess carrier lifetime in the buffer layer sinks the excess holes, which speeds up the removal of holes from the drift region and therefore decreases the turn-off time. Nonpunch-through (NPT) IGBTs have higher carrier lifetimes and a low-doped shallow collector region, which affect their electrical characteristics. In order to prevent punch through, NPT IGBTs have a thicker drift region, which results in a higher base transit time. Therefore, in NPT structure the carrier lifetime is kept more than that of a PT structure, which causes conductivity modulation of the drift region and reduces the on-state voltage drop.

7.3 Static Characteristics

In the IGBT structure of Fig. 7.2 if a negative voltage is applied to the collector, the junction between the p^+-substrate and n^--drift region becomes reverse-biased. The drift region is lightly doped and the depletion layer extends principally into the drift region. An open-base transistor exists between the p^+-substrate, n^--drift region, and the p-base region. The doping concentration (N_D) and thickness of the n^--drift region (W_D) are designed to avoid the breakdown of this structure. The width of the drift region affects the forward voltage drop and therefore should be optimized for a desired breakdown voltage. The thickness of the drift region (W_D) is chosen equal to the sum of one diffusion length (L_p) and the width of the depletion layer at maximum applied voltage ($V_{\max}$):

$$W_D = \sqrt{\frac{2\varepsilon_s V_{\max}}{qN_D}} + L_p \tag{7.1}$$

When the gate is shorted to the emitter, no channel exists under the gate. Therefore, if a positive voltage is applied to the collector the junction between the p-base and n^--drift region is reverse-biased and only a small leakage current flows through IGBT. Similar to a MOSFET the depletion layer extends into the p-base and n^--drift region. The p-base doping concentration, which also controls the threshold voltage, is chosen to avoid punch through of the p-base to n^+-emitter. In ac circuit applications, which require identical forward and reverse blocking capability the drift-region thickness of the symmetrical IGBT shown in Fig. 7.2 is designed by use of Eq. 7.1 to avoid reach-through of the depletion layer to the junction between the p^+-collector and the n^--drift region. When IGBT is used in dc circuits, which do not require reverse blocking capability, a highly doped n-buffer layer is added to the drift region near the collector junction to form a PT IGBT. In this structure the depletion layer occupies the entire drift region and the n-buffer layer prevents reach-through of the depletion layer to the p^+-collector layer. Therefore, the required thickness of the drift region is reduced, which reduces the on-state losses. However, the highly doped n-buffer layer and p^+-collector layer degrade the reverse blocking capability to a very low value. Therefore, on-state characteristics of a PT IGBT can be optimized for a required forward blocking capability while the reverse blocking capability is neglected.

When a positive voltage is applied to the gate of an IGBT, a MOS channel is formed between the n^+-emitter and the n^--drift region. Therefore, a base current is provided for the parasitic pnp-BJT. By applying a positive voltage between the collector and emitter electrodes of an n-type IGBT, minority carriers (holes) are injected into the drift region. The injected minority carriers reduce the resistivity of the drift region and also the on-state voltage drop resulting in a much higher current density compared to a power MOSFET.

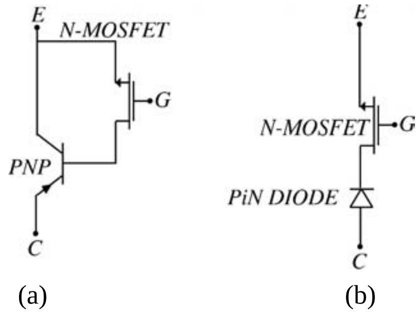


FIGURE 7.5 The IGBT equivalent circuits (a) BJT/MOSFET, and (b) *pin*/MOSFET.

If the shorting resistance between the base and emitter of the npn-transistor is small, the n^+-emitter p-base junction does not become forward-biased and therefore the parasitic npn-transistor is not active and can be deleted from the equivalent IGBT circuit. The analysis of the forward conduction characteristics of an IGBT is possible by use of the two equivalent circuit approaches shown in Fig. 7.5. The model based on a *pin*-rectifier in series with a MOSFET shown in Fig. 7-5b is easy to analyze and gives a reasonable understanding of the IGBT operation. However, this model does not account for the hole-current component flowing into the p-base region. The junction between the p-base and the n^--drift region is reverse-biased. This requires that the free carrier density be zero at this junction and therefore results in a different boundary condition for IGBT compared to those for a *pin*-rectifier. The IGBT conductivity modulation in the drift region is identical to the *pin*-rectifier near the collector junction, but it is less than a *pin*-rectifier near the p-base junction. Therefore, the model based on a bipolar pnp-transistor driven by a MOSFET in Fig. 7.5a gives a more complete description of the conduction characteristics.

Analyzing the IGBT operation by use of these models shows that IGBT has one diode drop due to the parasitic diode. Below the diode knee voltage there is negligible current flow due to the lack of minority carrier injection from the collector. Also, by increasing the applied voltage between the gate and emitter the base of the internal bipolar transistor is supplied by more base current, which results in an increase in the collector current. The IGBT current shows saturation due to the pinch-off of the MOS channel, which limits the input base current of the bipolar transistor. The MOS channel of the IGBT reverse-biases the collector-base junction and forces the bipolar pnp-transistor to operate in its active region. The drift region is in high-level injection at the required current densities and wider n^--drift region results in higher breakdown voltage.

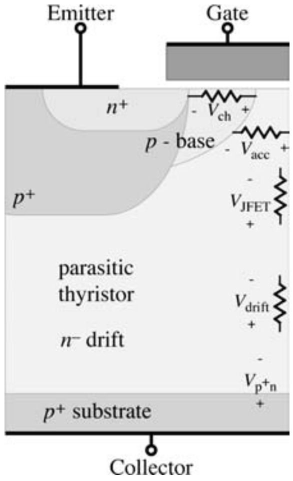


FIGURE 7.6 Components of on-state voltage drop within the IGBT structure.

Because of the very low gain of the *pnp*-BJT, the driver MOSFET in the equivalent circuit of the IGBT carries a major portion of the total collector current. Therefore, the IGBT on-state voltage drop as is shown in Fig. 7.6 consists of voltage drop across the collector junction, drop across the drift region, and the drop across the MOSFET portion. The low value of the drift-region conductivity modulation near the *p*-base junction causes a substantial drop across the JFET resistance of the MOSFET (V_{JFET}) in addition to the voltage drop across the channel resistance (V_{ch}) and the accumulation layer resistance (V_{acc}):

$$V_{\mathrm{CE(on)}} = V_{p^+n} + V_{\mathrm{drift}} + V_{\mathrm{MOSFET}} \qquad (7.2)$$

$$V_{\mathrm{MOSFET}} = V_{\mathrm{ch}} + V_{\mathrm{JFET}} + V_{\mathrm{acc}} \qquad (7.3)$$

When the lifetime in the n$^-$-drift region is large, the gain of the *pnp*-bipolar transistor is high and its collector current is much larger than the MOSFET current. Therefore, the voltage drop across the MOSFET component of IGBT is a small fraction of the total voltage drop. When lifetime control techniques are used to increase the switching speed, the current gain of the bipolar transistor is reduced and a greater portion of the current flows through the MOSFET channel and thus the voltage drop across the MOSFET increases. In order to decrease the resistance of the MOSFET current path, trench IGBTs can be used as is shown in Fig. 7.7. Extending the trench gate below the *p*-base and n$^-$-drift region junction forms a channel between the n^+-emitter and the n$^-$-drift region. This eliminates the JFET and accumulation layer resistance and thus reduces the voltage drop across the MOSFET component of IGBT, which results in superior conduction characteristics. By use of trench structure the IGBT cell density and latching current density are also improved.

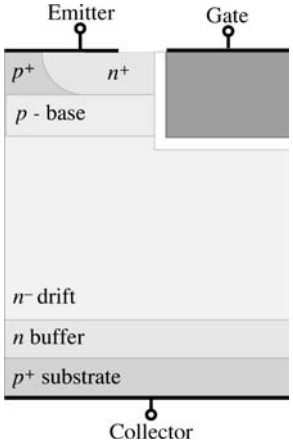


FIGURE 7.7 Trench IGBT structure.

7.4 Dynamic Switching Characteristics

7.4.1 Turn-on Characteristics

The switching waveforms of an IGBT in a clamped inductive circuit are shown in Fig. 7.8. The inductance-to-resistance (L/R) time constant of the inductive load is assumed to be large compared to the switching frequency and therefore can be considered as a constant current source I_{on}. The IGBT turn-on switching performance is dominated by its MOS structure. During $t_{d(\mathrm{on})}$ the gate current charges the constant input capacitance with a constant slope until the gate-emitter voltage reaches the threshold voltage $V_{\mathrm{GE(th)}}$ of the device.

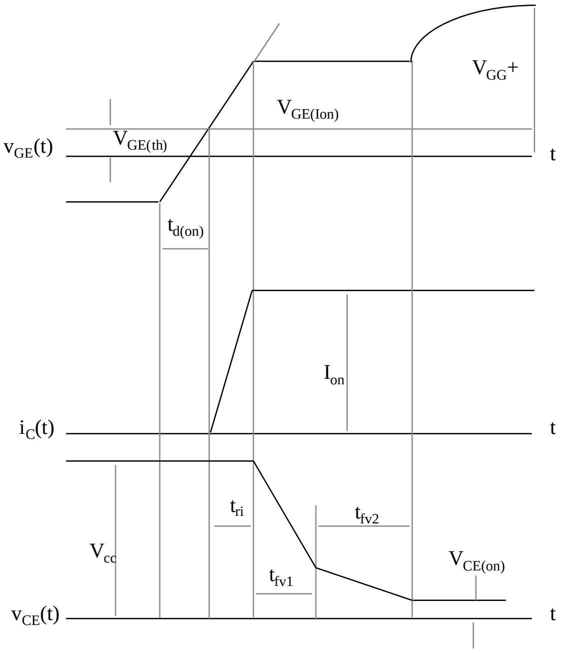


FIGURE 7.8 The IGBT turn-on waveforms in a clamped inductive load circuit.

During t_{ri} load current is transferred from the diode into the device and increases to its steady-state value.

The gate voltage rise time and IGBT transconductance determine the current slope and as a result t_{ri}. When the gate-emitter voltage reaches $V_{\mathrm{GE(Ion)}}$ that will support the steady-state collector current, collector-emitter voltage starts to decrease. After this there are two distinct intervals during IGBT turn-on. In the first interval the collector-to-emitter voltage drops rapidly as the gate-drain capacitance C_{gd} of the MOSFET portion of IGBT discharges. At low collector-emitter voltage C_{gd} increases. A finite time is required for high-level injection conditions to set in the drift region. The *pnp*-transistor portion of IGBT has a slower transition to its on-state than the MOSFET. The gate voltage starts rising again only after the transistor comes out of its saturation region into the linear region, when complete conductivity modulation occurs and the collector-emitter voltage reaches its final on-state value.

7.4.2 Turn-off Characteristics

Turn-off begins by removing the gate-emitter voltage. Voltage and current remain constant until the gate voltage reaches $V_{\mathrm{GE(Ion)}}$ required to maintain the collector steady-state current as shown in Fig. 7.9. After this delay time ($t_{d(\mathrm{off})}$) the collector voltage rises, while the current is held constant. The gate resistance determines the rate of collector-voltage rise. As the MOS channel turns off, collector current decreases sharply during t_{fi1}. The MOSFET portion of IGBT determines the turn-off delay time $t_{d(\mathrm{off})}$ and the voltage rise time t_{rv}. When the collector voltage reaches the bus voltage, the freewheeling diode starts to conduct.

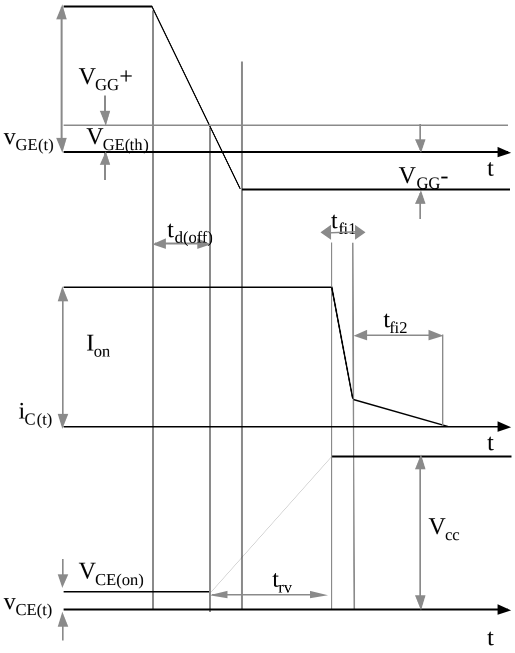


FIGURE 7.9 Switching waveforms during IGBT clamped inductive load turn-off.

However, the excess stored charge in the n$^-$-drift region during on-state conduction must be removed for the device to turn off. The high minority-carrier concentration stored in the n$^-$-drift region supports the collector current after the MOS channel is turned off. Recombination of the minority carriers in the wide-base region gradually decreases the collector current and results in a current tail. Because there is no access to the base of the *pnp*-transistor, the excess minority carriers cannot be removed by reverse-biasing the gate. The t_{fi2} interval is long because the excess carrier lifetime in this region is normally kept high to reduce the on-state voltage drop. Because the collector-emitter voltage has reached the bus voltage in this interval a significant power loss occurs that increases with frequency. Therefore, the current tail limits the IGBT operating frequency and there is a trade-off between the on-state losses and faster switching times. For an on-state current of I_{on}, the magnitude of current tail, and time required for the collector current to decrease to 10% of its on-state value, turn-off (t_{off}) time, are approximated as:

$$I_c(t) = \alpha_{pnp} I_{\mathrm{on}} e^{-(t/\tau_{HL})} \tag{7.4}$$

$$t_{\mathrm{off}} = \tau_{HL} \ln(10\alpha_{pnp}) \tag{7.5}$$

where

$$\alpha_{pnp} = \mathrm{sech}\left(\frac{l}{L_a}\right) \tag{7.6}$$

is the gain of the bipolar *pnp*-transistor, l is the undepleted basewidth and L_a is the ambipolar diffusion length and it is assumed that the high-level lifetime (τ_{HL}) is independent of the minority carrier injection during the collector current decay.

Lifetime control techniques are used to reduce the lifetime (τ_{HL}) and the gain of the bipolar transistor (α_{pnp}). As a result the magnitude of the current tail and t_{off} decrease. However, the conductivity modulation decreases, which increases the on-state voltage drop in the drift region. Therefore, higher-speed IGBTs have a lower current rating. Thermal diffusion of impurities such as gold and platinum introduces recombination centers, which reduce the lifetime. The device can also be irradiated with high-energy electrons to generate recombination centers. Electron irradiation introduces a uniform distribution of defects, which results in reduction of lifetime in the entire wafer and affects the conduction properties of the device. Another method of lifetime control is proton implantation, which can place defects at a specific depth. Therefore, it is possible to have a localized control of lifetime to improve the trade-off between the on-state voltage and switching speed of the device. The turn-off loss can be minimized by curtailing the current tail as a result of speeding up the recombination process in the portion of the drift region, which is not swept by the reverse bias.

7.4.3 Latch-up of Parasitic Thyristor

A portion of the minority carriers injected into the drift region from the collector of an IGBT flows directly to the emitter terminal. The negative charge of electrons in the inversion layer attracts the majority of holes and generates the lateral component of hole current through the *p*-type body layer as shown in Fig. 7.10. This lateral current flow develops a voltage drop across the spreading resistance of the *p*-base region, which forward-biases the base-emitter junction of the *npn*-parasitic BJT. By designing a small spreading resistance, the voltage drop is lower than the built-in potential and therefore the parasitic thyristor between the p^+-collector region, n^--drift region, *p*-base region, and n^+-emitter does not latch up. Larger values of on-state current density produce a larger voltage drop, which causes injection of electrons from the emitter region into the *p*-base region and hence turn-on of the *npn*-transistor. When this occurs the *pnp*-transistor will turn on, and therefore the parasitic thyristor will latch up and the gate loses control over the collector current.

Under dynamic turn-off conditions the magnitude of the lateral hole current flow increases and latch-up can occur at lower on-state currents compared to the static condition. The parasitic thyristor latches up when the sum of the current gains of the *npn*- and *pnp*-transistors exceeds one. When the gate voltage is removed from IGBT with a clamped inductive load, its MOSFET component turns off and reduces the MOSFET current to zero very rapidly. As a result the drain-source voltage rises rapidly and is supported by the junction between the n^--drift region and the *p*-base region. The drift region has a lower doping and therefore the depletion layer extends more in the drift region. Hence, the current gain of the *pnp*-transistor portion, α_{pnp}, increases and a greater portion of the injected holes into the drift region will be collected at the junction of *p*-base and n^--drift regions. Therefore, the magnitude of the lateral hole current increases, which increases the lateral voltage drop. As a result the parasitic thyristor will latch up even if the on-state current is less than the static latch-up value.

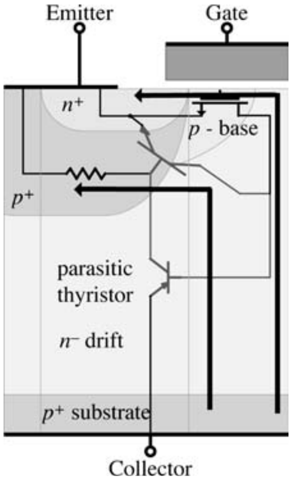


FIGURE 7.10 On-state current flow paths in an IGBT structure.

Reducing the gain of the *npn*- or *pnp*-transistors can prevent the parasitic thyristor latch-up. A reduction in the gain of the *pnp*-transistor increases the IGBT on-state voltage drop. Therefore, in order to prevent the parasitic thyristor latch up it is better to reduce the gain of the *npn*-transistor component of IGBT. Reduction of carrier lifetime, use of buffer layer, and use of deep p^+-diffusion improve the latch-up immunity of IGBT. However, inadequate extension of the p^+-region may fail to prevent the device from latch-up. Also, care should be taken that the p^+-diffusion does not extend into the MOS channel because this causes an increase in the MOS threshold voltage.

7.5 IGBT Performance Parameters

The IGBTs are characterized by certain performance parameters. The manufacturers specify these parameters, which are described in what follows, in the IGBT data sheet. The important ratings of IGBTs are values that establish either a minimum or maximum limiting capability or limiting condition. The IGBTs cannot be operated beyond the maximum or minimum rating value, which is determined for a specified operating point and environment condition.

Collector-Emitter Blocking Voltage (BV_{CES}) This parameter specifies the maximum off-state collector-emitter voltage when the gate and emitter are shorted. Breakdown is specified at a specific leakage current and varies with temperature by a positive temperature coefficient.

Emitter-Collector Blocking Voltage (BV_{ECS}) This parameter specifies the reverse breakdown of the collector-base junction of the *pnp*-transistor component of IGBT.

Gate-Emitter Voltage (V_{GES}) This parameter determines the maximum allowable gate-emitter voltage when the collector is shorted to emitter. The thickness and characteristics of the gate-oxide layer determine this voltage. The gate voltage should be limited to a much lower value to limit the collector current under fault conditions.

Continuous Collector Current (I_C) This parameter represents the value of the dc current required to raise the junction to its maximum temperature from a specified case temperature. This rating is specified at a case temperature of 25 °C and maximum junction temperature of 150 °C. Because normal operating condition cause higher case temperatures, a plot is given to show the variation of this rating with case temperature.

Peak Collector Repetitive Current (I_{CM}) Under transient conditions the IGBT can withstand higher peak currents compared to its maximum continuous current, which is described by this parameter.

Maximum Power Dissipation (P_D) This parameter represents the power dissipation required to raise the junction temperature to its maximum value of 150 °C, at a case temperature of 25 °C. Normally a plot is provided to show the variation of this rating with temperature.

Junction Temperature (T_j) Specifies the allowable range of the IGBT junction temperature during its operation.

Clamped Inductive Load Current (I_{LM}) This parameter specifies the maximum repetitive current that IGBT can turn off under a clamped inductive load. During IGBT turn-on, the reverse recovery current of the freewheeling diode in parallel with the inductive load increases the IGBT turn-on switching loss.

Collector-Emitter Leakage Current (I_{CES}) This parameter determines the leakage current at the rated voltage and specific temperature when the gate is shorted to emitter.

Gate-Emitter Threshold Voltage ($V_{GE(th)}$) This parameter specifies the gate-emitter voltage range, where the IGBT is turned on to conduct the collector current. The threshold voltage has a negative temperature coefficient. Threshold voltage increases linearly with gate-oxide thickness and as the square root of the *p*-base doping concentration. Fixed surface charge at the oxide-silicon interface and mobile ions in the oxide shift the threshold voltage.

Collector-Emitter Saturation Voltage ($V_{CE(SAT)}$) This parameter specifies the collector-emitter forward voltage drop and is a function of collector current, gate voltage, and temperature. Reducing the resistance of the MOSFET channel and JFET region, and increasing the gain of the *pnp*-bipolar transistor can minimize the on-state voltage drop. The voltage drop across the MOSFET component of IGBT, which provides the base current of the *pnp*-transistor is reduced by a larger channel width, shorter channel length, lower threshold voltage, and wider gate length. Higher minority carrier lifetime and a thin *n*-epi region cause high carrier injection and reduce the voltage drop in the drift region.

Forward Transconductance (g_{FE}) Forward transconductance is measured with a small variation on the gate voltage, which linearly increases the IGBT collector current to its rated current at 100 °C. The transconductance of an IGBT is reduced at currents much higher than its thermal-handling capability. Therefore, unlike the bipolar transistors, the current-handling capability of IGBTs is limited by thermal consideration and not by its gain. At higher temperatures, the transconductance starts to decrease at lower collector currents. Therefore these features of transconductance protect the IGBT under short-circuit operation.

Total Gate Charge (Q_G) This parameter helps to design a suitably sized gate-drive circuit and approximately calculate its losses. Because of the minority-carrier behavior of the device, the switching times cannot be approximately calculated by use of gate-charge value. This parameter varies as a function of the gate-emitter voltage.

Turn-on Delay Time (t_d) This is defined as the time between 10% of gate voltage to 10% of the final collector current.

Rise Time (t_r) This is the time required for the collector current to increase to 90% of its final value from 10% of its final value.

Turn-off Delay Time ($t_{d(\mathrm{off})}$) This is the time between 90% of gate voltage to 10% of final collector voltage.

Fall Time (t_f) This is the time required for the collector current to drop from 90% of its initial value to 10% of its initial value.

Input Capacitance (C_{ies}) The measured gate-emitter capacitance when collector is shorted to emitter. The input capacitance is the sum of the gate-emitter and the Miller capacitance. The gate-emitter capacitance is much larger than the Miller capacitance.

Output Capacitance (C_{oes}) The capacitance between collector and emitter when the gate is shorted to the emitter, which has the typical *pn*-junction voltage dependency.

Reverse Transfer Capacitance (C_{res}) The Miller capacitance between gate and collector, which has a complex voltage dependency.

Safe Operating Area (**SOA**) The safe operating area determines the current and voltage boundary within which the IGBT can be operated without destructive failure. At low currents the maximum IGBT voltage is limited by the open-base transistor breakdown. The parasitic thyristor latch-up limits the maximum collector current at low voltages. While IGBTs immune to static latch-up may be vulnerable to dynamic latch-up, operation in short-circuit and inductive load switching are conditions that would subject an IGBT to a combined voltage and current stress. A forward-biased safe operating area (FBSOA) is defined during the turn-on transient of the inductive load switching when both electron and hole current flow in the IGBT in the presence of high voltage across the device. The reverse-biased safe operating area (RBSOA) is defined during the turn-off transient, where only hole current flows in the IGBT with high voltage across it.

If the time duration of simultaneous high voltage and high current is long enough, the IGBT failure will occur because of thermal breakdown. However, if this time duration is short, the temperature rise due to power dissipation will not be enough to cause thermal breakdown. Under this condition the avalanche breakdown occurs at voltage levels lower than the breakdown voltage of the device. Compared to the steady-state forward blocking condition the much larger charge in the drift region causes a higher electric field and narrower depletion region at the *p*-base and n^--drift junction. Under RBSOA conditions there is no electron in the space-charge region and therefore there is a larger increase in electric field than the FBSOA condition.

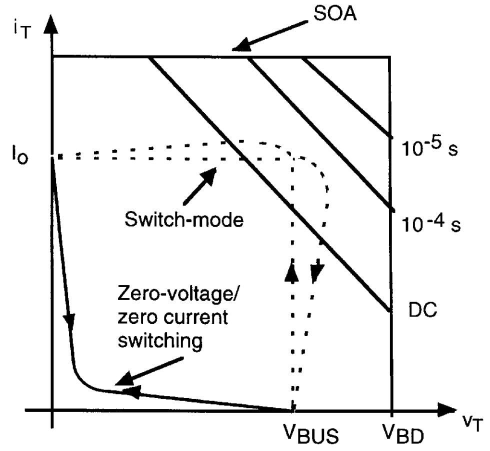


FIGURE 7.11 The IGBT safe operating area (SOA).

The IGBT SOA is indicated in Fig. 7.11. Under short switching times the rectangular SOA shrinks by an increase in the duration of the on-time. Thermal limitation is the reason for smaller SOA and the lower limit is set by dc operating conditions. The device switching loci under hard switching (dashed lines) and zero voltage or zero current switching (solid lines) is also indicated in Fig. 7.11. The excursion is much wider for switch-mode hard-switching applications than for the soft-switching case and therefore a much wider SOA is required for hard-switching applications. At present, IGBTs are optimized for hard-switching applications. In soft-switching applications the conduction losses of IGBT can be optimized at the cost of smaller SOA. In this case the *p*-base doping can be adjusted to result in a much lower threshold voltage and hence forward voltage drop. However, in hard-switching applications the SOA requirements dominate over forward voltage drop and switching time. Therefore, the *p*-base resistance should be reduced, which causes a higher threshold voltage. As a result, the channel resistance and forward voltage drop will increase.

7.6 Gate-Drive Requirements

The gate-drive circuit acts as an interface between the logic signals of the controller and the gate signals of the IGBT, which reproduces the commanded switching function at a higher power level. Nonidealities of the IGBT such as finite voltage and current rise and fall times, turn-on delay, voltage and current overshoots, and parasitic components of the circuit cause differences between the commanded and real waveforms. Gate-drive characteristics affect the IGBT nonidealities. The MOSFET portion of the IGBT drives the base of the *pnp*-transistor and therefore the turn-on transient and losses are greatly affected by the gate drive.

Due to lower switching losses, soft-switched power converters require gate drives with higher power ratings. The IGBT gate drive must have sufficient peak current capability to provide the required gate charge for zero current switching and zero voltage switching. The delay of the input signal to the gate drive should be small compared to the IGBT switching period and therefore the gate drive speed should be designed properly to be able to use the advantages of faster switching speeds of the new generation IGBTs.

7.6.1 Conventional Gate Drives

The first IGBT gate drives used fixed passive components and were similar to MOSFET gate drives. Conventional gate-drive circuits use a fixed gate resistance for turn-on and turn-off as shown in Fig. 7.12.

The turn-on gate resistor R_{gon} limits the maximum collector current during turn-on, and the turn-off gate resistor R_{goff} limits the maximum collector-emitter voltage. In order to decouple the dv_{ce}/dt and di_c/dt control an external capacitance C_g can be used at the gate, which increases the time constant of the gate circuit and reduces the di_c/dt as shown in Fig. 7.13. However, C_g does not affect the dv_{ce}/dt transient, which occurs during the Miller plateau region of the gate voltage.

7.6.2 New Gate-Drive Circuits

In order to reduce the delay time required for the gate voltage to increase from v_{gg}^- to $V_{ge}(th)$, the external gate capacitor can

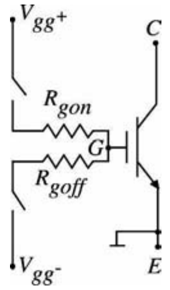


FIGURE 7.12 Gate-drive circuit with independent turn-on and turn-off resistors.

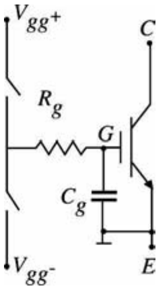


FIGURE 7.13 External gate capacitor for decoupling dv_{ce}/dt and di_c/dt during switching transient.

be introduced in the circuit only after V_{ge} reaches $V_{ge}(th)$ as is shown in Fig. 7.14, where the collector current rise occurs. The voltage tail during turn-on transient is not affected by this method. In order to prevent shoot-through caused by accidental turn-on of IGBT due to noise, a negative gate voltage is required during the off-state. Low gate impedance reduces the effect of noise on the gate.

During the first slope of the gate voltage turn-on transient the rate of charge supply to the gate determines the collector-current slope. During the Miller-effect zone of the turn-on transient the rate of charge supply to the gate determines the collector-voltage slope. Therefore, the slope of the collector current, which is controlled by the gate resistance, strongly affects the turn-on power loss. Reduction in switching power loss requires low gate resistance. However, the collector-current slope also determines the amplitude of the conducted electromagnetic interference during turn-on switching transient. Lower electromagnetic interference generation requires higher values of gate resistance. Therefore, in conventional gate-drive circuits by selecting an optimum value for R_g, there is a trade-off between lower switching losses and lower electromagnetic interference generation.

However, the turn-off switching of IGBT depends on the bipolar characteristics. Carrier lifetime determines the rate at which the minority carriers stored in the drift region recombine. The charge removed from the gate during turn-off has small influence on minority-carrier recombination. The tail current and *di*/*dt* during turn-off, which determine the turn-off losses, depend mostly on the amount of stored charge and the minority-carrier lifetime. Therefore, the gate-drive circuit has a minor influence on turn-off losses of the IGBT, while it affects the turn-on switching losses.

The turn-on transient is improved by use of the circuit shown in Fig. 7.15. The additional current source increases the gate current during the tail voltage time and thus reduces the turn-on loss. The initial gate current is determined by V_{gg}^{+} and R_{gon}, which are chosen to satisfy device electrical specifications and EMI requirements. After the collector current reaches its maximum value, the Miller effect occurs and the controlled-current source is enabled to increase the gate current to increase the rate of collector-voltage fall. This reduces the turn-on switching loss. Turn-off losses can only be reduced during the Miller effect and MOS turn-off portion of the turn-off transient, by reducing the gate resistance. However, this increases the rate of change of collector voltage, which strongly affects the IGBT latching current and RBSOA. During the turn-off period, the turn-off gate resistor R_{goff} determines the maximum rate of collector-voltage change. After the device turns off, turning on transistor T_1 prevents the spurious turn-on of IGBT by preventing the gate voltage from reaching the threshold voltage.

7.6.3 Protection

Gate-drive circuits can also provide fault protection of IGBT in the circuit. The fault-protection methods used in IGBT converters are different from their gate-turn-off thyristor (GTO) counterparts. In a GTO converter a crowbar is used for protection and as a result there is no current limiting. When the short-circuit is detected the control circuit turns on all the GTO switches in the converter, which results in opening of a fuse or circuit breaker on the dc input. Therefore, series *di*/*dt* snubbers are required to prevent rapid increase of the fault current and the snubber inductor has to be rated for large currents in the fault condition. However, IGBT has an important ability to intrinsically limit the current under overcurrent and short-circuit fault conditions, and the value of the fault current can be much larger than the nominal IGBT current. Thus IGBT has to be turned off rapidly after the fault occurs. The magnitude of the fault current depends on the positive-gate bias voltage V_{gg}^{+}. A higher V_{gg}^{+} is required to reduce conduction loss in the device, but this leads to larger fault currents. In order to decouple the trade-off limitation between conduction loss and fault-current level, a protection circuit can reduce the gate voltage when a fault occurs. However, this does not limit the peak value of the fault current, and therefore a fast fault-detection circuit is required to limit the peak value of the fault current. Fast integrated sensors in the gate-drive circuit are essential for proper IGBT protection.

Various methods have been studied to protect IGBTs under fault conditions. One of the techniques uses a capacitor to reduce the gate voltage when the fault occurs. However,

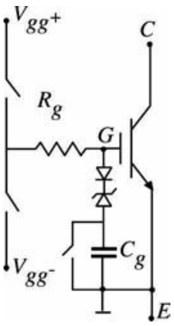


FIGURE 7.14 A circuit for reducing the turn-on delay.

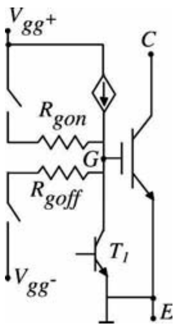


FIGURE 7.15 Schematic circuit of an IGBT gate-drive circuit.

depending on the initial condition of the capacitor and its value, the IGBT current may reduce to zero and then turn on again. Another method is to softly turn off the IGBT after the fault and to reduce the overvoltage due to di_c/dt. Therefore, the overvoltage on IGBT caused by the parasitic inductance is limited while turning off large currents. The most common method of IGBT protection is collector-voltage monitoring or desaturation detection. The monitored parameter is the collector-emitter voltage, which makes fault detection easier compared to measuring the device current. However, voltage detection can be activated only after the complete turn on of IGBT. If the fault current increases slowly due to large fault inductance, the fault detection is difficult because the collector-emitter voltage will not change significantly. In order to determine whether the current that is being turned off is overcurrent or nominal current, the Miller voltage plateau level can be used. This method can be used to initiate soft turn-off and to reduce the overvoltage during overcurrents.

Special sense IGBTs have been introduced at low-power levels with a sense terminal to provide a current signal proportional to the IGBT collector current. A few active device cells are used to mirror the current carried by the other cells. Unfortunately, however, sense IGBTs are not available at high-power levels and there are problems related to the higher conduction losses in the sense device. The most reliable method to detect an overcurrent fault condition is to introduce a current sensor in series with the IGBT. The additional current sensor makes the power circuit more complex and may lead to parasitic bus inductance, which results in higher overvoltages during turn off.

After the fault occurs the IGBT has to be safely turned off. Due to large di_c/dt during turn-off, the overvoltage can be very large. Therefore, many techniques have been investigated to obtain soft turn-off. The most common method is to use a large turn-off gate resistor when the fault occurs. Another method to reduce the turn-off overvoltage is to lower the fault-current level by reducing the gate voltage before initiating the turn-off. A resistive voltage divider can be used to reduce the gate voltage during fault turn-off. For example, the gate-voltage reduction can be obtained by turning on simultaneously R_{goff} and R_{gon} in the circuit of Fig. 7.12. Another method is to switch a capacitor into the gate and rapidly discharge the gate during the occurrence of a fault. To prevent the capacitor from charging back up to the nominal on-state gate voltage, a large capacitor should be used, which may cause a rapid gate discharge. Also, a Zener diode can be used in the gate to reduce the gate voltage after a fault occurs, but the slow transient behavior of the Zener diode leads to large initial peak fault current. The power dissipation during a fault determines the time duration that the fault current can flow in the IGBT without damaging it. Therefore, the IGBT fault-endurance capability is improved by the use of fault-current limiting circuits to reduce the power dissipation in the IGBT under fault conditions.

7.7 Circuit Models

A high-quality IGBT model for circuit simulation is essential for improving the efficiency and reliability in the design of power electronic circuits. Conventional models for power semiconductor devices simply described an abrupt or linear switching behavior and a fixed resistance during the conduction state. Low switching frequencies of power circuits made it possible to use these approximate models. However, moving to higher switching frequencies to reduce the size of a power electronic system requires high-quality power semiconductor device models for circuit simulation.

The *n*-channel IGBT consists of a *pnp*-bipolar transistor whose base current is provided by an *n*-channel MOSFET, as is shown in Fig. 7.1. Therefore, the IGBT behavior is determined by physics of the bipolar and MOSFET devices. Several effects dominate the static and dynamic device characteristics. The influence of these effects on a low-power semiconductor device is negligible and therefore they cannot be described by standard device models. The conventional circuit models were developed to describe the behavior of low-power devices, and therefore were not adequate to be modified for IGBT. The reason is that the bipolar transistor and MOSFET in the IGBT have a different behavior compared to their low-power counterparts; they also have different structures.

The currently available models have different levels of accuracy at the expense of speed. Circuit issues such as switching losses and reliability are strongly dependent on the device and require accurate device models. However, simpler models are only adequate for system-oriented issues such as the behavior of an electric motor driven by a pulsewidth modulation (PWM) converter. Finite-element models have high accuracy, but are slow and require internal device structure details. Macromodels are fast but have low accuracy, which depends on the operating point. Commercial circuit simulators have introduced one-dimensional (1D) physics-based models, which offer a compromise between the finite-element models and macromodels. The Hefner model and the Kraus model are such examples that have been implemented in Saber and there has been some effort to implement them in PSPICE. The Hefner model depends on the redistribution of charge in the drift region during transients. The Kraus model depends on the extraction of charge from the drift region by the electric field and emitter back-injection.

The internal BJT of the IGBT has a wide base, which is lightly doped to support the depletion region to have high blocking voltages. The excess carrier lifetime in the base region is low to have fast turn-off. However, low-power bipolar transistors have high excess carrier lifetime in the base, narrow base and high current gain. A finite base transit time is required for a change in the injected base charge to change the collector current. Therefore, quasi-static approximation cannot be used at high speeds and the transport of carriers in the base should be described by ambipolar transport theory.

7.7.1 Input and Output Characteristics

The bipolar and MOSFET components of a symmetric IGBT are shown in Fig. 7.16. The components between the emitter (e), base (b), and collector (c) terminals correspond to the bipolar transistor and those between gate (g), source (s), and drain (d) are associated with MOSFET. The combination of the drain-source and gate-drain depletion capacitances is identical to the base-collector depletion capacitance, and therefore they are shown for the MOSFET components. The gate-oxide capacitance of the source overlap (C_{oxs}) and source metallization capacitance (C_{m}) form the gate-source capacitance (C_{gs}). When the MOSFET is in its linear region the gate-oxide capacitance of the drain overlap (C_{oxd}) forms the gate-drain capacitance (C_{gd}). In the saturation region of MOSFET the equivalent series connection of gate-drain overlap oxide capacitance and the depletion capacitance of the gate-drain overlap (C_{gdj}) forms the gate-drain Miller capacitance. The gate-drain depletion width and the drain-source depletion width are voltage dependent, which has the same effect on the corresponding capacitances.

The most important capacitance in IGBT is the capacitance between the input terminal (g) and output terminal (a), because the switching characteristics are affected by this feedback.

$$C_{\mathrm{ga}} = \frac{dQ_g}{dv_{\mathrm{ga}}} = C_{\mathrm{ox}} \frac{dv_{\mathrm{ox}}}{dv_{\mathrm{ga}}} \tag{7.7}$$

C_{ox} is determined by the oxide thickness and device area. The accumulation, depletion, and inversion states below the gate cause different states of charge and therefore different capacitance values.

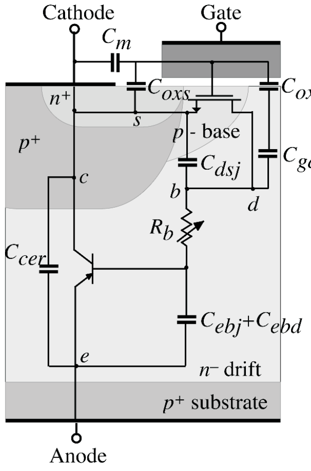


FIGURE 7.16 Symmetric IGBT half cell.

The stored charge in the lightly doped wide base of the bipolar component of IGBT causes switching delays and switching losses. The standard quasi-static charge description is not adequate for IGBT because it assumes that the charge distribution is a function of the IGBT terminal voltage. However, the stored charge density ($p(x,t)$) changes with time and position and therefore the ambipolar diffusion equation must be used to describe the charge variation:

$$\frac{dP(x, t)}{dt} = -\frac{P(x, t)}{\tau_a} + D_a \frac{d^2 P(x, t)}{dx^2} \tag{7.8}$$

The slope of the charge-carrier distribution determines the sum of electron and hole currents. The nonquasistatic behavior of the stored charge in the base of the bipolar component of IGBT results in the collector-emitter redistribution capacitance (C_{cer}). This capacitance dominates the output capacitance of IGBT during turn-off and describes the rate of change of the base-collector depletion layer with the rate of change of the base-collector voltage. However, the base-collector displacement current is determined by the gate-drain (C_{gdj}) and drain-source (C_{dsj}) capacitance of the MOSFET component.

7.7.2 Implementing the IGBT Model into a Circuit Simulator

Usually a netlist is employed in a circuit simulator such as Saber to describe an electrical circuit. Each component of the circuit is defined by a model template with the component terminal connection and the model parameters values. While Saber libraries provide some standard component models, the models can be generated by implementing the model equations in a defined Saber template. Electrical component models of IGBT are defined by the current through each component element as a function of component variables, such as terminal and internal node voltages and explicitly defined variables. The circuit simulator uses the Kirchhoff current law to solve for electrical component variables such that the total current into each node is equal to zero, while satisfying the explicitly defined component variables needed to describe the state of the device.

The IGBT circuit model is generated by defining the currents between terminal nodes as a nonlinear function of component variables and their rate of change. An IGBT circuit model is shown in Fig. 7.17. Compared to Fig. 7.16 the bipolar transistor is replaced by the two base and collector-current sources. There is a distributed voltage drop due to diffusion and drift in the base regions. The drift terms in the ambipolar diffusion equation depend on base and collector currents. Therefore, both of these currents generate the resistive voltage drop V_{ae} and R_b is placed at the emitter terminal in the IGBT circuit model. The capacitance of the emitter-base junction

(C_{eb}) is implicitly defined by the emitter-base voltage as a function of base charge; I_{ceb} is the emitter-base capacitor current that defines the rate of change of the base charge. The current through the collector-emitter redistribution capacitance (I_{ccer}) is part of the collector current, which in contrast to I_{css} depends on the rate of change of the base-emitter voltage; I_{bss} is part of the base current that does not flow through C_{eb} and does not depend on the rate of change of base-collector voltage.

Impact ionization causes carrier multiplication in the high electric field of the base-collector depletion region. This carrier multiplication generates an additional base-collector current component (I_{mult}), which is proportional to I_c, I_{mos}, and the multiplication factor. The resulting Saber IGBT model should be able to describe accurately the experimental results for the range of static and dynamic conditions where IGBT operates. Therefore, the model can be used to describe the steady-state and dynamic characteristics under various circuit conditions.

The currently available models have different levels of accuracy at the expense of speed. Circuit issues such as switching losses and reliability are strongly dependent on the device and require accurate device models. However, simpler models are adequate for system-oriented issues such as the behavior of an electric motor driven by a PWM converter. Finite-element models have high accuracy, but are slow and require internal device structure details. Macromodels are fast but have low accuracy, which depends on the operating point. Commercial circuit simulators have introduced 1D physics-based models, which offer a compromise between the finite-element models and macromodels.

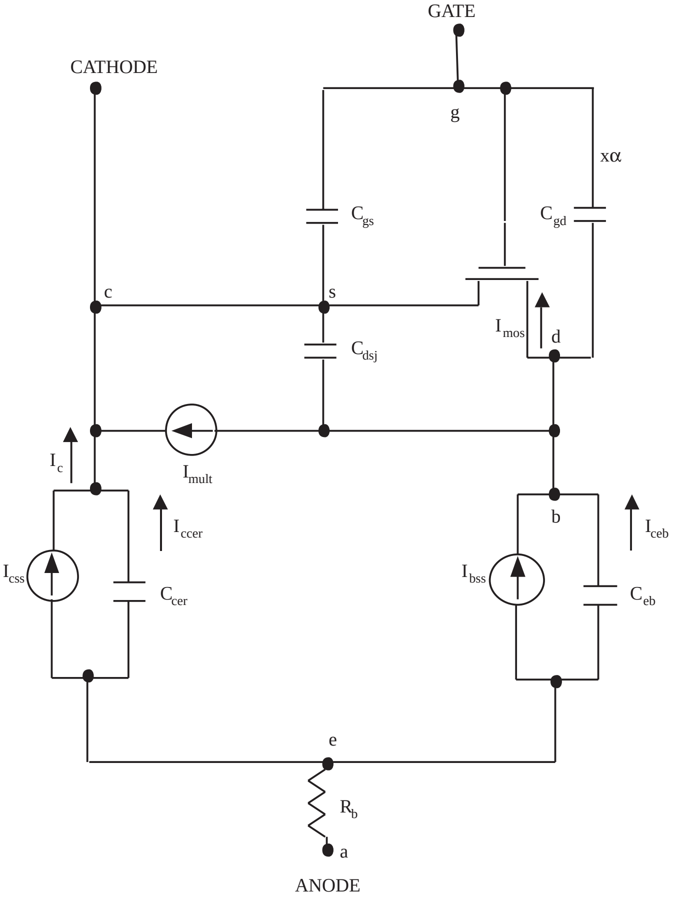


FIGURE 7.17 IGBT circuit model.

7.8 Applications

Power electronics evolution is a result of the evolution of power semiconductor devices. Applications of power electronics are still expanding in industrial and utility systems. A major challenge in designing power electronic systems is simultaneous operation at high power and high switching frequency. The advent of IGBTs has revolutionized power electronics by extending the power and frequency boundary. During the last decade the conduction and switching losses of IGBTs have been reduced in the process of transition from the first- to the third-generation IGBTs. The improved characteristics of the IGBTs have resulted in higher switching speed and lower energy losses. High-voltage IGBTs are expected to take the place of high-voltage GTO thyristor converters in the near future. To advance the performance beyond the third-generation IGBTs, the fourth-generation devices will require exploiting fine-line lithographic technology and employing the trench technology used to produce power MOSFETs with very low on-state resistance. Intelligent IGBT or intelligent power module (IPM) is an attractive power device integrated with circuits to protect against overcurrent, overvoltage, and overheating. The main application of IGBT is for use as a switching component in inverter circuits, which are used in both power supply and motor drive applications. The advantages of using IGBT in these converters are simplicity and modularity of the converter, simple gate drive, elimination of snubber circuits due to the square SOA, lower switching loss, improved protection characteristics in case of overcurrent and short-circuit fault, galvanic isolation of the modules, and simpler mechanical construction of the power converter. These advantages have made the IGBT the preferred switching device in the power range below 1 MW.

Power supply applications of IGBTs include uninterruptible power supplies (UPS) as is shown in Fig. 7.18, constant-voltage constant-frequency power supplies, induction heating systems, switch mode power supplies, welders (Fig. 7.19), cutters, traction power supplies, and medical equipment (CT, X-ray). Low-noise operation, small size, low cost and high accuracy are characteristics of the IGBT converters in these applications. Examples of motor drive applications include the variable-voltage variable-frequency inverter as is shown in Fig. 7.20. The IGBTS have been introduced at high voltage and current levels, which has enabled their use in high-power converters utilized for medium-voltage motor drives. The improved characteristics of the IGBTs have introduced power converters in megawatt power applications such as traction drives. One of the critical issues in realizing high-power converters is the reliability of the power switches. The devices used in these applications must be robust and capable of withstanding faults long enough for a protection scheme to be activated. The hard-switching voltage source power converter is the most commonly used topology. In this switch-mode operation the switches are subjected to high switching stresses and high-switching power loss that increase linearly with the switching frequency of the pulsewidth modulation (PWM). The resulting switching loci in the $v_t - i_t$ plane is shown by the dotted lines in Fig. 7.11. Because of simultaneous large switch voltage and large switch current, the switch must be capable of withstanding high switching stresses with a large SOA. The requirement of being able to withstand large stresses results in design compromises in other characteristics of the power semiconductor device. Often forward voltage drop and switching speed are sacrificed for enhanced short-circuit capability. Process parameters of the IGBT such as threshold voltage, carrier lifetime, and the device thickness can be varied to obtain various combinations of SOA, on-state voltage, and switching time. However, there is very little overlap in the optimum combination for more than one performance parameter. Therefore, improved performance in one parameter is achieved at the cost of other parameters.

In order to reduce the size, the weight, and the cost of circuit components used in a power electronics converter very high switching frequencies of the order of a few megahertz are being contemplated. In order to be able to increase the switching frequency, the problems of switch stresses, switching losses and the EMI associated with switch-mode applications need to be solved. Use of soft-switching converters reduces the problems of high dv/dt and high di/dt by use of external inductive and capacitive components to shape the switching trajectory of the device. The device-switching loci resulting from soft switching is shown in Fig. 7.11, where significant reduction in switching stress can be noticed. The traditional snubber circuits achieve this goal without the added control complexity, but the power dissipation in these snubber circuits can be large and limit the switching frequency of the converter. Also, passive components significantly add to the size, weight, and cost of the converter at high power levels. Soft switching uses lossless resonant circuits, which solves the problem of power loss in the snubber circuit, but increases the conduction loss. Resonant transition circuits eliminate the problem of high peak device stress in the soft-switched converters. The main drawback of these circuits is the increased control complexity required to obtain the resonant switching transition. The large number of circuit variables to be sensed in such power converters can affect their reliability. With short-circuit capability no longer being the primary concern, designers can push the performance envelope for their circuits until the device becomes the limiting factor once again.

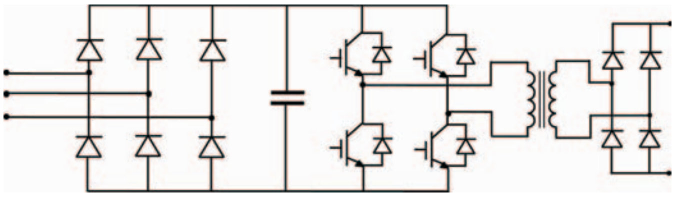


FIGURE 7.19 IGBT welder.

The transient response of the conventional volts/hertz induction motor drive is sluggish because both torque and flux are functions of stator voltage and frequency. Use of vector or field-oriented control methods makes the performance of the induction motor drive almost identical to that of a separately excited dc motor. Therefore, the transient response is similar to a dc machine, where torque and flux can be controlled in a decoupled manner. Vector-controlled induction motors with shaft encoders or speed sensors have been widely applied in combination with voltage-source PWM inverters using IGBT modules. According to the specification of the new products, vector-controlled induction motor drive systems ranging from kilowatts to megawatts provide a broad range of speed control, constant torque operation, and high starting torque.

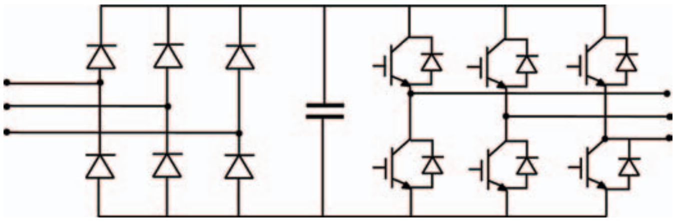


FIGURE 7.18 Constant-voltage, constant-frequency inverter (UPS).

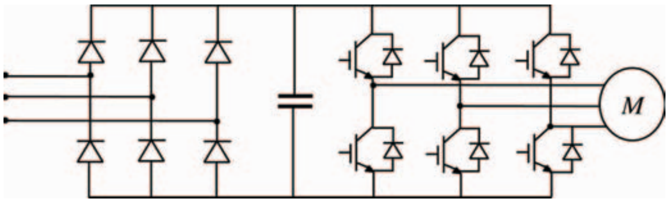


FIGURE 7.20 Variable-voltage, variable-frequency inverter (PWM).

Because of their simple gate drives and modular packaging, IGBTs led to simpler construction of power electronic circuits. This feature has lead to a trend to standardize and modularize power electronic circuits. Simplification of the overall system design and construction and significant cost reduction are the main implications of this approach. With these goals the Power Electronics Building Block (PEBB) program has been introduced, where the entire power electronic converter system is reduced to a single block. Similar modular power electronic blocks are commercially available at low power levels in the form of power-integrated circuits. At higher power levels, these blocks have been realized in the form of intelligent power modules and power blocks. However, these high-power modules do not encompass entire power electronic systems such as motor drives and UPS. The aim of the PEBB program is to realize the whole power-handling system within standardized blocks. A PEBB is a universal power processor that changes any electrical power input to any desired form of voltage, current and frequency output. A PEBB is a single package with a multifunction controller that replaces the complex power electronic circuits with a single device and therefore reduces the development and design costs of the complex power circuits and simplifies the development and design of large electric power systems.

The applications of power electronics are varied and various applications have their own specific design requirement. There is a wide choice of available power devices. Because of physical, material and design limitations none of the currently available devices behave as an ideal switch, which should block arbitrarily large forward and reverse voltages with zero current in the off-state, conduct arbitrarily large currents with zero-voltage drop in the on-state, and have negligible switching time and power loss. Therefore, power electronic circuits should be designed by considering the capabilities and limitations of available devices. Traditionally, there has been limited interaction between device manufacturers and circuit designers. Thus manufacturers have been fabricating generic power semiconductor devices with inadequate consideration of the specific applications where the devices are used. The diverse nature of power electronics does not allow the use of generic power semiconductor devices in all applications as it leads to nonoptimal systems. Therefore, the devices and circuits need to be optimized at the application level. Soft switching topologies offer numerous advantages over conventional hard-switching applications such as reduced switching stress and EMI, and higher switching speed at reduced power loss. The IGBTs behave dissimilarly in the two circuit conditions. As a result devices optimized for hard-switching conditions do not necessarily give the best possible performance when used in soft-switching circuits. In order to extract maximum system performance, it is necessary to develop IGBTs suited for specific applications. These optimized devices need to be manufacturable and cost effective in order to be commercially viable.

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8

M Controlled Thyristors MCTs

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8.1 Introduction

The efficiency, capacity, and ease of control of power converters depend mainly on the power devices employed. Power devices, in general, belong to either bipolar-junction type or field-effect type and each one has its advantages and disadvantages. The silicon controlled rectifier (SCR), also known as a thyristor, is a popular power device that has been used over the past several years. It has a high current density and a low forward voltage drop, both of which make it suitable for use in large power applications. The inability to turn off through the gate and the low switching speed are the main limitations of an SCR. The gate turn-off (GTO) thyristor was proposed as an alternative to SCR. However, the need for a higher gate turn-off current limited its application.

The power MOSFET has several advantages such as high input impedance, ease of control, and higher switching speeds. Lower current density and higher forward drop limited the device to low-voltage and low-power applications. An effort to combine the advantages of bipolar junction and field-effect structures has resulted in hybrid devices such as the insulated gate bipolar Transistor (IGBT) and the MOS controlled thyristor (MCT). While an IGBT is an improvement over a bipolar junction transistor (BJT) using a MOSFET to turn on and turn off current, an MCT is an improvement over a thyristor with a pair of MOSFETs to turn on and turn off current. The MCT overcomes several of the limitations of the existing power devices and promises to be a better switch for the future. While there are several devices in the MCT family with distinct combinations of channel and gate structures [1],

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one type, called the P-channel MCT, has been widely reported and is discussed here. Because the gate of the device is referred to with respect to the anode rather than the cathode, it is sometimes referred to as a complementary MCT (C-MCT) [2]. Harris Semiconductors (Intersil) originally made the MCTs, but the MCT division was sold to Silicon Power Corporation (SPCO), which has continued the development of MCTs.

8.2 Equivalent Circuit and Switching Characteristics

The SCR is a 4-layer *pnpn* device with a control gate, and applying a positive gate pulse turns it on when it is forward-biased. The regenerative action in the device helps to speed up the turn-on process and to keep it in the "ON" state even after the gate pulse is removed. The MCT uses an auxiliary MOS device (PMOSFET) to turn on and this simplifies the gate control. The turn-on has all the characteristics of a power MOSFET. The turn-off is accomplished using another MOSFET (NMOSFET), which essentially diverts the base current of one of the BJTs and breaks the regeneration.

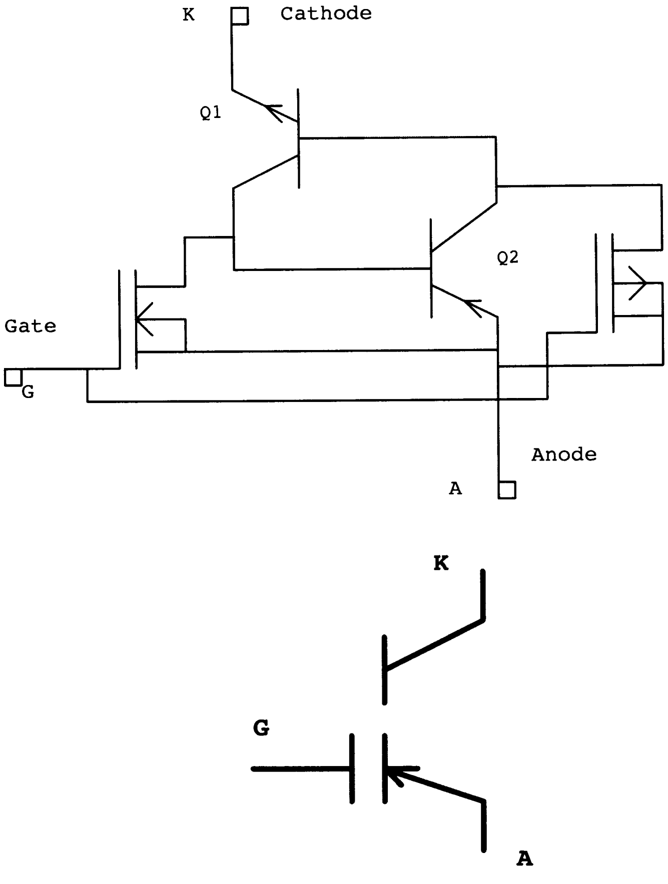


FIGURE 8.1 Equivalent circuit and symbol of an MCT.

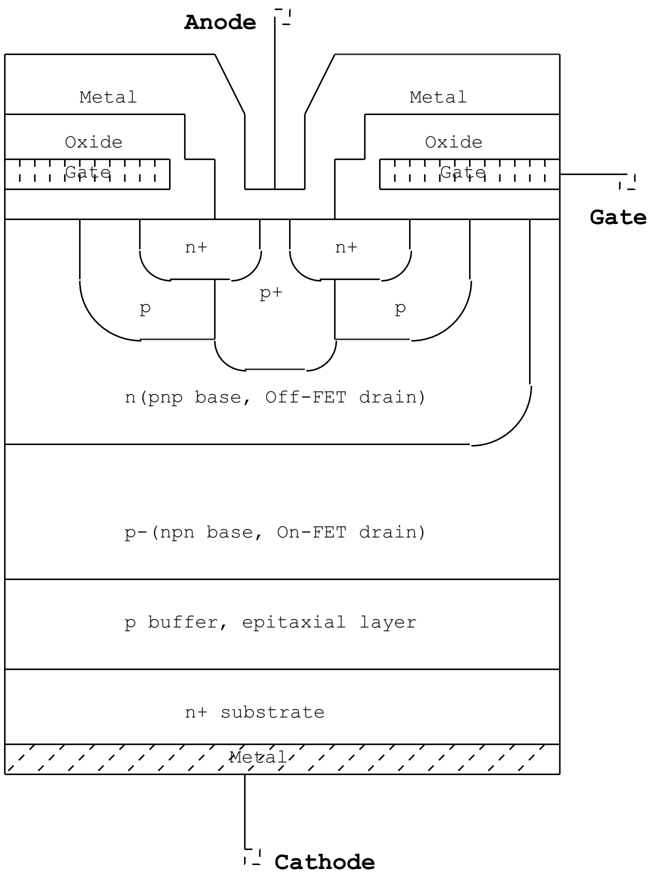

Anode
Metal
Metal
Oxide
Oxide
Gate
Gate
Gate
n+
n+
p+
p
p
n(pnp base, Off-FET drain)
p-(npn base, On-FET drain)
p buffer, epitaxial layer
n+ substrate
Metal
Cathode

FIGURE 8.2 Cross section of an MCT unit cell.

The transistor-level equivalent circuit of a P-channel MCT and the circuit symbol are shown in Fig. 8.1. The cross section of a unit cell is shown in Fig. 8.2. The MCT is modeled as an SCR merged with a pair of MOSFETs. The SCR consists of the bipolar junction transistors (BJTs) Q_1 and Q_2, which are interconnected to provide regenerative feedback such that the transistors drive each other into saturation. Of the two MOSFETs, the PMOS located between the collector and emitter of Q_2 helps to turn the SCR on, and the NMOS located across the base-emitter junction of Q_2 turns it off. In the actual fabrication, each MCT is made up of a large number (~100,000) cells, each of which contains a wide-base *npn* transistor and a narrow-base *pnp* transistor. While each *pnp* transistor in a cell is provided with an N-channel MOSFET across its emitter and base, only a small percentage (~4%) of *pnp* transistors are provided with P-channel MOSFETs across their emitters and collectors. The small percentage of PMOS cells in an MCT provides just enough current for turn-on and the large number of NMOS cells provide plenty of current for turn-off.

8.2.1 Turn-on and Turn-off

When the MCT is in the forward blocking state, it can be turned on by applying a negative pulse to its gate with respect to the anode. The negative pulse turns on the PMOSFET (On-FET) whose drain current flows through the base-emitter junction of Q_1 (*npn*) thereby turning it on. The regenerative action within $Q_1 - Q_2$ turns the MCT on into full conduction within a very short time and maintains it even after the gate pulse is removed. The MCT turns on without a plasma-spreading phase giving a high dI/dt capability and ease of overcurrent protection. The on-state resistance of an MCT is slightly higher than that of an equivalent thyristor because of the degradation of the injection efficiency of the N^+ emitter/p-base junction. Also, the peak current rating of an MCT is much higher than its average or rms current rating.

An MCT will remain in the "ON" state until the device current is reversed or a turn-off pulse is applied to its gate. Applying a positive pulse to its gate turns off a conducting MCT. The positive pulse turns on the NMOSFET (Off-FET), thereby diverting the base current of Q_2 (*pnp*) away to the anode of the MCT and breaking the latching action of the SCR. This stops the regenerative feedback within the SCR and turns the MCT off. All the cells within the device are to be turned off at the same time to avoid a sudden increase in current density. When the Off-FETs are turned on, the SCR section is heavily shorted and this results in a high dV/dt rating for the MCT. The highest current that can be turned off with the application of a gate bias is called the "maximum controllable current." The MCT can be gate controlled if the device current is less than the maximum controllable current. For smaller device currents, the width of the turn-off pulse is not critical. However, for larger currents, the gate pulse has to be wider and more often has to occupy the entire off-period of the switch.

8.3 Comparison of MCT and Other Power Devices

An MCT can be compared to a power MOSFET, a power BJT, and an IGBT of similar voltage and current ratings. The operation of the devices is compared under on-state, off-state, and transient conditions. The comparison is simple and very comprehensive.

The current density of an MCT is ≈70 higher than that of an IGBT having the same total current [2]. During its on-state, an MCT has a lower conduction drop compared to other devices. This is attributed to the reduced cell size and the absence of emitter shorts present in the SCR within the MCT. The MCT also has a modest negative temperature coefficient at lower currents with the temperature coefficient turning positive at larger current [2]. Figure 8.3 shows the conduction drop as a function of current density. The forward drop of a 50-A MCT at 25 °C is around 1.1 V, while that for a comparable IGBT is over 2.5 V. The equivalent voltage drop calculated from the value of r_{DS}(ON) for a power MOSFET will be much higher. However, the power MOSFET has a much lower delay time (30 ns) compared to that of an MCT (300 ns). The turn-on of a power MOSFET can be so much faster than an MCT or an IGBT therefore, the switching losses would be negligible compared to the conduction losses. The turn-on of an IGBT is intentionally slowed down to control the reverse recovery of the freewheeling diode used in inductive switching circuits [3].

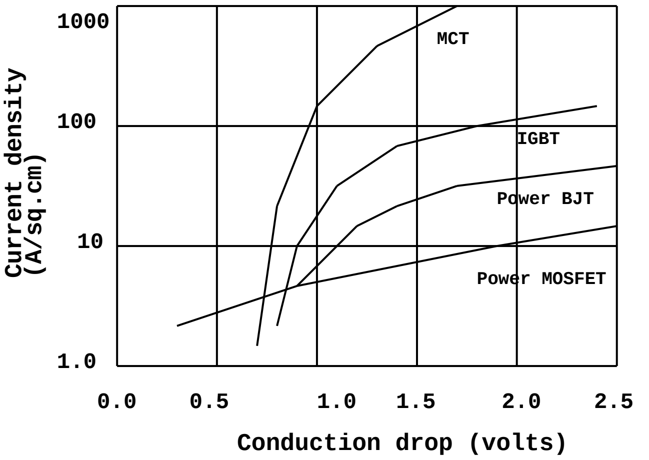


FIGURE 8.3 Comparison of forward drop for different devices.

The MCT can be manufactured for a wide range of blocking voltages. Turn-off speeds of MCTs are supposed to be higher as initially predicted. The turn-on performance of Generation-2 MCTs are reported to be better compared to Generation-1 devices. Even though the Generation-1 MCTs have higher turn-off times compared to IGBTs, the newer ones with higher radiation (hardening) dosage have comparable turn-off times. At present, extensive development activity in IGBTs has resulted in high-speed switched mode power supply (SMPS) IGBTs that can operate at switching speeds ≈150 kHz [4]. The turn-off delay time and the fall time for an MCT are much higher compared to a power MOSFET, and they are found to increase with temperature [2]. Power MOSFETs becomes attractive at switching frequencies above 200 kHz, and they have the lowest turn-off losses among the three devices.

The turn-off safe operating area (SOA) is better in the case of an IGBT than an MCT. For an MCT, the full switching current is sustainable at ≈50 to 60 of the breakdown voltage rating, while for an IGBT it is about 80 . The use of capacitive snubbers becomes necessary to shape the turn-off locus of an

MCT. The addition of even a small capacitor improves the SOA considerably.

8.4 Gate Drive for MCTs

The MCT has a MOS gate similar to a power MOSFET or an IGBT and hence it is easy to control. In a PMCT, the gate voltage must be applied with respect to its anode. A negative voltage below the threshold of the On-FET must be applied to turn on the MCT. The gate voltage should fall within the specified steady-state limits in order to give a reasonably low delay time and to avoid any gate damage due to overvoltage [3]. Similar to a GTO, the gate voltage rise-time has to be limited to avoid hot spots (current crowding) in the MCT cells. A gate voltage less than −5 V for turn-off and greater than 10 V for turn-on ensures proper operation of the MCT. The latching of the MCT requires that the gate voltage be held at a positive level in order to keep the MCT turned off.

Because the peak-to-peak voltage levels required for driving the MCT exceeds those of other gate-controlled devices, the use of commercial drivers is limited. The MCT can be turned on and off using a push-pull pair with discrete NMOS–PMOS devices, which, in turn, are driven by commercial integrated circuits (ICs). However, some drivers developed by MCT manufacturers are not commercially available [3].

A Baker's clamp push-pull can also be used to generate gate pulses of negative and positive polarity of adjustable width for driving the MCT [5–7]. The Baker's clamp ensures that the push-pull transistors will be in the quasi-saturated state prior to turn-off and this results in a fast switching action. Also, the negative feedback built into the circuit ensures satisfactory operation against variations in load and temperature. A similar circuit with a push-pull transistor pair in parallel with a pair of power BJTs is available [8]. An intermediate section, with a BJT that is either cut off or saturated, provides −10 and +15 V through potential division.

8.5 Protection of MCTs

8.5.1 Paralleling of MCTs

Similar to power MOSFETs, MCTs can be operated in parallel. Several MCTs can be paralleled to form larger modules with only slight derating of the individual devices provided the devices are matched for proper current sharing. In particular, the forward voltage drops of individual devices have to be matched closely.

8.5.2 Overcurrent Protection

The anode-to-cathode voltage in an MCT increases with its anode current and this property can be used to develop a protection scheme against overcurrent [5, 6]. The gate pulses to the MCT are blocked when the anode current and hence the anode-to-cathode voltage exceeds a preset value. A Schmitt trigger comparator is used to allow gate pulses to the MCT when it is in the process of turning on, during which time the anode voltage is relatively large and decreasing.

8.5.2.1 Snubbers

As with any other power device, the MCT is to be protected against switching-induced transient voltage and current spikes by using suitable snubbers. The snubbers modify the voltage and current transients during switching such that the switching trajectory is confined within the safe operating area (SOA). When the MCT is operated at high frequencies, the snubber increases the switching loss due to the delayed voltage and current responses. The power circuit of an MCT chopper including an improved snubber circuit is shown in Fig. 8.4 [5, 7]. The turn-on snubber consists of L_s and D_{LS} and the turn-off snubber consists of R_s, C_s, and D_{Cs}. The series-connected turn-on snubber reduces the rate of change of the anode current di_A/dt. The MCT does not support V_s until the current through the freewheeling diode reaches zero at turn-on. The turn-off snubber helps to reduce the peak power and the total power dissipated by the MCT by reducing the voltage across the MCT when the anode current decays to zero. The analysis and design of the snubber and the effect of the snubber on switching loss and electromagnetic interference are given in References [5] and [7]. An alternative snubber configuration for the two MCTs in an ac-ac converter has also been reported [8]. This snubber uses only one capacitor and one inductor for both the MCT switches (PMCT and NMCT) in a power-converter leg.

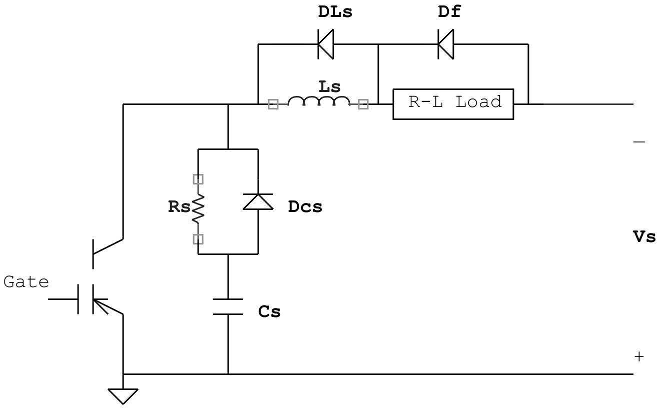


FIGURE 8.4 An MCT chopper with turn-on and turn-off snubbers.

8.6 Simulation Model of an MCT

The operation of power converters can be analyzed using PSPICE and other simulation software. As it is a new device, models of MCTs are not provided as part of the simulation libraries. However, an appropriate model for the MCT would be helpful in predicting the performance of novel converter topologies and in designing the control and protection circuits. Such a model must be simple enough to keep the simulation time and effort at a minimum, and must represent most of the device properties that affect the circuit operation. The PSPICE models for Harris PMCTs are provided by the manufacturer and can be downloaded from the internet. However, a simple model presenting most of the characteristics of an MCT is available [9, 10]. It is derived from the transistor-level equivalent circuit of the MCT by expanding the SCR model already reported the literature. The improved model [10] is capable of simulating the breakover and breakdown characteristics of an MCT and can be used for the simulation of high-frequency converters.

8.7 Generation-1 and Generation-2 MCTs

The Generation-1 MCTs were commercially introduced by Harris Semiconductors in 1992. However, the development of Generation-2 MCTs is continuing. In Gen-2 MCTs, each cell has its own turn-on field-effect transistor (FET). Preliminary test results on Generation-2 devices and a comparison of their performance with those of Generation-1 devices and high-speed IGBTs are available [11, 12]. The Generation-2 MCTs have a lower forward drop compared to the Generation-1 MCTs. They also have a higher dI/dt rating for a given value of capacitor used for discharge. During hard switching, the fall time and the switching losses are lower for the Gen-2 MCTs. The Gen-2 MCTs have the same conduction loss characteristics as Gen-1with drastic reductions in turn-off switching times and losses [13].

Under zero-current switching conditions, Gen-2 MCTs have negligible switching losses [13]. Under zero-voltage switching, the turn-off losses in a Gen-2 device are one-half to one-fourth (depending on temperature and current level) the turn-off losses in Gen-1 devices. In all soft-switching applications, the predominant loss, namely, the conduction loss, reduces drastically allowing the use of fewer switches in a module.

8.8 N-channel MCT

The PMCT discussed in this chapter uses an NMOSFET for turn-off and this results in a higher turn-off current capability. The PMCT can only replace a P-channel IGBT and inherits all the limitations of a P-channel IGBT. The results of a 2D simulation show that the NMCT can have a higher controllable current [13]. It is reported that NMCT versions of almost all Harris PMCTs have been fabricated for analyzing the potential for a commercial product [3]. The NMCTs are also being evaluated for use in zero-current soft-switching applications. However, the initial results are not quite encouraging in that the peak turn-off current of an NMCT is one-half to one-third of the value achievable in a PMCT. It is hoped that the NMCTs will eventually have a lower switching loss and a larger SOA as compared to PMCTs and IGBTs.

8. Base Resistance-Controlled Thyristor 14

The base resistance-controlled thyristor (BRT) is another gate-controlled device that is similar to the MCT but with a different structure. The Off-FET is not integrated within the *p*-base region but is formed within the *n*-base region. The diverter region is a shallow *p*-type junction formed adjacent to the *p*-base region of the thyristor. The fabrication process is simpler for this type of structure. The transistor level equivalent circuit of a BRT is shown in Fig. 8.5.

The BRT will be in the forward blocking state with a positive voltage applied to the anode and with a zero gate bias. The forward blocking voltage will be equal to the breakdown voltage of the open-base *pnp* transistor. A positive gate bias turns on the BRT. At low current levels, the device behaves similarly to an IGBT. When the anode current increases, the operation changes to thyristor mode resulting in a low forward

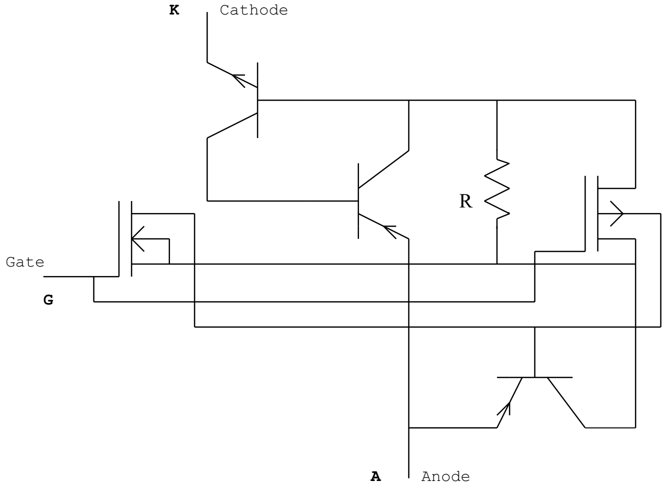


FIGURE 8.5 Equivalent circuit of base resistance-controlled thyristor (BRT).

drop. Applying a negative voltage to its gate turns off the BRT. During the turn-off process, the anode current is diverted from the N^+ emitter to the diverter. The BRT has a current tail during turn-off that is similar to an MCT or an IGBT.

8.1 MOS Turn-Off Thyristor 15

The MOS turn-off (MTO) thyristor or the MTOT is a replacement for the GTO and it requires a much smaller gate drive. It is more efficient than a GTO, it can have a maximum blocking voltage of about 9 kV, and it will be used to build power converters in the 1- to 20-MVA range. Silicon Power Corporation (SPCO) manufactures the device.

The transistor-level equivalent circuit of the MTOT (hybrid design) and the circuit symbol are shown in Fig. 8.6. Applying a current pulse at the turn-on gate (G1), as with a conventional GTO, turns on the MTOT. The turn-on action, including regeneration, is similar to a conventional SCR. Applying a positive voltage pulse to the turn-off gate (G2), as with an MCT, turns off the MTOT. The voltage pulse turns on the FET, thereby shorting the emitter and base of the *npn* transistor and breaking the regenerative action. The MTOT is a faster switch than a GTO in that it is turned off with a reduced storage time compared to a GTO. The disk-type construction allows double-side cooling.

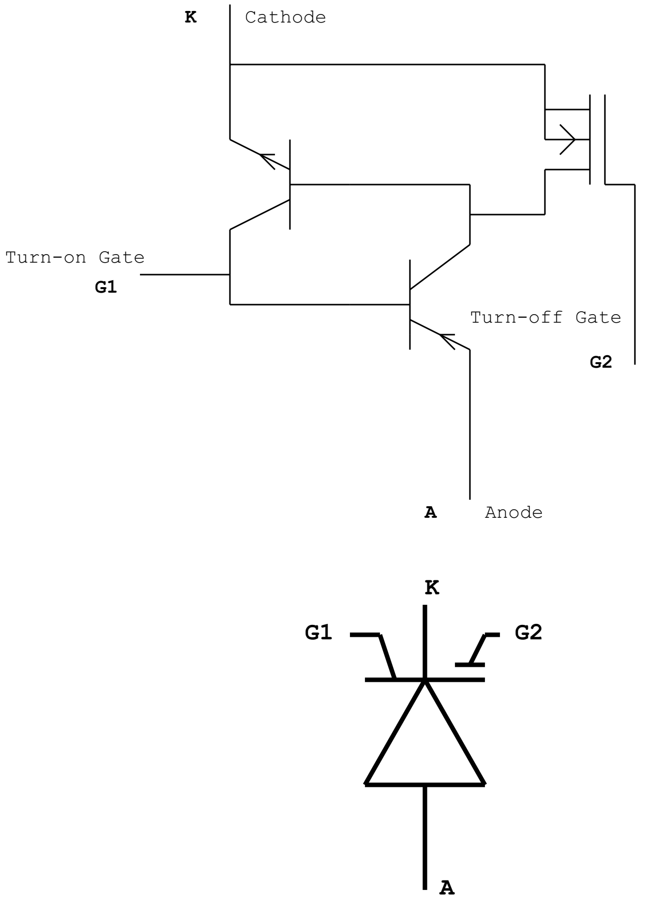


FIGURE 8.6 Equivalent circuit and symbol of a MOS turn-off (MTO) thyristor.

8.11 Applications of PMCT

The MCTs have been used in various applications, some of which are in the area of ac-dc and ac-ac conversion where the input is 60-Hz ac. Variable power factor operation was achieved using the MCTs as a force-commutated power switch [5]. The power circuit of an ac voltage controller capable of operating at a leading, lagging, and unity power factor is shown in Fig. 8.7. Because the switching frequency is low, the switching losses are negligible. Because the forward drop is low, the conduction losses are also small. The MCTs are also used in circuit breakers.

8.11.1 Soft-switching

The MCT is intended for high-frequency switching applications where it is supposed to replace a MOSFET or an IGBT. Similar to a Power MOSFET or an IGBT, the switching losses will be high at high switching frequencies. The typical characteristics of an MCT during turn-on and turn-off under hard switching (without snubber) are shown in Fig. 8.8. During turn-on and turn off, the device current and voltage take a finite time to reach their steady-state values. Each time the device changes state, there is a short period during which the voltage and current variations overlap. This results in a transient power loss that contributes to the average power loss.

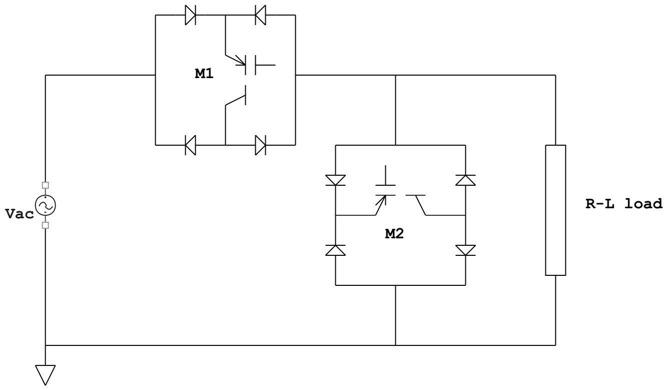
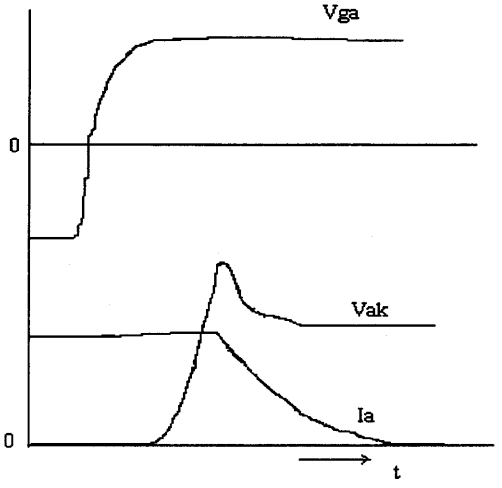
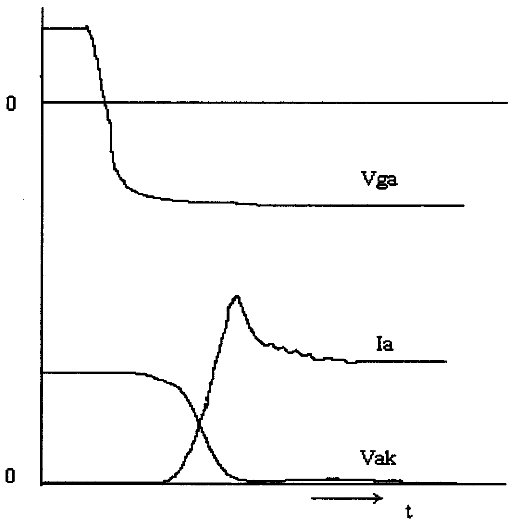


FIGURE 8.7 Power circuit of MCT ac voltage controller.



(a) Turn-off waveforms



(b) Turn-on waveforms

FIGURE 8.8 The MCT turn-off and turn-on waveforms under hard switching.

Soft-switching converters are being designed primarily to enable operation at higher switching frequencies. In these converters, the power devices switch at zero voltage or zero current, thereby eliminating the need for a large safe operating area (SOA) and at the same time eliminating the switching losses entirely. The MCT converters will outperform IGBT and power MOSFET converters in such applications by giving the highest possible efficiency. In soft-switching applications, the MCT will have only conduction loss, which is low and is close to that in a power diode with similar power ratings [12]. The Generation-1 MCTs did not turn on rapidly in the vicinity of zero anode-cathode voltage and this posed a problem in soft-switching applications of an MCT. However, Generation-2 MCTs have enhanced dynamic characteristics under zero voltage soft switching [16]. In an MCT, the PMOS On-FET together with the *pnp* transistor constitute a *p*-IGBT. An increase in the number of turn-on cells (decrease in the on-resistance of the *p*-IGBT) and an enhancement of their distribution across the MCT active area enable the MCT to turn on at a very low transient voltage allowing zero voltage switching (ZVS). During zero voltage turn-on, a bipolar device such as the MCT takes more time to establish conductivity modulation. Before the device begins to conduct fully, a voltage spike appears, thus causing a modest switching loss [12]. Reducing the tail-current amplitude and duration by proper circuit design can minimize the turn-off losses in soft-switching cases.

8.11.2 Resonant Converters

Resonant and quasi-resonant converters are known for their reduced switching loss [17]. Resonant converters with zero current switching are built using MCTs and the circuit of one such, a buck-converter, is shown in Fig. 8.9. The resonant commutating network consisting of L_r, C_r, auxiliary switch T_r, and diode D_r enables the MCT to turn off under zero current. The MCT must be turned off during the conduction period of D_Z. Commutating switch T_r must be turned off when the resonant current reaches zero.

A resonant dc link circuit with twelve parallel MCTs has been reported [18]. In this circuit, the MCTs switch at zero-voltage instants. The elimination of the switching loss allows operation at higher switching frequencies, which in turn increases the power density and offers better control of the spectral content. The use of MCTs with the same forward drop provides good current sharing.

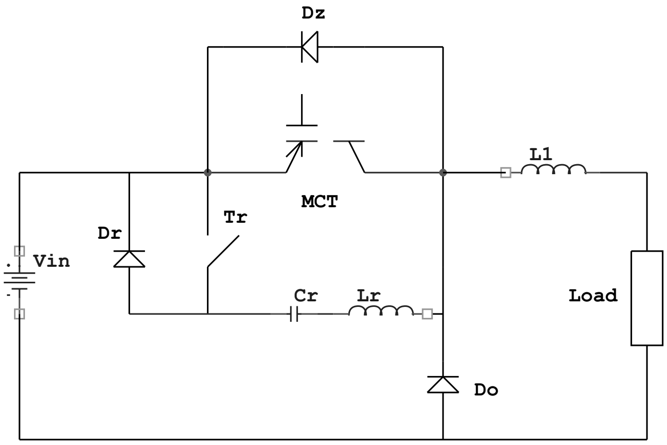


FIGURE 8.9 Power circuit of MCT resonant buck-converter.

The MCTs are also used in ac-resonant-link converters with pulse density modulation (PDM) [19]. The advantages of the PDM converter, such as zero-voltage switching, combined with those of the MCT make the PDM converter a suitable candidate for many ac-ac converter applications. In an ac-ac PDM converter, a low-frequency ac voltage is obtained by switching the high- frequency ac link at zero-crossing voltages. Two MCTs with reverse-connected diodes form a bidirectional switch that is used in the circuit. A single capacitor was used as a simple snubber for both MCTs in the bidirectional switch.

8.12 Conclusions

The MCT is a power switch with a MOS gate for turn-on and turn-off. It is derived from a thyristor by adding the features of a MOSFET. It has several advantages compared to modern devices such as the power MOSFET and the IGBT. In particular, the MCT has a low forward drop and a higher current density, which are required for high-power applications. The characteristics of Generation-2 MCTs are better than those of Generation-1 MCTs. The switching performance of Generation-2 MCTs is comparable to that of the IGBTs. However, with the development of high-speed IGBTs, it is yet to be seen which of the two devices will be dominant. Silicon Power Corporation is developing both PMCTs and NMCTs. A hybrid version of the MOS turn-off thyristor (MTOT) also is available. The data on MTOT and some preliminary data on PMCTs and NMCTs are available on the Internet.

Acknowledgment

The author is grateful to Ms. Jing He and Mr. Rahul Patil for their assistance in collecting the reference material for this chapter.

8.13 Appendix

The following is a summary of the specifications on a 600 V/150 A PMCT made by Silicon Power Corporation:

Peak Off State Voltage, V_{DRM}	−600 V
Peak Reverse Voltage, V_{RRM}	+40 V
Continuous Cathode Current, ($T = +90°C$), I_{K90}	150 A
Non-Repetitive Peak Cathode Current, I_{KSM}	5000 A
Peak Controllable Current, I_{KC}	300 A
Gate to Anode Voltage (Continuous), V_{GA}	±15 V
Gate to Anode Voltage (Peak), V_{GAM}	±20 V
Rate of Change of Voltage ($V_{GA} = 15$ V), dv/dt	10 kV/μs
Rate of Change of Current, di/dt	80 kA/μs
Peak Off-State Blocking Current (I_{DRM}) ($V_{KA} = -600$ V $V_{GA} = +15$ V, $Tc = +25°C$)	200 μA
On State Voltage (V_{TM}) ($I_K = 100$ A, $V_{GA} = -10$ V $Tc = +25°C$)	1.3 V

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9

tatic Induction Devices

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Summary

Several devices from the static induction family including static induction transistors (SIT), static induction diodes (SID), static induction thyristors, lateral punch-through transistors (LPTT), static induction transistor logic (SITL), static induction MOS transistors (SIMOS), and space charge limiting load (SCLL) are described. The theory of operation of static induction devices is given for both a current controlled by a potential barrier and a current controlled by space charge. The new concept of a punch-through emitter (PTE), which operates with majority carrier transport, is presented.

.1 Introduction

Static induction devices were invented by Nishizawa [28]. The idea was so innovative that the establishment in the solid-state electronics community at the time had difficulty understanding and accepting this discovery. Japan was the only country where static induction family devices were successfully fabricated [14]. The number of devices in this family continues to grow with time. Static induction transistors can operate with a power of 100 kW at 100 kHz or 10 W at 10 GHz. Static induction transistor logic had switching energy 100 × smaller than its I^2L competitor [8, 9]. The static induction thyristor has many advantages over the traditional SCR, and the static induction diode exhibits high switching speed, large reverse voltage, and low forward voltage drops.

.2 Theory of Static Induction Devices

The cross section of the static induction transistor is shown in Fig. 9.1, while its characteristics are shown in Fig. 9.2. An induced electrostatically potential barrier controls the current in static induction devices. The derivations of formulas will be done for an n-channel device, but the obtained results with a little modification also can be applied to p-channel devices. For a small electrical field existing in the vicinity of the potential barrier, the drift and diffusion current can be approximated by

$$J_n = -qn(x)\mu_n \frac{d\varphi(x)}{dx} + qD_n \frac{dn(x)}{dx} \tag{9.1}$$

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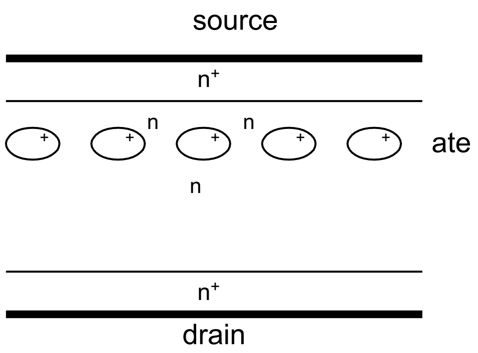


FIGURE 9.1 Cross section of the static induction transistor.

where $D_n = \mu_n V_T$ and $V_T = kT/q$. By multiplying both sides of the equation by $\exp(-\varphi(x)/V_T)$ and rearranging

$$J_n \exp\left(-\frac{\varphi(x)}{V_T}\right) = qD_n \frac{d}{dx}\left[n(x)\exp\left(-\frac{\varphi(x)}{V_T}\right)\right] \tag{9.2}$$

By integrating from x_1 to x_2, one can obtain

$$J_n = qD_n \frac{n(x_2)\exp(-\varphi(x_2)/V_T) - n(x_1)\exp(-\varphi(x_1)/V_T)}{\int_{x_1}^{x_2}\exp(-\varphi(x)/V_T)dx} \tag{9.3}$$

With the following boundary conditions

$$\begin{aligned} \varphi(x_1) &= 0; & n(x_1) &= N_S; \\ \varphi(x_2) &= V_D; & n(x_2) &= N_D; \end{aligned} \tag{9.4}$$

Equation (9.3) reduces to

$$J_n = \frac{qD_n N_S}{\int_{x_1}^{x_2}\exp(-\varphi(x)/V_T)dx} \tag{9.5}$$

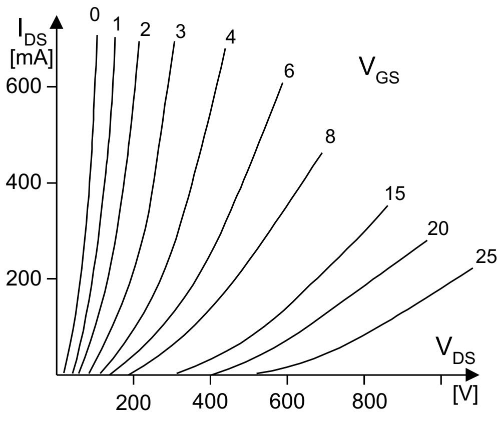


FIGURE 9.2 Characteristics of the early SIT design [7].

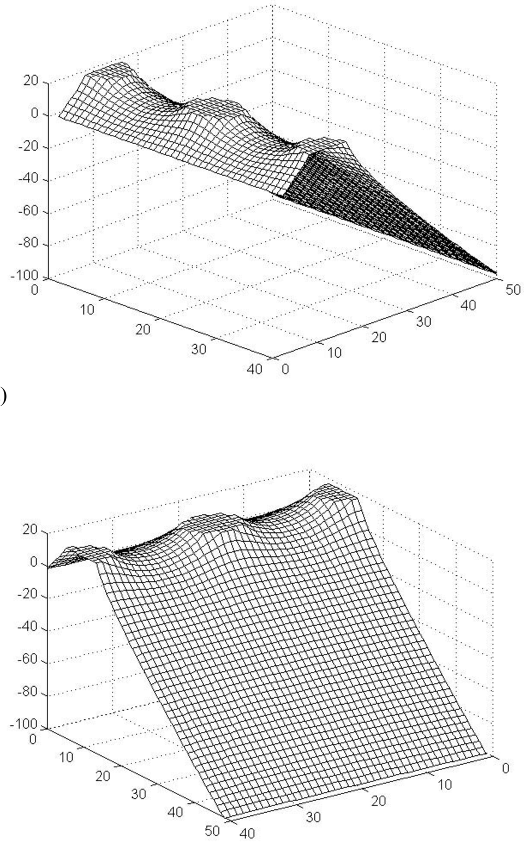
Note that the preceding equations derived for SIT also can be used to find current in any devices controlled by a potential barrier, such as a bipolar transistor or a MOS transistor operating in subthreshold mode, or in a Schottky diode.

.3 Characteristics of Static Induction Transistor

Samples of the potential distribution in SI devices are shown in Fig. 9.3 [1, 20]. The vicinity of the potential barrier was approximated by Plotka [11, 12] by using parabolic formulas (Fig. 9.4) along and across the channel.

$$\varphi(x) = \Phi\left[1 - \left(2\frac{x}{L} - 1\right)^2\right] \tag{9.6}$$

$$\varphi(y) = \Phi\left[1 - \left(2\frac{y}{W} - 1\right)^2\right] \tag{9.7}$$



(a)

(b)

FIGURE 9.3 Potential distribution in SIT: (a) view from the source side; and (b) view from the drain side.

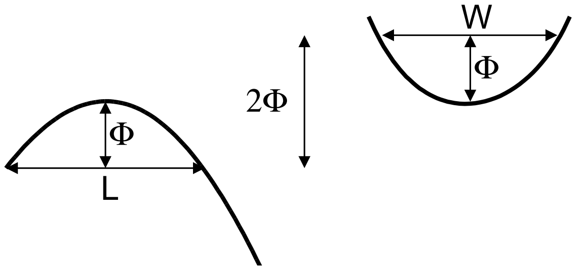


FIGURE 9.4 Potential distribution in the vicinity of the barrier approximated by parabolic shapes.

Integrating Eq. (9.5) first along the channel and then across the channel yields a very simple formula for drain currents in *n*-channel SIT transistors

$$I_D = qD_pN_SZ\frac{W}{L}\exp\left(\frac{\Phi}{V_T}\right) \tag{9.8}$$

where Φ is the potential barrier height in reference to the source potential, N_S is the electron concentration at the source, the W/L ratio describes the shape of the potential saddle in the vicinity of the barrier, and Z is the length of the source strip.

As barrier height Φ can be a linear function of gate and drain voltages,

$$I_D = qD_pN_SZ\frac{W}{L}\exp\left(\frac{a(V_{GS}+bV_{DS}+\Phi_0)}{V_T}\right) \tag{9.9}$$

Equation (9.9) describes the characteristics of a static induction transistor for small current range. For large current levels the device current is controlled by the space charge of moving carriers. In the one-dimensional (1D) case the potential distribution is described by the Poisson equation:

$$\frac{d^2\varphi}{dx_2} = -\frac{\rho(x)}{\varepsilon_{Si}\varepsilon_0} = \frac{I_{DS}}{Av(x)} \tag{9.10}$$

Where A is the effective device cross section and $v(x)$ is carrier velocity. For a small electrical field $v(x) = \mu E(x)$ and the solution of Eq. (9.10) is

$$I_{DS} = \frac{9}{8}V_{DS}^2\mu\varepsilon_{Si}\varepsilon_0\frac{A}{L^3} \tag{9.11}$$

and for a large electrical field $v(x) = \text{const}$ and Eq. (9.10) results in:

$$I_{DS} = 2V_{DS}v_{\text{sat}}\varepsilon_{Si}\varepsilon_0\frac{A}{L^2} \tag{9.12}$$

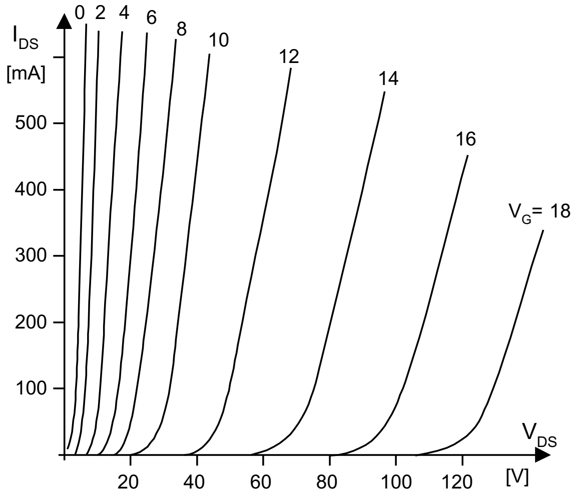


FIGURE 9.5 Characteristics of the static induction transistor drawn in linear scale.

where L is the channel length and $v_{\text{sat}} \approx 10^{11}$ μm/s is the carrier saturation velocity. In practical devices the current-voltage relationship is described by an exponential relationship Eq. (9.9) for small currents, a quadratic relationship eq. (9.11), and, finally, for large voltages by an almost linear relationship Eq. (9.12). The SIT characteristics drawn in linear and logarithmic scales are shown in Fig. 9.5 and Fig. 9.6, respectively.

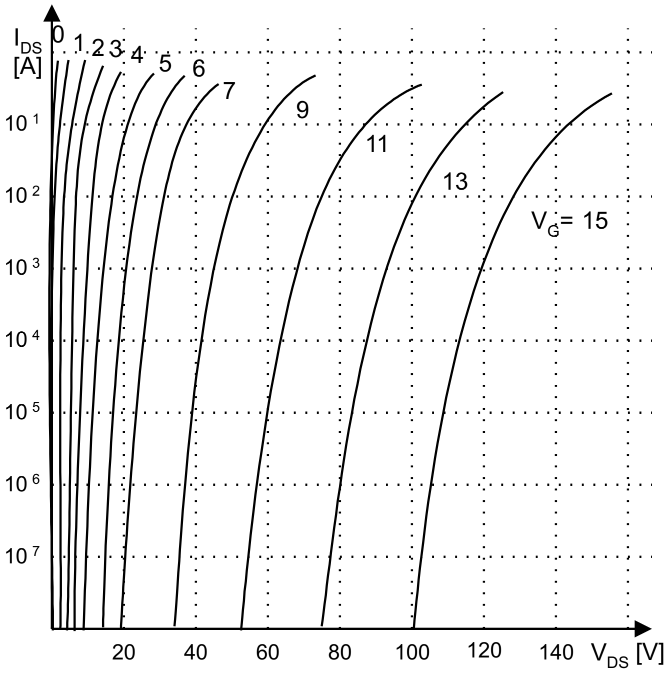


FIGURE 9.6 Characteristics of the static induction transistor drawn in logarithmic scale.

.4 Bipolar Mode Operation of SI devices BSIT

The bipolar mode of operation of SIT was first reported in 1976 by Nishizawa and Wilamowski [8, 9]. Several complex theories for the bipolar mode of operation were developed [2, 5, 6, 10, 23, 24], but actually the simple Eq. (9.5) works well not only for the typical mode of the SIT operation, but also for the bipolar mode of the SIT operation. Furthermore, the same formula works very well for classical bipolar transistors. Typical characteristics of the SI transistor operating in both normal and bipolar modes are shown in Figs. 9.7 and Fig. 9.8.

A potential barrier controls the current in the SIT and it is given by

$$J_n = \frac{qD_nN_S}{\int_{x_1}^{x_2} \exp(-\varphi(x)/V_T)dx} \tag{9.13}$$

where $\varphi(x)$ is the profile of the potential barrier along the channel.

For example, in the case of *npn* bipolar transistors the potential distribution across the base in reference to emitter potential at the reference impurity level $N_E = N_S$ is described by:

$$\varphi(x) = V_T \ln\left(\frac{N_B(x)N_S}{n_i^2}\right) \exp\left(-\frac{V_{BE}}{V_T}\right) \tag{9.14}$$

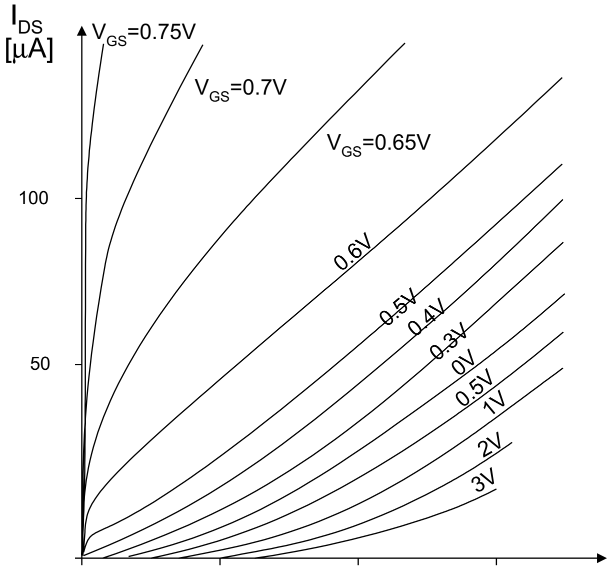


FIGURE 9.7 Small-sized SIT transistor characteristic, operating in both normal and bipolar modes, $I_D = f(V_{DS})$ with V_{GS} as parameter.

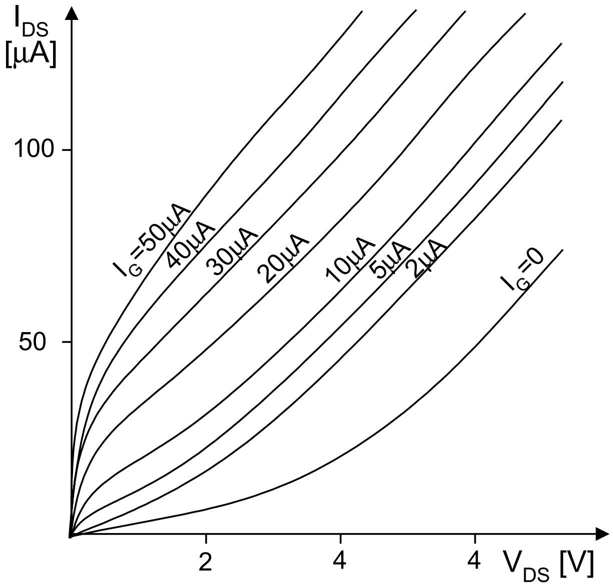


FIGURE 9.8 Small-sized SIT transistor characteristic, operating in both normal and bipolar modes, $I_D = f(V_{DS})$ with I_G as a parameter.

After inserting Eq. (9.14) into (9.13) one can obtain the well-known equation for electron current injected into the base

$$J_n = \frac{qD_nn_i^2}{\int_{x_1}^{x_2} N_B(x)dx} \exp\left(\frac{V_{BE}}{V_T}\right) \tag{9.15}$$

If Eq. (9.13) is valid for SIT and BJT then one may assume that it is also valid for the bipolar mode of operation of the SIT transistor. This is a well-known equation for the collector current in the bipolar transistor, but this time it was derived using the concept of current flow through a potential barrier.

.5 Emitters for Static Induction Devices

One of the disadvantages of the SIT is the relatively flat shape of the potential barrier (Fig. 9.9a). This leads to slow, diffusion-based transport of carriers in the vicinity of the potential barrier. The carrier transit time can be estimated using the formula:

$$t_{\text{transit}} = \frac{l_{\text{eff}}^2}{D} \tag{9.16}$$

where l_{eff} is the effective length of the channel and $D = \mu V_T$ is the diffusion constant. In the case of a traditional SIT transistor this channel length is $\approx 2\,\mu\text{m}$, while in the case of SIT transistors with sharper barriers (Fig. 9.9b) the channel length is reduced to about $\approx 0.2\,\mu\text{m}$. The corresponding transient times are 2 ns and 20 ps respectively.

The potential distributions shown in Fig. 9.3 are valid for SIT with an emitter made of a traditional *p-n* junction. A

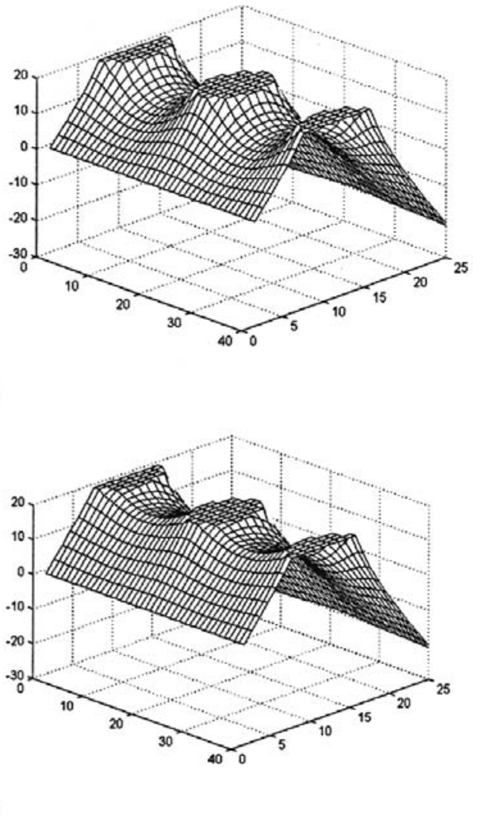


FIGURE 9.9 Potential distributions in SIT: (a) traditional; and (b) with sharp potential barrier.

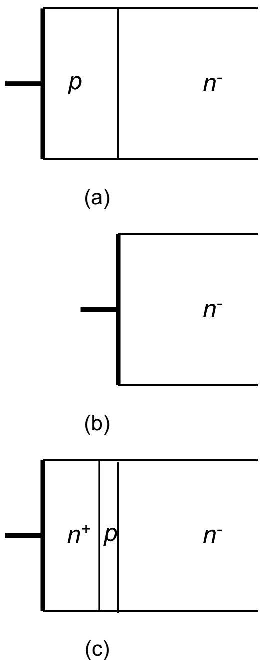


FIGURE 9.10 Various structures of emitters: (a) *p*-*n* junction including heterostructure with SiGe materials; (b) Schottky junction; and (c) punch-through emitter (in normal operational condition the *p* region is depleted from carriers).

much narrower potential barrier can be obtained when other types of emitter are used. There are two well-known emitters: (1) *p*-*n* junction (Fig. 9.10a); and (2) Schottky junction (Fig. 9.10b). For silicon devices *p*-*n* junctions have a forward voltage drop of 0.7–0.8 V while Schottky emitters have 0.2–0.3 V only. As the Schottky diode is a majority carrier device, carrier storage effect is negligible.

Another interesting emitter structure is shown in Fig. 9.10c. This emitter has all the advantages of the Schottky diode even though it is fabricated out of *p*-*n* junctions.

The concept of static induction devices can be used independently of the type of emitter shown in Fig. 9.10. With Schottky type and punch-through type emitters the potential barrier is much narrower and this results in faster response time and larger current gain in the bipolar mode of operation.

.6 Static Induction Diode SID

The bipolar mode of operation of SIT also can be used to obtain diodes with low forward voltage drop and negligible carrier storage effect [2, 5, 13, 23, 24]. A static induction diode can be obtained by shorting a gate to the emitter of the static induction transistor. Such a diode has all the advantages of a static induction transistor such as thermal stability and short switching time. The cross section of such a diode is shown in Fig. 9.11.

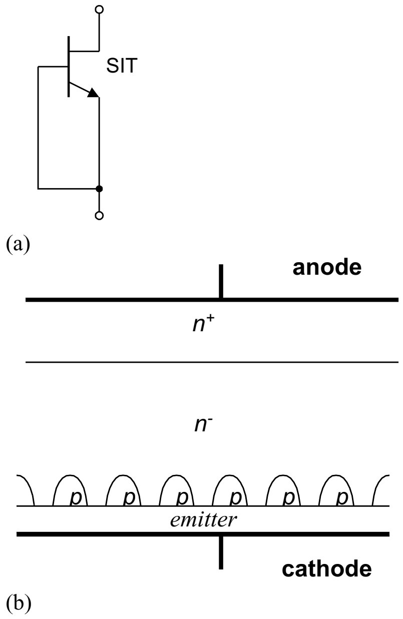


FIGURE 9.11 Static induction diode: (a) circuit diagram; and (b) cross section.

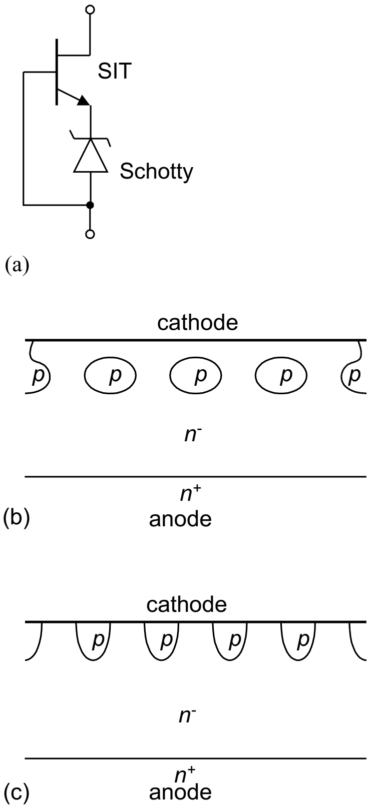


FIGURE 9.12 Schottky diode with enlarged breakdown voltages: (a) circuit diagram; and (b) and (c) two cross-sections of possible implementation.

The quality of the static induction diode can be further improved with more sophisticated emitters (Fig. 9.10b,c). The SI diode with Schottky emitter was described by Wilamowski in 1983 [17] (Fig. 9.12). A similar structure was later described by Baliga [1].

.7 Lateral Punch-Through Transistor LPTT

Fabrications of SI transistors usually require very sophisticated technology. It is much simpler to fabricate a lateral punch-through transistor, which operates on the same principle and has similar characteristics [15]. The LPTT cross section is shown in Fig. 9.13 and its characteristics are shown in Fig. 9.14.

.8 Static Induction Transistor Logic SITL

The static induction transistor logic (SITL) was proposed by Nishizawa and Wilamowski [8, 9]. This logic circuit has almost 100 times better power-delay product than its I^2L competitor. Such a great improvement of the power-delay product is possible because the SITL structure has a significantly smaller junction parasitic capacitance and voltage swing is reduced. Figures 9.15 and 9.16 illustrate the concept of SITL. Measured characteristics of the *n*-channel transistor of the static induction logic are shown in Fig. 9.17.

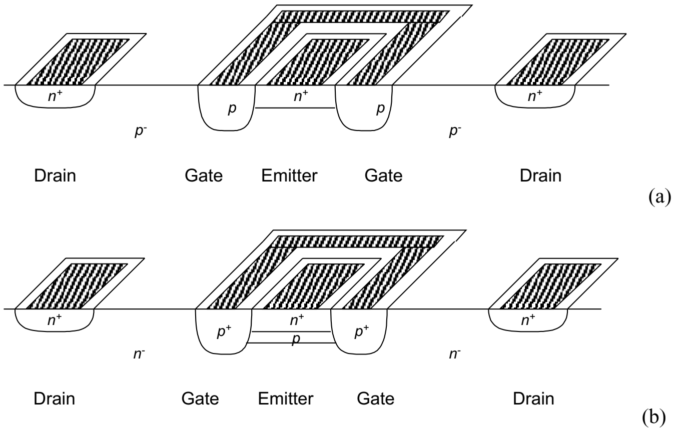


FIGURE 9.13 Structures of the lateral punch-through transistors: (a) simple; and (b) with sharper potential barrier.

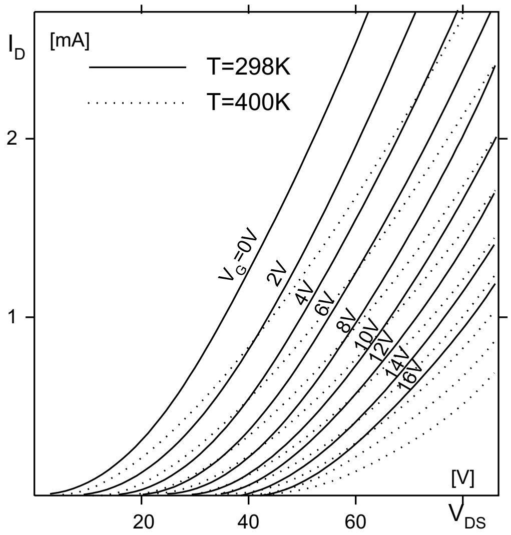


FIGURE 9.14 Characteristics of lateral punch-through transistor.

. BJT Saturation Protected by SIT

The SI transistor also can be used instead of a Schottky diode to protect a bipolar junction transistor against saturation [20]. This leads to faster switching time. The concept is shown in Figs. 9.18 and 9.19. Note that this approach is advantageous to the solution with Schottky diode because it does not require additional area on a chip and does not introduce additional capacitance between the base and the collector. The base

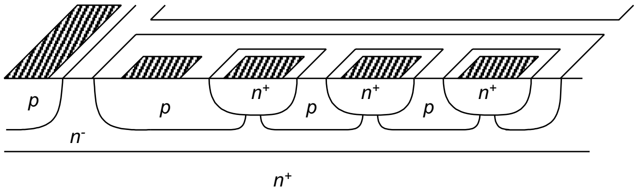


FIGURE 9.15 Cross section of SIT logic.

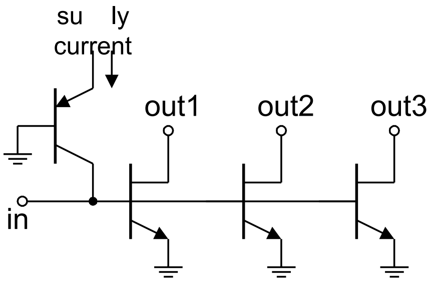

supply current
out1
out2
out3
in

FIGURE 9.16 Diagram of SIT logic.

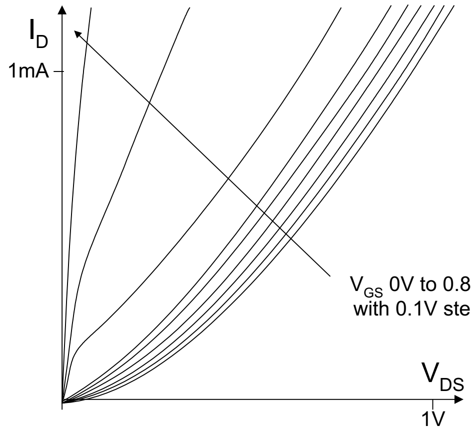


FIGURE 9.17 Measured characteristic of an n-channel transistor of the logic circuit of Fig. 9.16.

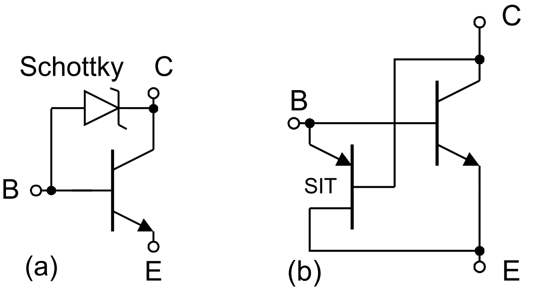

Schottky
C
B
E
(a)
C
B
SIT
E
(b)

FIGURE 9.18 Protection of a bipolar transistor against deep saturation: (a) using a Schottky diode; and (b) using SIT.

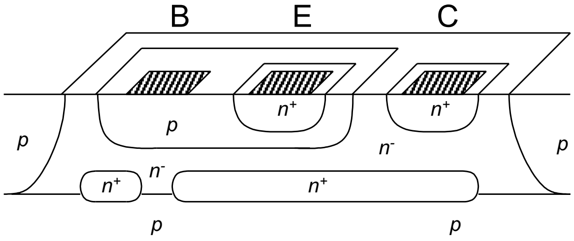

B
E
C
n+
n+
p
p
n-
p
n-
n+
n+
p
p

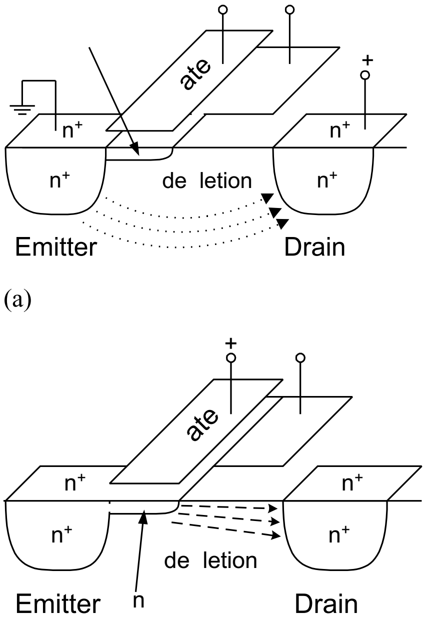
FIGURE 9.19 Cross sections of bipolar transistors protected against deep saturation using SIT.

collector capacitance is always enlarged by the Miller effect and this leads to slower switching in the case of the solution with the Schottky diode.

.1 Static Induction MOS Transistor SIMOS

The punch-through transistor with MOS controlled gate was described in 1983 [18, 9]. In the structure in Fig. 9.20a current can flow in a similar fashion as in the lateral punch-through transistor [15]. In this mode of operation, carriers are moving far from the surface with a velocity close to saturation. The real advantage of such a structure is the very low gate capacitance.

Another implementation of SIMOS is shown in Fig. 9.21. The buried p^+-layer is connected to the substrate, which has a


(a)

(b)
gate
+
n+
n+
n+
depletion
n+
Emitter
Drain
+
gate
n+
n+
n+
depletion
n+
Emitter
n
Drain

FIGURE 9.20 MOS-controlled punch-through transistor: (a) transistor in the punch-through mode for the negative gate potential; and (b) transistor in the on-state for the positive gate potential.

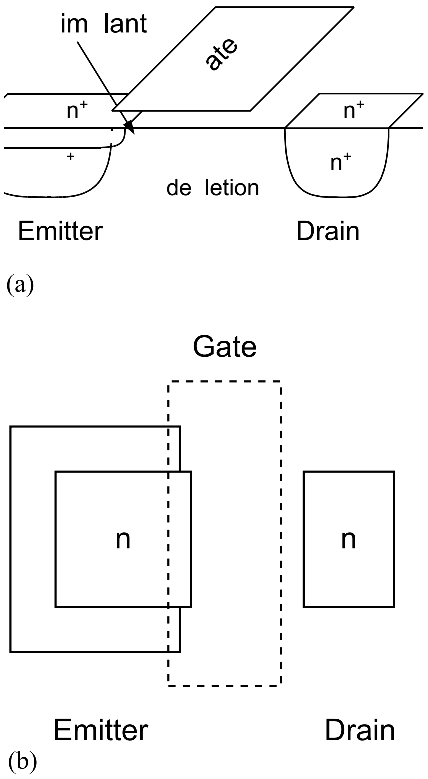


FIGURE 9.21 Static induction MOS structure: (a) cross section; and (b) top view.

large negative potential. As a result the potential barrier is high and the emitter-drain current cannot flow. The punch-through current may start to flow when the positive voltage is applied to the gate and in this way the potential barrier is lowered. The *p*-implant layer is depleted and due to the high horizontal electrical field under the gate there is no charge accumulation under this gate. Such a transistor has several advantages over the traditional MOS are:

1. The gate capacitance is very small because there is no accumulation layer under the gate;
2. carriers are moving with a velocity close to saturation velocity; and
3. much lower substrate doping and the existing depletion layer lead to much smaller drain capacitance.

The device operates in a similar fashion as the MOS transistor in subthreshold conditions, but this process occurs at much higher current levels. Such a "bipolar mode" of operation may have many advantages in VLSI applications.

.11 Space-Charge Limiting Load SCLL

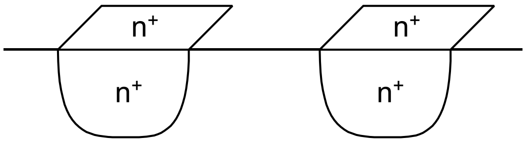


FIGURE 9.22 Space-charge limiting load (SCLL).

Using the concept of the space-charge limited current flow (see Fig. 9.22), it is possible to fabricate very large resistors on a very small area. Moreover, these resistors have a very small parasitic capacitance. The 50-kΩ resistor requires only several square μm using 2-μm technology [22].

Depending upon the value of the electric field, the device current is described by the following two equations. For a small electrical field $v(x) = \mu E(x)$

$$I_{DS} = \frac{9}{8} V_{DS}^2 \mu \varepsilon_{Si} \varepsilon_0 \frac{A}{L^3} \tag{9.17}$$

and for a large electrical field $v(x) = \text{const}$,

$$I_{DS} = 2 V_{DS} v_{\text{sat}} \varepsilon_{Si} \varepsilon_0 \frac{A}{L^2} \tag{9.18}$$

Moreover, these resistors, which are based on the space-charge limit flow, have a very small parasitic capacitance.

.12 Power MOS Transistors

Power MOS transistors are being used for fast switching power supplies and for switching power converters. They can be driven with relatively small power and switching frequencies could be very high. High switching frequencies lead to compact circuit implementations with small inductors and small capacitances. Basically only two technologies (VMOS and DMOS) are used for power MOS devices as shown in Figs. 9.23 and 9.24, respectively.

A more popular structure is the DMOS shown in Fig. 9.24. This structure also uses the static induction transistor concept. Note that for large drain voltages the *n*-region is depleted from carriers and the statically induced electrical field in the vicinity of the virtual drain is significantly reduced. As a result, this transistor may withstand much larger drain voltages and the effect of channel length modulation also is significantly reduced. The latter effect leads to larger output resistances of the transistor. Therefore, the drain current is less sensitive to

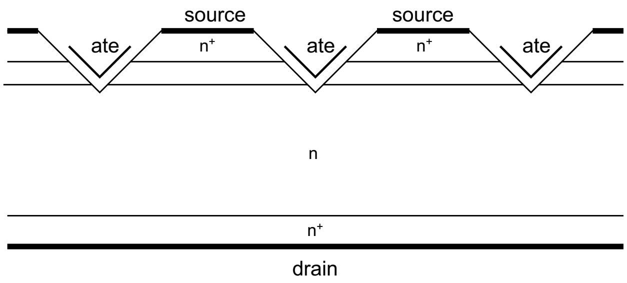


FIGURE 9.23 Cross section of the VMOS transistor.

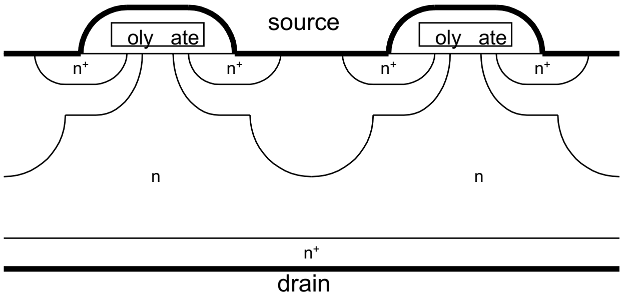


FIGURE 9.24 Cross section of the DMOS transistor.

drain voltage variations. The structure in Fig. 9.24 can be considered as a composite of the MOS transistor and the SIT transistor as it is shown in Fig. 9.25.

The major disadvantage of power MOS transistors is their relatively large drain series resistance and much smaller transconductance in comparison to bipolar transistors. Both of these parameters can be improved dramatically by a simple change of the type of drain. In the case of an n-channel device, this change would be from an n-type to a p-type. This way, the integrated structure being built has a diagram of a MOS transistor integrated with a bipolar transistor. Such a structure has β times larger transconductance (β is the current gain of a bipolar transistor) and much smaller series resistance due to the conductivity modulation effect caused by holes injected into the lightly doped drain region. Such devices are known as insulated gate bipolar transistors (IGBT) as shown in Fig. 9.26. Their main disadvantage is that of large switching time limited primarily by the poor switching performance of the bipolar transistor. Another difficulty is related to a possible latch-up action of four layer $n^{+}pn^{-}p^{+}$-structure. This undesirable effect could be suppressed by using a heavily doped p^{+}-region in the base of the npn structure, which leads to significant reduction of the current gain of this parasitic transistor. The gain of the pnp transistor must be kept large so that the transconductance of the entire device is also large. The IGBTs have breakdown voltages of up to 1500 V and turn-off times in the range of 0.1 to 0.5 µs. They may operate with currents >100 A with a forward voltage drop of ≈3 V.

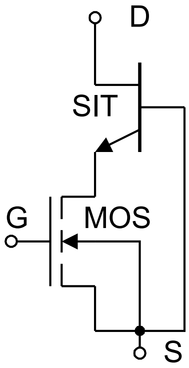


FIGURE 9.25 Equivalent diagram with MOS and SI transistors of the structure of Fig. 9.24.

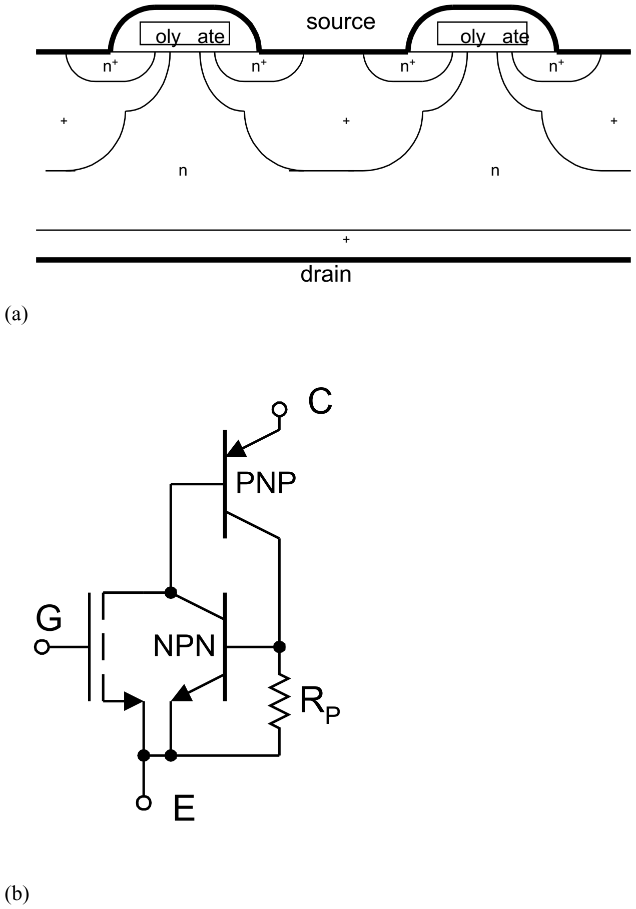


FIGURE 9.26 Insulated gate bipolar transistor (IGBT): (a) cross section; and (b) equivalent diagram.

.13 Static Induction Thyristor

There are several special semiconductor devices dedicated to high-power applications. The most popular is a thyristor known as the silicon control rectifier (SCR). This device has a four-layer structure (Fig 9.27a) and it can be considered as two transistors npn and pnp connected as shown in Fig. 9.27b.

In a normal mode of operation (the anode has positive potential) only one junction is reverse biased and it can be represented by capacitance C. A spike of anode voltage can therefore get through capacitor C and it can trigger SRC. This behavior is not acceptable in practical application and therefore as Fig. 9.28 shows a different device structure is being used. Note that shorting the gate to the cathode by resistor R makes it much more difficult to trigger the npn transistor by spike of anode voltage. This way, rapid anode voltage changes are not able to trigger a thyristor. Therefore, this structure has a very large dV/dt parameter. At the same time, much energy

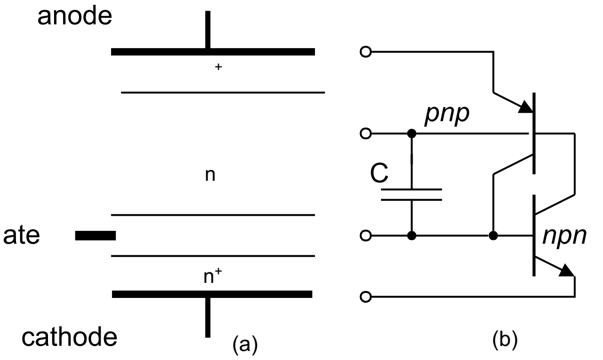


FIGURE 9.27 Silicon control rectifier (SCR): (a) cross section; and (b) equivalent diagram.

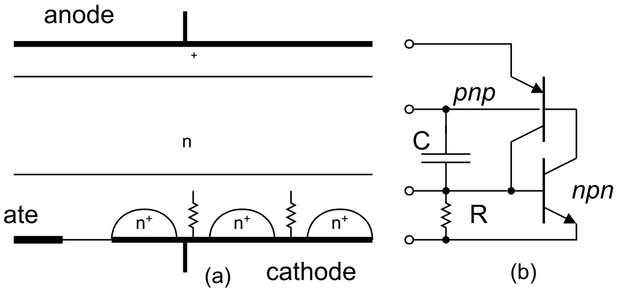


FIGURE 9.28 Silicon control rectifier (SCR) with larger dV/dt parameter: (a) cross section; and (b) equivalent diagram.

is required to trigger the thyristor with the gate signal, which is an undesirable effect and switching on time (described by the di/dt parameter) is lengthy.

Most of the SCRs sold on the market consist of an integrated structure composed of two or more thyristors. This structure has both large dV/dt and di/dt parameters. This structure consists of an internal thyristor, which significantly amplifies the gate signal.

One can notice that the classical thyristor as shown in Fig. 9.27 can be turned off by the gate voltage while the integrated SCR shown in Fig. 9.29 can only be turned off by reducing anode current to zero. Most of the SCRs sold on the market have an integrated structure composed of two or more thyristors. This structure has both large dV/dt and di/dt parameters.

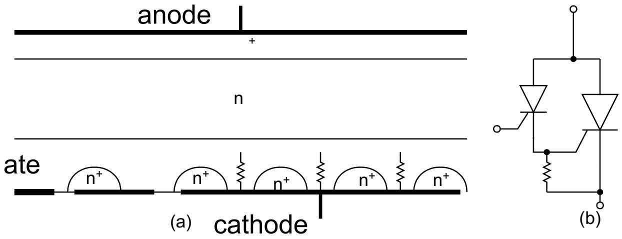


FIGURE 9.29 Integrated structure of silicon control rectifier: (a) cross section; and (b) equivalent diagram.

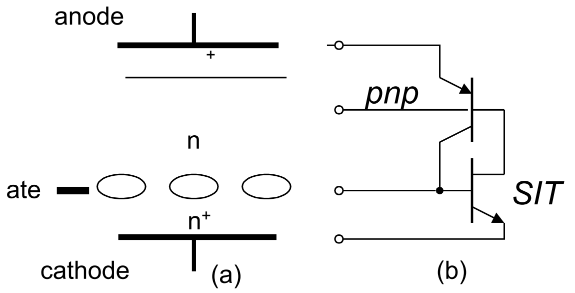


FIGURE 9.30 The GTO SITh: (a) cross section; and (b) equivalent diagram.

.14 Gate Turn-Off Thyristor GTO

For dc operation it is important to have a thyristor that can be turned off by the gate voltage. Such a thyristor has a structure similar to that shown in Fig. 9.27. It is important, however, to have significantly different current gains β for *pnp* and *npn* transistors. The current gain of an *npn* transistor should be as large as possible and the current gain of a *pnp* transistor should be small. The product of β_{npn} and β_{pnp} should be larger than unity. This can be easily implemented using the SI structure as shown in Fig. 9.30.

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10

Diode Rectifiers

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10.1 Introduction

This chapter is concerned with the application and design of diode rectifier circuits. It covers single-phase, three-phase, poly-phase and high-frequency rectifier circuits [1, 2]. The objectives of this chapter are:

- To enable readers to understand the operation of typical rectifier circuits.
- To enable readers to appreciate the different qualities of rectifiers required for different applications.
- To enable the reader to design practical rectifier circuits.

The high-frequency rectifier waveforms given are obtained from PSpice simulations, [3–5] which take into account the secondary effects of stray and parasitic components. In this way, these waveforms will closely resemble real waveforms. These waveforms are particularly useful to help designers determine the practical voltage, current, and other ratings of high-frequency rectifiers.

10.2 Single-Phase Diode Rectifiers

There are two types of single-phase diode rectifier that convert a single-phase ac supply into a dc voltage, namely, single-phase half-wave rectifiers and single-phase full-wave rectifiers. In the following subsections, the operations of these rectifier circuits are examined and their performances are analyzed and compared in tabular form. For the sake of simplicity the diodes are considered to be ideal, that is, they have zero forward voltage drop and reverse recovery time. This assumption is generally valid for the case of diode rectifiers that use the mains, a low-frequency source, as the input, and when the forward voltage drop is small compared with the peak voltage of the mains. Furthermore, it is assumed that the load is purely resistive such that load voltage and load current have similar waveforms. In Section 10.5 the effects of both inductive and capacitive load on a diode rectifier are considered in detail.

10.2.1 Single-Phase Half-Wave Rectifiers

The simplest single-phase diode rectifier is the single-phase half-wave rectifier. A single-phase half-wave rectifier with resistive load is shown in Fig. 10.1. The circuit consists of only one diode that is usually fed with a transformer secondary as shown. During the positive half-cycle of the transformer secondary voltage, diode D conducts. During the negative half-cycle, diode D stops conducting. Assuming that the transformer has zero internal impedance and provides perfect sinusoidal voltage on its secondary winding, the voltage and

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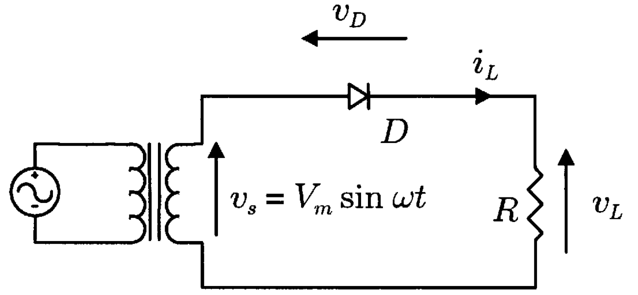

FIGURE 10.1 A single-phase half-wave rectifier with resistive load.

current waveforms of resistive load R and the voltage waveform of diode D are shown in Fig. 10.2.

By observing the voltage waveform of diode D in Fig. 10.2, it is clear that the peak inverse voltage (PIV) of diode D is equal to V_m during the negative half-cycle of the transformer secondary voltage. Hence the *Peak Repetitive Reverse Voltage* (V_{RRM}) rating of diode D must be chosen to be higher than V_m to avoid reverse breakdown. In the positive half-cycle of the transformer secondary voltage, diode D has a forward current which is equal to the load current and, therefore, the *Peak Repetitive Forward Current* (I_{FRM}) rating of diode D must be chosen to be higher than the peak load current V_m/R, in practice. In addition, the transformer has to carry a dc current that may result in a dc saturation problem of the transformer core.

1 .2.2 Single-Phase Full-Wave Rectifiers

There are two types of single-phase full-wave rectifier, namely, full-wave rectifiers with center-tapped transformer and bridge rectifiers. A full-wave rectifier with a center-tapped transformer is shown in Fig. 10.3. It is clear that each diode, together with the associated half of the transformer, acts as a half-wave rectifier. The outputs of the two half-wave rectifiers are combined to produce full-wave rectification in the load. As far as the transformer is concerned, the dc currents of the two half-wave rectifiers are equal and opposite, such that there is no dc current for creating a transformer core saturation problem. The voltage and current waveforms of the full-wave rectifier are shown in Fig. 10.4. By observing diode

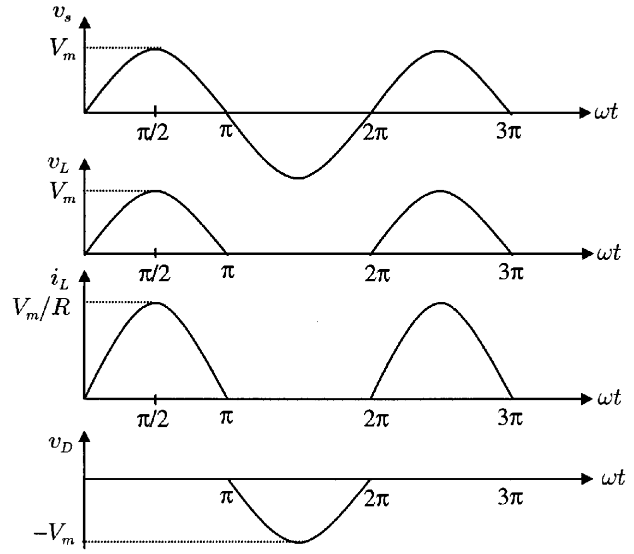

FIGURE 10.2 Voltage and current waveforms of the half-wave rectifier with resistive load.

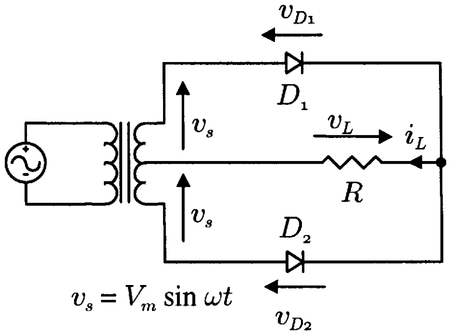

FIGURE 10.3 Full-wave rectifier with center-tapped transformer.

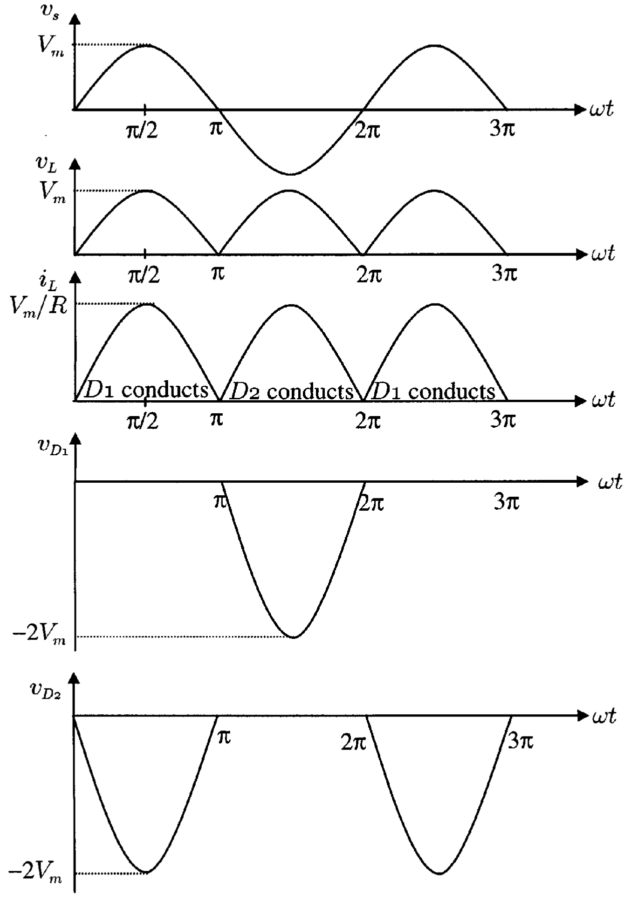

FIGURE 10.4 Voltage and current waveforms of the full-wave rectifier with center-tapped transformer.

voltage waveforms v_{D1} and v_{D2} in Fig. 10.4, it is clear that the peak inverse voltage (PIV) of the diodes is equal to $2V_m$ during their blocking state. Hence the *Peak Repetitive Reverse Voltage* (V_{RRM}) rating of the diodes must be chosen to be higher than $2V_m$ to avoid reverse breakdown. (Note that, compared with the half-wave rectifier shown in Fig. 10.1, the full-wave rectifier has twice the dc output voltage, as shown in Section 10.2.4.) During its conducting state, each diode has a forward current that is equal to the load current and, therefore, the *Peak Repetitive Forward Current* (I_{FRM}) rating of these diodes must be chosen to be higher than the peak load current V_m/R in practice.

Employing four diodes instead of two, a bridge rectifier as shown in Fig. 10.5 can provide full-wave rectification without using a center-tapped transformer. During the positive half-cycle of the transformer secondary voltage, the current flows to the load through diodes $D1$ and $D2$. During the negative half cycle, $D3$ and $D4$ conduct. The voltage and current waveforms of the bridge rectifier are shown in Fig. 10.6. As with the full-wave rectifier with center-tapped transformer, the *Peak Repetitive Forward Current* (I_{FRM}) rating of the employed diodes must be chosen to be higher than the peak load current V_m/R. However, the peak inverse voltage (PIV) of the diodes is reduced from $2V_m$ to V_m during their blocking state.

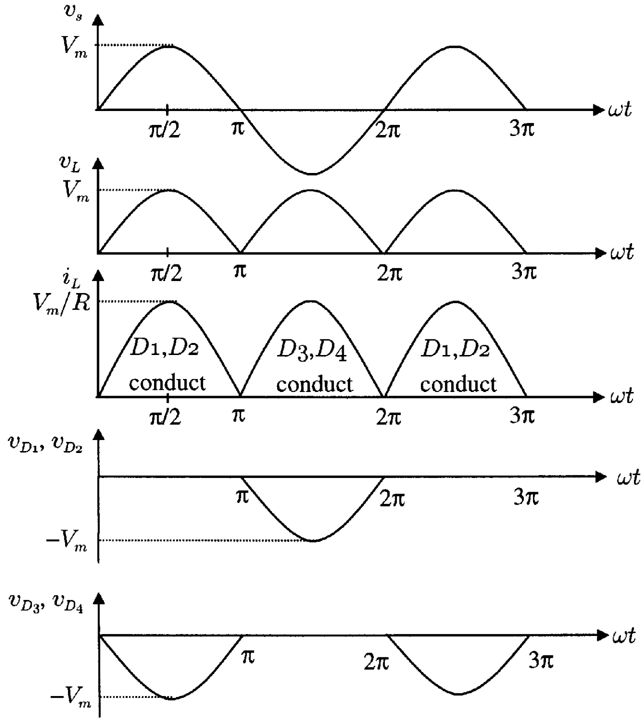

FIGURE 10.6 Voltage and current waveforms of the bridge rectifier.

10.2.3 Performance Parameters

In this section the performance of the rectifiers mentioned in the preceding will be evaluated in terms of the following parameters.

10.2.3.1 Voltage Relationships

The average value of the load voltage v_L is V_{dc} and it is defined as

$$V_{\text{dc}} = \frac{1}{T}\int_0^T v_L(t)dt \tag{10.1}$$

In the case of a half-wave rectifier, Fig. 10.2 indicates that load voltage $v_L(t) = 0$ for the negative half-cycle. Note that the angular frequency of the source $\omega = 2\pi/T$, and Eq. (10.1) can be rewritten as

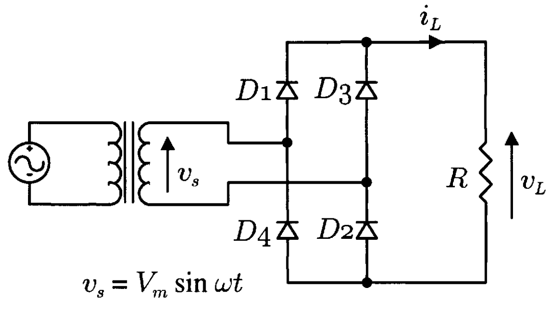

FIGURE 10.5 Bridge rectifier.

$$V_{\text{dc}} = \frac{1}{2\pi}\int_0^{\pi} V_m \sin \omega t d(\omega t) \tag{10.2}$$

Therefore,

$$\text{Half-wave } V_{\text{dc}} = \frac{V_m}{\pi} = 0.318\, V_m \tag{10.3}$$

In the case of a full-wave rectifier, Figs. 10.4 and 10.6 indicate that $v_L(t) = V_m|\sin \omega t|$ for both the positive and negative half-cycles. Hence Eq. (10.1) can be rewritten as

$$V_{\text{dc}} = \frac{1}{\pi}\int_0^{\pi} V_m \sin \omega t \, d(\omega t) \tag{10.4}$$

Therefore,

$$\text{Full-wave } V_{\text{dc}} = \frac{2V_m}{\pi} = 0.636\, V_m \tag{10.5}$$

The root-mean-square (rms) value of load voltage v_L is V_L, which is defined as

$$V_L = \left[\frac{1}{T}\int_0^T v_L^2(t)dt\right]^{1/2} \tag{10.6}$$

In the case of a half-wave rectifier, $v_L(t) = 0$ for the negative half-cycle, therefore, Eq. (10.6) can be rewritten as

$$V_L = \sqrt{\frac{1}{2\pi}\int_0^{\pi}(V_m \sin \omega t)^2 d(\omega t)} \tag{10.7}$$

or

$$\text{Half-wave } V_L = \frac{V_m}{2} = 0.5\ V_m \tag{10.8}$$

In the case of a full-wave rectifier, $v_L(t) = V_m|\sin \omega t|$ for both the positive and negative half-cycles. Hence, Eq. (10.6) can be rewritten as

$$V_L = \sqrt{\frac{1}{\pi}\int_0^{\pi}(V_m \sin \omega t)^2 d(\omega t)} \tag{10.9}$$

or

$$\text{Full-wave } V_L = \frac{V_m}{\sqrt{2}} = 0.707\ V_m \tag{10.10}$$

The result of Eq. (10.10) is as expected because the rms value of a full-wave rectified voltage should be equal to that of the original ac voltage.

1 .2.3.2 Current Relationships

The average value of load current i_L is I_{dc} and because load R is purely resistive it can be found as

$$I_{\text{dc}} = \frac{V_{\text{dc}}}{R} \tag{10.11}$$

The root-mean-square (rms) value of load current i_L is I_L and it can be found as

$$I_L = \frac{V_L}{R} \tag{10.12}$$

In the case of a half-wave rectifier, from Eq. (10.3)

$$\text{Half-wave } I_{\text{dc}} = \frac{0.318\ V_m}{R} \tag{10.13}$$

and from Eq. (10.8)

$$\text{Half-wave} = I_L = \frac{0.5\ V_m}{R} \tag{10.14}$$

In the case of a full-wave rectifier, from Eq. (10.5)

$$\text{Full-wave } I_{\text{dc}} = \frac{0.636\ V_m}{R} \tag{10.15}$$

and from Eq. (10.10)

$$\text{Full-wave } I_L = \frac{0.707\ V_m}{R} \tag{10.16}$$

1 .2.3.3 Rectification Ratio

The rectification ratio, which is a figure of merit for comparing the effectiveness of rectification, is defined as

$$\sigma = \frac{P_{\text{dc}}}{P_L} = \frac{V_{\text{dc}} I_{\text{dc}}}{V_L I_L} \tag{10.17}$$

In the case of a half-wave diode rectifier, the rectification ratio can be determined by substituting Eqs. (10.3), (10.13), (10.8), and (10.14) into Eq. (10.17).

$$\text{Half-wave } \sigma = \frac{(0.318\ V_m)^2}{(0.5\ V_m)^2} = 40.5\% \tag{10.18}$$

In the case of a full-wave rectifier, the rectification ratio is obtained by substituting Eq. (10.5), (10.15), (10.10), and (10.16) into Eq. (10.17).

$$\text{Full-wave } \sigma = \frac{(0.636\ V_m)^2}{(0.707\ V_m)^2} = 81\% \tag{10.19}$$

1 .2.3.4 orm actor

The form factor (FF) is defined as the ratio of the root-mean-square value (heating component) of a voltage or current to its average value,

$$\text{FF} = \frac{V_L}{V_{\text{dc}}} \quad \text{or} \quad \frac{I_L}{I_{\text{dc}}} \tag{10.20}$$

In the case of a half-wave rectifier, the FF can be found by substituting Eqs. (10.8) and (10.3) into Eq. (10.20)

$$\text{Half-wave FF} = \frac{0.5\ V_m}{0.318\ V_m} = 1.57 \tag{10.21}$$

In the case of a full-wave rectifier, the FF can be found by substituting Eqs. (10.16) and (10.15) into Eq. (10.20)

$$\text{Full-wave FF} = \frac{0.707\ V_m}{0.636\ V_m} = 1.11 \tag{10.22}$$

1 .2.3.5 Ripple actor

The ripple factor (RF), which is a measure of the ripple content, is defined as

$$\text{RF} = \frac{V_{\text{ac}}}{V_{\text{dc}}} \tag{10.23}$$

where V_{ac} is the effective (rms) value of the ac component of load voltage v_L,

$$V_{\text{ac}} = \sqrt{V_L^2 - V_{\text{dc}}^2} \tag{10.24}$$

Substituting Eq. (10.24) into Eq. (10.23), the ripple factor can be expressed as

$$\text{RF} = \sqrt{\left(\frac{V_L}{V_{\text{dc}}}\right)^2 - 1} = \sqrt{\text{FF}^2 - 1} \tag{10.25}$$

In the case of a half-wave rectifier,

$$\text{Half-wave RF} = \sqrt{1.57^2 - 1} = 1.21 \tag{10.26}$$

In the case of a full-wave rectifier,

$$\text{Full-wave RF} = \sqrt{1.11^2 - 1} = 0.482 \tag{10.27}$$

1 .2.3.6 Transformer Utilization Factor

The transformer utilization factor (TUF), which is a measure of the merit of a rectifier circuit, is defined as the ratio of the dc output power to the transformer volt-ampere (VA) rating required by the secondary winding,

$$\text{TUF} = \frac{P_{\text{dc}}}{V_s I_s} = \frac{V_{\text{dc}} I_{\text{dc}}}{V_s I_s} \tag{10.28}$$

where V_s and I_s are the rms voltage and rms current ratings of the transformer secondary

$$V_s = \frac{V_m}{\sqrt{2}} = 0.707\ V_m \tag{10.29}$$

The rms value of the transformer secondary current I_s is the same as that for the load current I_L. For a half-wave rectifier, I_s can be found from Eq. (10.14)

$$\text{Half-wave } I_s = \frac{0.5\ V_m}{R} \tag{10.30}$$

For a full-wave rectifier, I_s is found from Eq. (10.16).

$$\text{Full-wave } I_s = \frac{0.707\ V_m}{R} \tag{10.31}$$

Therefore, the TUF of a half-wave rectifier can be obtained by substituting Eqs. (10.3), (10.13), (10.29), and (10.30) into Eq. (10.28).

$$\text{Half-wave TUF} = \frac{0.318^2}{0.707 \times 0.5} = 0.286 \tag{10.32}$$

The poor TUF of a half-wave rectifier signifies that the transformer employed must have a 3.496 (1/0.286) VA rating in order to deliver 1 W dc output power to the load. In addition, the transformer secondary winding has to carry a dc current that may cause magnetic core saturation. As a result, half-wave rectifiers are used only when the current requirement is small.

In the case of a full-wave rectifier with a center-tapped transformer, the circuit can be treated as two half-wave rectifiers operating together. Therefore, the transformer secondary VA rating $V_s I_s$ is double that of a half-wave rectifier, but the output dc power is increased by a factor of four due to the higher rectification ratio as indicated by Eqs. (10.5) and (10.15). Therefore, the TUF of a full-wave rectifier with center-tapped transformer can be found from Eq. (10.32)

$$\begin{aligned}\text{Full-wave TUF} &= \frac{4 \times 0.318^2}{2 \times 0.707 \times 0.5} \\ &= 0.572\end{aligned} \tag{10.33}$$

The bridge rectifier has the highest TUF in single-phase rectifier circuits because the currents flowing in both the primary and secondary windings are continuous sinewaves. By substituting Eqs. (10.5), (10.15), (10.29), and (10.31) into Eq. (10.28), the TUF of a bridge rectifier can be found

$$\text{Bridge TUF} = \frac{0.636^2}{0.707 \times 0.707} = 0.81 \tag{10.34}$$

The transformer primary VA rating of a full-wave rectifier is equal to that of a bridge rectifier because the current flowing in the primary winding is also a continuous sinewave.

1 .2.3.7 Harmonics

Full-wave rectifier circuits with resistive load do not produce harmonic currents in their transformers but they are produced in half-wave rectifiers. The amplitudes of the harmonic currents of a half-wave rectifier with resistive load, relative to the fundamental, are given in Table 10.1. The extra loss caused by the harmonics in the resistively loaded rectifier circuits is often neglected because it is not high compared with other losses. However, with nonlinear loads, harmonics can cause appreciable loss and other problems such as poor power factor and interference.

TABLE 10.1 Harmonic percentages of a half-wave rectifier with resistive load

Harmonic	2nd	3rd	4th	5th	6th	7th	8th
	21.2	0	4.2	0	1.8	0	1.01

TABLE 10.2 Important design parameters of basic single-phase rectifier circuits with resistive load

	Half-Wave Rectifier	Full-Wave Rectifier with Center-Tapped Transformer	Full-Wave Bridge Rectifier
Peak repetitive reverse voltage V_{RRM}	$3.14\ V_{\mathrm{dc}}$	$3.14\ V_{\mathrm{dc}}$	$1.57\ V_{\mathrm{dc}}$
Rms input voltage per transformer leg V_s	$2.22\ V_{\mathrm{dc}}$	$1.11\ V_{\mathrm{dc}}$	$1.11\ V_{\mathrm{dc}}$
Diode average current $I_{F(\mathrm{AV})}$	$1.00\ I_{\mathrm{dc}}$	$0.50\ I_{\mathrm{dc}}$	$0.50\ I_{\mathrm{dc}}$
Peak repetitive forward current I_{FRM}	$3.14\ I_{F(\mathrm{AV})}$	$1.57\ I_{F(\mathrm{AV})}$	$1.57\ I_{F(\mathrm{AV})}$
Diode rms current $I_{F(\mathrm{RMS})}$	$1.57\ I_{\mathrm{dc}}$	$0.785\ I_{\mathrm{dc}}$	$0.785\ I_{\mathrm{dc}}$
Form factor of diode current $I_{F(\mathrm{RMS})}/I_{F(\mathrm{AV})}$	1.57	1.57	1.57
Rectification ratio	0.405	0.81	0.81
Form factor	1.57	1.11	1.11
Ripple factor	1.21	0.482	0.482
Transformer rating primary VA	$2.69\ P_{\mathrm{dc}}$	$1.23\ P_{\mathrm{dc}}$	$1.23\ P_{\mathrm{dc}}$
Transformer rating secondary VA	$3.49\ P_{\mathrm{dc}}$	$1.75\ P_{\mathrm{dc}}$	$1.23\ P_{\mathrm{dc}}$
Output ripple frequency f_r	$1\ f_i$	$2\ f_i$	$2\ f_i$

1 .2.4 Design Considerations

The goal in practical design is to achieve a given dc output voltage. Therefore, it is more convenient to put all the design parameters in terms of V_{dc}. For example, the rating and turns ratio of the transformer in a rectifier circuit can be easily determined if the rms input voltage to the rectifier is in terms of the required output voltage V_{dc}. Denote the rms value of the input voltage to the rectifier as V_s, which is equal to $0.707\ V_m$. Based on this relation and Eq. (10.3), the rms input voltage to a half-wave rectifier is found as

$$\text{Half-wave } V_s = 2.22\ V_{\mathrm{dc}} \tag{10.35}$$

Similarly, from Eqs. (10.5) and (10.29), the rms input voltage per secondary winding of a full-wave rectifier is found as

$$\text{Full-wave } V_s = 1.11\ V_{\mathrm{dc}} \tag{10.36}$$

Another important design parameter is the *Peak Repetitive Reverse Voltage* (V_{RRM}) rating of the diodes employed.

In the case of a half-wave rectifier, from Eq. (10.3),

$$\text{Half-wave } V_{\mathrm{RRM}} = V_m = \frac{V_{\mathrm{dc}}}{0.318} = 3.14\ V_{\mathrm{dc}} \tag{10.37}$$

In the case of a full-wave rectifier with center-tapped transformer, from Eq. (10.5),

$$\text{Full-wave } V_{\mathrm{RRM}} = 2\ V_m = 2\frac{V_{\mathrm{dc}}}{0.636} = 3.14\ V_{\mathrm{dc}} \tag{10.38}$$

In the case of a bridge rectifier, also from Eq. (10.5),

$$\text{Bridge } V_{\mathrm{RRM}} = V_m = \frac{V_{\mathrm{dc}}}{0.636} = 1.57\ V_{\mathrm{dc}} \tag{10.39}$$

It is important to evaluate the *Peak Repetitive Forward Current* (I_{FRM}) rating of the employed diodes in rectifier circuits.

In the case of a half-wave rectifier, from Eq. (10.13),

$$\text{Half-wave } I_{\mathrm{FRM}} = \frac{V_m}{R} = \frac{I_{\mathrm{dc}}}{0.318} = 3.41 I_{\mathrm{dc}} \tag{10.40}$$

In the case of full-wave rectifiers, from Eq. (10.15),

$$\text{Full-wave } I_{\mathrm{FRM}} = \frac{V_m}{R} = \frac{I_{\mathrm{dc}}}{0.636} = 1.57 I_{\mathrm{dc}} \tag{10.41}$$

The important design parameters of basic single-phase rectifier circuits with resistive loads are summarized in Table 10.2.

1 .3 Three-Phase Diode Rectifiers

In Section 10.2 we showed that single-phase diode rectifiers require a rather high transformer VA rating for a given dc output power. Therefore, these rectifiers are suitable only for low to medium power applications. For power output higher than 15 kW, three-phase or polyphase diode rectifiers should be employed. There are two types of three-phase diode rectifier that convert a three-phase ac supply into a dc voltage, star rectifiers and bridge rectifiers. In the following, the operations of these rectifiers are examined and their performances are analyzed and compared in a table. For the sake of simplicity, the diodes and transformers are considered to be ideal, that is, the diodes have zero forward voltage drop and reverse current, and the transformers do not possess either resistance or leakage inductance. Furthermore, it is assumed that the load is purely resistive, such that the load voltage and the load current have similar waveforms. The effects of inductive load and capacitive load on a diode rectifier are considered in detail in Section 10.5.

10.3.1 Three-Phase Star Rectifiers

10.3.1.1 Basic Three-Phase Star Rectifier Circuit

A basic three-phase star rectifier circuit is shown in Fig. 10.7. This circuit can be considered as three single-phase half-wave rectifiers combined together. Therefore, it is sometimes referred to as a three-phase half-wave rectifier. The diode in a particular phase conducts during the period when the voltage on that phase is higher than that on the other two phases. The voltage waveforms of each phase and the load are shown in Fig. 10.8. It is clear that, unlike the single-phase rectifier circuit, the conduction angle of each diode is $2\pi/3$, instead of π. This circuit finds uses where the required dc output voltage is relatively low and the required output current is too large for a practical single-phase system.

Taking phase R as an example, diode D conducts from $\pi/6$ to $5\pi/6$. Therefore, by using Eq. (10.1) the average value of the output can be found as

$$V_{\text{dc}} = \frac{3}{2\pi}\int_{\pi/6}^{5\pi/6} V_m \sin\theta \, d\theta \tag{10.42}$$

or

$$V_{\text{dc}} = V_m \frac{3}{\pi}\frac{\sqrt{3}}{2} = 0.827\ V_m \tag{10.43}$$

Similarly, using Eq. (10.6), the rms value of the output voltage can be found as

$$V_L = \sqrt{\frac{3}{2\pi}\int_{\pi/6}^{5\pi/6} (V_m \sin\theta)^2 d\theta} \tag{10.44}$$

or

$$V_L = V_m\sqrt{\frac{3}{2\pi}\left(\frac{\pi}{3}+\frac{\sqrt{3}}{4}\right)} = 0.84\ V_m \tag{10.45}$$

In addition, the rms current in each transformer secondary winding can also be found as

$$I_s = I_m\sqrt{\frac{1}{2\pi}\left(\frac{\pi}{3}+\frac{\sqrt{3}}{4}\right)} = 0.485\ I_m \tag{10.46}$$

where $I_m = V_m/R$.

Based on the relationships stated in Eqs. (10.43), (10.45) and (10.46), all the important design parameters of the three-phase star rectifier can be evaluated as listed in Table 10.3. Note that, as with a single-phase half-wave rectifier, the three-phase star rectifier shown in Fig. 10.7 has direct currents in the secondary windings that can cause a transformer core saturation problem. In addition, the currents in the primary do not sum to zero. Therefore, it is preferable not to have star-connected primary windings.

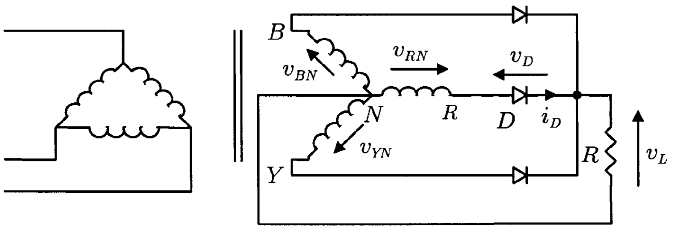

FIGURE 10.7 Three-phase star rectifier.

10.3.1.2 Three-Phase Inter-Star Rectifier Circuit

The transformer core saturation problem in the three-phase star rectifier can be avoided by a special arrangement in its secondary windings, known as zig-zag connection. The modified circuit is called the three-phase interstar or zig-zag rectifier circuit, as shown in Fig. 10.9. Each secondary phase voltage is obtained from two equal-voltage secondary windings (with a phase displacement of $\pi/3$) connected in series so that the dc magnetizing forces due to the two secondary windings on any limb are equal and opposite. At the expense of extra secondary windings (increasing the transformer secondary rating factor from 1.51 VA/W to 1.74 VA/W), this circuit connection eliminates the effects of core saturation and reduces the transformer primary rating factor to the minimum of 1.05 VA/W. Apart from transformer ratings, all the design parameters of this circuit are the same as those of a three-phase star rectifier (therefore, they are not separately listed in

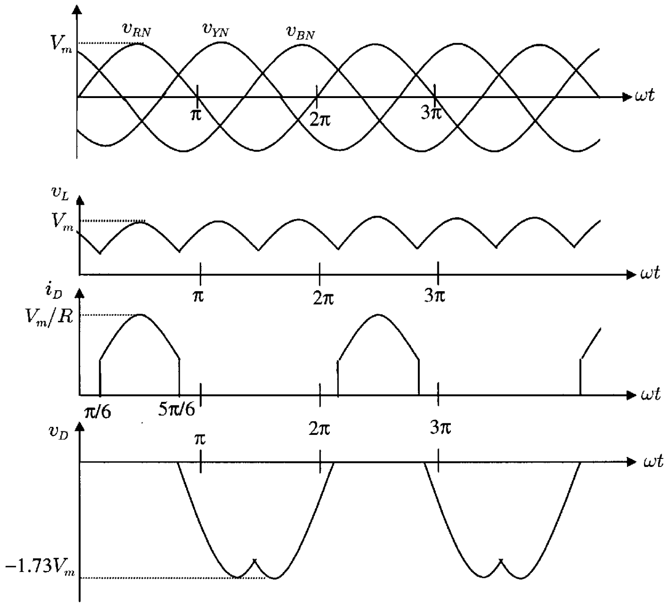

FIGURE 10.8 Waveforms of voltage and current of the three-phase star rectifier as shown in Fig. 10.7.

TABLE 10.3 Important design parameters of three-phase rectifier circuits with resistive load

	Three-Phase Star Rectifier	Three-Phase Double-Star Rectifier With Inter-Phase Transformer	Three-Phase Bridge Rectifier
Peak repetitive reverse voltage V_{RRM}	2.092 V_{dc}	1.06 V_{dc}	1.05 V_{dc}
Rms input voltage per transformer leg V_s	0.855 V_{dc}	0.855 V_{dc}	0.428 V_{dc}
Diode average current $I_{F(\mathrm{AV})}$	0.333 I_{dc}	0.167 I_{dc}	0.333 I_{dc}
Peak repetitive forward current I_{FRM}	3.63 $I_{F(\mathrm{AV})}$	3.15 $I_{F(\mathrm{AV})}$	3.14 $I_{F(\mathrm{AV})}$
Diode rms current $I_{F(\mathrm{RMS})}$	0.587 I_{dc}	0.293 I_{dc}	0.579 I_{dc}
Form factor of diode current $I_{F(\mathrm{RMS})}/I_{F(\mathrm{AV})}$	1.76	1.76	1.74
Rectification ratio	0.968	0.998	0.998
Form factor	1.0165	1.0009	1.0009
Ripple factor	0.182	0.042	0.042
Transformer rating primary VA	1.23 P_{dc}	1.06 P_{dc}	1.05 P_{dc}
Transformer rating secondary VA	1.51 P_{dc}	1.49 P_{dc}	1.05 P_{dc}
Output ripple frequency f_r	3 f_i	6 f_i	6 f_i

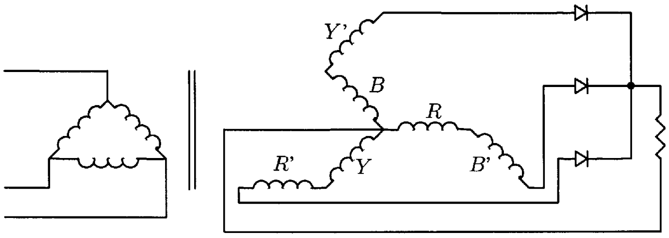

FIGURE 10.9 Three-phase inter-star rectifier.

Table 10.3). Furthermore, a star-connected primary winding with no neutral connection is equally permissible because the sum of all primary phase currents is zero at all times.

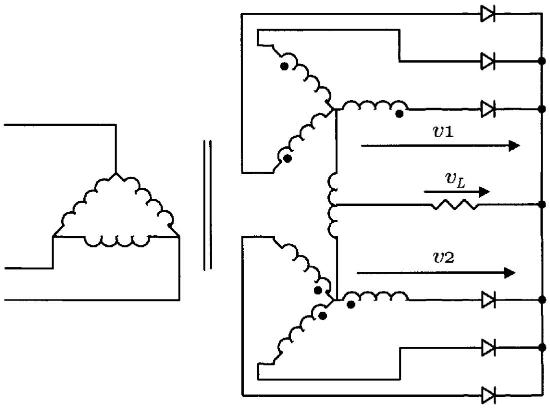

FIGURE 10.10 Three-phase double-star rectifier with interphase transformer.

1 .3.1.3 Three-Phase Double-Star Rectifier with Interphase Transformer

This circuit consists essentially of two three-phase star rectifiers with their neutral points interconnected through an interphase transformer or reactor. The polarities of the corresponding secondary windings in the two interconnected systems are reversed with respect to each other, so that the rectifier output voltage of one three-phase unit is at a minimum when the rectifier output voltage of the other unit is at a maximum as shown in Fig. 10.10. The interphase transformer causes the output voltage v_L to be the average of the rectified voltages v_1 and v_2 as shown in Fig. 10.11. In addition, the ripple frequency of the output voltage is now six times that of the mains and, therefore, the component size of the filter (if there is any) becomes smaller. In a balanced circuit, the output currents of two three-phase units flowing in opposite directions in the interphase transformer winding will produce no dc magnetization current. Similarly, the dc magnetization currents in the secondary windings of two three-phase units cancel each other out. By virtue of the symmetry of the secondary circuits, the three primary currents add up to zero at all times. Therefore, a star primary winding with no neutral connection would be equally permissible.

1 .3.2 Three-Phase Bridge Rectifiers

Three-phase bridge rectifiers are commonly used for high-power applications because they have the highest possible transformer utilization factor for a three-phase system. The circuit of a three-phase bridge rectifier is shown in Fig. 10.12.

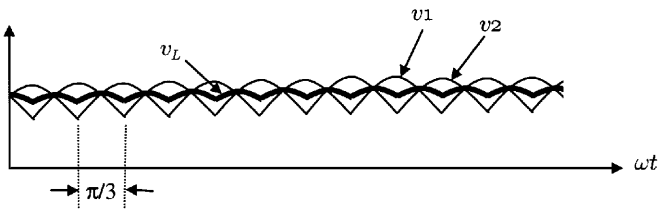

FIGURE 10.11 Voltage waveforms of the three-phase double-star rectifier.

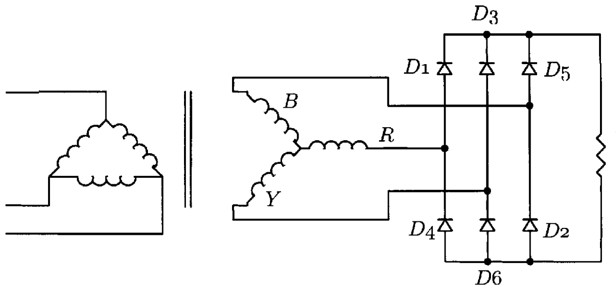

FIGURE 10.12 Three-phase bridge rectifier.

The diodes are numbered in the order of conduction sequences and the conduction angle of each diode is $2\pi/3$.

The conduction sequence for diodes is 12, 23, 34, 45, 56, and 61. The voltage and current waveforms of the three-phase bridge rectifier are shown in Fig. 10.13. The line voltage is 1.73 times the phase voltage of a three-phase star-connected source. It is permissible to use any combination of star- or delta-connected primary and secondary windings because the currents associated with the secondary windings are symmetrical.

Using Eq. (10.1), the average value of the output can be found as

$$V_{\text{dc}} = \frac{6}{2\pi}\int_{\pi/3}^{2\pi/3} \sqrt{3}\; V_m \sin\theta \, d\theta \tag{10.47}$$

or

$$V_{\text{dc}} = V_m \frac{3\sqrt{3}}{\pi} = 1.654\; V_m \tag{10.48}$$

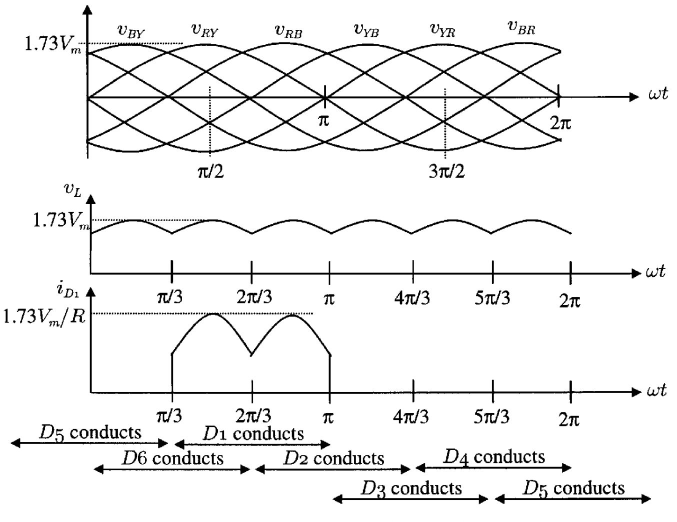

FIGURE 10.13 Voltage and current waveforms of the three-phase bridge rectifier.

Similarly, using Eq. (10.6), the rms value of the output voltage can be found as

$$V_L = \sqrt{\frac{9}{\pi}\int_{\pi/3}^{2\pi/3} (V_m \sin\theta)^2 d\theta} \tag{10.49}$$

or

$$V_L = V_m\sqrt{\frac{3}{2} + \frac{9\sqrt{3}}{4\pi}} = 1.655\; V_m \tag{10.50}$$

In addition, the rms current in each transformer secondary winding can also be found as

$$I_s = I_m\sqrt{\frac{2}{\pi}\left(\frac{\pi}{6} + \frac{\sqrt{3}}{4}\right)} = 0.78\; I_m \tag{10.51}$$

and the rms current through a diode is

$$I_D = I_m\sqrt{\frac{1}{\pi}\left(\frac{\pi}{6} + \frac{\sqrt{3}}{4}\right)} = 0.552\; I_m \tag{10.52}$$

where $I_m = 1.73\; V_m/R$.

Based on Eqs. (10.48), (10.50), (10.51), and (10.52), all the important design parameters of the three-phase star rectifier can be evaluated as listed in Table 10.3. The dc output voltage is slightly lower than the peak line voltage or 2.34 times the rms phase voltage. The *Peak Repetitive Reverse Voltage* (V_{RRM}) rating of the employed diodes is 1.05 times the dc output voltage, and the *Peak Repetitive Forward Current* (I_{FRM}) rating of the employed diodes is 0.579 times the dc output current. Therefore, this three-phase bridge rectifier is very efficient and popular wherever both dc voltage and current requirements are high. In many applications, no additional filter is required because the output ripple voltage is only 4.2%. Even if a filter is required, the size of the filter is relatively small because the ripple frequency is increased to six times the input frequency.

10.3.3 Operation of Rectifiers with Finite Source Inductance

It has been assumed in the preceding sections that the commutation of current from one diode to the next takes place instantaneously when the interphase voltage assumes necessary polarity. In practice, this is hardly possible because there are finite inductances associated with the source. For the purpose of discussing the effects of the finite source inductance, a three- phase star rectifier with transformer leakage inductances is shown in Fig. 10.14, where l_1, l_2, l_3, denote the leakage inductances associated with the transformer secondary windings.

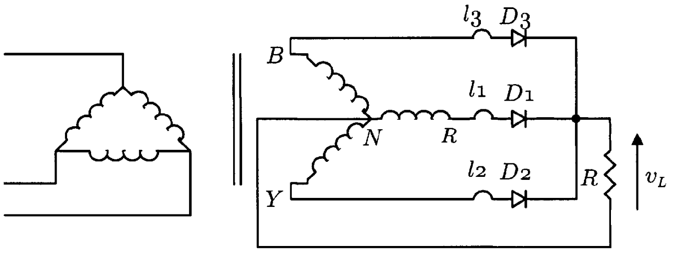

FIGURE 10.14 Three-phase star rectifier with transformer leakage inductances.

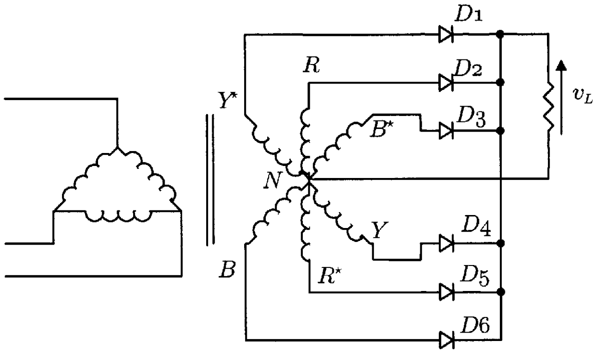

FIGURE 10.16 Six-phase star rectifier.

Refer to Fig. 10.15. At the time that v_{YN} is about to become larger than v_{RN}, due to leakage inductance l_1, the current in D_1 cannot fall to zero immediately. Similarly, due to the leakage inductance l_2, the current in D_2 cannot increase immediately to its full value. The result is that both diodes conduct for a certain period, which is called the overlap (or commutation) angle. The overlap reduces the rectified voltage v_L as shown in the upper voltage waveform of Fig. 10.15. If all the leakage inductances are equal, that is, $l_1 = l_2 = l_3 = l_c$, then the amount of reduction of dc output voltage can be estimated as $mf_i l_c I_{\mathrm{dc}}$, where m is the ratio of the lowest-ripple frequency to the input frequency.

For example, for a three-phase star rectifier operating from a 60-Hz supply with an average load current of 50 A, the amount of reduction of the dc output voltage is 2.7 V if the leakage inductance in each secondary winding is 300 μH.

1 .4 Poly-Phase Diode Rectifiers

1 .4.1 Six-Phase Star Rectifier

A basic six-phase star rectifier circuit is shown in Fig. 10.16. The six-phase voltages on the secondary are obtained by means of a center-tapped arrangement on a star-connected three-phase winding. Therefore, it is sometimes referred to as a three-phase full-wave rectifier. The diode in a particular phase conducts during the period when the voltage on that phase is higher than that on the other phases. The voltage waveforms of each phase and the load are shown in Fig. 10.17. It is clear that, unlike the three-phase star rectifier circuit, the conduction angle of each diode is $\pi/3$ instead of $2\pi/3$. Currents flow in only one rectifying element at a time, resulting in a low average current, but a high peak-to-average current ratio in the diodes and poor transformer secondary utilization. Nevertheless, the dc currents in the secondary of the six-phase star rectifier cancel in the secondary windings like a full-wave rectifier and, therefore, core saturation is not encountered. This six-phase star circuit is attractive in applications that require a low ripple factor and a common cathode or anode for the rectifiers.

By considering the output voltage provided by v_{RN} between $\pi/3$ and $2\pi/3$, the average value of the output voltage can be found as

$$V_{\mathrm{dc}} = \frac{6}{2\pi} \int_{\pi/3}^{2\pi/3} V_m \sin\theta \, d\theta \tag{10.53}$$

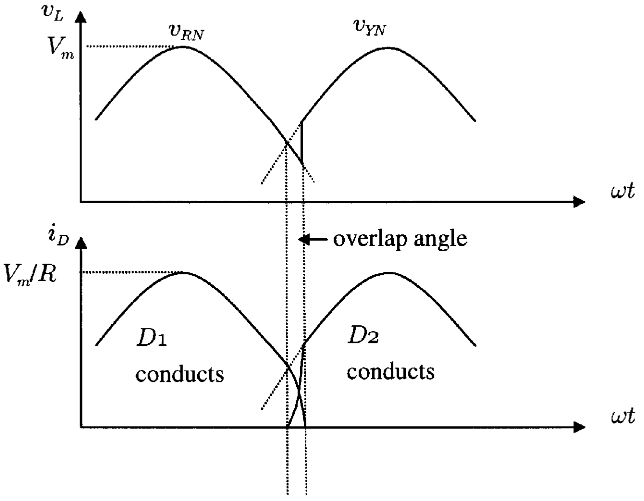

FIGURE 10.15 Waveforms during commutation in Fig. 10.14.

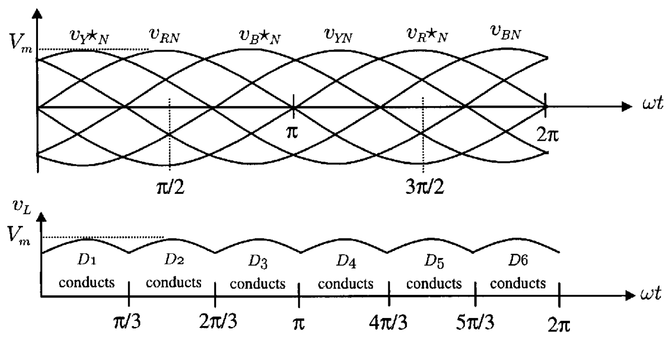

FIGURE 10.17 Voltage waveforms of the six-phase star rectifier.

or

$$V_{dc} = V_m \frac{6}{\pi} \frac{1}{2} = 0.955\ V_m \tag{10.54}$$

Similarly, the rms value of the output voltage can be found as

$$V_L = \sqrt{\frac{6}{2\pi} \int_{\pi/3}^{2\pi/3} (V_m \sin\theta)^2 d\theta} \tag{10.55}$$

or

$$V_L = V_m \sqrt{\frac{6}{2\pi}\left(\frac{\pi}{6} + \frac{\sqrt{3}}{4}\right)} = 0.956\ V_m \tag{10.56}$$

In addition, the rms current in each transformer secondary winding can be found as

$$I_s = I_m \sqrt{\frac{1}{2\pi}\left(\frac{\pi}{6} + \frac{\sqrt{3}}{4}\right)} = 0.39\ I_m \tag{10.57}$$

where $I_m = V_m/R$.

Based on the relationships stated in Eqs. (10.55), (10.56), and (10.57), all the important design parameters of the six-phase star rectifier can be evaluated, as listed in Table 10.4 (given at the end of Section 10.4.3).

10.4.2 Six-Phase Series Bridge Rectifier

The star- and delta-connected secondaries have an inherent $\pi/6$-phase displacement between their output voltages. When a star-connected bridge rectifier and a delta-connected bridge rectifier are connected in series as shown in Fig. 10.18, the combined output voltage will have a doubled ripple frequency (12 times that of the mains). The ripple of the combined output voltage will also be reduced from 4.2% (for each individual bridge rectifier) to 1%. The combined bridge rectifier is referred to as a six-phase series bridge rectifier.

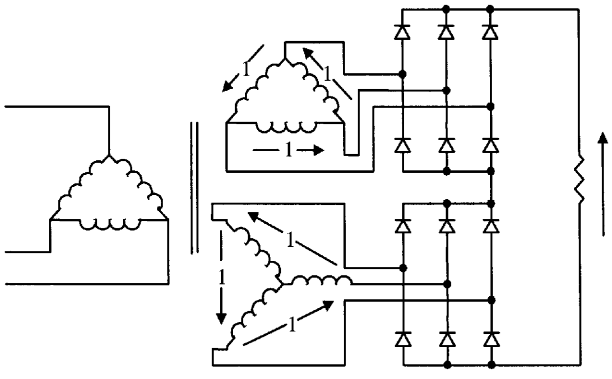

FIGURE 10.18 Six-phase series bridge rectifier.

In the six-phase series bridge rectifier shown in Fig. 10.18, let V_m^* be the peak voltage of the delta-connected secondary. The peak voltage between the lines of the star-connected secondary is also V_m^*. The peak voltage across the load, denoted as V_m, is equal to $2\ V_m^* \times \cos(\pi/12)$ or $1.932\ V_m^*$ because there is $\pi/6$-phase displacement between the secondaries. The ripple frequency is 12 times the mains frequency. The average value of the output voltage can be found as

$$V_{dc} = \frac{12}{\pi} \int_{5\pi/12}^{7\pi/12} V_m \sin\theta\, d\theta \tag{10.58}$$

or

$$V_{dc} = V_m \frac{12}{\pi} \frac{\sqrt{3}-1}{2\sqrt{2}} = 0.98862\ V_m \tag{10.59}$$

The rms value of the output voltage can be found as

$$V_L = \sqrt{\frac{12}{2\pi} \int_{5\pi/12}^{7\pi/12} (V_m \sin\theta)^2 d\theta} \tag{10.60}$$

or

$$V_L = V_m \sqrt{\frac{12}{2\pi}\left(\frac{\pi}{12} + \frac{1}{4}\right)} = 0.98867\ V_m \tag{10.61}$$

The rms current in each transformer secondary winding is

$$I_s = I_m \sqrt{\frac{4}{\pi}\left(\frac{\pi}{12} + \frac{1}{4}\right)} = 0.807\ I_m \tag{10.62}$$

The rms current through a diode is

$$I_s = I_m \sqrt{\frac{2}{\pi}\left(\frac{\pi}{12} + \frac{1}{4}\right)} = 0.57\ I_m \tag{10.63}$$

where $I_m = V_m/R$.

Based on Eqs. (10.59), (10.61), (10.62), and (10.63), all the important design parameters of the six-phase series bridge rectifier can be evaluated, as listed in Table 10.4.

10.4.3 Six-Phase Parallel Bridge Rectifier

The six-phase series bridge rectifier described in the preceding is useful for high-output voltage applications. However, for high-output current applications, the six-phase parallel bridge rectifier (with an interphase transformer) shown in Fig. 10.19 should be used.

TABLE 10.4 Important design parameters of six-phase rectifier circuits with resistive load

	Six-Phase Star Rectifier	Six-Phase Series Bridge Rectifier	Six-Phase Parallel Bridge Rectifier (With Inter-Phase Transformer)
Peak repetitive reverse voltage V_{RRM}	2.09 V_{dc}	0.524 V_{dc}	1.05 V_{dc}
Rms input voltage per transformer leg V_s	0.74 V_{dc}	0.37 V_{dc}	0.715 V_{dc}
Diode average current $I_{F(AV)}$	0.167 I_{dc}	0.333 I_{dc}	0.167 I_{dc}
Peak repetitive forward current I_{FRM}	6.28 $I_{F(AV)}$	3.033 $I_{F(AV)}$	3.14 $I_{F(AV)}$
Diode rms current $I_{F(RMS)}$	0.409 I_{dc}	0.576 I_{dc}	0.409 I_{dc}
Form factor of diode current $I_{F(RMS)}/I_{F(AV)}$	2.45	1.73	2.45
Rectification ratio	0.998	1.00	1.00
Form factor	1.0009	1.00005	1.00005
Ripple factor	0.042	0.01	0.01
Transformer rating primary VA	1.28 P_{dc}	1.01 P_{dc}	1.01 P_{dc}
Transformer rating secondary VA	1.81 P_{dc}	1.05 P_{dc}	1.05 P_{dc}
Output ripple frequency f_r	6 f_i	12 f_i	12 f_i

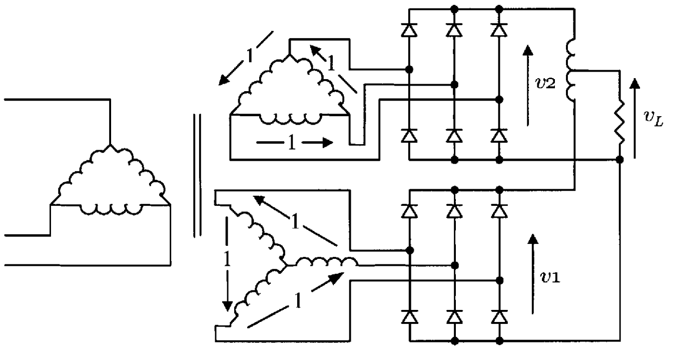

FIGURE 10.19 Six-phase parallel bridge rectifier.

The interphase transformer causes the output voltage v_L to be the average of the rectified voltages v_1 and v_2 as shown in Fig. 10.20. As with the six-phase series bridge rectifier, the output ripple frequency of the six-phase parallel bridge rectifier is also 12 times that of the mains. Further filtering on the output voltage is usually not required. Assuming a balanced circuit, the output currents of two three-phase units (flowing in opposite directions in the interphase transformer winding) produce no dc magnetization current.

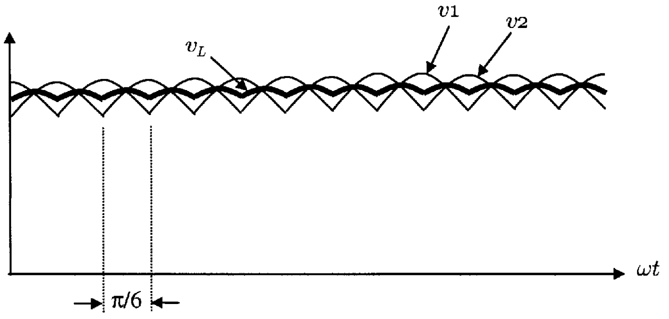

FIGURE 10.20 Voltage waveforms of the six-phase bridge rectifier with interphase transformer.

All the important design parameters of the six-phase parallel rectifiers with interphase transformer are also listed in Table 10.4.

1 .5 iltering Systems in Rectifier Circuits

Filters are commonly employed in rectifier circuits for smoothing out the dc output voltage of the load. They are classified as inductor-input dc filters and capacitor-input dc filters. Inductor-input dc filters are preferred in high-power applications because more efficient transformer operation is obtained due to the reduction in the form factor of the rectifier current. Capacitor-input dc filters can provide volumetrically efficient operation, but they demand excessive turn-on and repetitive surge currents. Therefore, capacitor-input dc filters are suitable only for lower-power systems where close regulation is usually achieved by an electronic regulator cascaded with the rectifier.

1 .5.1 Inductive-Input dc ilters

The simplest inductive-input dc filter is shown in Fig. 10.21a. The output current of the rectifier can be maintained at a steady value if the inductance of L_f is sufficiently large ($\omega L_f \gg R$). The filtering action is more effective in heavy load conditions than in light load conditions. If the ripple attenuation is not sufficient even with large values of inductance, an L-section filter as shown in Fig. 10.21b can be used for further filtering. In practice, multiple L-section filters can also be employed if the requirement on the output ripple is very stringent.

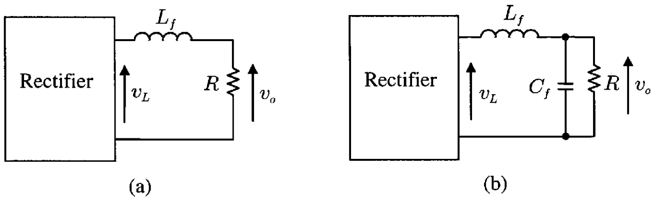

FIGURE 10.21 Inductive-input dc filters. (a) Simplest inductive-input dc filter; (b) L-section filter.

For the simple inductive-input dc filter shown in Fig. 10.21a, the ripple is reduced by the factor

$$\frac{v_o}{v_L} = \frac{R}{\sqrt{R^2 + (2\pi f_r L_f)^2}} \tag{10.64}$$

where v_L is the ripple voltage before filtering, v_o is the ripple voltage after filtering, and f_r is the ripple frequency.

For the inductive-input dc filter shown in Fig. 10.21b, the amount of reduction in the ripple voltage can be estimated as

$$\frac{v_o}{v_L} = \left| \frac{1}{1 - (2\pi f_r)^2 L_f C_f} \right| \tag{10.65}$$

where f_r is the ripple frequency, if $R \gg 1/2\pi f_r C_f$.

10.5.1.1 Voltage and Current Waveforms for a Full-Wave Rectifier with Inductor-Input dc Filter

Figure 10.22 shows a single-phase full-wave rectifier with an inductor-input dc filter. The voltage and current waveforms are illustrated in Fig. 10.23.

When the inductance of L_f is infinite, the current through the inductor and the output voltage are constant. When inductor L_f is finite, the current through the inductor has a ripple component, as shown by the dotted lines in Fig. 10.23. If the input inductance is too small, the current decreases to zero (becoming discontinuous) during a portion of the time between the peaks of the rectifier output voltage. The minimum value of inductance required to maintain a continuous current is known as the critical inductance L_C.

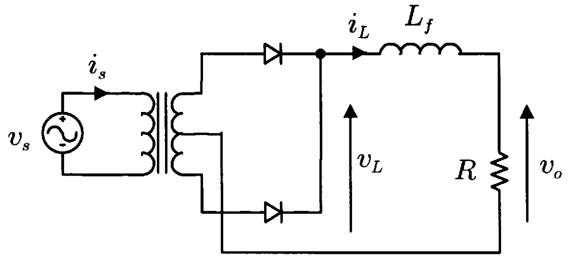

FIGURE 10.22 A full-wave rectifier with inductor-input dc filter.

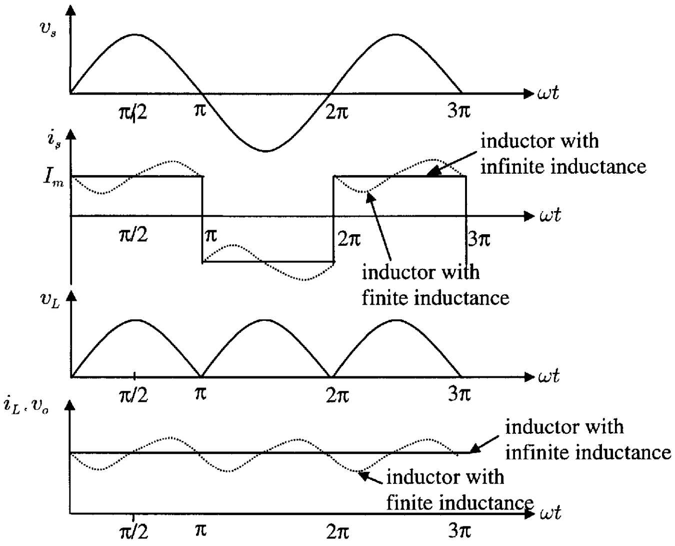

FIGURE 10.23 Voltage and current waveforms of full-wave rectifier with inductor-input dc filter.

10.5.1.2 Critical Inductance L_C

In the case of single-phase full-wave rectifiers, the critical inductance can be found as

$$\text{Full-wave } L_C = \frac{R}{6\pi f_i} \tag{10.66}$$

where f_i is the input mains frequency.

In the case of polyphase rectifiers, the critical inductance can be found as

$$\text{Polyphase } L_C = \frac{R}{3\pi m(m^2 - 1) f_i} \tag{10.67}$$

where m is the ratio of the lowest ripple frequency to the input frequency, for example, $m = 6$ for a three-phase bridge rectifier.

10.5.1.3 Determining the Input Inductance for a Given Ripple Factor

In practice, the choice of the input inductance depends on the required ripple factor of the output voltage. The ripple voltage of a rectifier without filtering can be found by means of Fourier analysis. For example, the coefficient of the nth harmonic component of the rectified voltage v_L shown in Fig. 10.22 can be expressed as

$$v_{L_n} = \frac{-4V_m}{\pi(n^2 - 1)} \tag{10.68}$$

where $n = 2, 4, 8, \ldots$, etc.

The dc component of the rectifier voltage is given by Eq. (10.5). Therefore, in addition to Eq. (10.27), the ripple factor can also be expressed as

$$\mathrm{RF} = \sqrt{2 \sum_{n=2,4,8} \left(\frac{1}{n^2 - 1}\right)^2} \tag{10.69}$$

Considering only the lowest-order harmonic ($n = 2$), the output ripple factor of a simple inductor-input dc filter (without C_f) can be found, from Eqs. (10.64) and (10.69), as

$$\text{Filtered RF} = \frac{0.4714}{\sqrt{1 + (4\pi f_i L_f / R)^2}} \tag{10.70}$$

10.5.1.4 Harmonics of the Input Current

In general, the total harmonic distortion (THD) of an input current is defined as

$$\mathrm{THD} = \sqrt{\left(\frac{I_s}{I_{s1}}\right)^2 - 1} \tag{10.71}$$

where I_s is the rms value of the input current and I_{s1} and the rms value of the fundamental component of the input current. The THD can also be expressed as

$$\mathrm{THD} = \sqrt{\sum_{n=2,3,4} \left(\frac{I_{sn}}{I_{s1}}\right)^2} \tag{10.72}$$

where I_{sn} is the rms value of the nth harmonic component of the input current.

Moreover, the input power factor is defined as

$$\mathrm{PF} = \frac{I_{s1}}{I_s} \cos\phi \tag{10.73}$$

where ϕ is the displacement angle between the fundamental components of the input current and voltage.

Assume that inductor L_f of the circuit shown in Fig. 10.22 has an infinitely large inductance. The input current is then a square wave. This input current contains undesirable higher harmonics that reduce the input power factor of the system. The input current can be easily expressed as

$$i_s = \frac{4I_m}{\pi} \sum_{n=1,3,5} \frac{1}{n} \sin 2n\pi f_i t \tag{10.74}$$

The rms values of the input current and its fundamental component are I_m and $4I_m/(\pi\sqrt{2})$, respectively. Therefore, the THD of the input current of this circuit is 0.484. As the displacement angle $\phi = 0$, the power factor is $4/(\pi\sqrt{2}) = 0.9$.

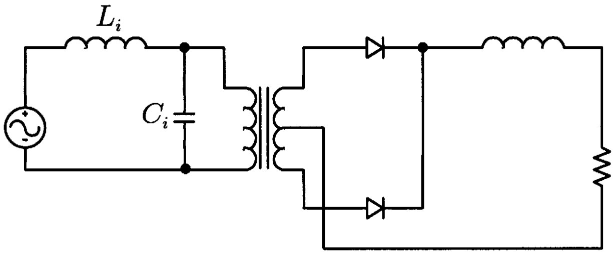

FIGURE 10.24 Equivalent circuit for input ac filter.

The power factor of the circuit shown in Fig. 10.22 can be improved by installing an ac filter between the source and the rectifier, as shown in Fig. 10.24.

Considering only the harmonic components, the equivalent circuit of the rectifier given in Fig. 10.24 can be found as shown in Fig. 10.25. The rms value of the nth harmonic current appearing in the supply can then be obtained using the current-divider rule,

$$I_{sn} = \left| \frac{1}{1 - (2n\pi f_i)^2 L_i C_i} \right| I_{rn} \tag{10.75}$$

where I_{rn} is the rms value of the nth harmonic current of the rectifier.

Applying Eq. (10.73) and knowing $I_{rn}/I_{r1} = 1/n$ from Eq. (10.74), the THD of the rectifier with input filter shown in Fig. 10.24 can be found as

$$\text{Filtered THD} = \sqrt{\sum_{n=3,5} \frac{1}{n^2} \left| \frac{1}{1 - (2n\pi f_i)^2 L_i C_i} \right|^2} \tag{10.76}$$

The important design parameters of typical single-phase and three-phase rectifiers with inductor-input dc filter are listed in Table 10.5. Note that, in a single-phase half-wave rectifier, a freewheeling diode is required to be connected across the input of the dc filters such that the flow of load current can be maintained during the negative half-cycle of the supply voltage.

10.5.2 Capacitive-Input dc Filters

Figure 10.26 shows a full-wave rectifier with capacitor-input dc filter. The voltage and current waveforms of this rectifier are

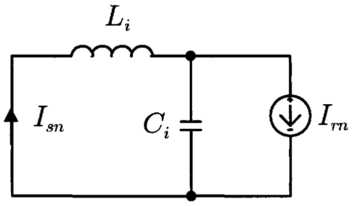

FIGURE 10.25 Equivalent circuit for input ac filter.

TABLE 10.5 Important design parameters of typical rectifier circuits with inductor-input dc filter

	Full-wave Rectifier With Center-Tapped Transformer	Full-Wave Bridge Rectifier	Three-Phase Star Rectifier	Three-Phase Bridge Rectifier	Three-Phase Double-Star Rectifier With Interphase Transformer
Peak repetitive reverse voltage V_{RRM}	3.14 V_{dc}	1.57 V_{dc}	2.09 V_{dc}	1.05 V_{dc}	2.42 V_{dc}
Rms input voltage per transformer leg V_s	1.11 V_{dc}	1.11 V_{dc}	0.885 V_{dc}	0.428 V_{dc}	0.885 V_{dc}
Diode average current $I_{F(\mathrm{AV})}$	0.5 I_{dc}	0.5 I_{dc}	0.333 I_{dc}	0.333 I_{dc}	0.167 I_{dc}
Peak repetitive forward current I_{FRM}	2.00 $I_{F(\mathrm{AV})}$	2.00 $I_{F(\mathrm{AV})}$	3.00 $I_{F(\mathrm{AV})}$	3.00 $I_{F(\mathrm{AV})}$	3.00 $I_{F(\mathrm{AV})}$
Diode rms current $I_{F(\mathrm{RMS})}$	0.707 I_{dc}	0.707 I_{dc}	0.577 I_{dc}	0.577 I_{dc}	0.289 I_{dc}
Form factor of diode current $I_{F(\mathrm{RMS})}/I_{F(\mathrm{AV})}$	1.414	1.414	1.73	1.73	1.73
Transformer rating primary VA	1.11 P_{dc}	1.11 P_{dc}	1.21 P_{dc}	1.05 P_{dc}	1.05 P_{dc}
Transformer rating secondary VA	1.57 P_{dc}	1.11 P_{dc}	1.48 P_{dc}	1.05 P_{dc}	1.48 P_{dc}
Output ripple frequency f_r	2 f_i	2 f_i	3 f_i	6 f_i	6 f_i
Ripple component V_r at					
(a) fundamental	0.667 V_{dc}	0.667 V_{dc}	0.250 V_{dc}	0.057 V_{dc}	0.057 V_{dc}
(b) second harmonic	0.133 V_{dc}	0.133 V_{dc}	0.057 V_{dc}	0.014 V_{dc}	0.014 V_{dc}
(c) third harmonic of the ripple frequency	0.057 V_{dc}	0.057 V_{dc}	0.025 V_{dc}	0.006 V_{dc}	0.006 V_{dc}

shown in Fig. 10.27. When the instantaneous voltage of the secondary winding v_s is higher than the instantaneous value of capacitor voltage v_L, either D_1 or D_2 conducts, and capacitor C is charged up from the transformer. When the instantaneous voltage of the secondary winding v_s falls below the instantaneous value of capacitor voltage v_L, both diodes are reverse biased and capacitor C is discharged through load resistance R. The resulting capacitor voltage v_L varies between a maximum value of V_m and a minimum value of $V_m - V_{r(\mathrm{pp})}$ as shown in Fig. 10.27. ($V_{r(\mathrm{pp})}$ is the peak-to-peak ripple voltage.) As shown in Fig. 10.27, the conduction angle θ_c of the diodes becomes smaller when the output ripple voltage decreases. Consequently, the power supply and diodes suffer from high repetitive surge currents. An LC ac filter, as shown in Fig. 10.24, may be required to improve the input power factor of the rectifier.

In practice, if the peak-to-peak ripple voltage is small, it can be approximated as

$$V_{r(\mathrm{pp})} = \frac{V_m}{f_r RC} \tag{10.77}$$

where f_r is the output ripple frequency of the rectifier.

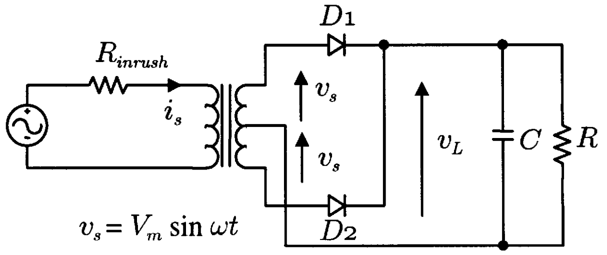

FIGURE 10.26 Full-wave rectifier with capacitor-input dc filter.

Therefore, the average output voltage V_{dc} is given by

$$V_{\mathrm{dc}} = V_m\left(1 - \frac{1}{2f_r RC}\right) \tag{10.78}$$

The rms output ripple voltage V_{ac} is approximated by

$$V_{\mathrm{ac}} = \frac{V_m}{2\sqrt{2}f_r RC} \tag{10.79}$$

The ripple factor RF can be found from

$$\mathrm{RF} = \frac{1}{\sqrt{2}(2f_r RC - 1)} \tag{10.80}$$

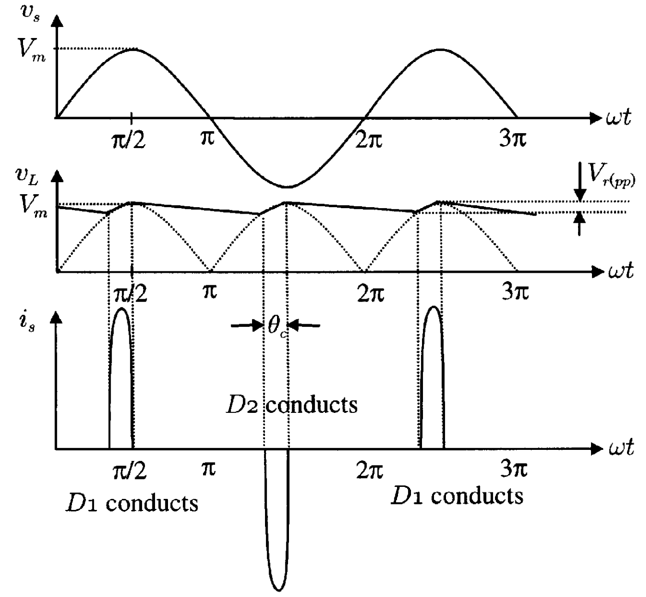

FIGURE 10.27 Voltage and current waveforms of the full-wave rectifier with capacitor-input dc filter.

10.5.2.1 Inrush Current

The resistor R_{inrush} in Fig. 10.26 is used to limit the inrush current imposed on the diodes during the instant the rectifier is being connected to the supply. The inrush current can be very large because capacitor C initially has zero charge. The worst case occurs when the rectifier is connected to the supply at its maximum voltage. The worst-case inrush current can be estimated from

$$I_{\text{inrush}} = \frac{V_m}{R_{\text{sec}} + R_{\text{ESR}}} \tag{10.81}$$

where R_{sec} is the equivalent resistance looking from the transformer secondary and equivalent series resistance (ESR) of the filtering capacitor is R_{ESR}. Hence, the employed diode should be able to withstand the inrush current for a half-cycle of the input voltage. In other words, the *Maximum Allowable Surge Current* (I_{FSM}) rating of the employed diodes must be higher than the inrush current. The equivalent resistance associated with the transformer windings and the filtering capacitor is usually sufficient to limit the inrush current to an acceptable level. However, in cases where the transformer is omitted, for example, the rectifier of an off-line switch-mode supply, resistor R_{inrush} must be added for controlling inrush current.

Consider as an example a single-phase bridge rectifier, which is to be connected to a 120-V 60-Hz source (without transformer). Assume that the *Maximum Allowable Surge Current* (I_{FSM}) rating of the diodes is 150 A for an interval of 8.3 ms. If the ESR of the filtering capacitor is zero, we estimate from Eq. (10.81) that the value of the resistor for limiting inrush current resistance is 1.13 Ω.

10.6 High-Frequency Diode Rectifier Circuits

In high-frequency converters, diodes perform various functions, such as rectifying, flywheeling, and clamping. One special quality a high-frequency diode must possess is a fast switching speed. In technical terms, it must have a short reverse recovery time and a short forward recovery time.

The reverse recovery time of a diode may be understood as the time a forwardly conducting diode takes to recover to a blocking state when the voltage across it is suddenly reversed (which is known as forced turn-off). The temporary short circuit during the reverse recovery period may result in large reverse current, excessive ringing, and large power dissipation, all of which are highly undesirable.

The forward recovery time of a diode may be understood as the time a nonconducting diode takes to change to the fully on state when a forward current is suddenly forced into it (which is known as forced turn-on). Before the diode reaches the fully on state, the forward voltage drop during the forward recovery time can be significantly higher than the normal on-state voltage drop. This may cause voltage spikes in the circuit.

It should be interesting to note that, as far as circuit operation is concerned, a diode with a long reverse recovery time is similar to a diode with a large parasitic capacitance. A diode with a long forward recovery time is similar to a diode with a large parasitic inductance. (Spikes caused by the slow forward recovery of diodes are often wrongly thought to be caused by leakage inductance.) Comparatively, the adverse effect of a long reverse recovery time is much worse than that of a long forward recovery time.

Among commonly used diodes, the Schottky diode has the shortest forward and reverse recovery times. Schottky diodes are therefore most suitable for high-frequency applications. However, Schottky diodes have relatively low reverse breakdown voltage (normally lower than 200 V) and large leakage current. If, due to these limitations, Schottky diodes cannot be used, ultra-fast diodes should be used in high-frequency converter circuits.

Using the example of a forward converter, the operations of a forward rectifier diode, a flywheel diode, and a clamping diode will be studied in Section 10.6.1. Because of the difficulties encountered in full analyses when taking into account parasitic/stray/leakage components, PSpice simulations are extensively used here to study the following [3–5]:

- The idealized operation of the converter;
- the adverse effects of relatively slow rectifiers (e.g., the so-called ultra-fast diodes, which are actually much slower than Schottky diodes);
- the improvement achievable by using high-speed rectifiers (Schottky diodes);
- the effects of leakage inductance of the transformer;
- the use of snubber circuits to reduce ringing; and
- the operation of a practical converter with snubber circuits.

Using the example of a flyback converter, the operations of a flyback rectifier diode and a clamping diode also will be studied in Section 10.6.2.

The design considerations for high-frequency diode rectifier circuits will be discussed in Section 10.6.3. The precautions that must be taken in the interpretation of computer simulation results are briefly discussed in Section 10.6.4.

10.6.1 Forward Rectifier Diode, Flywheel Diode, and Magnetic-Reset Clamping Diode in a Forward Converter

10.6.1.1 Ideal Circuit

Fig. 10.28 shows the basic circuit of a forward converter. Fig. 10.29 shows the idealized steady-state waveforms for continuous-mode operation (the current in L_1 is continuous). These waveforms are obtained from PSpice simulations, based on the following assumptions:

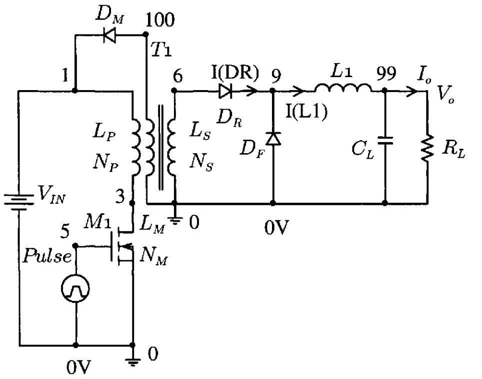

FIGURE 10.28 Basic circuit of forward converter. Note that: $V_{IN} = 50\,V$; $L_1 = 8\,\mu H$; $C_L = 300\,\mu F$; $L_P = 0.576\,mH$; $L_M = 0.576\,mH$; $L_S = 0.036\,mH$; $R_L = 0.35\,\Omega$; and $N_P : N_M : N_S = 4 : 4 : 1$.

- Rectifier diode D_R, flywheel diode D_F, and magnetic-reset clamping diode D_M are ideal diodes with infinitely fast switching speed.
- Electronic switch M_1 is an idealized MOS switch with infinitely fast switching speed, with on-state resistance of 0.067 Ω, and off-state resistance of 1 MΩ.

  It should be noted that PSpice does not allow a switch to have zero on-state resistance and infinite off-state resistance.
- Transformer T_1 has a coupling coefficient of 0.99999999. The PSpice program does not accept a coupling coefficient of 1.
- The switching operation of the converter has reached a steady state.

Referring to the circuit shown in Fig. 10.28 and the waveforms shown in Fig. 10.29, the operation of the converter can be explained as follows:

1. For $0 < t < DT$ (D is the duty cycle of the MOS switch M_1 and T is the switching period of the converter, M_1 is turned on when V1(VPULSE) is 15 V, and turned off when V1(VPULSE) is 0 V.)

   The switch M_1 is turned on at $t = 0$.

   The voltage at node 3, denoted as V(3), is

   $$V(3) = 0 \quad \text{for} \quad 0 < t < DT \tag{10.82}$$

   The voltage induced at node 6 of the secondary winding L_S is

   $$V(6) = V_{IN}(N_S/N_P) \tag{10.83}$$

   This voltage drives a current I(DR) (current through rectifier diode D_R) into the output circuit to produce the output voltage V_o. The rate of increase of I(DR) is given by

   $$\frac{dI(DR)}{dt} = \left(V_{IN}\frac{N_S}{N_P} - V_o\right)\frac{1}{L_1} \tag{10.84}$$

   where V_o is the dc output voltage of the converter.

   The flywheel diode D_F is reversely biased by $V(9)$, the voltage at node 9

   $$V(9) = V_{IN}(N_S/N_p) \quad \text{for} \quad 0 < t < DT \tag{10.85}$$

   The magnetic-reset clamping diode D_M is reversely biased by the negative voltage at node 100. Assuming that L_M and L_P have the same number of turns, we have

   $$V(100) = -V_{IN} \quad \text{for} \quad 0 < t < DT \tag{10.86}$$

   A magnetizing current builds up linearly in L_P. This magnetizing current reaches the maximum value of $(V_{IN}DT)/L_P$ at $t = DT$.

2. For $DT < t < 2DT$

   The switch M_1 is turned off at $t = DT$.

   The collapse of magnetic flux induces a back emf in L_M, which is equal to L_P, to turn on the clamping diode D_M. The magnetizing current in L_M drops (from the maximum value of $(V_{IN}DT)/L_P$, as mentioned in the preceding) at the rate of V_{IN}/L_P. It reaches zero at $t = 2DT$.

   The back emf induced across L_P is equal to V_{IN}. The voltage at node 3 is

   $$V(3) = 2V_{IN} \quad \text{for} \quad DT < t < 2DT \tag{10.87}$$

   The back emf across L_S forces D_R to stop conducting.

   The inductive current in L_1 forces the flywheel diode D_F to conduct. Here I(L_1) (current through L_1) falls at the rate of

   $$\frac{dI(L_1)}{dt} = \frac{-V_o}{L_1} \tag{10.88}$$

   The voltage across D_R, denoted as V(6, 9) (the voltage at node 6 with respect to node 9), is

   $$\begin{aligned} V(DR) &= V(6, 9) \\ &= -V_{IN}(N_S/N_P) \quad \text{for} \quad DT < t < 2DT \end{aligned} \tag{10.89}$$

3. For $2DT < t < T$

   Here D_M stops conducting at $t = 2DT$. The voltage across L_M then falls to zero.

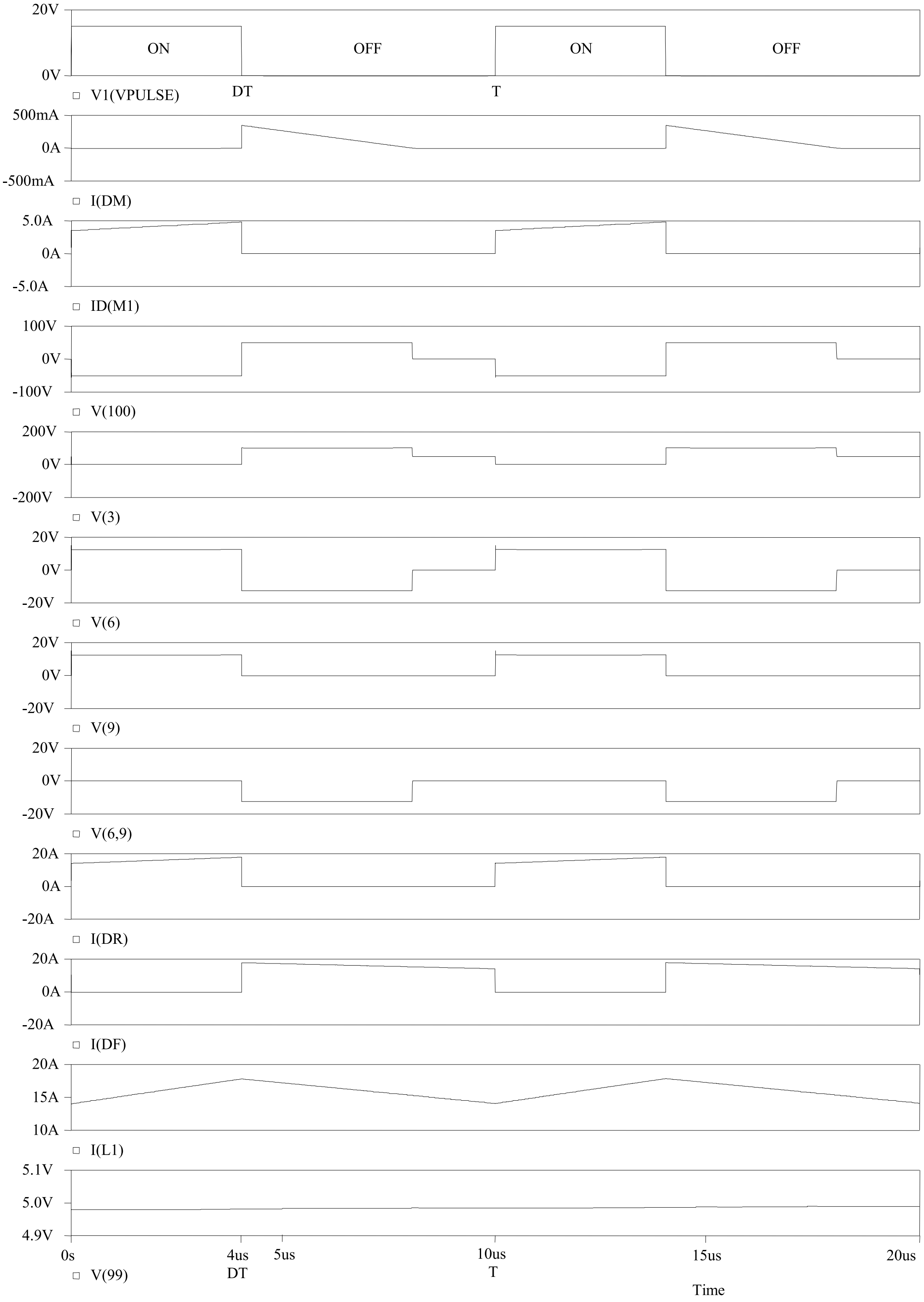

FIGURE 10.29 Idealized steady-state waveforms of forward converter for continuous-mode operation.

The voltage across L_P is zero

$$V(3) = V_{IN} \tag{10.90}$$

The voltage across L_S is also zero

$$V(6) = 0 \tag{10.91}$$

Inductive current $I(L_1)$ continues to fall at the rate of

$$\frac{dI(L_1)}{dt} = \frac{-V_o}{L_1} \tag{10.92}$$

The switching cycle restarts when the switch M_1 is turned on again at $t = T$.

From the waveforms shown in Fig. 10.29, the following useful information (for continuous-mode operation) can be found:

- The output voltage V_o is equal to the average value of V(9),

$$V_o = D\frac{N_S}{N_P}V_{IN} \tag{10.93}$$

- The maximum current in the forward rectifying diode D_R and flywheel diode D_F is

$$\begin{aligned} I(DR)_{max} &= I(DE)_{max} \\ &= I_o + \frac{1}{2}\frac{V_o}{L_1}(1-D)T \end{aligned} \tag{10.94}$$

  where $V_o = DV_{IN}(N_S/N_P)$ and I_o is the output loading current.
- The maximum reverse voltage of D_R and D_F is

$$\begin{aligned} V(DR)_{max} &= V(DF)_{max} \\ &= V(6, 9)_{max} = V_{IN}\frac{N_S}{N_P} \end{aligned} \tag{10.95}$$

- The maximum reverse voltage of D_M is

$$V(DM)_{max} = V_{IN} \tag{10.96}$$

- The maximum current in D_M is

$$I(DM)_{max} = DT\frac{V_{IN}}{L_P} \tag{10.97}$$

- The maximum current in the switch M_1, denoted as $ID(M_1)$, is

$$\begin{aligned} ID(M_1)_{max} &= \frac{N_S}{N_P}I(DR)_{max} + I(DM)_{max} \\ &= \frac{N_S}{N_P}\left(I_o + \frac{1}{2}\frac{V_0}{L_1}(1-D)T\right) + DT\frac{V_{IN}}{L_P} \end{aligned} \tag{10.98}$$

However, it should be understood that, due to the nonideal characteristics of practical components, the idealized waveforms shown in Fig. 10.29 cannot actually be achieved in the real world. In the following, the effects of nonideal diodes and transformers will be examined.

1 .6.1.2 Circuit Using Ultra-Fast Diodes

Fig. 10.30 shows the waveforms of the forward converter (circuit given in Fig. 10.28) when ultra-fast diodes are used as D_M, D_R, and D_F. (Note that ultra-fast diodes are actually much slower than Schottky diodes.) The waveforms are obtained by PSpice simulations, based on the following assumptions:

- D_M is an MUR460 ultra-fast diode, and D_R and D_F are MUR1560 ultra-fast diodes;
- M_1 is an IRF640 MOS transistor;
- transformer T_1 has a coupling coefficient of 0.99999999 (which may be assumed to be 1); and
- the switching operation of the converter has reached a steady state.

It is observed that a large spike appears in the current waveforms of diodes D_R and D_F (denoted as I(DR) and I(DF) in Fig. 10.30) whenever the MOS transistor M_1 is turned on. This is due to the relatively slow reverse recovery of the flywheel diode D_F. During the reverse recovery time, the positive voltage suddenly appearing across L_S (which is equal to $V_{IN}(N_S/N_P)$) drives a large transient current through D_R and D_F. This current spike results in large current stress and power dissipation in D_R, D_F, and M_1.

A method of reducing the current spikes is to use Schottky diodes as D_R and D_F, as will be described in what follows.

1 .6.1.3 Circuit Using Schottky Diodes

In order to reduce the current spikes caused by the slow reverse recovery of rectifiers, Schottky diodes are now used as D_R and D_F. The assumptions made here are (referring to the circuit shown in Fig. 10.28):

- D_R and D_F are MBR2540 Schottky diodes;
- D_M is an MUR460 ultra-fast diode;
- M_1 is an IRF640 MOS transistor;
- transformer T_1 has a coupling coefficient of 0.99999999; and
- the switching operation of the converter has reached a steady state.

The new simulated waveforms are given in Fig. 10.31. It is found that when Schottky diodes are used as D_R and D_F, the amplitudes of the current spikes in ID(M1), I(DR), and I(DF) can be reduced to practically zero. This solves the slow-speed problem of ultra-fast diodes.

1 .6.1.4 Circuit with Practical Transformer

The simulation results given in Figs. 10.29–10.31 (for the forward converter circuit shown in Fig. 10.28) are based on

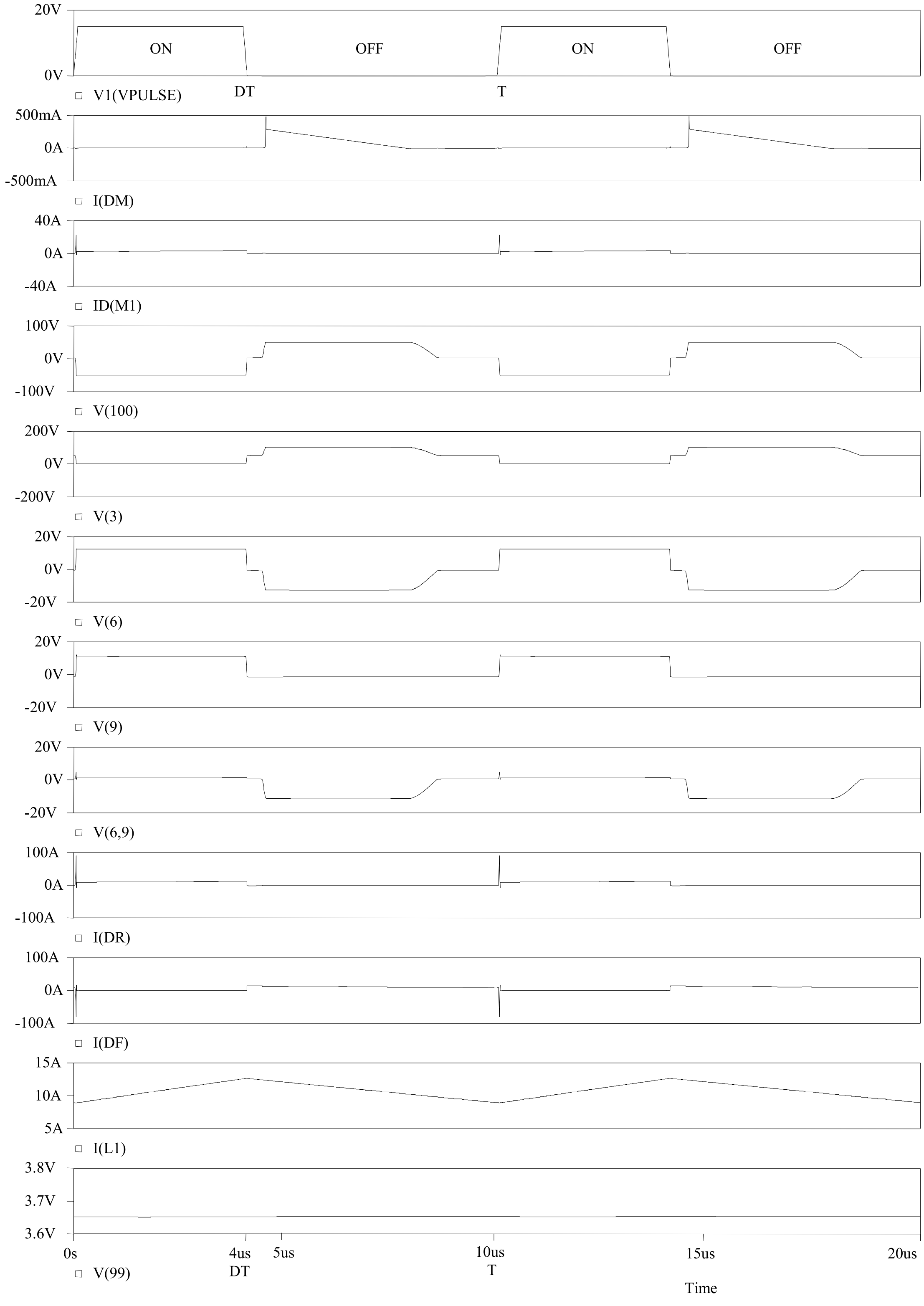

FIGURE 10.30 Waveforms of a forward converter using "ultra-fast" diodes (which are actually much slower than Schottky diodes).

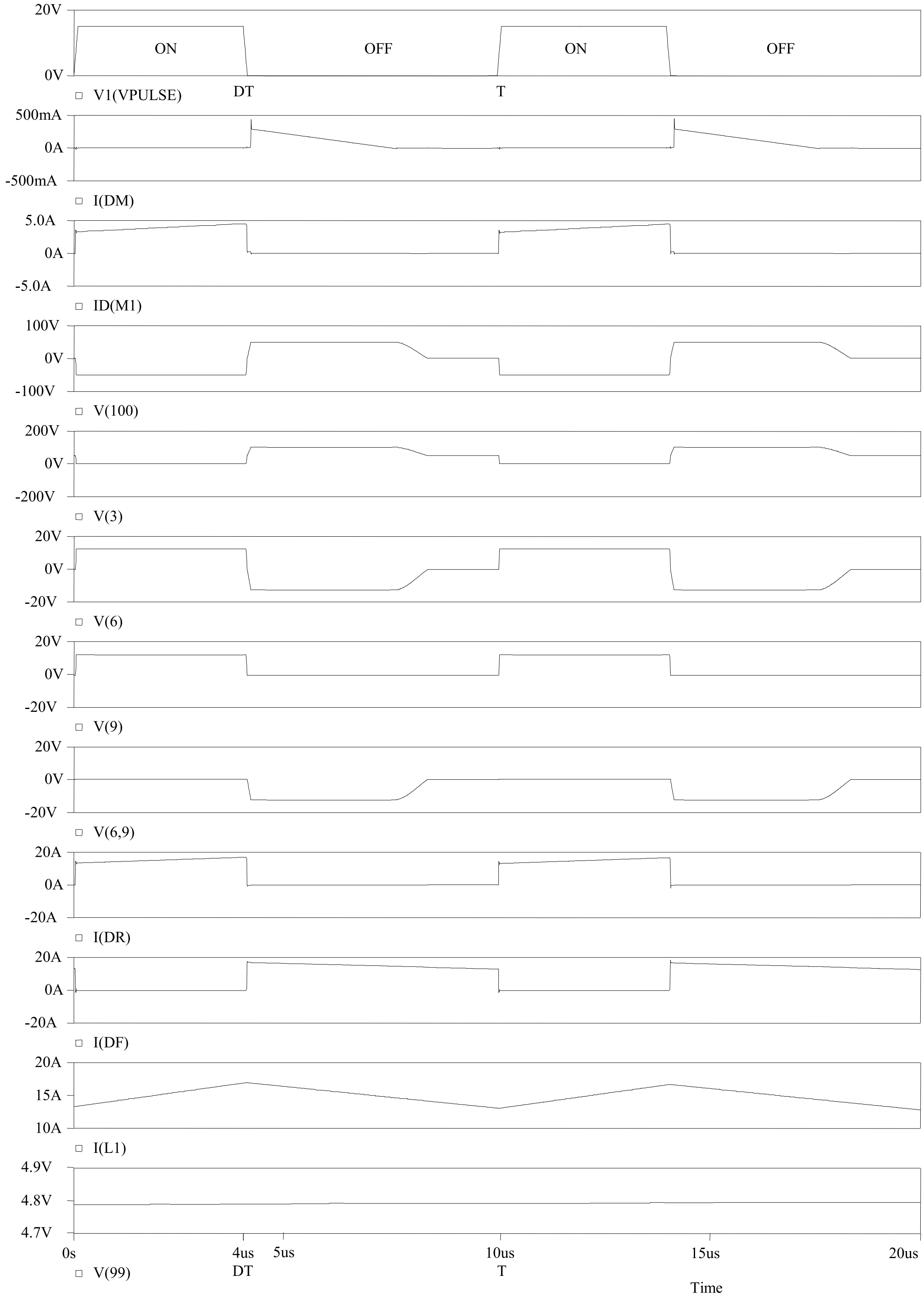

FIGURE 10.31 Waveforms of a forward converter using Schottky (fast-speed) diodes as output rectifiers.

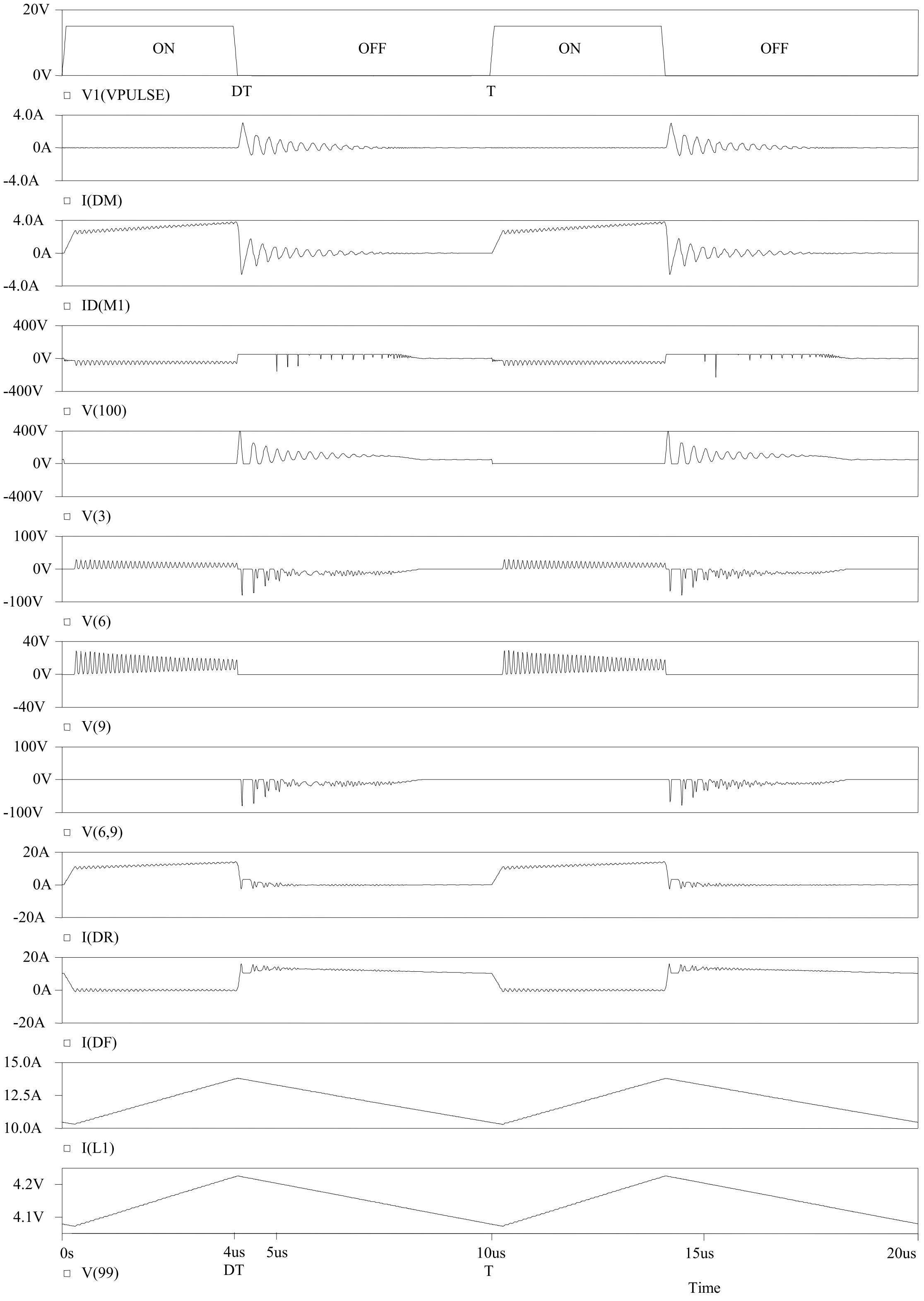

FIGURE 10.32 Waveforms of the forward converter with practical transformer and output filtering capacitor having nonzero series effective resistance.

the assumption that transformer T_1 effectively has no leakage inductance (with coupling coefficient $K = 0.99999999$). However, it is found that when a practical transformer (having a slightly lower K) is used, severe ringings occur. Fig. 10.32 shows some simulation results to demonstrate this phenomenon and the following assumptions are made:

- D_R and D_F are MBR2540 Schottky diodes and D_M is an MUR460 ultra fast diode;
- M_1 is an IRF640 MOS transistor;
- transformer T_1 has a practical coupling coefficient of 0.996;
- the effective winding resistance of L_P is 0.1 Ω, the effective winding resistance of L_M is 0.4 Ω, and the effective winding resistance of L_S is 0.01 Ω;
- the effective series resistance of the output filtering capacitor is 0.05 Ω; and
- the switching operation of the converter has reached a steady state.

The resultant waveforms shown in Fig. 10.32 indicate that there are large voltage and current ringings in the circuit. These ringings are caused by the resonant circuits formed by the leakage inductance of the transformer and the parasitic capacitances of the diodes and the transistor.

Therefore, a practical converter may need snubber circuits to damp these ringings, as will be described in what follows.

10.6.1.5 Circuit with Snubber Across Transformer

To suppress the ringing voltage caused by the resonant circuit formed by transformer leakage inductance and the parasitic capacitance of the MOS switch, a snubber circuit, shown as R_1 and C_1 in Fig. 10.33, is now connected across the primary winding of transformer T_1. The new waveforms are shown in Fig. 10.34. Here the drain-to-source voltage waveform of the MOS transistor V(3) is found to be acceptable. However, there are still large ringing voltages across the output rectifiers (V(6, 9) and V(9)).

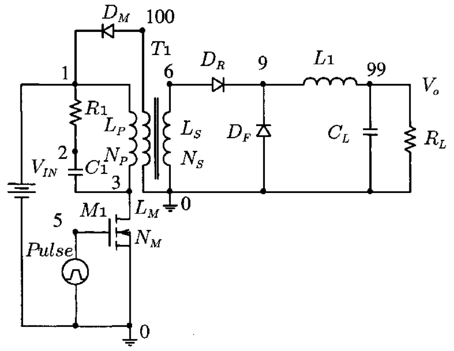

FIGURE 10.33 Forward converter with snubber circuit (R_1C_1) across transformer: $V_{IN} = 50\,V$; $D_M = $ MUR460; $D_R = $ MBR2540; $D_F = $ MBR2540; $M_1 = $ IRF640; $R_1 = 24\,\Omega$; $C_1 = 3000\,pF$; $C_L = 3500\,\mu F$; ESR of $C_L = 0.05\,\Omega$; $L_1 = 8\,\mu H$; $L_P = 0.576\,mH$; $L_M = 0.576\,mH$; $L_S = 0.036\,mH$; $N_P : N_M : N_S = 4 : 4 : 1$; $R_L = 0.35\,\Omega$; effective winding resistance of $L_P = 0.1\,\Omega$; effective winding resistance of $L_M = 0.4\,\Omega$; effective winding resistance of $L_S = 0.01\,\Omega$; and coupling coefficient $k = 0.996$.

To damp the ringing voltages across the output rectifiers, additional snubber circuits across the rectifiers may therefore also be required in a practical circuit, as will be described in what follows.

10.6.1.6 Practical Circuit

Fig. 10.35 shows a practical forward converter also with snubber circuits added to rectifiers (R_2C_2 for D_R and R_3C_3 for D_F) to reduce voltage ringing. Figs. 10.36 and 10.37 show the resultant voltage and current waveforms. Fig. 10.36 is for continuous-mode operation ($R_L = 0.35\,\Omega$), where I(L_1) (current in L_1) is continuous. Figure 10.37 is for discontinuous-mode operation ($R_L = 10\,\Omega$), where I(L_1) becomes discontinuous due to an increased value of R_L. These waveforms are considered to be acceptable.

The design considerations of diode rectifier circuits in high-frequency converters will be discussed later in Section 10.6.3.

10.6.2 Flyback Rectifier Diode and Clamping Diode in a Flyback Converter

10.6.2.1 Ideal Circuit

Fig. 10.38 shows the basic circuit of a flyback converter. Due to its simple circuit, this type of converter is widely used in low-cost low-power applications. Discontinuous-mode operation (meaning that the magnetizing current in the transformer falls to zero before the end of each switching cycle) is often used because it offers the advantages of easy control and low diode reverse-recovery loss. Fig. 10.39 shows the idealized steady-state waveforms for discontinuous-mode operation. These waveforms are obtained from PSpice simulations, based on the following assumptions:

- D_R is an idealized rectifier diode with infinitely fast switching speed;
- M_1 is an idealized MOS switch with infinitely fast switching speed, with on-state resistance of 0.067 Ω; and off-state resistance of 1 MΩ;
- transformer T_1 has a coupling coefficient of 0.99999999; and
- the switching operation of the converter has reached a steady state.

Referring to the circuit shown in Fig. 10.38 and the waveforms shown in Fig. 10.39, the operation of the converter can be explained as follows:

1. For $0 < t < DT$

   The switch M_1 is turned on at $t = 0$ and V(3) = 0 for $0 < t < DT$.

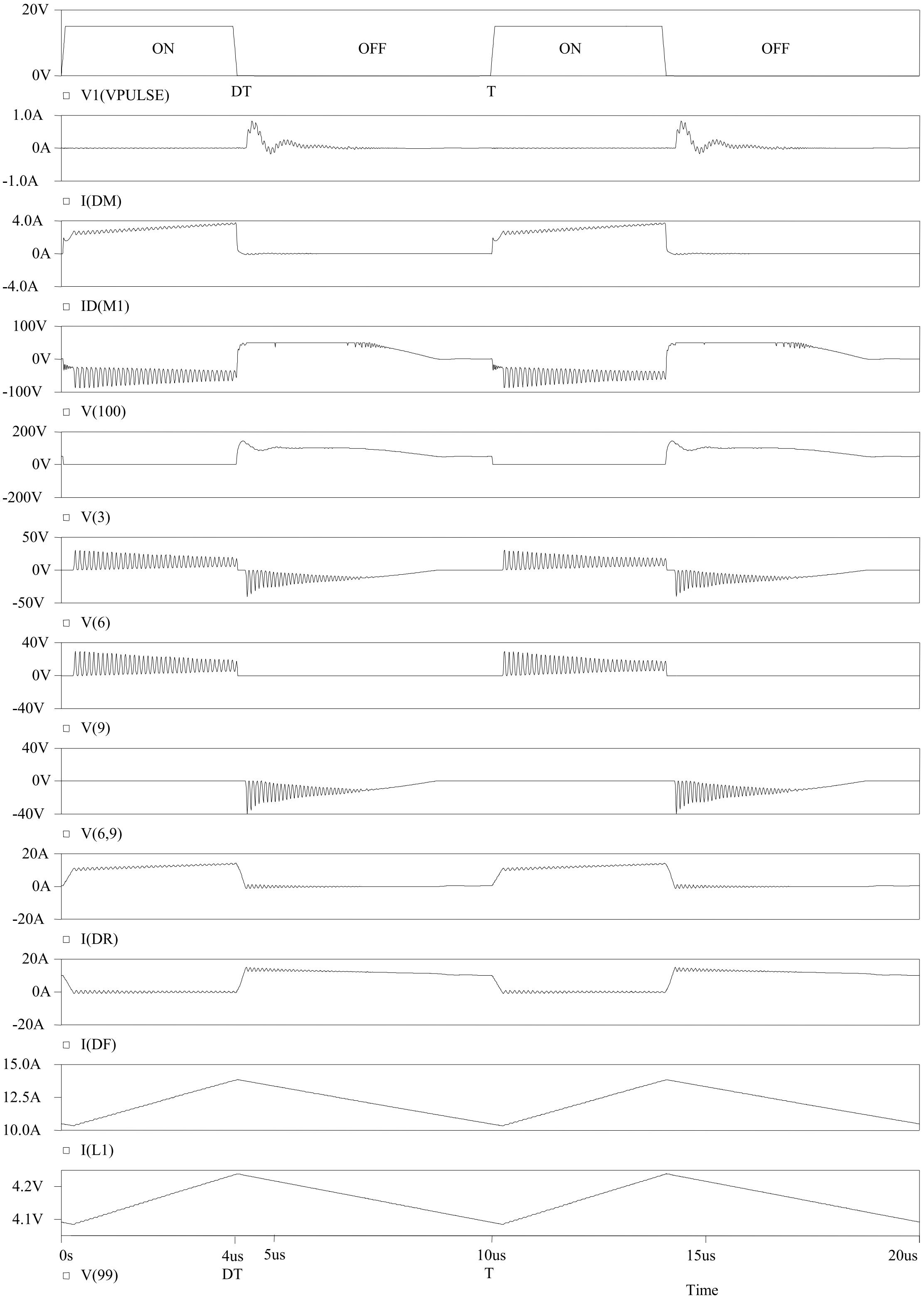

FIGURE 10.34 Waveforms of the forward converter with snubber circuit across transformer.

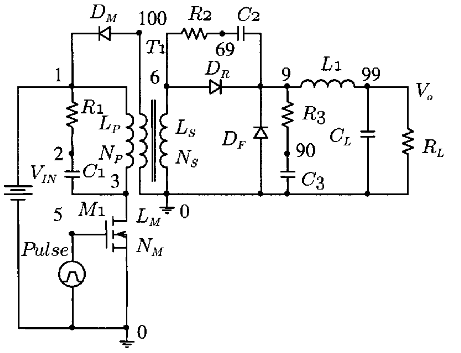

FIGURE 10.35 Practical forward converter with snubber circuits across transformer and rectifiers: $V_{\text{IN}} = 50\,\text{V}$; $D_M = \text{MUR460}$; $D_R = \text{MBR2540}$; $D_F = \text{MBR2540}$; $M_1 = \text{IRF640}$; $R_1 = 24\ \Omega$; $R_2 = 10\ \Omega$; $R_3 = 10\ \Omega$; $C_1 = 3000\,\text{pF}$; $C_2 = 10\,\text{nF}$; $C_3 = 10\,\text{nF}$; $C_L = 3500\,\mu\text{F}$; ESR of $C_L = 0.05\ \Omega$; $L_1 = 8\,\mu\text{H}$; $L_P = 0.576\,\text{mH}$; $L_M = 0.576\,\text{mH}$; $L_S = 0.036\,\text{mH}$; $N_P : N_M : N_S = 4 : 4 : 1$; effective winding resistance of $L_P = 0.1\ \Omega$; effective winding resistance of $L_M = 0.4\ \Omega$; and effective winding resistance of $L_S = 0.01\ \Omega$; and coupling coefficient $K = 0.996$.

The current in M_1, denoted as ID(M_1), increases at the rate of

$$\frac{d\text{ID}(\text{M}_1)}{dt} = \frac{V_{\text{IN}}}{L_P} \tag{10.99}$$

The output rectifier D_R is reversely biased.

2. For $DT < t < (D + D_2)T$

   The switching M_1 is turned off at $t = DT$.

   The collapse of magnetic flux induces a back emf in L_S to turn on the output rectifier D_R. The initial amplitude of the rectifier current I(DR), which is also denoted as I(LS), can be found by equating the energy stored in the primary-winding current I(LP) just before $t = DT$ to the energy stored in the secondary-winding current I(LS) just after $t = DT$:

$$\frac{1}{2}L_P(\text{I(LP)})^2 = \frac{1}{2}L_S(\text{I(LS)})^2 \tag{10.100}$$

$$\frac{1}{2}L_P\left(\frac{V_{\text{IN}}}{L_P}DT\right)^2 = \frac{1}{2}L_S(\text{I(LS)})^2 \tag{10.101}$$

$$\text{I(LS)} = \sqrt{\frac{L_P}{L_S}}\,\frac{V_{\text{IN}}}{L_P}DT \tag{10.102}$$

$$\text{I(LS)} = \frac{N_P}{N_S}\,\frac{V_{\text{IN}}}{L_P}DT \tag{10.103}$$

   The amplitude of I(LS) falls at the rate of

$$\frac{d\text{I(LS)}}{dt} = \frac{-V_o}{L_S} \tag{10.104}$$

   and I(LS) falls to zero at $t = (D + D_2)T$. As $D_2V_o = V_{\text{IN}}(N_S/N_P)D$,

$$D_2 = \frac{V_{\text{IN}}}{V_o}\,\frac{N_S}{N_P}D \tag{10.105}$$

   D_2 is effectively the duty cycle of the output rectifier D_R.

3. For $(D + D_2)T < t < T$

   The output rectifier D_R is off.

   The output capacitor C_L provides the output current to the load R_L.

The switching cycle restarts when the switch M_1 is turned on again at $t = T$.

From the waveforms shown in Fig. 10.39, the following information (for discontinuous-mode operation) can be obtained:

- The maximum value of the current in the switch M_1 is

$$\text{ID}(\text{M}_1)_{\max} = \frac{V_{\text{IN}}}{L_P}DT \tag{10.106}$$

- The maximum value of the current in the output rectifier D_R is

$$\text{I(DR)}_{\max} = \frac{N_P}{N_S}\,\frac{V_{\text{IN}}}{L_P}DT \tag{10.107}$$

- The output voltage V_o can be found by equating the input energy to the output energy within a switching cycle

$$V_{\text{IN}} \times [\text{Charge taken from } V_{\text{in}} \text{ in a switching cycle}$$

$$= \frac{V_o^2}{R_L}T$$

$$V_{\text{IN}}\left(\frac{1}{2}DT\frac{DT}{L_P}V_{\text{IN}}\right) = \frac{V_o^2}{R_L}T \tag{10.108}$$

$$V_o = \sqrt{\frac{R_LT}{2L_P}}DV_{\text{IN}} \tag{10.109}$$

- The maximum reverse voltage of D_R, V(6, 9) (which is the voltage at node 6 with respect to node 9), is

$$\text{V(DR)}_{\max} = V(6, 9)_{\max} = V_{\text{IN}}\frac{N_S}{N_P} + V_o \tag{10.110}$$

1 .6.2.2 Practical Circuit

When a practical transformer (with leakage inductance) is used in the flyback converter circuit shown in Fig. 10.38, there will be large ringings. In order to reduce these ringings to levels that are acceptable under actual conditions, snubber and clamping circuits have to be added. Fig. 10.40 shows a practical flyback converter circuit where a resistor-capacitor

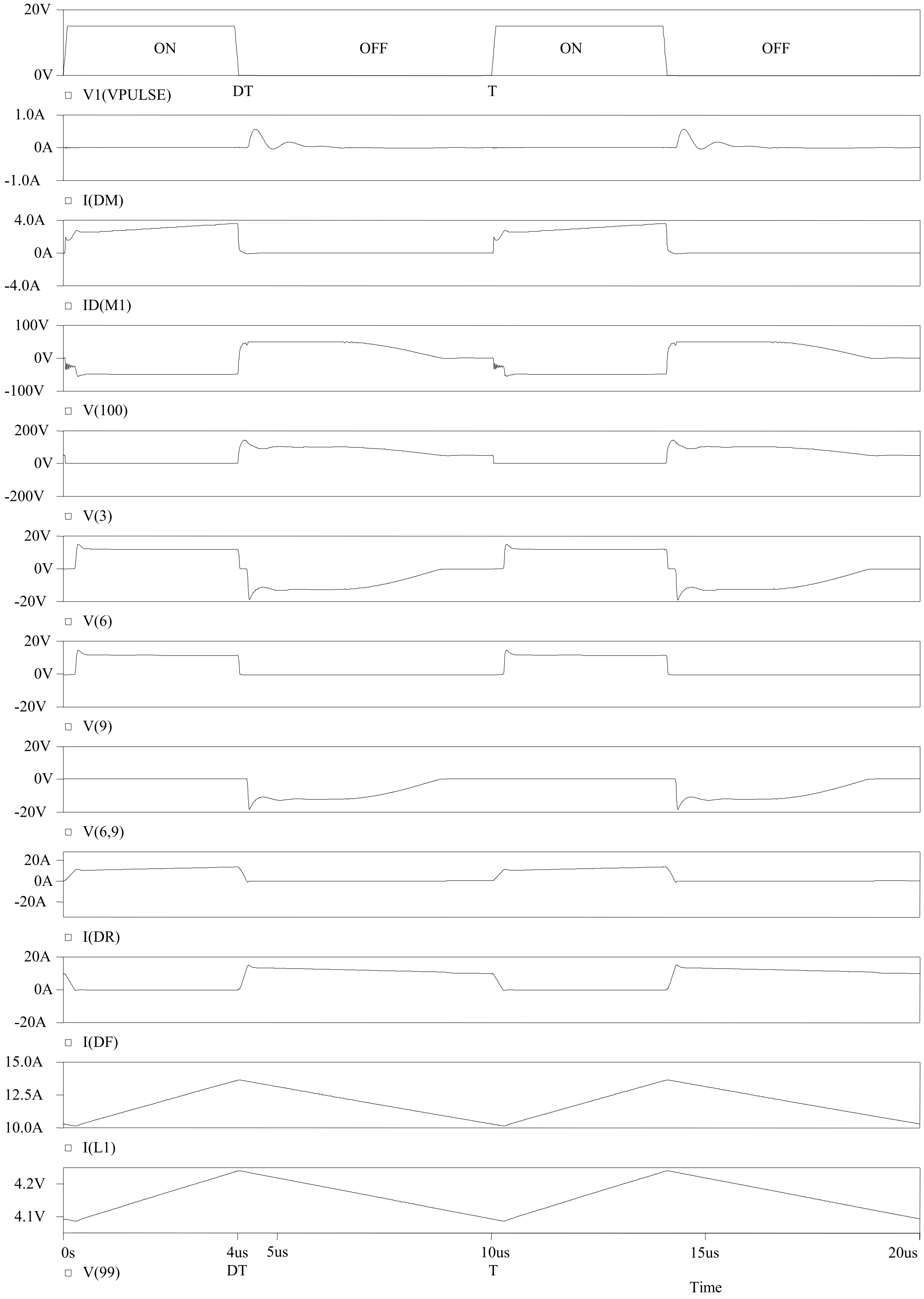

FIGURE 10.36 Waveforms of practical forward converter for continuous-mode operation.

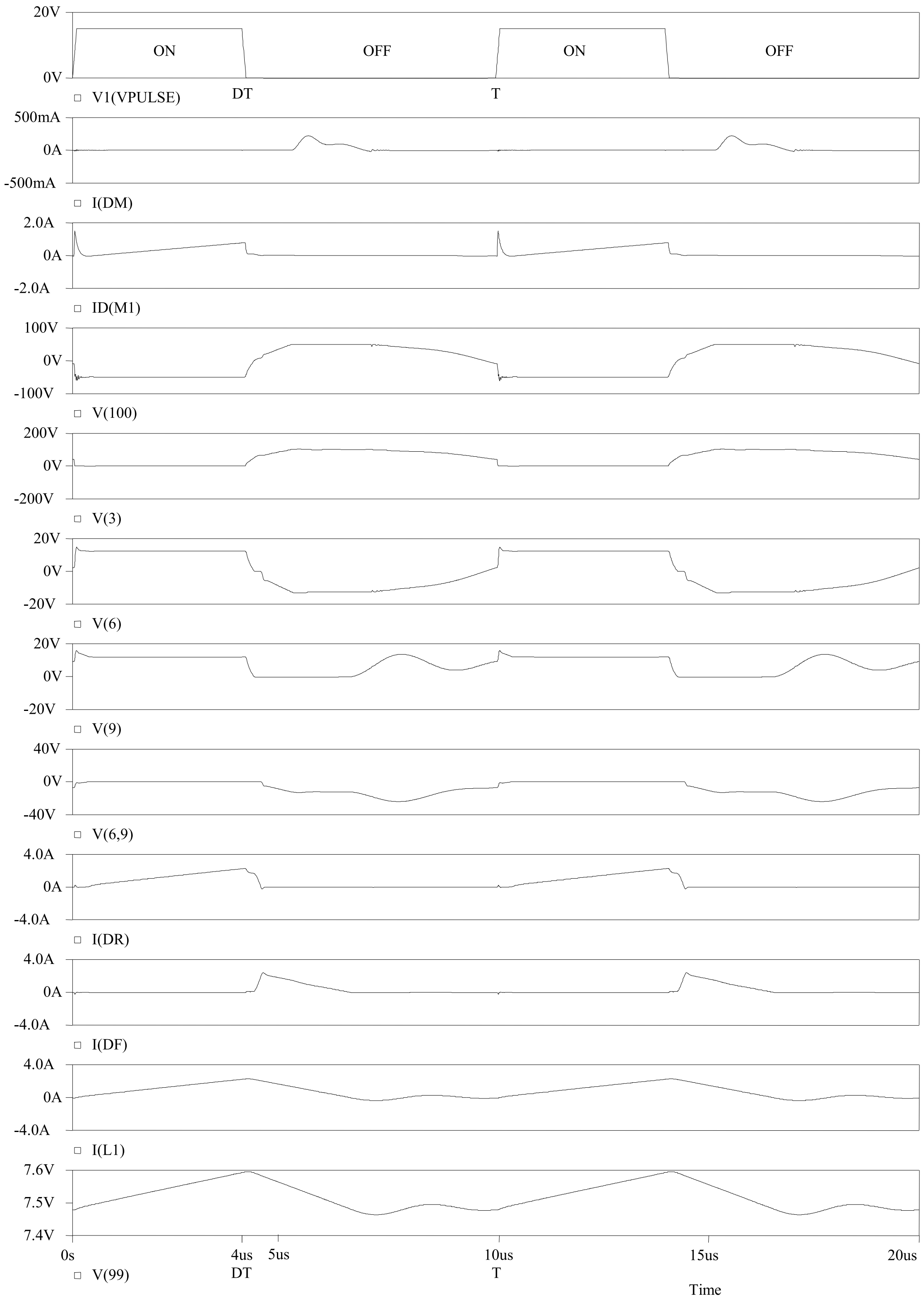

FIGURE 10.37 Waveforms of practical forward converter for discontinuous-mode operation.

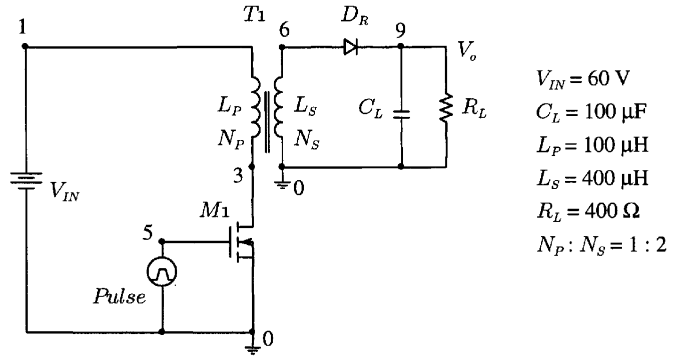
1
T1
6
DR
9
Vo
LP
NP
LS
NS
CL
RL
3
0
VIN
M1
5
Pulse
0
VIN = 60 V
CL = 100 µF
LP = 100 µH
LS = 400 µH
RL = 400 Ω
NP : NS = 1 : 2

FIGURE 10.38 Basic circuit of flyback converter.

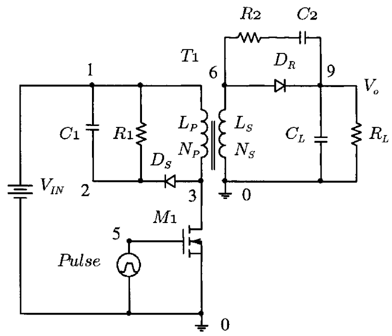
R2
C2
T1
DR
1
6
9
Vo
C1
R1
LP
NP
LS
NS
CL
RL
DS
VIN
2
3
0
M1
5
Pulse
0

FIGURE 10.40 Practical flyback converter circuit: $V_{IN} = 60\,V$; $D_S = MUR460$; $D_R = MUR460$; $M_1 = IRF640$; $R_1 = 4.7\,K\Omega$; $R_2 = 100\,\Omega$; $C_1 = 0.1\,\mu F$; $C_2 = 680\,pF$; $C_L = 100\,\mu F$; ESR of $C_L = 0.05\,\Omega$; $L_p = 100\,\mu H$; $L_S = 400\,\mu H$; $R_L = 400\,\Omega$; $N_P : N_S = 1 : 2$; effective winding resistance of $L_P = 0.025\,\Omega$; effective winding resistance of $L_S = 0.1\,\Omega$; and coupling coefficient $K = 0.992$.

snubber (R_2C_2) is used to damp the ringing voltage across the output rectifier D_R and a resistor-capacitor-diode clamping ($R_1C_1D_S$) is used to clamp the ringing voltage across the switch M_1. The diode D_S here allows the energy stored by the current in the leakage inductance to be converted to the form of a dc voltage across the clamping capacitor C_1. The energy transferred to C_1 is then dissipated slowly in the parallel resistor R_1 without ringing problems.

The simulated waveforms of the flyback converter (circuit given in Fig. 10.40) for discontinuous-mode operation are

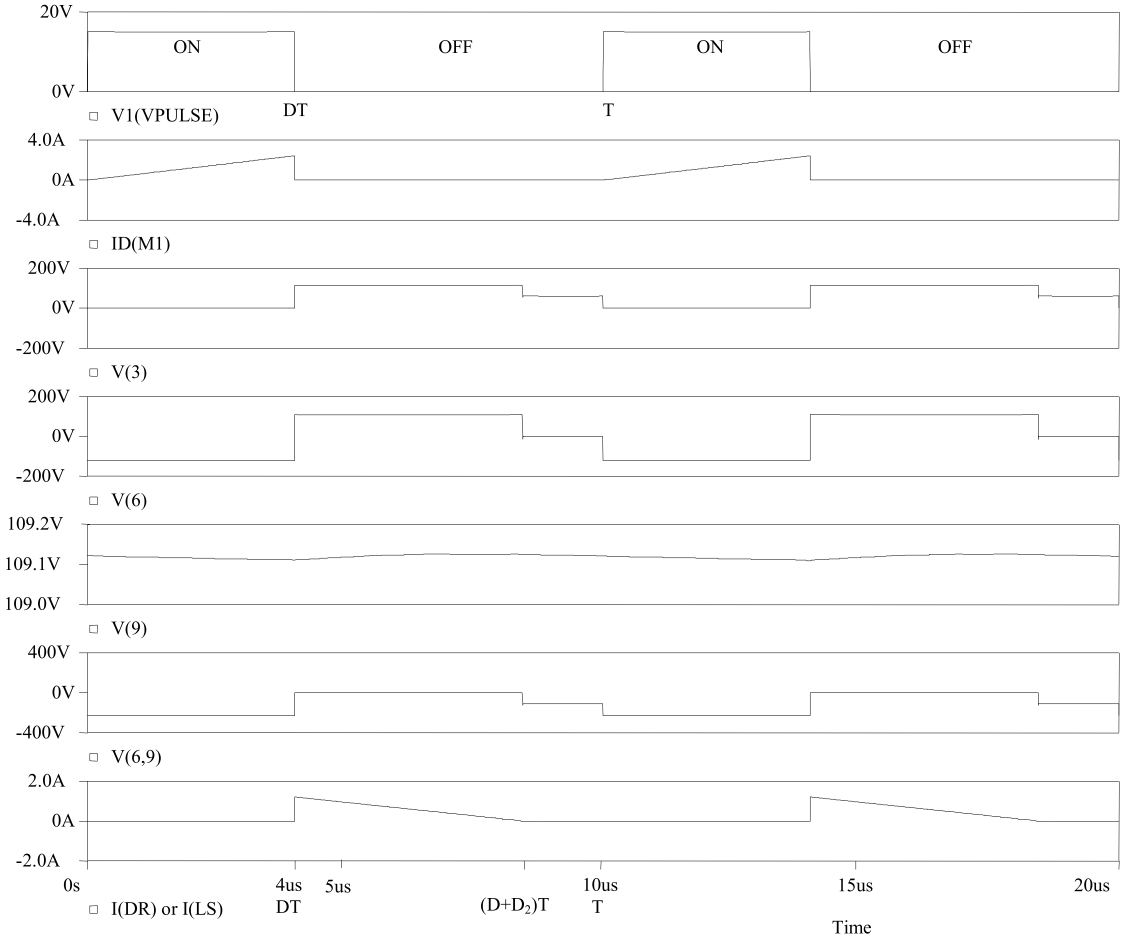

FIGURE 10.39 Idealized steady-state waveforms of flyback converter for discontinuous-mode operation.

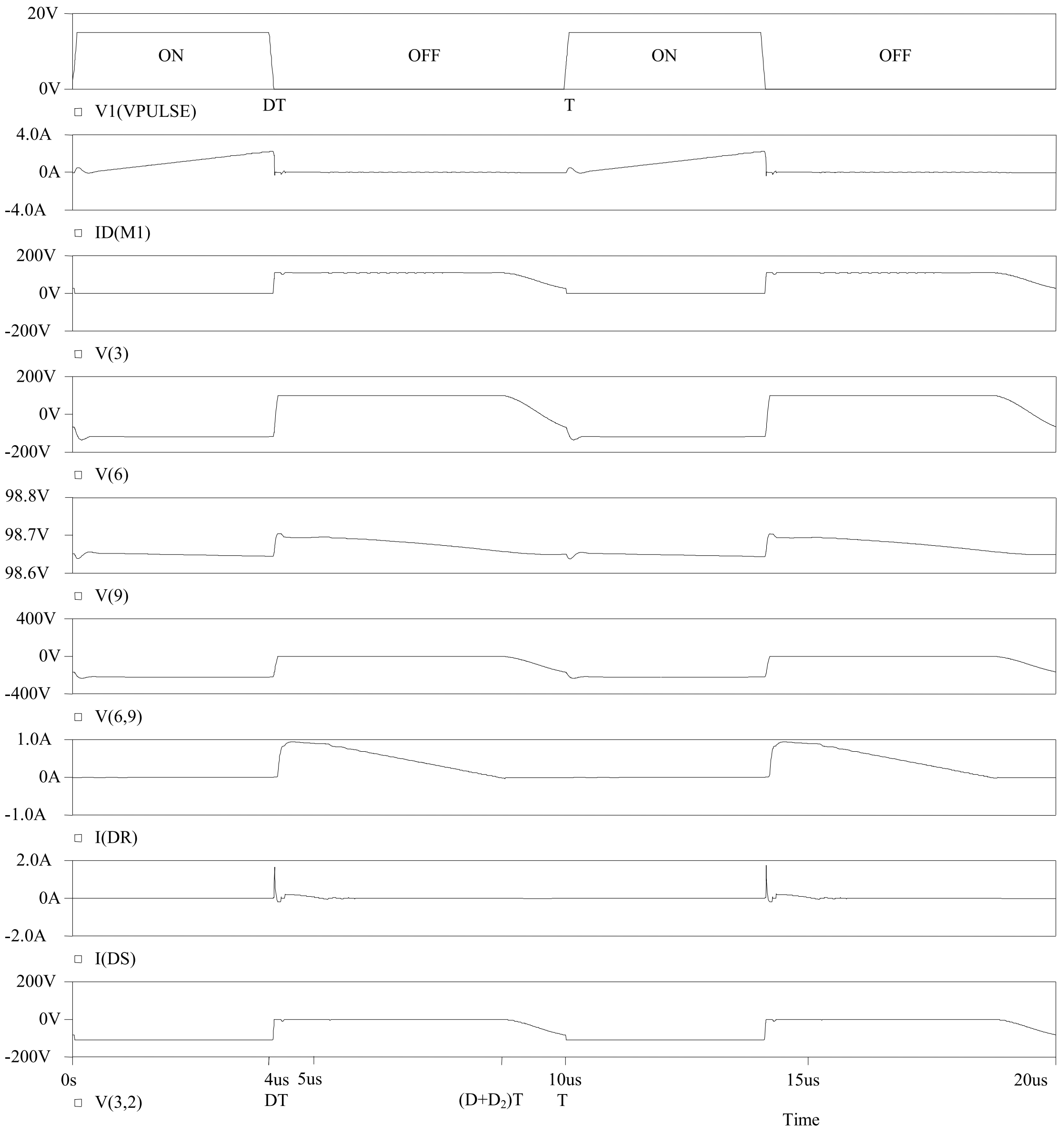

FIGURE 10.41 Waveforms of practical flyback converter for discontinuous-mode operation.

shown in Fig. 10.41, where the following assumptions are made:

- D_R and D_S are MUR460 ultra-fast diodes;
- M_1 is an IRF640 MOS transistor;
- transformer T_1 has a practical coupling coefficient of 0.992;
- the effective winding resistance of L_P is 0.025 Ω and the effective winding resistance of L_S is 0.1 Ω;
- the effective series resistance of the output filtering capacitor C_L is 0.05 Ω; and
- the switching operation of the converter has reached a steady state.

The waveforms shown in Fig. 10.41 are considered to be acceptable.

10.6.3 Design Considerations

It is necessary for the designer of rectifier circuits to determine the voltage and current ratings of the diodes. The idealized waveforms and expressions for the maximum diode voltages and currents given in Section 10.6.2.1 (for both forward and flyback converters) are a good starting point. However, when parasitic/stray components are also considered, the simulation results given in Section 10.6.1.6 are much more useful for determination of the voltage and current ratings of high-frequency rectifier diodes.

Assuming that the voltage and current ratings have been determined, diodes can be selected that meet the requirements. The following are some general guidelines on the selection of diodes:

- For low-voltage applications, Schottky diodes should be used because they have very fast switching speed and low forward voltage drop. If Schottky diodes cannot be used, either because of their low reverse breakdown voltage or because of their large leakage current (when reversely biased), ultra-fast diodes should be used.
- The reverse breakdown-voltage rating of the diode should be reasonably higher (e.g., 10 or 20 higher) than the maximum reverse voltage the diode is expected to encounter under the worst-case condition. However, an overly conservative design (using a diode with much higher breakdown voltage than necessary) would result in a lower rectifier efficiency, because a diode having a higher reverse-voltage rating would normally have a larger voltage drop when it is conducting.
- The current rating of the diode should be substantially higher than the maximum current the diode is expected to carry during normal operation. Using a diode with a relatively large current rating has the following advantages:
  (i) It reduces the possibility of damage due to transients caused by start-up, accidental short circuit, or random turning on and off of the converter.
  (ii) It reduces the forward voltage drop because the diode is operated in the lower current region of the V-I characteristic.

In some of the "high-efficiency" converter circuits, the current rating of the output rectifier can be many times larger than the actual current expected in the rectifier. In this way, higher efficiency is achieved at the expense of a larger silicon area.

In the design of RC snubber circuits for rectifiers, it should be understood that a larger C (and a smaller R) will give better damping. However, a large C (and a small R) will result in a large switching loss (which is equal to 0.5 CV^2f). As a guideline, a capacitor with 5 to 10 times the junction capacitance of the rectifier may be used as a starting point for iterations. The resistor chosen should be able to provide a slightly underdamped operating condition.

1 .6.4 Precautions in Interpreting Simulation Results

In using the simulated waveforms as references for design purposes, attention should be paid to the following:

- The voltage/current spikes that appear in those waveforms measured under actual conditions may not appear in the simulated waveforms. This is due to the lack of a model in computer simulation that is able to simulate unwanted coupling among the practical components.
- Most of the computer models of diodes, including those used in the simulations given here, do not take into account the effects of forward recovery time. (The forward recovery time is not even mentioned in most manufacturers' data sheets.) However, it is also interesting to note that in most cases the effect of forward recovery time of a diode is masked by that of the effective inductance in series with the diode (e.g., the leakage inductance of a transformer).

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11

Single Phase Controlled Rectifiers

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11.1 Line Commutated Single-Phase Controlled Rectifiers

11.1.1 Single-Phase Half-Wave Rectifier

As shown in Fig. 11.1, the single-phase half-wave rectifier uses a single thyristor to control the load voltage. The thyristor will conduct, ON state, when the voltage v_T is positive and a firing current pulse i_G is applied to the gate terminal. Delaying the firing pulse by an angle α does the control of the load voltage. The firing angle α is measured from the position where a diode would naturally conduct. In Fig. 11.1 the angle α is measured from the zero crossing point of the supply voltage v_s. The load in Fig. 11.1 is resistive and therefore current i_d has the same waveform as the load voltage. The thyristor goes to the nonconducting condition, OFF state, when the load voltage and, consequently, the current try to reach a negative value.

The load average voltage is given by:

$$V_{d\alpha} = \frac{1}{2\pi}\int_{\alpha}^{\pi} V_{\max}\sin\omega t d(\omega t) = \frac{V_{\max}}{2\pi}(1+\cos\alpha) \tag{11.1}$$

where $V_{\max}$ is the supply peak voltage. Hence, it can be seen from Eq. (11.1) that changing the firing angle α controls both the load average voltage and the power flow. Figure 11.2a shows the rectifier waveforms for an $R-L$ load. When the thyristor is turned ON, the voltage across the inductance is

$$v_L = v_S - v_R = L\frac{di_d}{dt} \tag{11.2}$$

The voltage in the resistance R is $v_R = R \cdot i_d$. While $v_S - v_R > 0$, Eq. (11.2) shows that the load current increases its value. On the other hand, i_d decreases its value when $v_S - v_R < 0$. The load current is given by

$$i_d(\omega t) = \frac{1}{\omega L}\int_{\alpha}^{\omega t} v_L d\theta \tag{11.3}$$

Graphically, Eq. (11.3) means that the load current i_d is equal to zero when $A_1 = A_2$, maintaining the thyristor in conduction state even when $v_s < 0$.

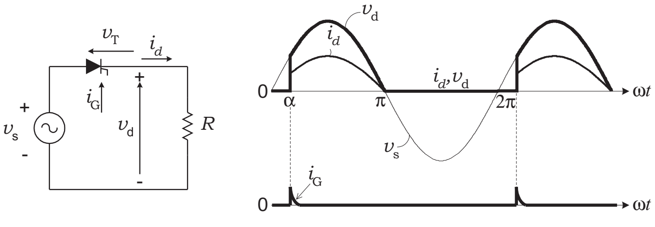

FIGURE 11.1 Single thyristor rectifier with resistive load.

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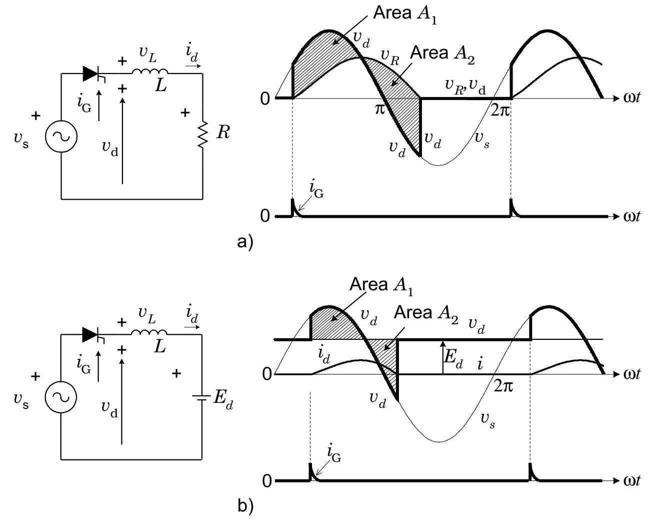


FIGURE 11.2 Single thyristor rectifier with: (a) resistive-inductive load; and (b) active load.

When an inductive-active load is connected to the rectifier, as depicted in Fig. 11.2b, the thyristor will be turned ON if the firing pulse is applied to the gate when $v_s > E_d$. Again, the thyristor will remain in the ON state until $A_1 = A_2$. When the thyristor is turned OFF, the load voltage will be $v_d = E_d$.

11.1.2 Biphase Half-Wave Rectifier

The biphase half-wave rectifier shown in Fig. 11.3 uses a center-tapped transformer to provide two voltages v_1 and v_2. These two voltages are 180° out-of-phase with respect to the mid-point neutral N. In this scheme, the load is fed via a thyristor in each positive cycle of voltages v_1 and v_2 and the load current returns via the neutral N.

With reference to Fig. 11.3, thyristor T_1 can be fired into the ON state at any time provided that voltage $v_{T1} > 0$. The firing pulses are delayed by an angle α with respect to the instant where diodes would conduct. Figure 11.3 also illustrates the current paths for each conduction state. Thyristor T_1 remains in the ON state until the load current tries to go to a negative value. Thyristor T_2 is fired into the ON state when $v_{T2} > 0$, which corresponds in Fig. 11.3 to the condition at which $v_2 > 0$.

The mean value of the load voltage with resistive load is given by

$$V_{d\alpha} = \frac{1}{\pi}\int_{\alpha}^{\pi} V_{\max} \sin \omega t d(\omega t) = \frac{V_{\max}}{\pi}(1 + \cos\alpha) \qquad (11.4)$$

The ac supply current is equal to $i_{T1}(N_2/N_1)$ when T_1 is in the on-state and $-i_{T2}(N_2/N_1)$ when T_2 is in the on-state, where N_2/N_1 is the transformer turns ratio.

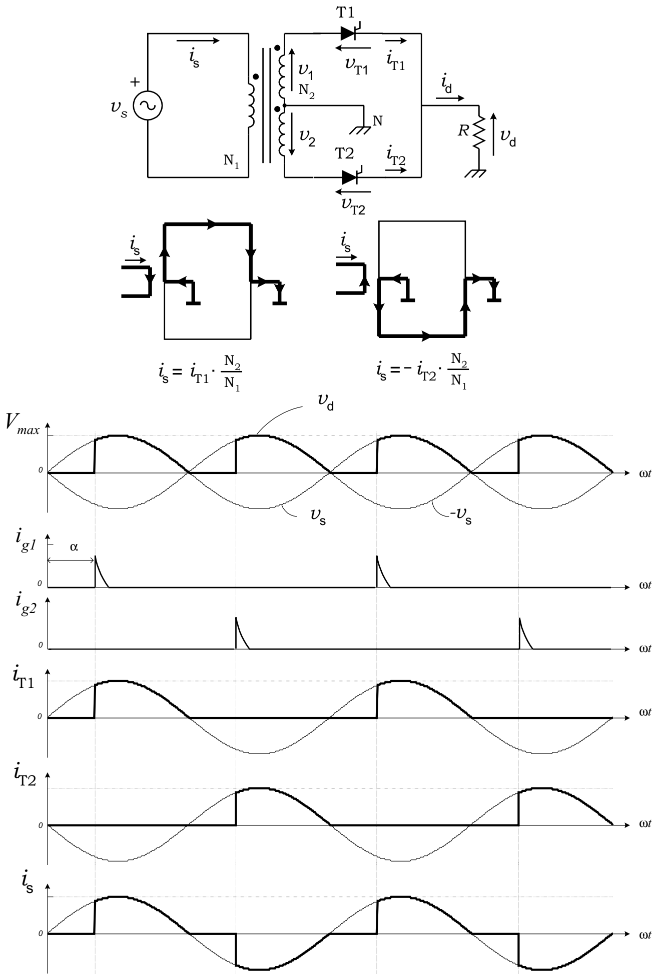


FIGURE 11.3 Biphase half-wave rectifier.

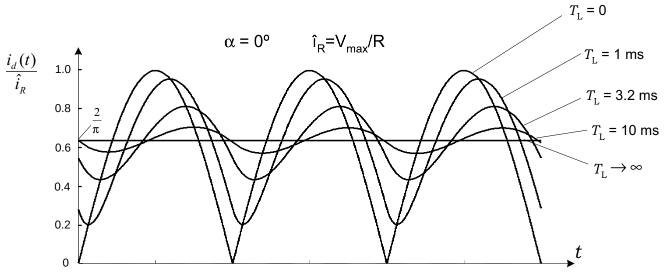
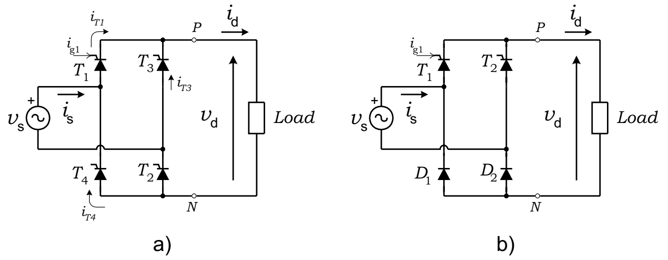


FIGURE 11.4 Effect of the load time constant over the current ripple.

Figure 11.4 shows the effect of the load time constant $T_L = L/R$ on the normalized load current $i_d(t)/\hat{i}_R(t)$ for a firing angle $\alpha = 0°$. The ripple in the load current reduces as the load inductance increases. If the load inductance $L \to \infty$, then the current is perfectly filtered.

11.1.3 Single-Phase Bridge Rectifier

Figure 11.5a shows a fully controlled bridge rectifier, which uses four thyristors to control the average load voltage. In



a) b)

FIGURE 11.5 Single-phase bridge rectifier: (a) fully controlled; and (b) half controlled.

addition, Fig. 11.5b shows the half-controlled bridge rectifier, which uses two thyristors and two diodes.

Figure 11.6 shows the voltage and current waveforms of the fully controlled bridge rectifier for a resistive load. Thyristors T_1 and T_2 must be fired simultaneously during the positive half wave of the source voltage v_s so as to allow conduction of current. Alternatively, thyristors T_3 and T_4 must be fired simultaneously during the negative half wave of the source voltage. To ensure simultaneous firing, thyristors T_1 and T_2 use the same firing signal. The load voltage is similar to the voltage obtained with the biphase half-wave rectifier. The input current is given by

$$i_S = i_{T1} - i_{T4} \tag{11.5}$$

and its waveform is shown in Fig. 11.6.

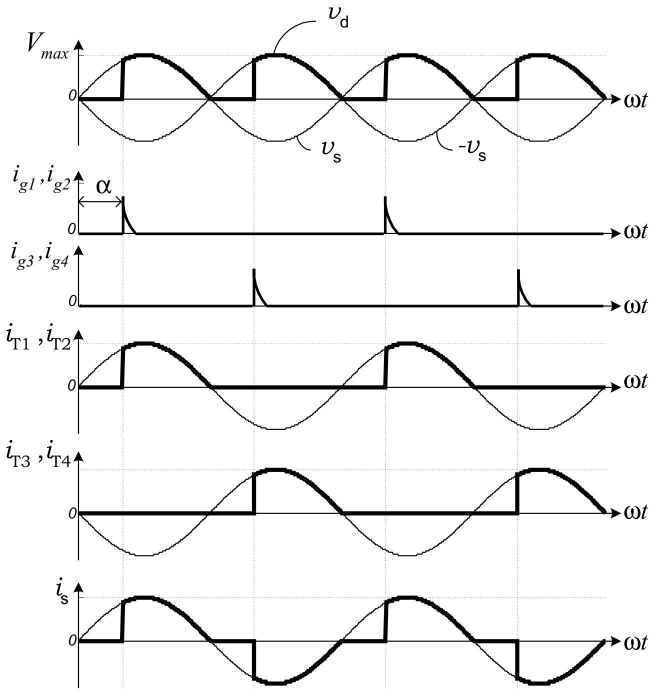


FIGURE 11.6 Waveforms of a fully controlled bridge rectifier with resistive load.

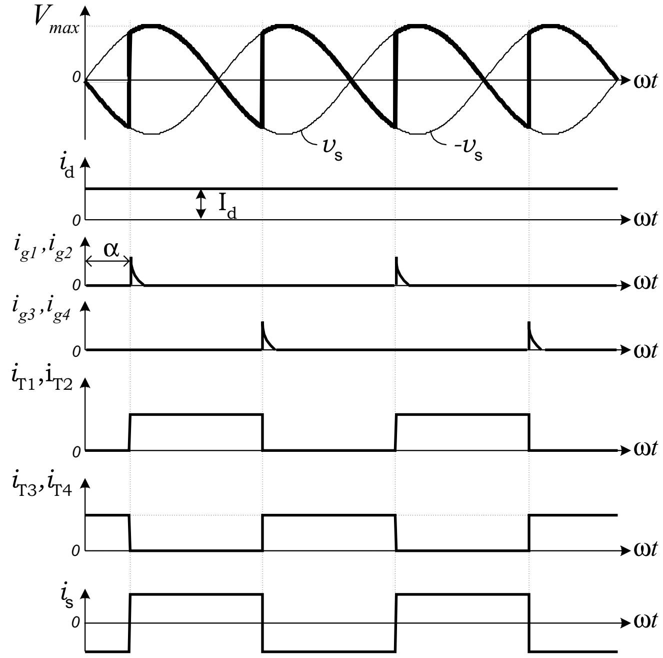


FIGURE 11.7 Waveforms of a fully controlled bridge rectifier with resistive-inductive load ($L \rightarrow \infty$).

Figure 11.7 presents the behavior of the fully controlled rectifier with resistive-inductive load (with $L \rightarrow \infty$). The high-load inductance generates a perfectly filtered current and the rectifier behaves like a current source. With continuous load current, thyristors T_1 and T_2 remain in the on-state beyond the positive half-wave of the source voltage v_s. For this reason, the load voltage v_d can have a negative instantaneous value. The firing of thyristors T_3 and T_4 has two effects:

i) they turn off thyristors T_1 and T_2; and
ii) after the commutation they conduct the load current.

This is the main reason why this type of converter is called a "naturally commutated" or "line commutated" rectifier. The supply current i_S has the square waveform shown in Fig. 11.7 for continuous conduction. In this case, the average load voltage is given by

$$V_{d\alpha} = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} V_{\max}\sin\omega t d(\omega t) = \frac{2V_{\max}}{\pi}\cos\alpha \tag{11.6}$$

11.1.4 Analysis of the Input Current

The input current in a bridge-controlled rectifier is a square waveform when the load current is perfectly filtered. In addition, the input current i_s is shifted by the firing angle α with respect to the input voltage v_s, as shown in Fig. 11.8a. The input current can be expressed as a Fourier series, where the amplitude of the different harmonics is given by

$$I_{s\max n} = \frac{4}{\pi}\frac{I_d}{n} \qquad (n = 1, 3, 5, \ldots) \tag{11.7}$$

where n is the harmonic order. The root mean square (rms) value of each harmonic can be expressed as

$$I_{sn} = \frac{I_{s\max n}}{\sqrt{2}} = \frac{2\sqrt{2}}{\pi}\frac{I_d}{n} \tag{11.8}$$

Thus, the rms value of the fundamental current i_{s1} is

$$I_{s1} = \frac{2\sqrt{2}}{\pi} I_d = 0.9 I_d \tag{11.9}$$

It can be observed from Fig. 11.8a that the displacement angle ϕ_1 of the fundamental current i_{s1} corresponds to the firing angle α. Fig. 11.8b shows that in the harmonic spectrum of the input current, only odd harmonics are present with decreasing amplitude. The rms value of the input current i_s is

$$I_s = I_d \tag{11.10}$$

The total harmonic distortion (THD) of the input current is given by

$$\mathrm{THD} = \frac{\sqrt{I_s^2 - I_{s1}^2}}{I_{s1}} 100 = 48.4\% \tag{11.11}$$

11.1.5 Power Factor of the Rectifier

The displacement factor of the fundamental current, obtained from Fig. 11.8a, is

$$\cos\phi_1 = \cos\alpha \tag{11.12}$$

In the case of nonsinusoidal current, the active power delivered by the sinusoidal single-phase supply is

$$P = \frac{1}{T}\int_0^T v_s(t) i_s(t) dt = V_s I_{s1} \cos\phi_1 \tag{11.13}$$

where V_s is the rms value of the single-phase voltage v_s.

The apparent power is given by

$$S = V_s I_s \tag{11.14}$$

The power factor (PF) is defined by

$$\mathrm{PF} = \frac{P}{S} \tag{11.15}$$

Substitution from Eqs. (11.12), (11.13), and (11.14) in Eq. (11.15) yields:

$$\mathrm{PF} = \frac{I_{s1}}{I_s}\cos\alpha \tag{11.16}$$

This equation shows clearly that due to the nonsinusoidal waveform of the input current, the power factor of the rectifier is negatively affected by both the firing angle α and the distortion of the input current. In effect, an increase in the

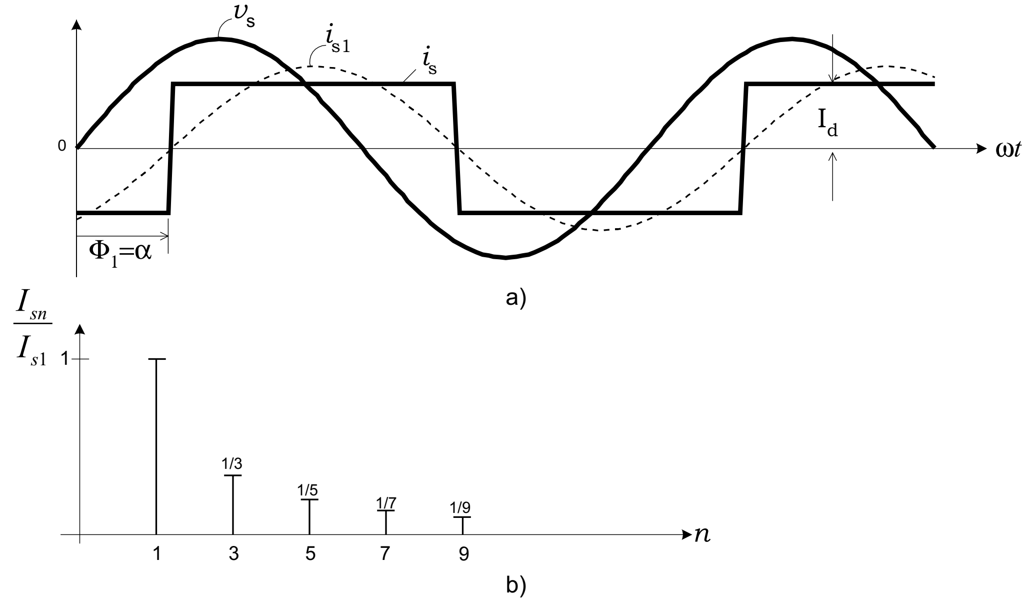


FIGURE 11.8 Input current of the single-phase controlled rectifier in bridge connection: (a) waveforms; and (b) harmonics spectrum.

distortion of the current produces an increase in the value of I_s in Eq. (11.16), which deteriorates the power factor.

11.1.6 The Commutation of the Thyristors

Until now the current commutation between thyristors has been considered to be instantaneous. This consideration is not valid in real cases due to the presence of the line inductance L, as shown in Fig. 11.9a. During commutation, the current through the thyristors cannot change instantaneously, and for this reason, during the commutation angle μ, all four thyristors are conducting simultaneously. Therefore, during the commutation the following relationship for the load voltage holds:

$$v_d = 0 \qquad \alpha \leq \omega t \leq \alpha + \mu \tag{11.17}$$

The effect of the commutation on the supply current, voltage waveforms, and the thyristor current waveforms is observed in Fig. 11.9b.

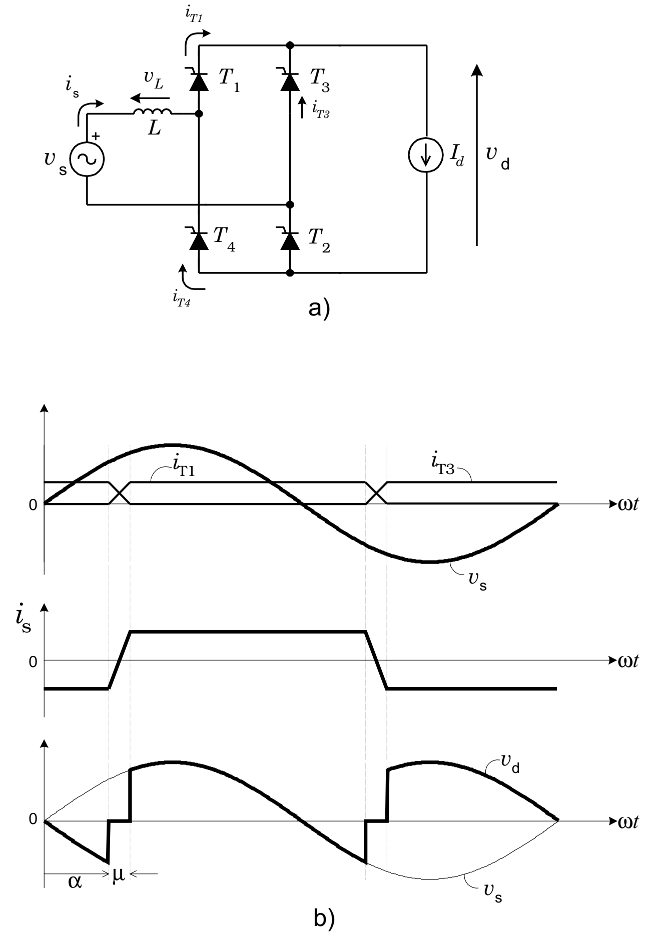


FIGURE 11.9 The commutation process: (a) circuit; and (b) waveforms.

During commutation the following expression holds:

$$L\frac{di_s}{dt} = v_s = V_{\max} \sin \omega t \qquad \alpha \leq \omega t \leq \alpha + \mu \tag{11.18}$$

Integrating Eq. (11.18) over the commutation interval yields

$$\int_{-I_d}^{I_d} di_s = \frac{V_{\max}}{L} \int_{\alpha/\omega}^{\alpha+\mu/\omega} \sin \omega t dt \tag{11.19}$$

From Eq. (11.19), the following relationship for the commutation angle μ is obtained:

$$\cos(\alpha + \mu) = \cos \alpha - \frac{2\omega L}{V_{\max}} I_d \tag{11.20}$$

Equation (11.20) shows that an increase of the line inductance L or an increase of the load current I_d increases the commutation angle μ. In addition, the commutation angle is affected by the firing angle α. In effect, Eq. (11.18) shows that with different values of α, the supply voltage v_s has a different instantaneous value, which produces different di_s/dt, thereby affecting the duration of the commutation.

Equation (11.17) and the waveform of Fig. 11.9b show that the commutation process reduces the average load voltage $V_{d\alpha}$. When commutation is considered, the expression for the average load voltage is given by

$$V_{d\alpha} = \frac{1}{\pi} \int_{\alpha+\mu}^{\pi+\alpha} V_{\max} \sin \omega t d(\omega t) = \frac{V_{\max}}{\pi} [\cos(\alpha + \mu) + \cos \alpha] \tag{11.21}$$

Substituting Eq. (11.20) into Eq. (11.21) yields

$$V_{d\alpha} = \frac{2}{\pi} V_{\max} \cos \alpha - \frac{2\omega L}{\pi} I_d \tag{11.22}$$

11.1.7 Operation in the Inverting Mode

When the angle $\alpha > 90°$, it is possible to obtain a negative average load voltage. In this condition, the power is fed back to the single-phase supply from the load. This operating mode is called inverter or inverting mode, because the energy is transferred from the dc to the ac side. In practical cases this operating mode is obtained when the load configuration is as shown in Fig. 11.10a. It must be noticed that this rectifier allows unidirectional load current flow.

Figure 11.10b shows the waveform of the load voltage with the rectifier in the inverting mode, neglecting the source inductance L.

Section 11.1.6 described how supply inductance increases the conduction interval of the thyristors by the angle μ. As

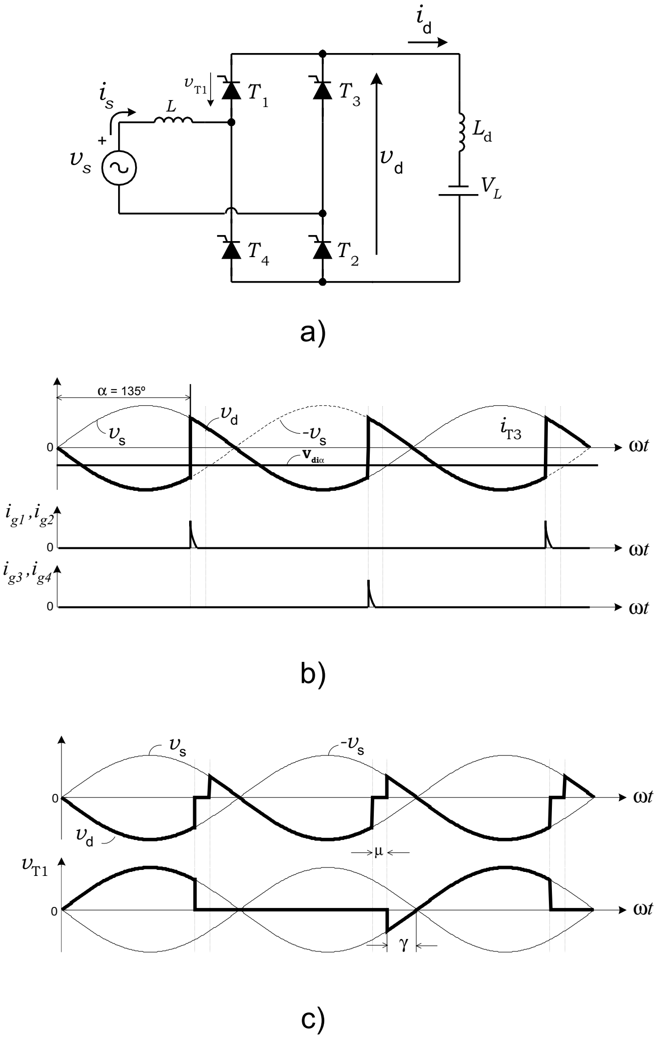


FIGURE 11.10 Rectifier in the inverting mode: (a) circuit; (b) waveforms neglecting source inductance L; and (c) waveforms considering L.

shown in Fig. 11.10c, the thyristor voltage v_{T1} has a negative value during the extinction angle γ, defined by

$$\gamma = 180 - (\alpha + \mu) \tag{11.23}$$

To ensure that the outgoing thyristor will recover its blocking capability after commutation, the extinction angle should satisfy the following restriction:

$$\gamma > \omega t_q \tag{11.24}$$

where ω is the supply frequency and t_q is the thyristor turn-off time. Considering Eqs. (11.23) and (11.24) the maximum firing angle is, in practice,

$$\alpha_{\max} = 180 - \mu - \gamma \tag{11.25}$$

If the condition of Eq. (11.25) is not satisfied, the commutation process will fail and then destructive currents will occur.

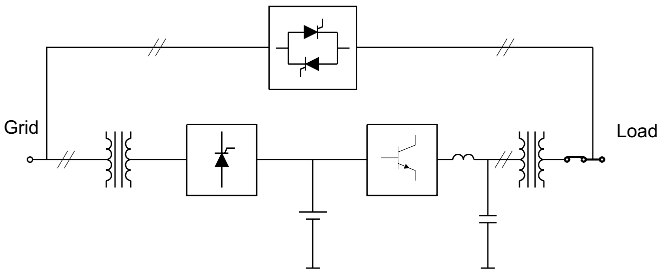


FIGURE 11.11 Application of a rectifier in single-phase UPS.

11.1.8 Applications

Important application areas of controlled rectifiers include uninterruptible power supplies (UPS) for feeding critical loads. Figure 11.11 shows a simplified diagram of a single-phase UPS configuration, typically rated for $< 10\,\mathrm{kVA}$. A fully controlled or half-controlled rectifier is used to generate the dc voltage for the inverter. In addition, the input rectifier acts as a battery charger. The output of the inverter is filtered before it is fed to the load. The most important operational modes of the UPS are:

i) Normal mode. In this case the line voltage is present. The critical load is fed through the rectifier-inverter scheme. The rectifier keeps the battery charged.
ii) Outage mode. During a loss of the ac main supply, the battery provides the energy for the inverter.
iii) Bypass operation. When the load demands an overcurrent to the inverter, the static bypass switch is turned on and the critical load is fed directly from the mains.

The control of low-power dc motors is another interesting application of controlled single-phase rectifiers. In the circuit of Fig. 11.12, the controlled rectifier regulates the armature voltage and consequently controls the motor current i_d in order to establish a required torque.

This configuration allows only positive current flow in the load. However, the load voltage can be both positive and negative. For this reason, this converter works in the two-quadrant mode of operation in the plane i_d vs $V_{d\alpha}$.

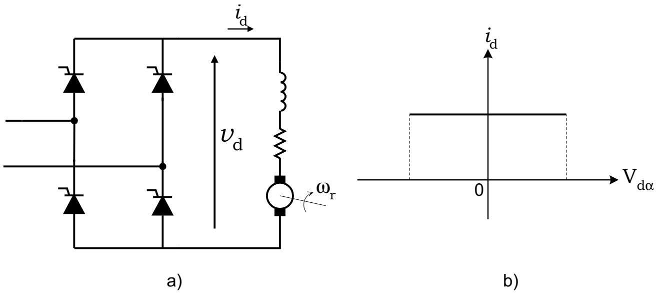


FIGURE 11.12 Two quadrant dc drive: (a) circuit; and (b) quadrants of operation.

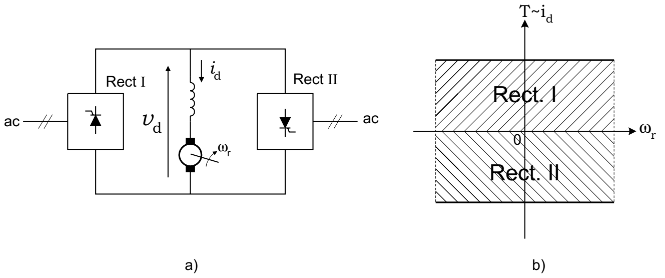


FIGURE 11.13 Single-phase dual-converter drive: (a) connection; and (b) four-quadrant operation.

As shown in Fig. 11.13, a better performance can be obtained with two rectifiers in back-to-back connection at the dc terminals. This arrangement, known as a dual converter one, allows four-quadrant operation of the drive. Rectifier I provides positive load current i_d, while rectifier II provides negative load current. The motor can work in forward powering, forward braking (regenerating), reverse powering, and reverse braking (regenerating). These operating modes are shown in Fig. 11.13b, where the torque T vs the rotor speed ω_R is illustrated.

11.2 Unity Power Factor Single-Phase Rectifiers

11.2.1 The Problem of Power Factor in Single-Phase Line-Commutated Rectifiers

The main disadvantages of classical line-commutated rectifiers are that

i) they generate both a lagging displacement factor with respect to the voltage of the utility, and
ii) an important amount of input current harmonics.

These aspects have a negative influence on both power factor and power quality. In the last several years, the massive use of single-phase power converters has increased the problems of power quality in electrical systems. In effect, modern commercial buildings have 50% and even up to 90% of the demand originated by nonlinear loads, which are composed mainly of rectifiers [1]. Today it is not unusual to find rectifiers with total harmonic distortion of the current $\mathrm{THD}_i > 40\%$ originating severe overloads in conductors and transformers.

Figure 11.14 shows a single-phase rectifier with a capacitive filter, used in much of today's low power equipment. The input current is highly distorted due to the presence of the filter capacitor. This current has a harmonic content as shown in Fig. 11.15 and Table 11.1, with a $\mathrm{THD}_i = 197\%$.

The rectifier of Fig. 11.14 has a very low power factor of $\mathrm{PF} = 0.45$, due mainly to its large harmonic content.

11.2.2 Standards for Harmonics in Single-Phase Rectifiers

The relevance of the problems originated by harmonics in line-commutated single-phase rectifiers has motivated some agencies to introduce restrictions to these converters. The IEC 1000-3-2 International Standard establishes limits to all low-power single-phase equipment having an input current with a "special wave shape" and an active input power $P \leq 600\,\mathrm{W}$. Class D equipment has an input current with a special wave shape contained within the envelope given in Fig. 11.14b. This class of equipment must satisfy certain harmonic limits, shown in Fig. 11.15. It is clear that a single-phase line-commutated rectifier with parameters as shown in Fig. 11.14a is not able to comply with the standard IEC 1000-3-2 Class D. The standard can be satisfied only by adding huge passive filters, which increases the size, weight, and cost of the

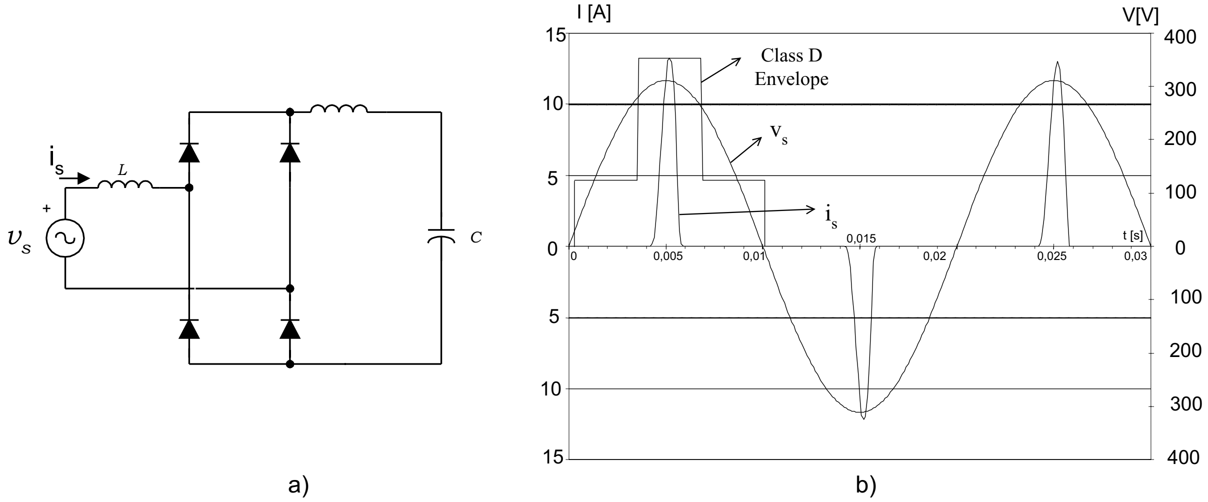


FIGURE 11.14 Single-phase rectifier: (a) circuit; and (b) waveforms of the input voltage and current.

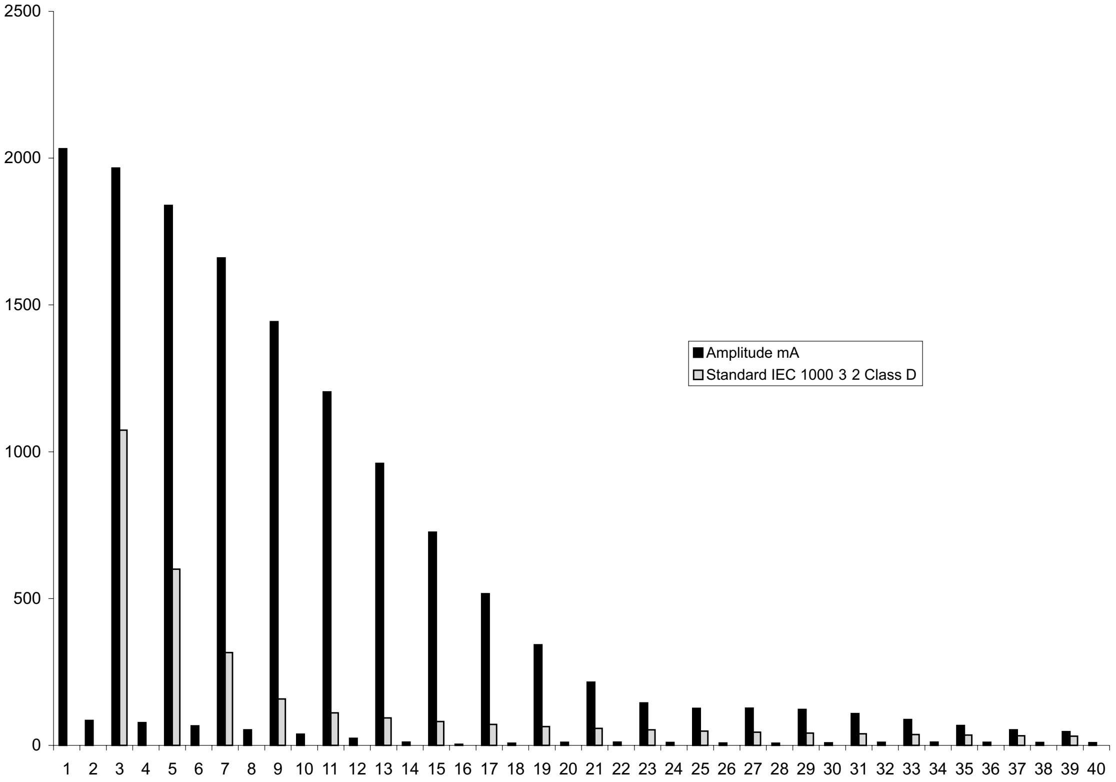


FIGURE 11.15 Harmonics in the input current of the rectifier of Fig. 11.14.

TABLE 11.1 Harmonics in percentage of the current in Fig. 11.14

n	3	5	7	9	11	13	15	17	19	21
$\frac{I_n}{I_1}$ [ ]	96.8	90.5	81.7	71.0	59.3	47.3	35.7	25.4	16.8	10.6

rectifier. This standard has been the motivation for the development of active methods to improve the quality of the input current and, consequently, the power factor.

11.2.3 The Single-Phase Boost Rectifier

From both the theoretical and conceptual points of view, one of the most important high-power factor rectifiers is the so-called single-phase boost rectifier, shown in Fig. 11.16a. This rectifier is obtained from a classical noncontrolled bridge rectifier, with the addition of transistor T, diode D, and inductor L.

In this rectifier, the input current $i_s(t)$ is controlled by changing the conduction state of transistor T. When transistor T is in the ON state, the single-phase power supply is short-circuited through the inductance L, as shown in Fig. 11.16b; the diode D avoids the discharge of the filter capacitor C through the transistor. The current of the inductance i_L is given by the following equation

$$\frac{di_L}{dt} = \frac{v_L}{L} = \frac{|v_s|}{L} \tag{11.26}$$

Due to the fact that $|v_s| > 0$, the ON state of transistor T always produces an increase in the inductance current i_L and,

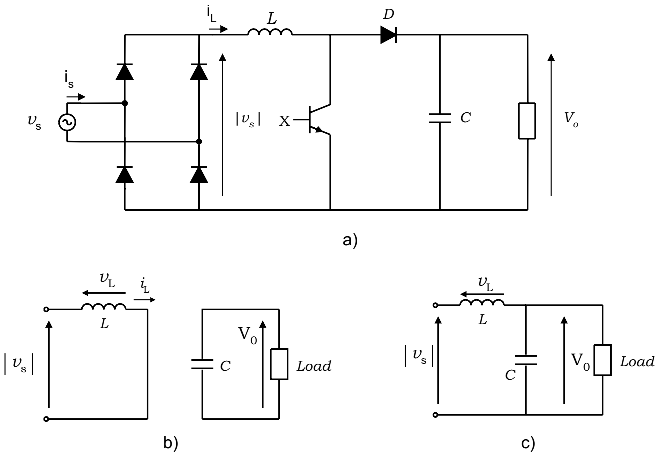


FIGURE 11.16 Single-phase boost rectifier: (a) power circuit and equivalent circuit for transistor T in (b) ON-state and (c) OFF-state.

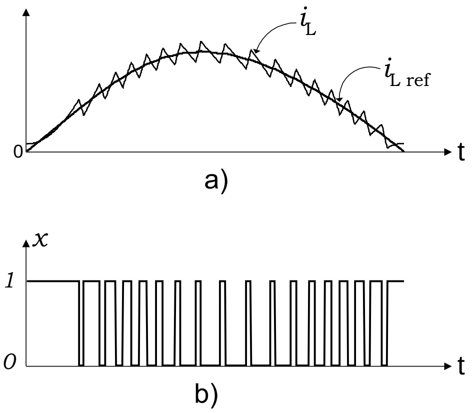


FIGURE 11.17 Behavior of the inductor current i_L: (a) waveforms; and (b) transistor T gate drive signal x.

consequently, an increase in the absolute value of the source current i_s.

When transistor T is turned OFF, the inductor current i_L cannot be interrupted abruptly and flows through diode D, charging capacitor C. This is observed in the equivalent circuit of Fig. 11.16c. In this condition the behavior of the inductor current is described by

$$\frac{di_L}{dt} = \frac{v_L}{L} = \frac{|v_s| - V_o}{L} \tag{11.27}$$

If $V_o > |v_s|$, which is an important condition for the correct behavior of the rectifier, then $|v_s| - V_o < 0$, and this means that in the OFF state the inductor current decreases its instantaneous value.

With an appropriate firing pulse sequence applied to transistor T, the waveform of the input current i_s can be controlled to follow a sinusoidal reference, as can be observed in the positive halfwave of i_s in Fig. 11.17. This figure shows the reference inductor current $i_{L\mathrm{ref}}$, the inductor current i_L, and the gate drive signal x for transistor T. Transistor T is ON when $x =$ "1" and it is OFF when $x =$ "0".

Figure 11.17 clearly shows that the ON(OFF) state of transistor T produces an increase (decrease) in the inductor current i_L.

Figure 11.18 presents a block diagram of the control system for the boost rectifier, which includes a proportional-integral (PI) controller to regulate the output voltage V_o. The reference value $i_{L\mathrm{ref}}$ for the inner current control loop is obtained from the multiplication between the output of the voltage controller and the absolute value $|v_s(t)|$. A hysteresis controller provides a fast control for the inductor current i_L, resulting in a practically sinusoidal input current i_s.

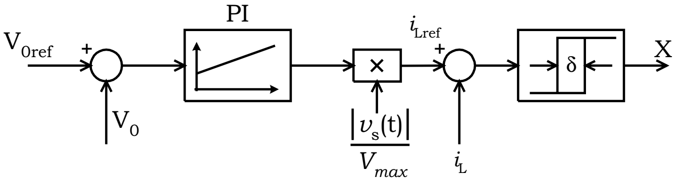


FIGURE 11.18 Control system of the boost rectifier.

Typically, the output voltage V_o should be at least 10 higher than the peak value of the source voltage $v_s(t)$ in order to assure good dynamic control of the current. The control works with the following strategy: a step increase in the reference voltage $V_{o\mathrm{ref}}$ will produce an increase in the voltage error $V_{o\mathrm{ref}} - V_o$ and an increase of the output of the PI controller, which originates an increase in the amplitude of the reference current $i_{L\mathrm{ref}}$. The current controller will follow this new reference and increase the amplitude of the sinusoidal input current i_s, which will increase the active power delivered by the single-phase supply and finally produce an increase in the output voltage V_o.

Figure 11.19a shows the waveform of the input current i_s and the source voltage v_s. The ripple of the input current can be diminished by reducing the hysteresis width δ. The price to be paid for this improvement is an increase in switching frequency, which is proportional to the commutation losses of transistor T. For a given hysteresis width δ, a reduction of inductance L also produces an increase in the switching frequency.

A drastic reduction in the harmonic content of input current i_s can be observed in the frequency spectrum of Fig. 11.19b. This current complies with the restrictions established by IEC standard 1000-3-2. The total harmonic distortion of the current in Fig. 11.19a is $\mathrm{THD} = 4.96$ and the power factor of the rectifier is $\mathrm{PF} = 0.99$.

Figure 11.20 shows the dc voltage control loop dynamic behavior for step changes in the load. An increase in the load, at $t = 0.3$ [s], produces an initial reduction of the output voltage V_o, which is compensated by an increase in the input current i_s. At $t = 0.6$ [s] a step decrease in the load is applied. The dc voltage controller again adjusts the supply current in order to balance the active power.

11.2.4 Voltage Doubler PWM Rectifier

Figure 11.21a shows the power circuit of the voltage doubler pulsewidth modulated (PWM) rectifier, which uses two transistors and two filter capacitors C_1 and C_2. Transistors T_1 and T_2 are switched in complement to control the waveform of input current i_s and output dc voltage V_o. Capacitor voltages V_{C1} and V_{C2} must be higher than the peak value of the input voltage v_s to ensure control of the input current.

The equivalent circuit of this rectifier with transistor T_1 in the ON state is shown in Fig. 11.21b. The inductor voltage dynamic equation is

$$v_L = \frac{di_s}{dt} = v_s(t) - V_{C1} < 0 \tag{11.28}$$

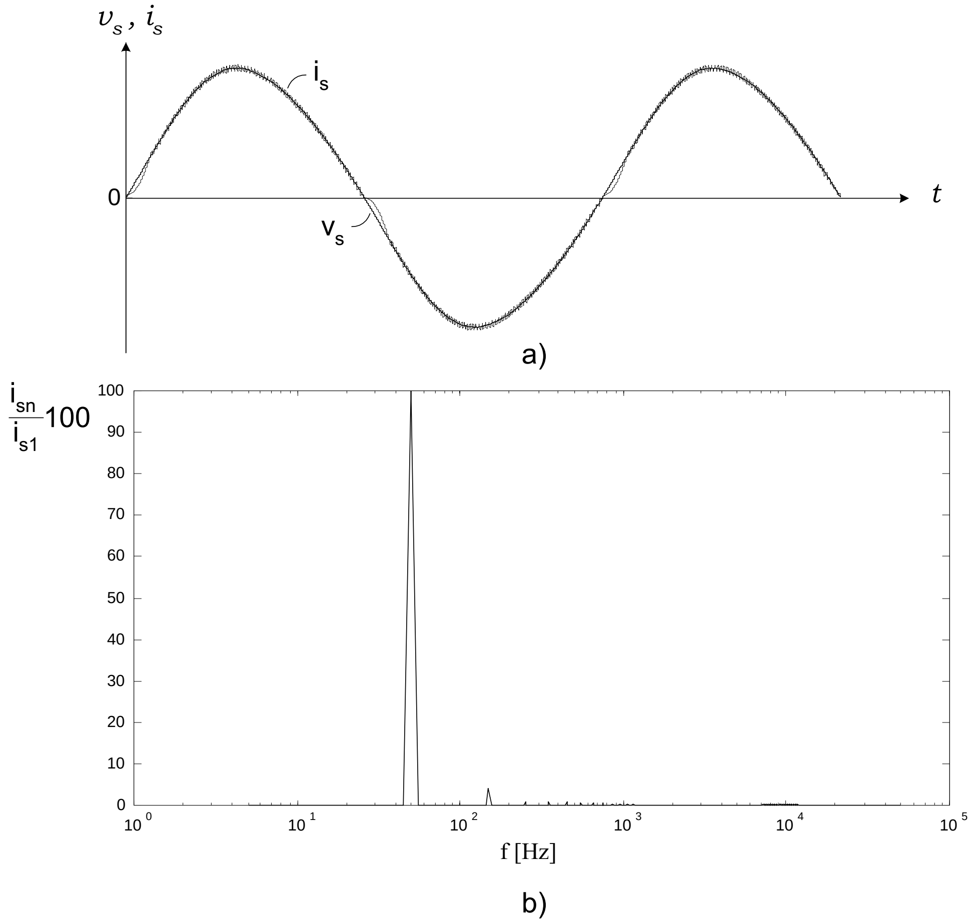


FIGURE 11.19 Input current of the single-phase boost rectifier: (a) voltage and current waveforms; and (b) frequency spectrum.

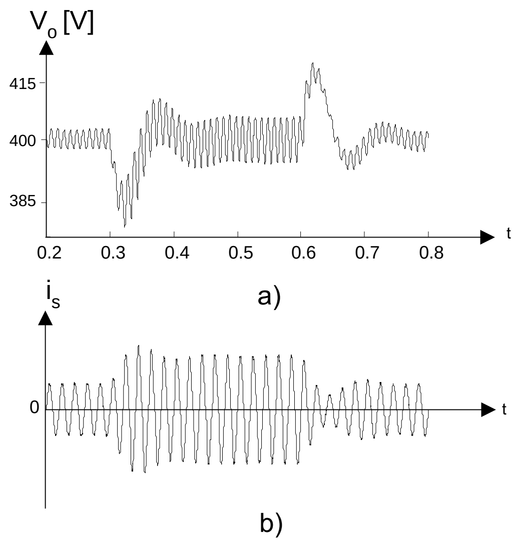


FIGURE 11.20 Response to a change in the load: (a) output-voltage V_o; and (b) input current i_s.

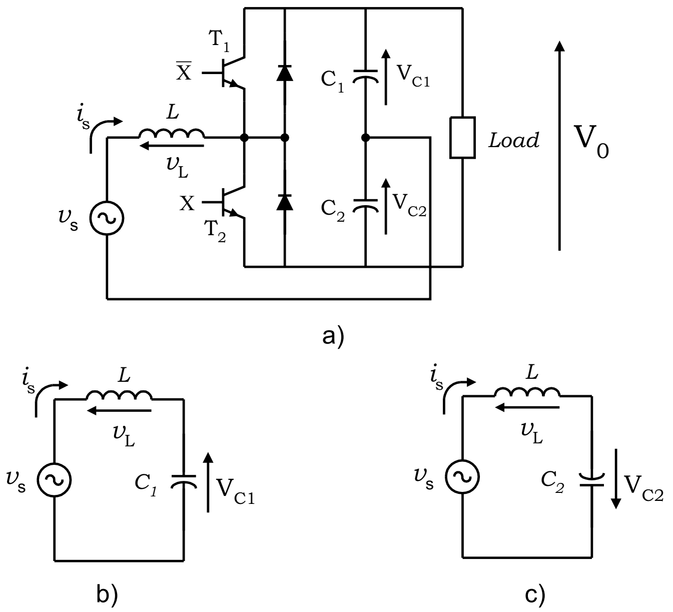

T_1
$\overline{X}$
C_1
V_{C1}
i_s
L
v_L
Load
V_0
X
T_2
C_2
V_{C2}
v_s
a)
i_s
L
v_L
v_s
C_1
V_{C1}
b)
i_s
L
v_L
v_s
C_2
V_{C2}
c)

FIGURE 11.21 Voltage doubler rectifier: (a) power circuit; (b) equivalent circuit with T_1 ON; and (c) equivalent circuit with T_2 ON.

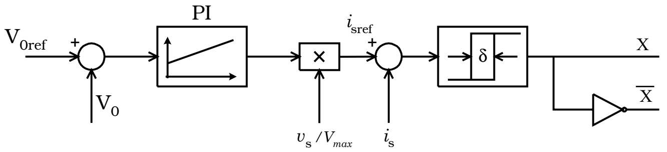


FIGURE 11.22 Control system of the voltage doubler rectifier.

Equation (11.28) means that under this conduction state, current $i_s(t)$ decreases its value.

On the other hand, the equivalent circuit of Fig. 11.21c is valid when transistor T_2 is in the conduction state, resulting in the following expression for the inductor voltage

$$v_L = L\frac{di_s}{dt} = v_s(t) + V_{C2} > 0 \tag{11.29}$$

hence, for this condition the input current $i_s(t)$ increases.

Therefore, the waveform of the input current can be controlled by appropriately switching transistors T_1 and T_2 in a similar way as shown in Fig. 11.17a for the single-phase boost converter. Figure 11.22 shows a block diagram of the control system for the voltage doubler rectifier, which is very similar to the control scheme of the boost rectifier. This topology can present an unbalance in the capacitor voltages V_{C1} and V_{C2}, which will affect the quality of the control. This problem is solved by adding to the actual current value i_s an offset signal proportional to the capacitor voltages difference.

Figure 11.23 shows the waveform of the input current. The ripple amplitude of this current can be reduced by decreasing the hysteresis of the controller.

11.2.5 The PWM Rectifier in Bridge Connection

Figure 11.24a shows the power circuit of the fully controlled single-phase PWM rectifier in bridge connection, which uses four transistors with antiparallel diodes to produce a controlled dc voltage V_o. Using a bipolar PWM switching strategy, this converter may have two conduction states:

i) transistors T_1 and T_4 in the ON state and T_2 and T_3 in the OFF state; or
ii) transistors T_2 and T_3 in the ON state and T_1 and T_4 in the OFF state.

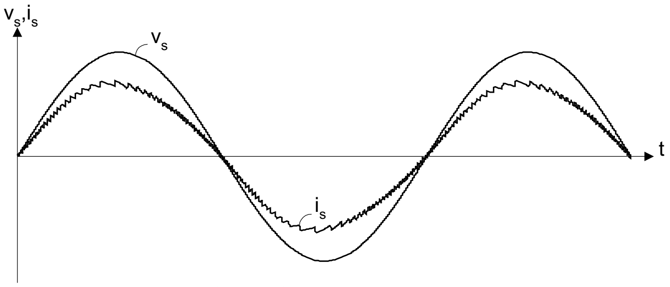


FIGURE 11.23 Waveform of the input current in the voltage doubler rectifier.

In this topology, the output voltage V_o must be higher than the peak value of the ac source voltage v_s in order to ensure proper control of the input current.

Figure 11.24b shows the equivalent circuit with transistors T_1 and T_4 ON. In this condition, the inductor voltage is given by

$$v_L = L\frac{di_s}{dt} = v_s(t) - V_0 < 0 \tag{11.30}$$

Therefore, in this condition a decrease in the inductor current i_s is produced.

Figure 11.24c shows the equivalent circuit with transistors T_2 and T_3 ON. Here, the inductor voltage has the following expression

$$v_L = L\frac{di_s}{dt} = v_s(t) + V_0 > 0 \tag{11.31}$$

which means an increase in the instantaneous value of the input current i_s.

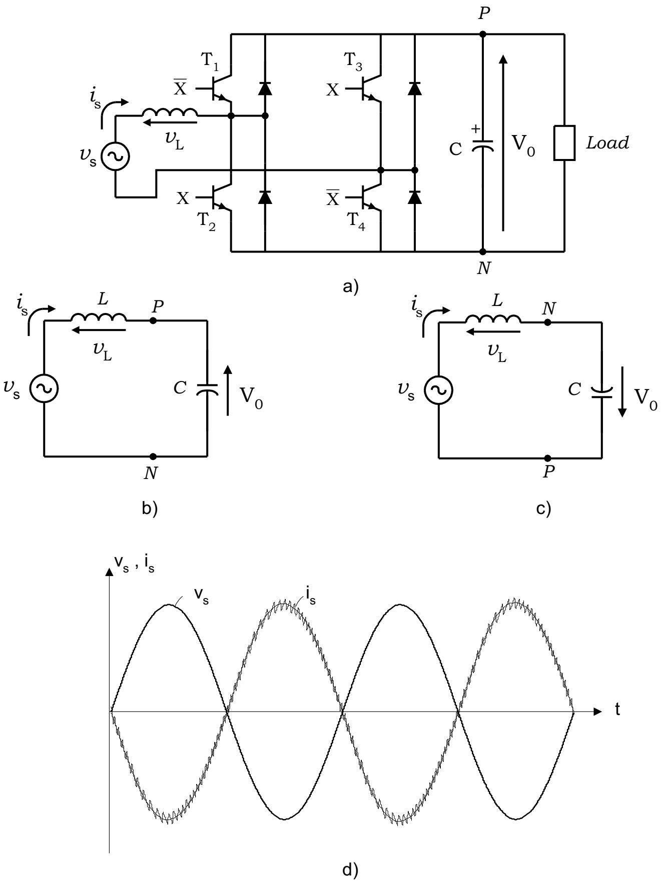


FIGURE 11.24 Single-phase PWM rectifier in bridge connection: (a) circuit; (b) equivalent circuit with T_1 and T_4 ON; (c) equivalent circuit with T_2 and T_3 ON; and (d) waveform of the input current during regeneration.

The waveform of the input current i_s can be controlled by appropriately switching transistors T_1-T_4 or T_2-T_3, creating a shape similar to the one shown in Fig. 11.17a for the single-phase boost rectifier.

The control strategy for the rectifier is similar to the one depicted in Fig. 11.22 for the voltage doubler topology. The quality of the input current obtained with this rectifier is the same as that presented in Fig. 11.23 for the voltage doubler configuration.

Finally, it must be said that one of the most attractive characteristics of the fully controlled PWM converter in bridge connection and the voltage doubler is their regeneration capability. In effect, these rectifiers can deliver power from the load to the single-phase supply, operating with sinusoidal current and a high power factor of PF > 0.99. Figure 11.24d shows that during regeneration the input current i_s is 180° out-of-phase with respect to the supply voltage v_s, which means operation with power factor PF ≈ -1 (PF is near to 1 because of the small harmonic content in the input current).

11.2.6 Applications of Unity Power Factor Rectifiers

11.2.6.1 Boost Rectifier

The single-phase boost rectifier has become the most popular topology for power factor correction (PFC) in general purpose power supplies. To reduce costs, the complete control system shown in Fig. 11.18 and the gate drive circuit of the power transistor have been included in a single integrated circuit (IC), such as the UC3854 [2] or MC33262, shown in Fig. 11.25.

Today there is increased interest in developing high-frequency electronic ballasts to replace the classical electromagnetic ballast in fluorescent lamps. These electronic ballasts require an ac–dc converter. To satisfy the harmonic current injection from electronic equipment and to maintain high power quality, a high-power factor rectifier can be used, as shown in Fig. 11.26 [3].

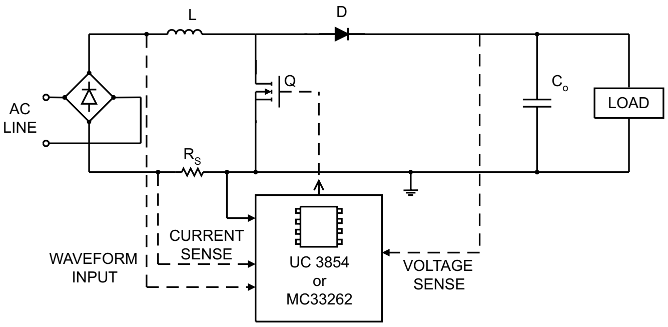


FIGURE 11.25 Simplified circuit of a power factor corrector with control integrated circuit.

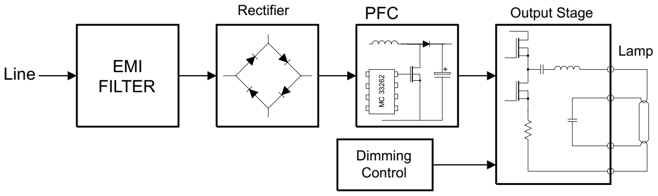


FIGURE 11.26 Functional block diagram of electronic ballast with power factor correction.

11.2.6.2 Voltage Doubler PWM Rectifier

The development of low-cost compact motor drive systems is a very relevant topic, particularly in the low-power range. Figure 11.27 shows a low-cost converter for low-power induction motor drives. In this configuration a three-phase induction motor is fed through the converter from a single-phase power supply. Transistors T_1, T_2 and capacitors C_1, C_2 constitute the voltage-doubler single-phase rectifier, which controls the dc link voltage and generates sinusoidal input current, working with a close-to-unity power factor [4]. On the other hand, transistors T_3, T_4, T_5, and T_6 and capacitors C_1 and C_2 constitute the power circuit of an asymmetric inverter that supplies the motor. An important characteristic of the power circuit shown in Fig. 11.27 is the capability of regenerating power to the single-phase mains.

11.2.6.3 PWM Rectifier in Bridge Connection

Distortion of input current in the line commutated rectifiers with capacitive filtering is particularly critical in uninterruptible power supplies (UPS) fed from motor-generator sets. In effect, due to the higher value of the generator impedance, the current distortion can originate an unacceptable distortion on the ac voltage, which affects the behavior of the whole system. For this reason, it is very attractive in this application to use rectifiers with low distortion in the input current.

Figure 11.28 shows the power circuit of a single-phase UPS, which has a PWM rectifier in bridge connection at the input side. This rectifier generates a sinusoidal input current and controls the charge of the battery [5].

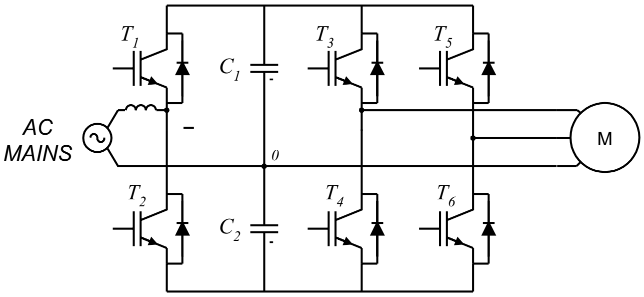


FIGURE 11.27 Low-cost induction motor drive.

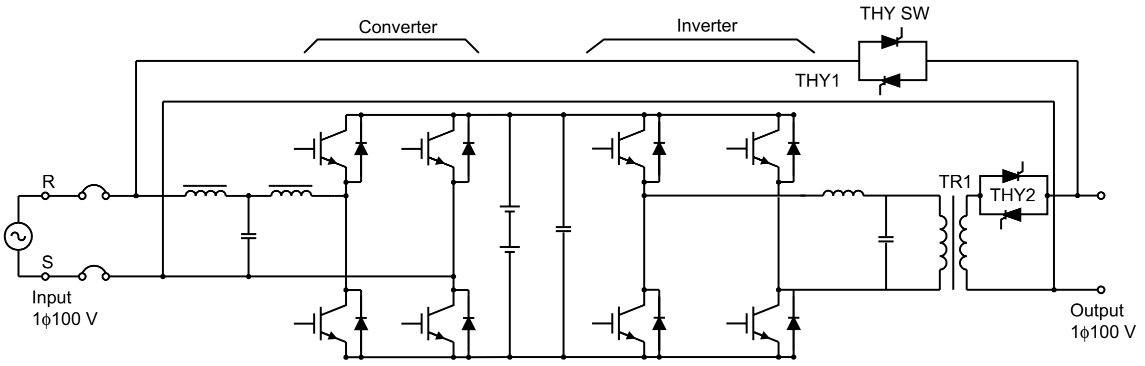

Converter
Inverter
THY SW
THY1
R
S
Input
1ϕ100 V
TR1
THY2
Output
1ϕ100 V

FIGURE 11.28 Single-phase UPS with PWM rectifier.

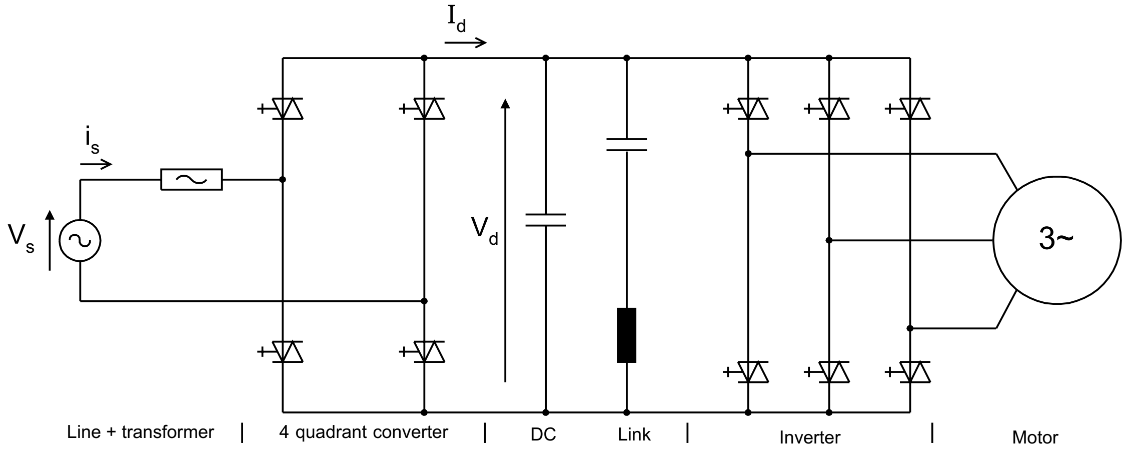

I_d
i_s
V_s
V_d
3~
Line + transformer
4 quadrant converter
DC
Link
Inverter
Motor

FIGURE 11.29 Typical power circuit of an ac drive for a locomotive.

Perhaps the most typical and widely accepted area of application of high-power factor single-phase rectifiers is in locomotive drives [6]. In effect, an essential prerequisite for proper operation of voltage source three-phase inverter drives in modern locomotives is the use of four quadrant line-side converters, which ensures motoring and braking of the drive, with reduced harmonics in the input current. Figure 11.29 shows a simplified power circuit of a typical drive for a locomotive connected to a single-phase power supply [6], which includes a high-power factor rectifier at the input.

Finally, Fig. 11.30 shows the main circuit diagram of the 300 series Shinkansen train [7]. In this application, ac power from the overhead catenary is transmitted through a transformer to single-phase PWM rectifiers, which provide dc voltage for the inverters. The rectifiers are capable of controlling the input ac current in an approximate sine waveform and in phase with the voltage, achieving a power factor of close to unity for both powering and regenerative braking. Regenerative braking produces energy savings and an important operational flexibility.

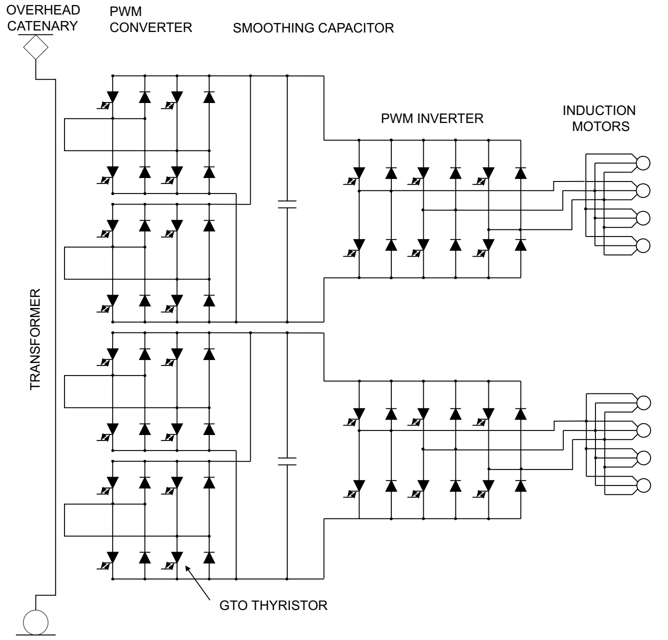

OVERHEAD CATENARY
PWM CONVERTER
SMOOTHING CAPACITOR
PWM INVERTER
INDUCTION MOTORS
TRANSFORMER
GTO THYRISTOR

FIGURE 11.30 Main circuit diagram of 300 series Shinkansen locomotives.

Acknowledgment

The authors gratefully acknowledge the valuable contribution of Dr. Rubén Peña.

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4. C. Jacobina, M. Beltrao, E. Cabral, and A. Nogueira, "Induction motor drive system for low-power applications," *IEEE Trans. Industry Applications* **35**:1, 52–60 (1999).
5. K. Hirachi, H. Yamamoto, T. Matsui, S. Watanabe, and M. Nakaoka, "Cost-effective practical developments of high-performance 1 kVA UPS with new system configurations and their specific control implementations," *European Conference on Power Electronics EPE 95*, Spain 1995, pp. 2035–2040.
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12

Three Phase Controlled Rectifiers

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12.1 Introduction

Three-phase controlled rectifiers have a wide range of applications, from small rectifiers to large high voltage direct current (HVDC) transmission systems. They are used for electrochemical processes, many kinds of motor drives, traction equipment, controlled power supplies, and many other applications. From the point of view of the commutation process, they can be classified into two important categories: *line-commutated controlled rectifiers (thyristor rectifiers)* and *force-commutated PWM rectifiers.*

12.2 Line-Commutated Controlled Rectifiers

12.2.1 Three-Phase Half-Wave Rectifier

Figure 12.1 shows the three-phase half-wave rectifier topology. To control the load voltage, the half-wave rectifier uses three common-cathode thyristor arrangement. In this figure, the power supply and the transformer are assumed ideal. The thyristor will conduct (ON state), when the anode-to-cathode voltage v_{AK} is positive, and a firing current pulse i_G is applied to the gate terminal. Delaying the firing pulse by an angle α controls the load voltage. As shown in Fig. 12.2, the firing angle α is measured from the crossing point between the phase supply voltages. At that point, the anode-to-cathode thyristor voltage v_{AK} begins to be positive. Figure 12.3 shows that the possible range for gating delay is between $\alpha = 0^\circ$ and $\alpha = 180^\circ$, but because of commutation problems in actual situations, the maximum firing angle is limited to $\approx 160^\circ$. As shown in Fig. 12.4, when the load is resistive, current i_d has the same waveform as the load voltage. As the load becomes more and more inductive, the current flattens and finally becomes constant. The thyristor goes to the nonconducting condition (OFF state) when the following thyristor is switched ON, or the current tries to reach a negative value.

With the help of Fig. 12.2, the load average voltage can be evaluated and is given by

$$V_D = \frac{V_{\max}}{2/3\pi} \int_{-\pi/3+\alpha}^{\pi/3+\alpha} \cos\omega t \cdot d(\omega t)$$

$$= V_{\max} \frac{\sin \pi/3}{\pi/3} \cdot \cos\alpha \approx 1.17 \cdot V_{f-N}^{\mathrm{rms}} \cdot \cos\alpha \qquad (12.1)$$

where $V_{\max}$ is the secondary phase-to-neutral peak voltage, V_{f-N}^{rms} its root mean square (rms) value, and ω is the angular frequency of the main power supply. It can be seen from Eq. (12.1) that the load average voltage V_D is modified by changing firing angle α. When α is $< 90^\circ$, V_D is positive and when α is $> 90^\circ$, the average dc voltage becomes negative. In such a case, the rectifier begins to work as an inverter, and the load needs to be able to generate power reversal by reversing its dc voltage.

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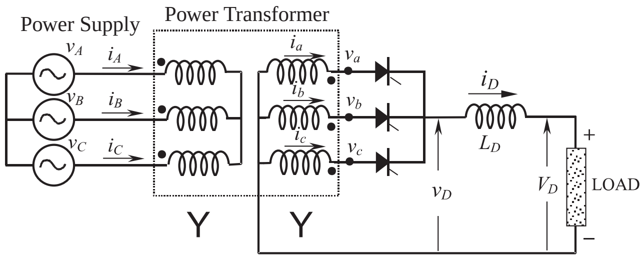


FIGURE 12.1 Three-phase half-wave rectifier.

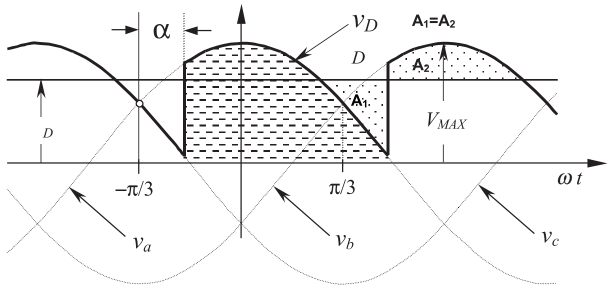


FIGURE 12.2 Instantaneous dc voltage v_D, average dc voltage V_D, and firing angle α.

The ac currents of the half-wave rectifier are shown in Fig. 12.5. This drawing assumes that the dc current is constant (very large L_D). Disregarding commutation overlap, each valve conducts during 120° per period. The secondary currents (and thyristor currents) present a dc component that is undesirable, and makes this rectifier not useful for high power applications. The primary currents show the same waveform, but with the dc component removed. This very distorted waveform requires an input filter to reduce harmonics contamination.

The current waveforms shown in Fig. 12.5 are useful for designing the power transformer. Starting from

$$\begin{aligned} VA_{\text{prim}} &= 3\cdot V^{\text{rms}}_{(\text{prim})f-N}\cdot I^{\text{rms}}_{\text{prim}} \\ VA_{\text{sec}} &= 3\cdot V^{\text{rms}}_{(\text{sec})f-N}\cdot I^{\text{rms}}_{\text{sec}} \\ P_D &= V_D\cdot I_D \end{aligned} \tag{12.2}$$

where VA_{prim} and VA_{sec} are the ratings of the transformer for the primary and secondary side, respectively. Here P_D is the power transferred to the dc side. The maximum power transfer is with $\alpha = 0°$ (or $\alpha = 180°$). Then, to establish a relation between ac and dc voltages, Eq. (12.1) for $\alpha = 0°$ is required:

$$V_D = 1.17\cdot V^{\text{rms}}_{(\text{sec})f-N} \tag{12.3}$$

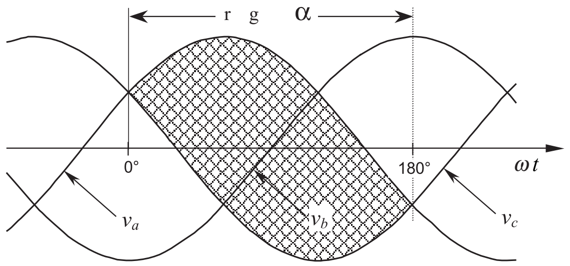


FIGURE 12.3 Possible range for gating delay in angle α.

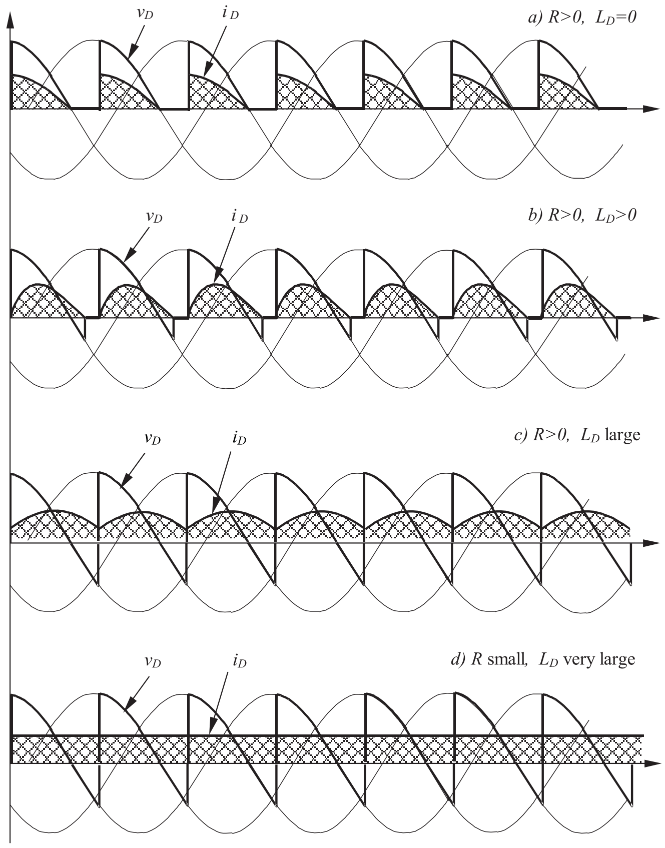


FIGURE 12.4 DC current waveforms.

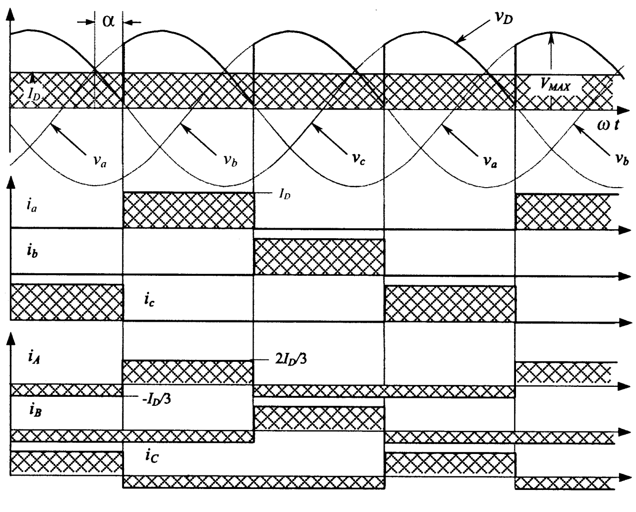


FIGURE 12.5 AC current waveforms for the half-wave rectifier.

and

$$V_D = 1.17 \cdot a \cdot V^{\text{rms}}_{(\text{prim})f-N} \tag{12.4}$$

where a is the secondary to primary turn relation of the transformer. On the other hand, a relation between the currents is also possible to obtain. With the help of Fig. 12.5,

$$I^{\text{rms}}_{\text{sec}} = \frac{I_D}{\sqrt{3}} \tag{12.5}$$

$$I^{\text{rms}}_{\text{prim}} = a \cdot \frac{I_D\sqrt{2}}{3} \tag{12.6}$$

Combining Eqs. (12.2) to (12.6), it yields

$$\begin{aligned} VA_{\text{prim}} &= 1.21 \cdot P_D \\ VA_{\text{sec}} &= 1.48 \cdot P_D \end{aligned} \tag{12.7}$$

Equation (12.7) shows that the power transformer has to be oversized 21% at the primary side, and 48% at the secondary side. Then a special transformer has to be built for this rectifier. In terms of average VA, the transformer needs to be 35% larger that the rating of the dc load. The larger rating of the secondary respect to primary is because the secondary carries a dc component inside the windings. Furthermore, the transformer is oversized because the circulation of current harmonics does not generate active power. Core saturation, due to the dc components inside the secondary windings, also needs to be taken into account for iron oversizing.

12.2.2 Six-Pulse or Double Star Rectifier

The thyristor side windings of the transformer shown in Fig. 12.6 form a six-phase system, resulting in a 6-pulse starpoint (midpoint connection). Disregarding commutation overlap, each valve conducts only during 60° per period. The direct voltage is higher than that from the half-wave rectifier, and its average value is given by

$$\begin{aligned} V_D &= \frac{V_{\max}}{\pi/3}\int_{-\pi/6+\alpha}^{\pi/6+\alpha} \cos\omega t \cdot d(\omega t) \\ &= V_{\max}\frac{\sin\pi/6}{\pi/6} \cdot \cos\alpha \approx 1.35 \cdot V^{\text{rms}}_{f-N} \cdot \cos\alpha \end{aligned} \tag{12.8}$$

The dc voltage ripple is also smaller than the one generated by the half-wave rectifier, due to the absence of the third harmonic with its inherently high amplitude. The smoothing reactor L_D is also considerably smaller than the one needed for a 3-pulse (half-wave) rectifier.

The ac currents of the 6-pulse rectifier are shown in Fig. 12.7. The currents in the secondary windings present a dc component, but the magnetic flux is compensated by the double star. As can be observed, only one valve is fired at a time, and then this connection in no way corresponds to a parallel connection. The currents inside the delta show a symmetrical waveform, with 60° conduction. Finally, due to the particular transformer connection shown in Fig. 12.6, the source currents also show a symmetrical waveform, but with 120° conduction.

Evaluation of the rating of the transformer is done in similar fashion to the way the half-wave rectifier is evaluated:

$$\begin{aligned} VA_{\text{prim}} &= 1.28 \cdot P_D \\ VA_{\text{sec}} &= 1.81 \cdot P_D \end{aligned} \tag{12.9}$$

Thus, the transformer must be oversized 28% at the primary side, and 81% at the secondary side. In terms of size it has an average apparent power of 1.55 times the power P_D (55% oversized). Because of the short conducting period of the valves, the transformer is not particularly well utilized.

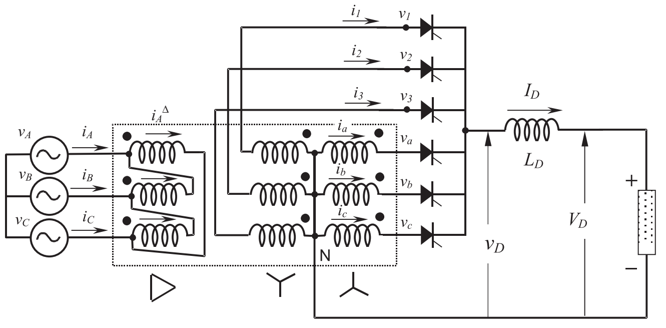


FIGURE 12.6 Six-pulse rectifier.

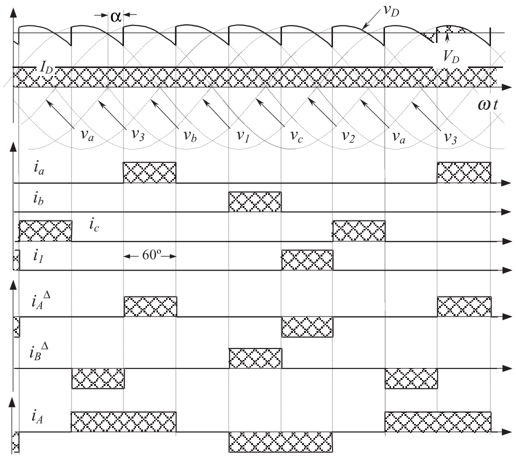


FIGURE 12.7 AC current waveforms for the 6-pulse rectifier.

12.2.3 Double Star Rectifier with Interphase Connection

This topology works as two half-wave rectifiers in parallel, and is very useful when high dc current is required. An optimal way to reach both good balance and eliminaton of harmonics is through the connection shown in Fig. 12.8. The two rectifiers are shifted by 180°, and their secondary neutrals are connected through a middle-point autotransformer, called an "interphase transformer". The interphase transformer is connected between the two secondary neutrals, and the middle point at the load return. In this way, both groups operate in parallel. Half the direct current flows in each half of the interphase transformer and then its iron core does not become saturated. The potential of each neutral can oscillate independently, generating an almost triangular voltage waveform (v_T) in the interphase transformer, as shown in Fig. 12.9. As this converter works like two half-wave rectifiers connected in parallel, the load average voltage is the same as in Eq. (12.1):

$$V_D \approx 1.17 \cdot V_{f-N}^{\mathrm{rms}} \cdot \cos\alpha \tag{12.10}$$

where V_{f-N}^{rms} is the phase-to-neutral rms voltage at the valve side of the transformer (secondary).

The Fig. 12.9 also shows the two half-wave rectifier voltages, related to their respective neutrals. Voltage v_{D1} represents the potential between the common cathode connection and the neutral N1. The voltage v_{D2} is between the common cathode connection and N2. It can be seen that the two instantaneous voltages are shifted, which gives as a result a voltage v_D that is smoother than v_{D1} and v_{D2}.

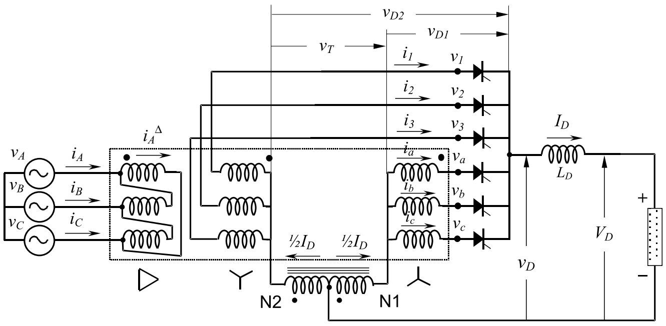


FIGURE 12.8 Double star rectifier with interphase transformer.

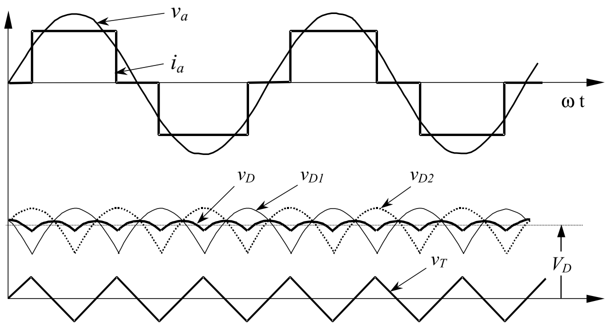


FIGURE 12.9 Operation of the interphase connection for $\alpha = 0°$.

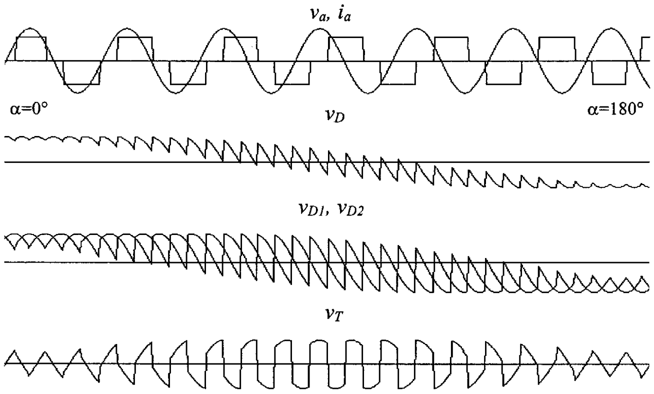


FIGURE 12.10 Firing angle variation from $\alpha = 0°$ to 180°.

Figure 12.10 shows how v_D, v_{D1}, v_{D2} and v_T change when the firing angle changes from $\alpha = 0°$ to $\alpha = 180°$.

The transformer rating in this case is

$$\begin{aligned} VA_{\mathrm{prim}} &= 1.05 \cdot P_D \\ VA_{\mathrm{sec}} &= 1.48 \cdot P_D \end{aligned} \tag{12.11}$$

and the average rating power will be $1.26P_D$, which is better than the previous rectifiers (1.35 for the half-wave rectifier, and 1.55 for the 6-pulse rectifier). Thus the transformer is well utilized. Figure 12.11 shows ac current waveforms for a rectifier with interphase transformer.

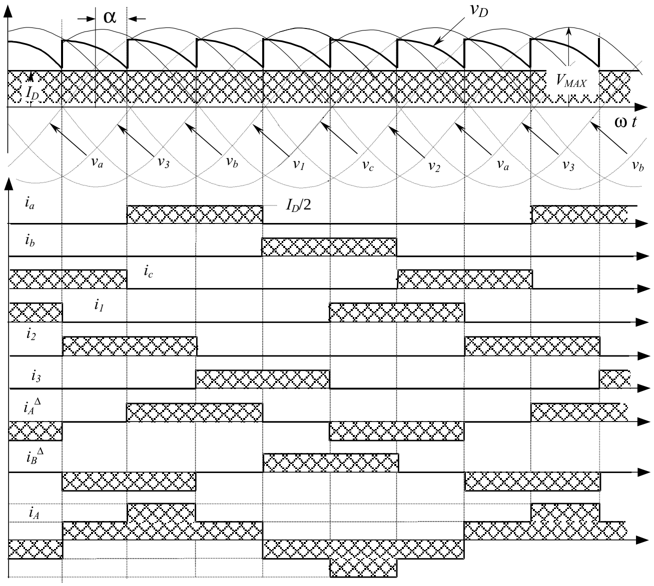


FIGURE 12.11 AC current waveforms for the rectifier with interphase transformer.

12.2.4 Three-Phase Full-Wave Rectifier or Graetz Bridge

Parallel connection via interphase transformers permits the implementation of rectifiers for high current applications. Series connection for high voltage is also possible, as shown in the full-wave rectifier of Fig. 12.12. With this arrangement, it can be seen that the three common cathode valves generate a positive voltage with respect to the neutral, and the three common anode valves produce a negative voltage. The result is a dc voltage twice the value of the half-wave rectifier. Each half of the bridge is a 3-pulse converter group. This bridge connection is a two-way connection, and alternating currents flow in the valve-side transformer windings during both half periods, avoiding dc components into the windings, and saturation in the transformer magnetic core. These characteristics make the so-called Graetz bridge the most widely used line-commutated thyristor rectifier. The configuration does not need any special transformer, and works as a 6-pulse rectifier. The series characteristic of this rectifier produces a dc voltage twice the value of the half-wave rectifier. The load average voltage is given by

$$\begin{aligned} V_D &= \frac{2 \cdot V_{\max}}{2/3\pi} \int_{-\pi/3+\alpha}^{\pi/3+\alpha} \cos \omega t \cdot d(\omega t) \\ &= 2 \cdot V_{\max} \frac{\sin \pi/3}{\pi/3} \cdot \cos \alpha \approx 2.34 \cdot V_{f-N}^{\text{rms}} \cdot \cos \alpha \end{aligned} \qquad (12.12)$$

or

$$V_D = \frac{3 \cdot \sqrt{2} \cdot V_{f-f}^{\text{sec}}}{\pi} \cos \alpha \approx 1.35 \cdot V_{f-f}^{\text{sec}} \cdot \cos \alpha \qquad (12.13)$$

where $V_{\max}$ is the peak phase-to-neutral voltage at the secondary transformer terminals, V_{f-N}^{rms} its rms value, and V_{f-f}^{sec} the rms phase-to-phase secondary voltage, at the valve terminals of the rectifier.

Figure 12.13 shows the voltages of each half-wave bridge of this topology v_D^{pos} and v_D^{neg}, the total instantaneous dc voltage v_D, and the anode-to-cathode voltage v_{AK} in one of the bridge thyristors. The maximum value of v_{AK} is $\sqrt{3} \cdot V_{\max}$, which is the same as that of the half-wave converter and the interphase transformer rectifier. The double star rectifier presents a maximum anode-to-cathode voltage of 2 times $V_{\max}$. Figure 12.14 shows the currents of the rectifier, which assumes that L_D is large enough to keep the dc current smooth. The example is for the same ΔY transformer connection shown in the topology of Fig. 12.12. It can be noted that the secondary currents do not carry any dc component, thereby avoiding overdesign of the windings and transformer saturation. These two figures have been drawn for a firing angle α of $\approx 30°$. The perfect symmetry of the currents in all windings and lines is one of the reasons why this rectifier is the most popular of its type. The transformer rating in this case is

$$\begin{aligned} VA_{\text{prim}} &= 1.05 \cdot P_D \\ VA_{\text{sec}} &= 1.05 \cdot P_D \end{aligned} \qquad (12.14)$$

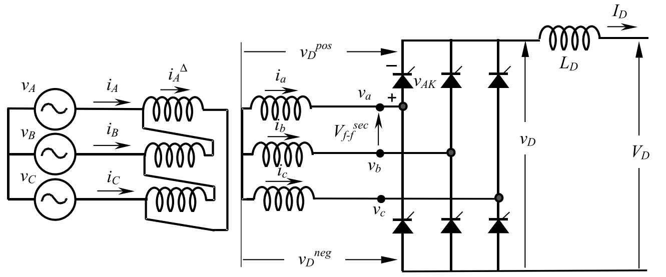


FIGURE 12.12 Three-phase full-wave rectifier or Graetz bridge.

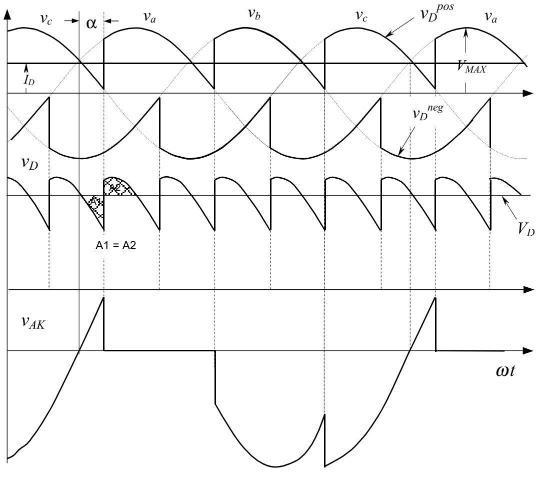


FIGURE 12.13 Voltage waveforms for the Graetz bridge.

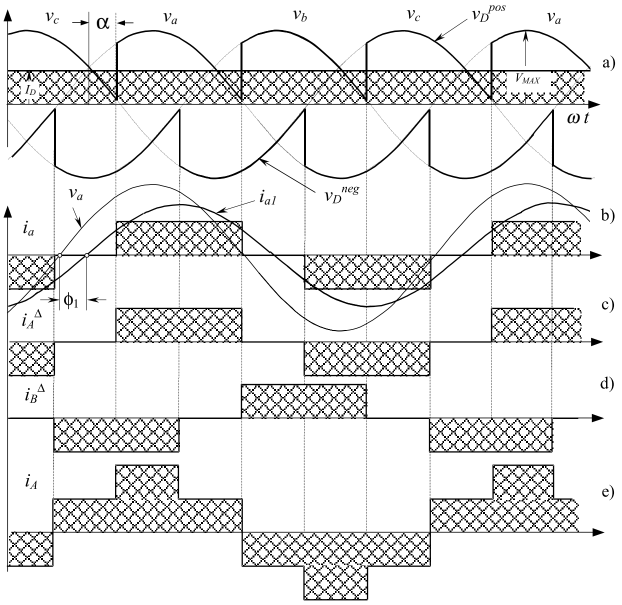
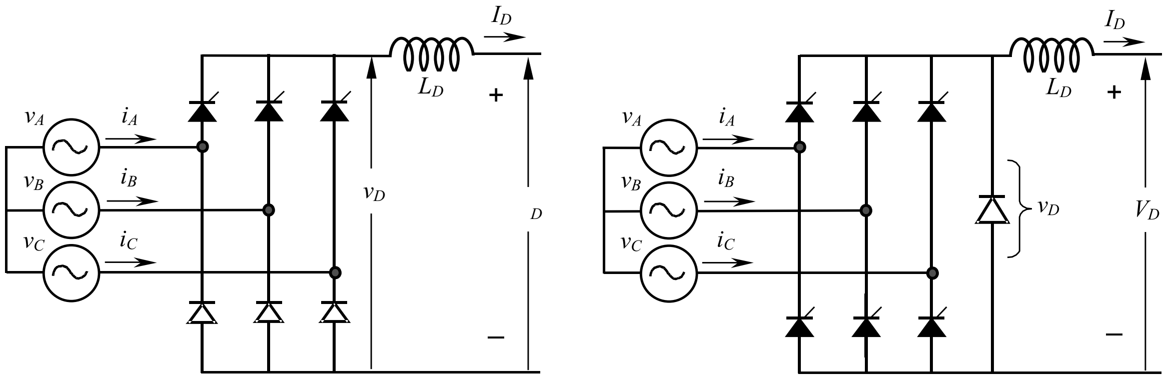


FIGURE 12.14 Current waveforms for the Graetz bridge.



a) b)

FIGURE 12.15 One-quadrant bridge converter circuits: (a) half-controlled bridge; and (b) free-wheeling diode bridge.

As can be noted, the transformer needs to be oversized only 5 , and both primary and secondary windings have the same rating. Again, this value can be compared with the previous rectifier transformers: $1.35P_D$ for the half-wave rectifier; $1.55P_D$ for the 6-pulse rectifier; and $1.26P_D$ for the interphase transformer rectifier. The Graetz bridge makes excellent use of the power transformer.

12.2.5 alf-Controlled Bridge Converter

The fully controlled three-phase bridge converter shown in Fig. 12.12 has six thyristors. As already explained here, this circuit operates as a rectifier when each thyristor has a firing angle α of $<90^\circ$ and functions as an inverter for $\alpha > 90^\circ$. If inverter operation is not required, the circuit may be simplified by replacing three controlled rectifiers with power diodes, as in Fig. 12.15a). This simplification is economically attractive because diodes are considerably less expensive than thyristors, and they do not require firing angle control electronics.

The half-controlled bridge, or "semiconverter," is analyzed by considering it as a phase-controlled half-wave circuit in series with an uncontrolled half-wave rectifier. The average dc voltage is given by the following equation:

$$V_D = \frac{3 \cdot \sqrt{2} \cdot V_{f-f}^{\text{sec}}}{2\pi}(1 + \cos\alpha) \qquad (12.15)$$

Then, the average voltage V_D never reaches negative values. The output voltage waveforms of the half-controlled bridge are similar to those of a fully controlled bridge with a free-wheeling diode. The advantage of the free-wheeling diode connection, shown in Fig. 12.15b is that there is always a path for the dc current, independent of the status of the ac line and of the converter. This can be important if the load is inductive-resistive with a large time constant, and there is an interruption in one or more of the line phases. In such a case, the load current could commutate to the free-wheeling diode.

12.2.6 Commutation

The description of the converters in the previous sections was based upon the assumption that the commutation was instantaneous. In practice, this is not possible because the transfer of current between two consecutive valves in a commutation group takes a finite time. This time, called overlap time, depends on the phase-to-phase voltage between the valves participating in the commutation process, and the line inductance L_S between the converter and power supply. During the overlap time, two valves conduct, and the phase-to-phase voltage drops entirely on the inductances L_S. Assuming the dc current I_D to be smooth, and with the help of Fig. 12.16, the following relation is deduced:

$$2L_S \cdot \frac{di_{sc}}{dt} = \sqrt{2} \cdot V_{f-f} \sin\omega t = v_A - v_B \qquad (12.16)$$

where i_{sc} is the current in the valve being fired during the commutation process (thyristor $T2$ in Fig. 12.16). This current can be evaluated, and it yields:

$$i_{sc} = -\frac{\sqrt{2}}{2L_S} \cdot V_{f-f} \frac{\cos\omega t}{\omega} + C \qquad (12.17)$$

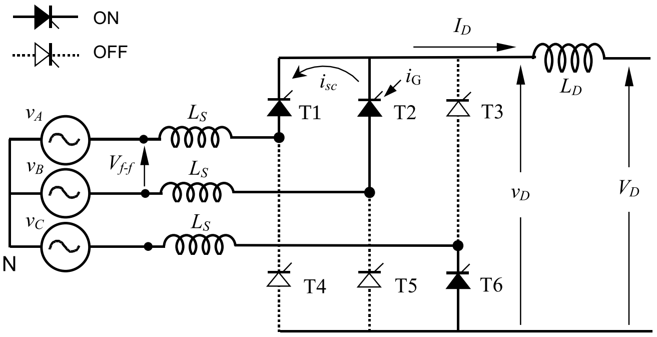


FIGURE 12.16 Commutation process.

Constant "C" is evaluated through initial conditions at the instant when $T2$ is ignited. In terms of angle, when $\omega t = \alpha$:

$$i_{sc} = 0 \qquad \therefore\ C = \frac{V_{f-f}^{\mathrm{sec}}}{\sqrt{2} \cdot \omega L_S} \cos \alpha \tag{12.18}$$

Replacing Eq. (12.18) in Eq. (12.17):

$$i_{sc} = \frac{V_{f-f}}{\sqrt{2} \cdot \omega L_S} \cdot (\cos \alpha - \cos \omega t) \tag{12.19}$$

Before commutation, the current I_D was carried by thyristor $T1$ (see Fig. 12.16). During the commutation time, the load current I_D remains constant, i_{sc} returns through $T1$, and $T1$ is automatically switched-off when the current i_{sc} reaches the value of I_D. This happens because thyristors cannot conduct in reverse direction. At this moment, the overlap time lasts, and the current I_D is then conducted by $T2$. In terms of angle, when $\omega t = \alpha + \mu$, $i_{sc} = I_D$, where μ is defined as the "*overlap angle*." Replacing this final condition in Eq. (12.19) yields:

$$I_D = \frac{V_{f-f}^{\mathrm{sec}}}{\sqrt{2} \cdot \omega L_S} \cdot [\cos \alpha - \cos(\alpha + \mu)] \tag{12.20}$$

To avoid confusion in a real analysis, it has to be remembered that V_{f-f} corresponds to the secondary voltage in the case of transformer utilization. For this reason, the abbreviation "sec" has been added to the phase-to-phase voltage in Eq. (12.20).

During commutation, two valves conduct at a time, which means that there is an instantaneous short circuit between the two voltages participating in the process. As the inductances of each phase are the same, the current i_{sc} produces the same voltage drop in each L_S, but with opposite sign because this current flows in reverse direction in each inductance. The phase with the higher instantaneous voltage suffers a voltage drop $-\Delta v$, and the phase with the lower voltage suffers a voltage increase $+\Delta v$. This situation affects the dc voltage V_C, reducing its value an amount ΔV_{med}. Figure 12.17 shows the meanings of Δv, ΔV_{med}, μ, and i_{sc}.

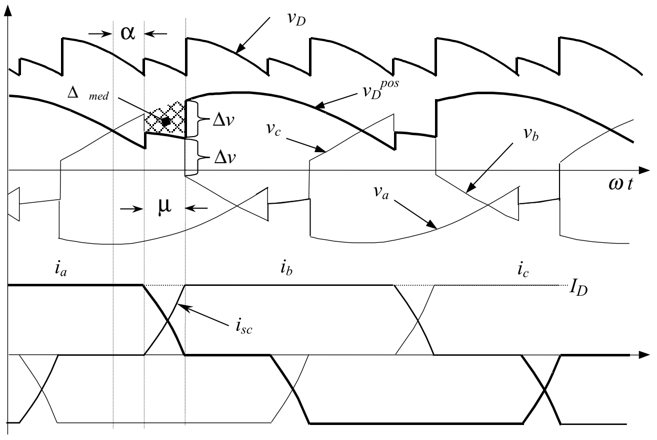


FIGURE 12.17 Effect of the overlap angle on the voltages and currents.

The area ΔV_{med} showed in Fig. 12.17 represents the loss of voltage that affects the average voltage V_C, and can be evaluated through the integration of Δv during the overlap angle μ. The voltage drop Δv can be expressed as

$$\Delta v = \left(\frac{v_A - v_B}{2}\right) = \frac{\sqrt{2} \cdot V_{f-f}^{\mathrm{sec}} \sin \omega t}{2} \tag{12.21}$$

Integrating Eq. (12.21) into the corresponding period (60°) and interval (μ), at the instant when the commutation begins (α):

$$\Delta V_{\mathrm{med}} = \frac{3}{\pi} \cdot \frac{1}{2} \int_{\alpha}^{\alpha+\mu} \sqrt{2} \cdot V_{f-f}^{\mathrm{sec}} \sin \omega t \cdot d\omega t \tag{12.22}$$

$$\Delta V_{\mathrm{med}} = \frac{3 \cdot V_{f-f}^{\mathrm{sec}}}{\pi \cdot \sqrt{2}} [\cos \alpha - \cos(\alpha + \mu)] \tag{12.23}$$

Subtracting ΔV_{med} in Eq. (12.13):

$$V_D = \frac{3 \cdot \sqrt{2} \cdot V_{f-f}^{\mathrm{sec}}}{\pi} \cos \alpha - \Delta V_{\mathrm{med}} \tag{12.24}$$

$$V_D = \frac{3 \cdot \sqrt{2} \cdot V_{f-f}^{\mathrm{sec}}}{2\pi} [\cos \alpha + \cos(\alpha + \mu)] \tag{12.25}$$

or

$$V_D = \frac{3 \cdot \sqrt{2} V_{f-f}^{\mathrm{sec}}}{\pi} \left[\cos\left(\alpha + \frac{\mu}{2}\right) \cos \frac{\mu}{2}\right] \tag{12.26}$$

Equations (12.20) and (12.25) can be written as a function of the primary winding of the transformer, if any transformer.

$$I_D = \frac{a \cdot V_{f-f}^{\mathrm{prim}}}{\sqrt{2} \cdot \omega L_S} \cdot [\cos \alpha - \cos(\alpha + \mu)] \tag{12.27}$$

$$V_D = \frac{3 \cdot \sqrt{2} \cdot a \cdot V_{f-f}^{\mathrm{prim}}}{2\pi} [\cos \alpha + \cos(\alpha + \mu)] \tag{12.28}$$

where $a = V_{f-f}^{\mathrm{sec}} / V_{f-f}^{\mathrm{prim}}$. With Eqs. (12.27) and (12.28) one obtains:

$$V_D = \frac{3 \cdot \sqrt{2}}{\pi} \cdot a \cdot V_{f-f}^{\mathrm{prim}} \cos \alpha - \frac{3 I_D \omega L_S}{\pi} \tag{12.29}$$

Equation (12.29) allows a very simple equivalent circuit of the converter to be made, as shown in Fig. 12.18. It is important to note that the equivalent resistance of this circuit is not real because it does not dissipate power.

From the equivalent circuit, regulation curves for the rectifier under different firing angles are shown in Fig. 12.19. It should be noted that these curves correspond only to an

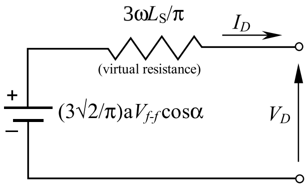


FIGURE 12.18 Equivalent circuit for the converter.

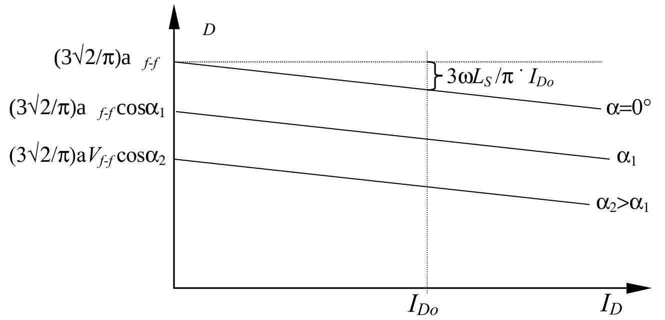


FIGURE 12.19 Direct current voltage regulation curves for rectifier operation.

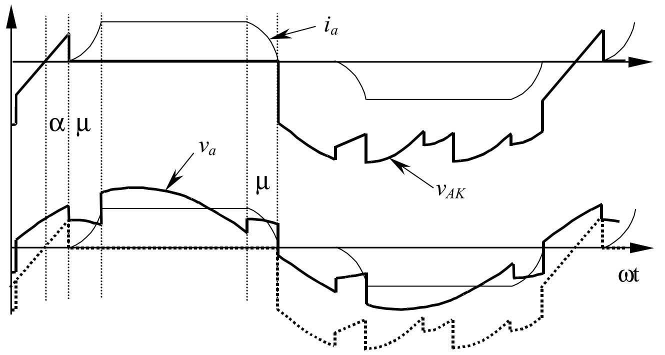


FIGURE 12.20 Effect of the overlap angle on v_a and on thyristor voltage v_{AK}.

ideal situation, but they help in understanding the effect of voltage drop Δv on dc voltage. The commutation process and the overlap angle also affects the voltage v_a and anode-to-cathode thyristor voltage, as shown in Fig. 12.20.

12.2.7 Power actor

The displacement factor of the fundamental current, obtained from Fig. 12.14 is

$$\cos\phi_1 = \cos\alpha \tag{12.30}$$

In the case of nonsinusoidal current, the active power delivered per phase by the sinusoidal supply is

$$P = \frac{1}{T}\int_0^T v_a(t) i_a(t) dt = V_a^{\mathrm{rms}} I_{a1}^{\mathrm{rms}} \cos\phi_1 \tag{12.31}$$

where V_a^{rms} is the rms value of the voltage v_a, and I_{a1}^{rms} the rms value of i_{a1} (fundamental component of i_a). Analog relations can be obtained for v_b and v_c.

The apparent power per phase is given by

$$S = V_a^{\mathrm{rms}} I_a^{\mathrm{rms}} \tag{12.32}$$

The power factor is defined by

$$PF = \frac{P}{S} \tag{12.33}$$

By substituting Eqs. (12.30), (12.31) and (12.32) into Eq. (12.33), the power factor can be expressed as follows

$$PF = \frac{I_{a1}^{\mathrm{rms}}}{I_a^{\mathrm{rms}}} \cos\alpha \tag{12.34}$$

This equation shows clearly that due to the nonsinusoidal waveform of the currents, the power factor of the rectifier is negatively affected by both the firing angle α and the distortion of the input current. In effect, an increase in the distortion of the current produces an increase in the value of I_a^{rms} in Eq. (12.34), which deteriorates the power factor.

12.2.8 armonic Distortion

The currents of the line-commutated rectifiers are far from being sinusoidal. For example, the currents generated from the Graetz rectifier (see Fig. 12.14b) have the following harmonic content:

$$i_A = \frac{2\sqrt{3}}{\pi} I_D \left(\cos\omega t - \frac{1}{5}\cos 5\omega t + \frac{1}{7}\cos 7\omega t - \frac{1}{11}\cos 11\omega t + \cdots \right) \tag{12.35}$$

Some of the characteristics of the currents obtained from Eq. (12.35) include: i) the absence of triple harmonics; ii) the presence of harmonics of order 6; ±1 for integer values of k; iii) those harmonics of orders $6k+1$ are of positive sequence, and those of orders $6k-1$ are of negative sequence; and iv) the rms magnitude of the fundamental frequency is

$$I_1 = \frac{\sqrt{6}}{\pi} I_D \tag{12.36}$$

v) the rms magnitude of the nth harmonic is:

$$I_n = \frac{I_1}{n} \tag{12.37}$$

If either the primary or the secondary three-phase windings of the rectifier transformer are connected in delta, the ac side current waveforms consist of the instantaneous differences between two rectangular secondary currents 120° apart as shown in Fig. 12.14e). The resulting Fourier series for the current in phase "a" on the primary side is

$$i_A = \frac{2\sqrt{3}}{\pi} I_D \bigg(\cos \omega t + \frac{1}{5} \cos 5\omega t - \frac{1}{7} \cos 7\omega t - \frac{1}{11} \cos 11\omega t + \cdots \bigg) \tag{12.38}$$

This series differs from that of a star-connected transformer only by the sequence of rotation of harmonic orders $6k \pm 1$ for odd values of k, that is, 5th, 7th, 17th, 19th, etc.

12.2. Special Configurations for Harmonic Reduction

A common solution for harmonic reduction is through the connection of passive filters, which are tuned to trap a particular harmonic frequency. A typical configuration is shown in Fig. 12.21.

However, harmonics also can be eliminated using special configurations of converters. For example, 12-pulse configuration consists of two sets of converters connected as shown in Fig. 12.22. The resultant ac current is given by the sum of the two Fourier series of the star connection (Eq. 12.35) and delta connection transformers (Eq. 12.38):

$$i_A = 2\left(\frac{2\sqrt{3}}{\pi}\right) I_D \bigg(\cos \omega t - \frac{1}{11} \cos 11\omega t + \frac{1}{13} \cos 13\omega t - \frac{1}{23} \cos 23t + \cdots \bigg) \tag{12.39}$$

The series contains only harmonics of order $12k \pm 1$. The harmonic currents of orders $6k \pm 1$ (with k odd), that is, 5th, 7th, 17th, 19th, etc., circulate between the two converter transformers but do not penetrate the ac network.

The resulting line current for the 12-pulse rectifier shown in Fig. 12.23 is closer to a sinusoidal waveform than previous line currents. The instantaneous dc voltage is also smoother with this connection.

Higher pulse configuration using the same principle is also possible. The 12-pulse rectifier was obtained with a 30° phase-shift between the two secondary transformers. The addition of further appropriately shifted transformers in parallel provides the basis for increasing pulse configurations. For instance, 24-pulse operation is achieved by means of four transformers with 15° phase-shift, and 48-pulse operation requires eight transformers with 7.5° phase-shift.

Although theoretically possible, pulse numbers > 48 are rarely justified due to the practical levels of distortion found in the supply voltage waveforms. Further, the converter topology becomes more and more complicated.

An ingenious and very simple way to reach high pulse operation is shown in Fig. 12.24. This configuration is called dc ripple reinjection. It consists of two parallel converters connected to the load through a multistep reactor. The reactor uses a chain of thyristor-controlled taps, which are connected to symmetrical points of the reactor. By firing the thyristors located at the reactor at the right time, high-pulse operation is reached. The level of pulse operation depends on the number of thyristors connected to the reactor. They multiply the basic level of operation of the two converters. The example of Fig. 12.24 shows a 48-pulse configuration, obtained by the multiplication of basic 12-pulse operation by four reactor thyristors. This technique also can be applied to series connected bridges.

Another solution for harmonic reduction is the utilization of active power filters. Active power filters are special pulse width modulated (PWM) converters, able to generate the

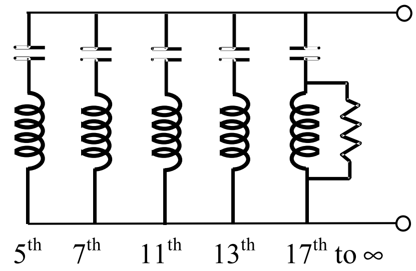


FIGURE 12.21 Typical passive filter for one phase.

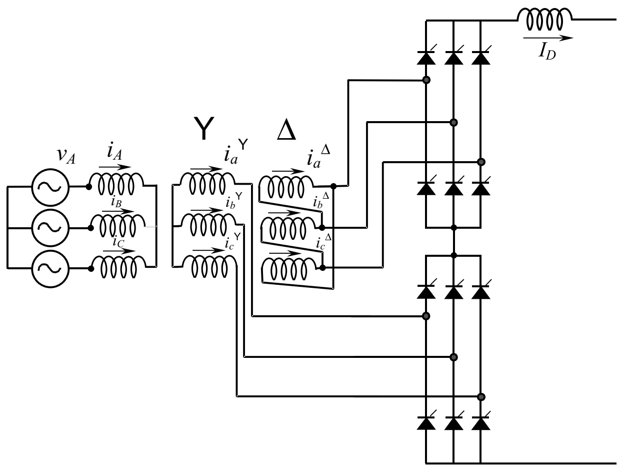


FIGURE 12.22 A 12-pulse rectifier configuration.

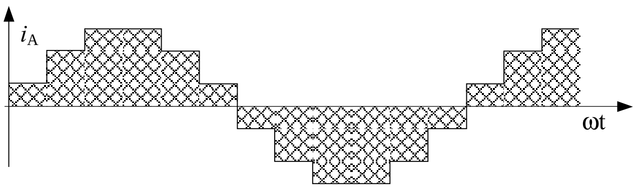


FIGURE 12.23 Line current for the 12-pulse rectifier.

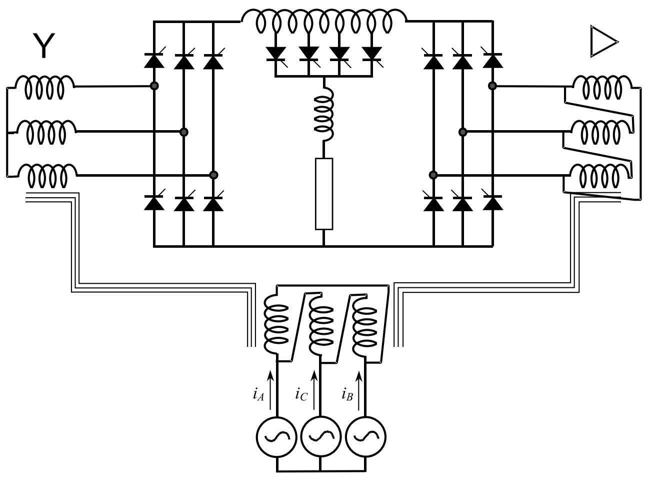


FIGURE 12.24 Direct current ripple reinjection technique for 48-pulse operation.

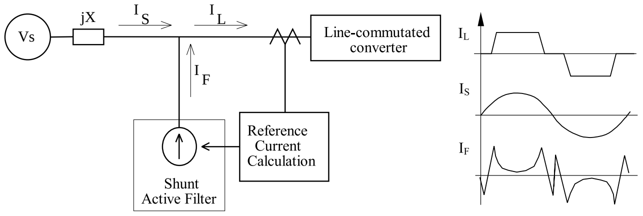


FIGURE 12.25 Current-controlled shunt active power filter.

harmonics the converter requires. Figure 12.25 shows a current-controlled shunt active power filter.

12.2.1 Applications of Line-Commutated Rectifiers in Machine Drives

Important applications for line-commutated three-phase controlled rectifiers are found in machine drives. Figure 12.26 shows a dc machine control implemented with a 6-pulse rectifier. Torque and speed are controlled through armature current I_D and excitation current I_{exc}. Current I_D is adjusted with V_D, which is controlled by the firing angle α through Eq. (12.12). This dc drive can operate in two quadrants positive and negative dc voltage. This two-quadrant operation allows regenerative braking when $\alpha > 90°$, and $I_{\text{exc}} < 0$.

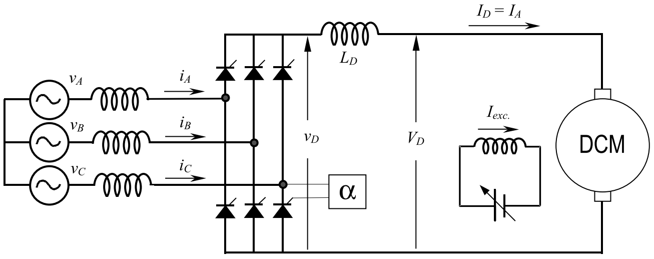


FIGURE 12.26 Direct Current machine drive with a 6-pulse rectifier.

The converter of Fig. 12.26 also can be used to control synchronous machines, as shown in Fig. 12.27. In this case, a second converter working in the inverting mode operates the machine as a self-controlled synchronous motor. With this second converter, the synchronous motor behaves like a dc motor but has none of the disadvantages of mechanical commutation. This converter is not line commutated, but machine commutated.

The nominal synchronous speed of the motor on a 50 or 60 Hz ac supply is now meaningless, and the upper speed limit is determined by the mechanical limitations of the rotor construction. There is the disadvantage that the rotational emfs required for load commutation of the machine side converter are not available at standstill and low speeds. In such a case, auxiliary force commutated circuits must be used.

The line-commutated rectifier through α controls the torque of the machine. This approach gives direct torque control of the commutatorless motor and is analogous to the use of armature current control as shown in Fig. 12.26 for the converter-fed dc motor drive.

Line-commutated rectifiers are also used for speed control of wound-rotor induction motors. Subsynchronous and supersynchronous static converter cascades using a naturally commutated dc link converter can be implemented. Figure 12.28 shows a supersynchronous cascade for a wound rotor induction motor, using a naturally commutated dc link converter.

In the supersynchronous cascade shown in Fig. 12.28, the right-hand bridge operates at slip frequency as a rectifier or inverter, while the other operates at network frequency as an inverter or rectifier. Control is difficult near synchronism when slip frequency emfs are insufficient for natural commutation, and special circuit configuration employing forced commutation or devices with a self-turn-off capability is necessary for a passage through synchronism. This kind of supersynchronous cascade works better with cycloconverters.

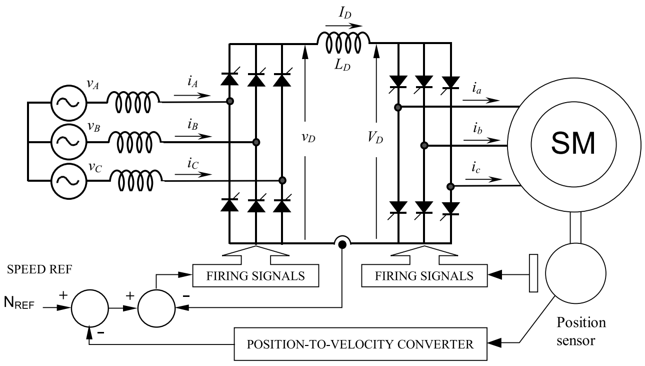


FIGURE 12.27 Self-controlled synchronous motor drive.

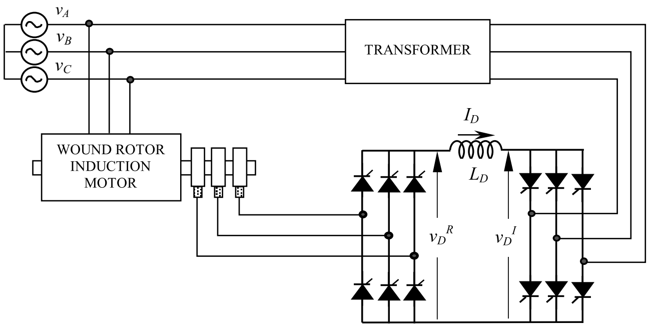


FIGURE 12.28 Supersynchronous cascade for a wound rotor induction motor.

12.2.11 Applications in HVDC Power Transmission

High voltage direct current (HVDC) power transmission is the most powerful application for line-commutated converters that exist today. There are power converters with ratings in excess of 1000 MW. Series operation of hundreds of valves can be found in some HVDC systems. In high-power and long distance applications, these systems become more economical than conventional ac systems. They also have some other advantages compared with ac systems:

1. they can link two ac systems operating unsynchronized or with different nominal frequencies, that is 50 Hz ↔ 60 Hz;
2. they can help in stability problems related with subsynchronous resonance in long ac lines;
3. they have very good dynamic behavior, and can interrupt short-circuits problems very quickly;
4. if transmission is by submarine or underground cable, it is not practical to consider ac cable systems exceeding 50 km, but dc cable transmission systems are in service whose length is in hundreds of kilometers and even distances of 600 km or greater have been considered feasible;
5. reversal of power can be controlled electronically by means of the delay firing angles α;
6. some existing overhead ac transmission lines cannot be increased. If overbuilt with or upgraded to dc transmission this can substantially increase the power transfer capability on the existing right-of-way.

The use of HVDC systems for interconnections of asynchronous systems is an interesting application. Some continental electric power systems consist of asynchronous networks such as those for the East-West Texas and Quebec networks in North America, and island loads such as that for the Island of Gotland in the Baltic Sea make good use of HVDC interconnections.

Nearly all HVDC power converters with thyristor valves are assembled in a converter bridge of 12-pulse configuration, as shown in Fig. 12.29. Consequently, the ac voltages applied to each 6-pulse valve group that makes up the 12-pulse valve group have a phase difference of 30° which is utilized to cancel

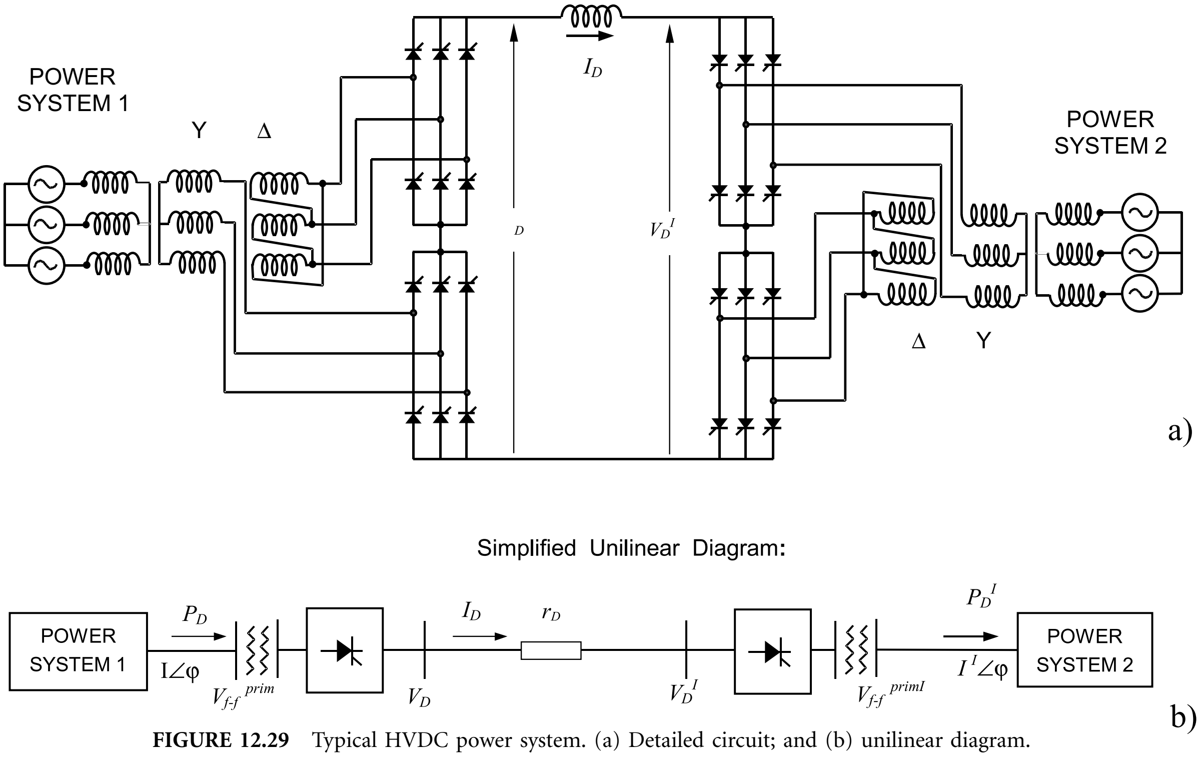


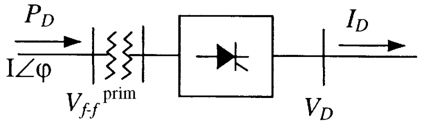
FIGURE 12.29 Typical HVDC power system. (a) Detailed circuit; and (b) unilinear diagram.

the ac side 5th and 7th harmonic currents and dc side 6th harmonic voltage, thus resulting in significant savings in harmonic filters.

Some useful relations for HVDC systems include:

(a) rectifier side:

$$P_D = V_D \cdot I_D = \sqrt{3} \cdot V_{f-f}^{\text{prim}} \cdot I_{\text{line}}^{\text{rms}} \cos\varphi \tag{12.40}$$



$$I_P = I\cos\varphi$$
$$I_Q = I\sin\varphi$$

$$\therefore \quad P_D = V_D \cdot I_D = \sqrt{3} \cdot V_{f-f}^{\text{prim}} \cdot I_P \tag{12.41}$$

$$I_P = \frac{V_D \cdot I_D}{\sqrt{3} \cdot V_{f-f}^{\text{prim}}} \tag{12.42}$$

$$I_P = \frac{a^2\sqrt{3} \cdot V_{f-f}^{\text{prim}}}{4\pi \cdot \omega L_S}[\cos 2\alpha - \cos 2(\alpha+\mu)] \tag{12.43}$$

$$I_Q = \frac{a^2\sqrt{3} \cdot V_{f-f}^{\text{prim}}}{4\pi \cdot \omega L_S}[\sin 2(\alpha+\mu) - \sin 2\alpha - 2\mu] \tag{12.44}$$

$$I_P = I_D\frac{\alpha\sqrt{6}}{\pi}\left[\frac{\cos\alpha + \cos(\alpha+\mu)}{2}\right] \tag{12.45}$$

Fundamental secondary component of I:

$$I = \frac{a\sqrt{6}}{\pi}I_D \tag{12.46}$$

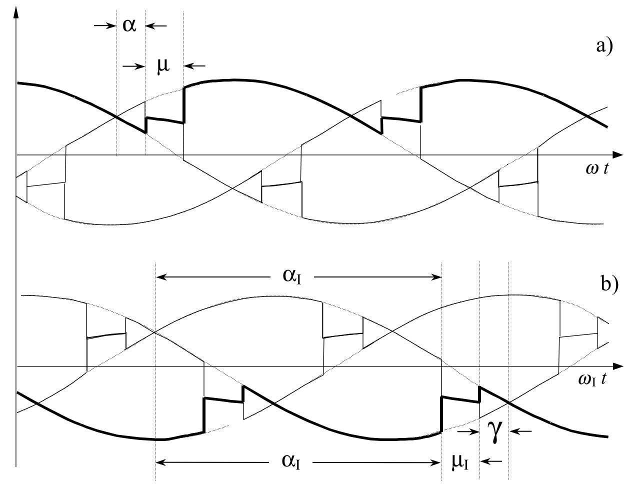


FIGURE 12.30 Definition of angle γ for inverter side: (a) rectifier side; and (b) inverter side.

Substituting (Eq. 12.46) into (12.45):

$$I_P = I \cdot \left[\frac{\cos\alpha + \cos(\alpha+\mu)}{2}\right] \tag{12.47}$$

as $I_P = I\cos\varphi$, it yields

$$\cos\varphi = \left[\frac{\cos\alpha + \cos(\alpha+\mu)}{2}\right] \tag{12.48}$$

(b) inverter side: The same equations are applied for the inverter side, but the firing angle α is replaced by γ, where γ is (see Fig. 12.30):

$$\gamma = 180^\circ - (\alpha_I + \mu_I) \tag{12.49}$$

As reactive power always goes in the converter direction, at the inverter side Eq. (12.44) becomes:

$$I_{Q_1} = -\frac{a_I^2\sqrt{3} \cdot V_{f-f_I}^{\text{prim}}}{4\pi \cdot \omega_I L_I}[\sin 2(\gamma+\mu_I) - \sin 2\gamma - 2\mu_I] \tag{12.50}$$

12.2.12 Dual Converters

In many variable-speed drives, four-quadrant operation is required, and three-phase dual converters are extensively used in applications up to the 2 MW level. Figure 12.31 shows a three-phase dual converter, where two converters are connected back-to-back.

In the dual converter, one rectifier provides the positive current to the load, and the other the negative current. Due to the instantaneous voltage differences between the output voltages of the converters, a circulating current flows through the bridges. The circulating current is normally limited by circulating reactor L_D as shown in Fig. 12.31. The two converters are controlled in such a way that if α^+ is the delay angle of the positive current converter, the delay angle of the negative current converter is $\alpha^- = 180^\circ - \alpha^+$.

Figure 12.32 shows the instantaneous dc voltages of each converter, v_D^+ and v_D^-. Despite the average voltage V_D is the same in both the converters, their instantaneous voltage

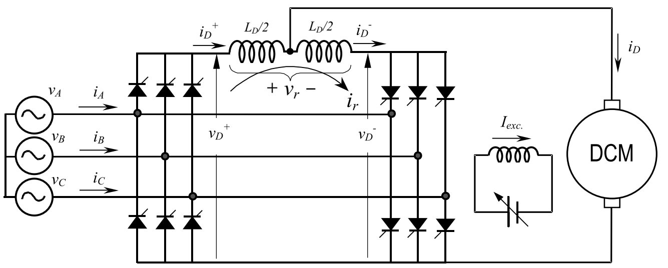


FIGURE 12.31 Dual converter in a four-quadrant dc drive.

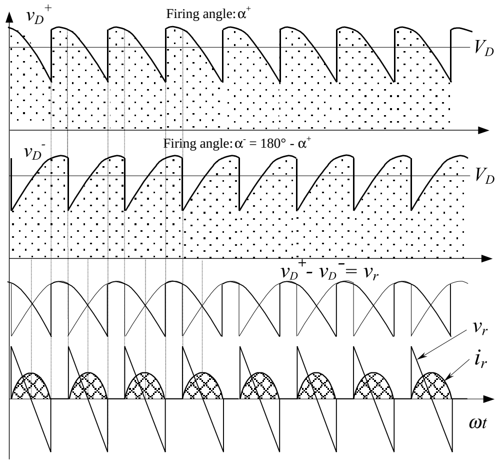


FIGURE 12.32 Waveform of circulating current: (a) instantaneous dc voltage from positive converter; (b) instantaneous dc voltage from negative converter; (c) voltage difference between v_D^+ and v_D^-, v_r, and circulating current i_r.

differences, given by voltage v_r, are not producing the circulating current i_r, which is superimposed with the load currents i_D^+, and i_D^-.

To avoid the circulating current i_r, it is possible to implement a "circulating current free" converter if a dead time of a few milliseconds is acceptable. The converter section not required to supply current remains fully blocked. When a current reversal is required, a logic switch-over system determines at first the instant at which the conducting converter's current becomes zero. This converter section is then blocked and the further supply of gating pulses to it prevented. After a short safety interval (dead time), the gating pulses for the other converter section are released.

12.2.13 Cycloconverters

A different principle of frequency conversion is derived from the fact that a dual converter is able to supply an ac load with a lower frequency than the system frequency. If the control signal of the dual converter is a function of time, the output voltage will follow this signal. If this control signal value alters sinusoidally with the desired frequency, then the waveform depicted in Fig. 12.33a consists of a single-phase voltage with a large harmonic current. As shown in Fig. 12.33b, if the load is inductive, the current will present less distortion than voltage.

The cycloconverter operates in all four quadrants during a period. A pause (dead time) at least as small as the time required by the switch-over logic occurs after the current reaches zero, that is, between the transfer to operation in the quadrant corresponding to the other direction of current flow.

Three single-phase cycloconverters may be combined to build a three-phase cycloconverter. The three-phase cycloconverters find an application in low-frequency, high-power requirements. Control speed of large synchronous motors in the low-speed range is one of the most common applications of three-phase cycloconverters. Figure 12.34 is a diagram of this application. They are also used to control slip frequency in wound rotor induction machines, for supersynchronous cascade (Scherbius system).

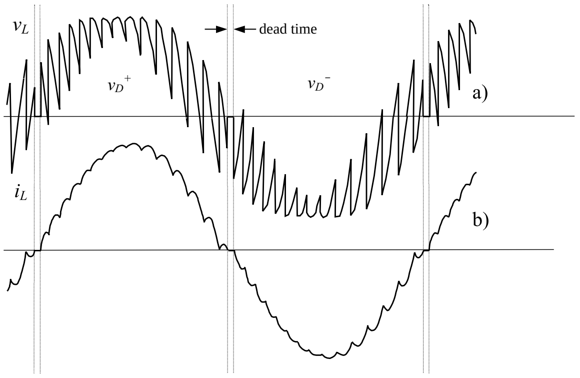


FIGURE 12.33 Cycloconverter operation: (a) voltage waveform; and (b) current waveform for inductive load.

12.2.14 Harmonic Standards and Recommended Practices

In view of the proliferation of power converter equipment connected to the utility system, various national and international agencies have been considering limits on harmonic

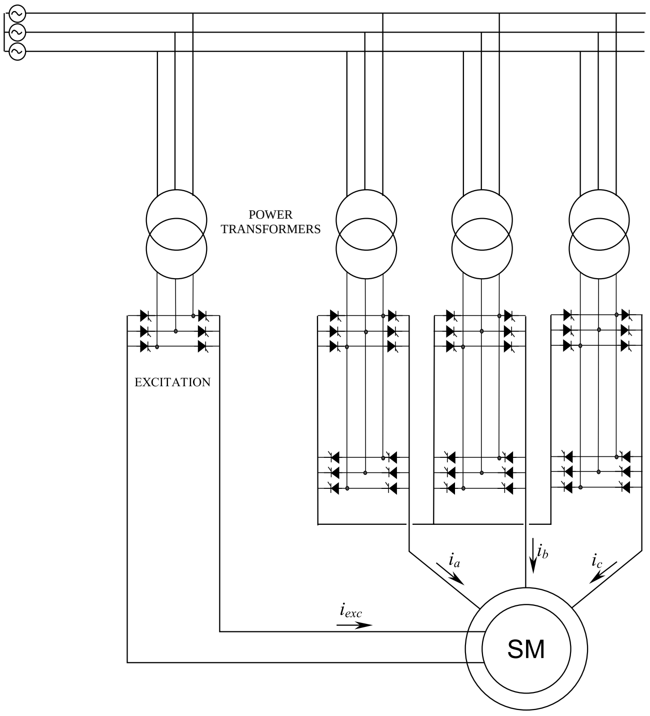


FIGURE 12.34 Synchronous machine drive with a cycloconverter.

TABLE 12.1 Harmonic current limits in percent of fundamental

Short circuit current [pu]	$h < 11$	$11 < h < 17$	$17 < h < 23$	$23 < h < 35$	$35 < h$	THD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20–50	7.0	3.5	2.5	1.0	0.5	8.0
50–100	10.0	4.5	4.0	1.5	0.7	12.0
100–1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

TABLE 12.2 Harmonic voltage limits in percent of fundamental

Voltage Level	2.3–6.9 kV	69–138 kV	>138 kV
Maximum for individual harmonic	3.0	1.5	1.0
Total Harmonic Distortion (THD)	5.0	2.5	1.5

current injection to maintain good power quality. As a consequence, various standards and guidelines have been established that specify limits on the magnitudes of harmonic currents and harmonic voltages.

The Comité Européen de Normalisation Electrotechnique (CENELEC), International Electrical Commission (IEC), and West German Standards (VDE) specify the limits on the voltages (as a percentage of the nominal voltage) at various harmonics frequencies of the utility frequency, when the equipment-generated harmonic currents are injected into a network whose impedances are specified.

In accordance with IEEE-519 standards (Institute of Electrical and Electronic Engineers), Table 12.1 lists the limits on the harmonic currents that a user of power electronics equipment and other nonlinear loads is allowed to inject into the utility system. Table 12.2 lists the quality of voltage that the utility can furnish the user.

In Table 12.1, the values are given at the point of connection of nonlinear loads. The THD is the total harmonic distortion given by Eq. (12.51), and h is the number of the harmonic.

$$\mathrm{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \tag{12.51}$$

The total current harmonic distortion allowed in Table 12.1 increases with the value of short-circuit current.

The total harmonic distortion in the voltage can be calculated in a manner similar to that given by Eq. (12.51). Table 12.2 specifies the individual harmonics and the THD limits on the voltage that the utility supplies to the user at the connection point.

12.3 orce-Commutated Three-Phase Controlled Rectifiers

12.3.1 Basic Topologies and Characteristics

Force-commutated rectifiers are built with semiconductors with gate-turn-off capability. The gate-turn-off capability allows full control of the converter, because valves can be switched *ON* and *OFF* whenever required. This allows commutation of the valves hundreds of times in one period, which is not possible with line-commutated rectifiers, where thyristors are switched ON and OFF only once a cycle. This feature confers the following advantages: (a) the current or voltage can be modulated (pulse width modulation or PWM), generating less harmonic contamination; (b) the power factor can be controlled, and it can even be made to lead; (c) rectifiers can be built as voltage or current source types; and (d) the reversal of power in thyristor rectifiers is by reversal of voltage at the dc link. By contrast, force-commutated rectifiers can be implemented for either reversal of voltage or reversal of current.

There are two ways to implement force-commutated three-phase rectifiers: (a) as a current source rectifier, where power reversal is by dc voltage reversal; and (b) as a voltage source rectifier, where power reversal is by current reversal at the dc link. Figure 12.35 shows the basic circuits for these two topologies.

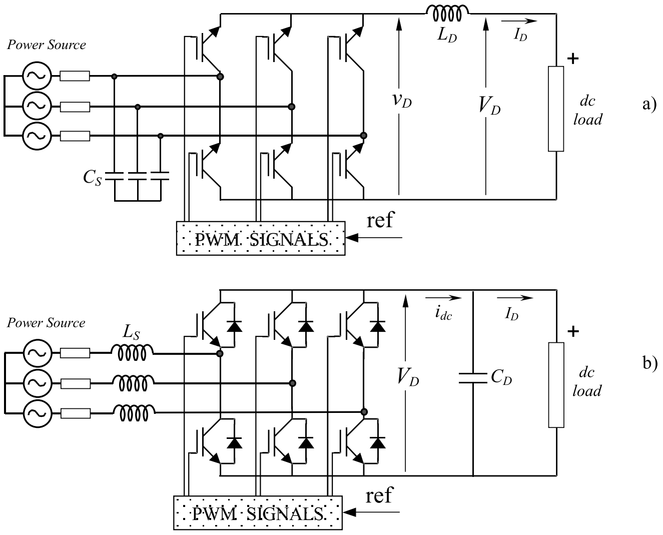


FIGURE 12.35 Basic topologies for force-commutated PWM rectifiers: (a) current source rectifier; and (b) voltage source rectifier.

12.3.2 Operation of the Voltage Source Rectifier

The voltage source rectifier is by far the most widely used, and because of the duality of the two topologies showed in Fig. 12.35, only this type of force-commutated rectifier will be explained in detail.

The voltage source rectifier operates by keeping the dc link voltage at a desired reference value, using a feedback control loop as shown in Fig. 12.36. To accomplish this task, the dc link voltage is measured and compared with a reference V_{REF}. The error signal generated from this comparison is used to switch the six valves of the rectifier *ON* and *OFF*. In this way, power can come or return to the ac source according to dc link voltage requirements. Voltage V_D is measured at capacitor C_D.

When the current I_D is positive (rectifier operation), the capacitor C_D is discharged, and the error signal ask the Control Block for more power from the ac supply. The Control Block takes the power from the supply by generating the appropriate PWM signals for the six valves. In this way, more current flows from the ac to the dc side, and the capacitor voltage is recovered. Inversely, when I_D becomes negative (inverter operation), the capacitor C_D is overcharged, and the error signal asks the control to discharge the capacitor and return power to the ac mains.

The PWM control not only can manage the active power, but also reactive power, allowing this type of rectifier to correct power factor. In addition, the ac current waveforms can be maintained as almost sinusoidal, which reduces harmonic contamination to the mains supply.

Pulsewidth-modulation consists of switching the valves ON and OFF, following a pre-established template. This template could be a sinusoidal waveform of voltage or current. For example, the modulation of one phase could be as the one shown in Fig. 12.37. This PWM pattern is a periodical waveform whose fundamental is a voltage with the same frequency of the template. The amplitude of this fundamental, called V_{MOD} in Fig. 12.37, is also proportional to the amplitude of the template.

To make the rectifier work properly, the PWM pattern must generate a fundamental V_{MOD} with the same frequency as the power source. Changing the amplitude of this fundamental, and its phase-shift with respect to the mains, the rectifier can be controlled to operate in the four quadrants: leading power factor rectifier, lagging power factor rectifier, leading power factor inverter, and lagging power factor inverter. Changing the pattern of modulation, as shown in Fig. 12.38, modifies the magnitude of $\mathrm{V_{MOD}}$. Displacing the PWM pattern changes the phase-shift.

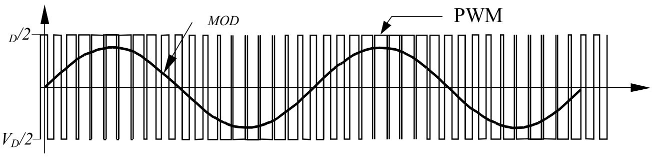


FIGURE 12.37 A PWM pattern and its fundamental V_{MOD}.

The interaction between V_{MOD} and V (source voltage) can be seen through a phasor diagram. This interaction permits understanding of the four-quadrant capability of this rectifier. In Fig. 12.39, the following operations are displayed: (a) rectifier at unity power factor; (b) inverter at unity power factor; (c) capacitor (zero power factor); and (d) inductor (zero power factor).

In Fig. 12.39 I_s is the rms value of the source current i_s. This current flows through the semiconductors in the same way as shown in Fig. 12.40. During the positive half cycle, the transistor T_N connected at the negative side of the dc link is switched *ON*, and the current i_s begins to flow through T_N (i_{Tn}). The current returns to the mains and comes back to the valves, closing a loop with another phase, and passing through a diode connected at the same negative terminal of the dc link. The current can also go to the dc load (inversion) and return through another transistor located at the positive terminal of the dc link. When the transistor T_N is switched *OFF*, the current path is interrupted, and the current begins to flow through diode D_P, connected at the positive terminal of the dc link. This current, called i_{Dp} in Fig. 12.39, goes directly

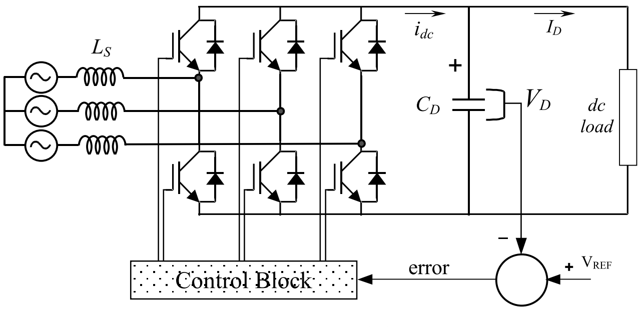


FIGURE 12.36 Operation principle of the voltage source rectifier.

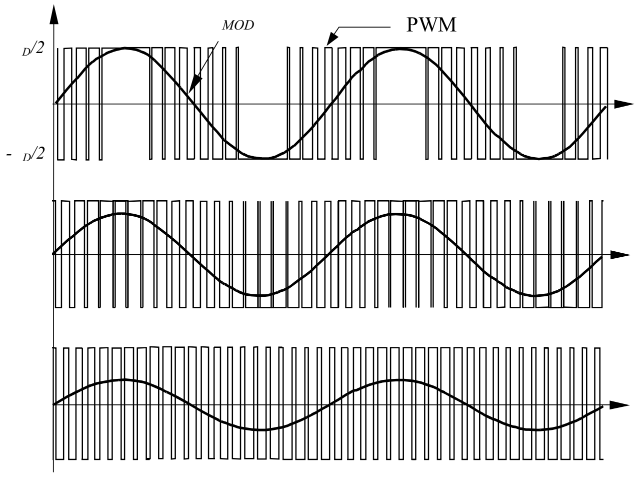


FIGURE 12.38 Changing V_{MOD} through the PWM pattern.

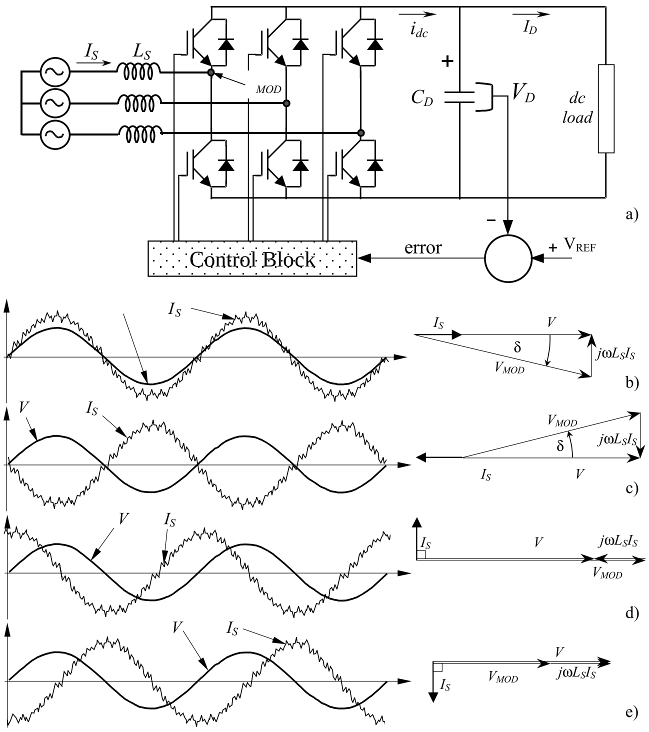


FIGURE 12.39 Four-quadrant operation of the force-commutated rectifier: (a) the PWM force-commutated rectifier; (b) rectifier operation at unity power factor; (c) inverter operation at unity power factor; (d) capacitor operation at zero power factor; and (e) inductor operation at zero power factor.

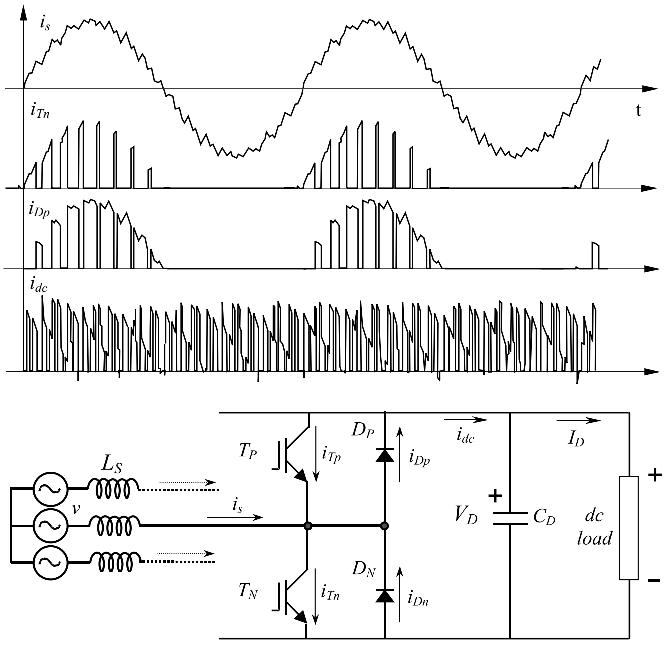


FIGURE 12.40 Current waveforms through the mains, the valves, and the dc link.

to the dc link, helping in the generation of the current i_{dc}. The current i_{dc} charges the capacitor C_D and permits the rectifier to produce dc power. The inductances L_S are very important in this process, because they generate an induced voltage that allows conduction of the diode D_P. A similar operation occurs during the negative half cycle, but with T_P and D_N (see Fig. 12.40).

Under inverter operation, the current paths are different because the currents flowing through the transistors come mainly from the dc capacitor C_D. Under rectifier operation, the circuit works like a Boost converter, and under inverter operation it works as a Buck converter.

To have full control of the operation of the rectifier, their six diodes must be polarized negatively at all values of instantaneous ac voltage supply. Otherwise, the diodes will conduct, and the PWM rectifier will behave like a common diode rectifier bridge. The way to keep the diodes blocked is to ensure a dc link voltage higher than the peak dc voltage generated by the diodes alone, as shown in Fig. 12.41. In this way, the diodes remain polarized negatively, and they will conduct only when at least one transistor is switched *ON*, and favorable instantaneous ac voltage conditions are given. In Fig. 12.41 V_D represents the capacitor dc voltage, which is kept higher than the normal diode-bridge rectification value v_{BRIDGE}. To maintain this condition, the rectifier must have a control loop like the one displayed in Fig. 12.36.

12.3.3 P M Phase-to-Phase and Phase-to-Neutral Voltages

The PWM waveforms shown in the preceding figures are voltages measured between the middle point of the dc voltage and the corresponding phase. The phase-to-phase PWM voltages can be obtained with the help of Eq. 12.52, where the voltage V_{PWM}^{AB} is evaluated,

$$V_{\mathrm{PWM}}^{AB} = V_{\mathrm{PWM}}^{A} - V_{\mathrm{PWM}}^{B} \qquad (12.52)$$

where V_{PWM}^{A}, and V_{PWM}^{B} are the voltages measured between the middle point of the dc voltage, and the phases *a* and *b*,

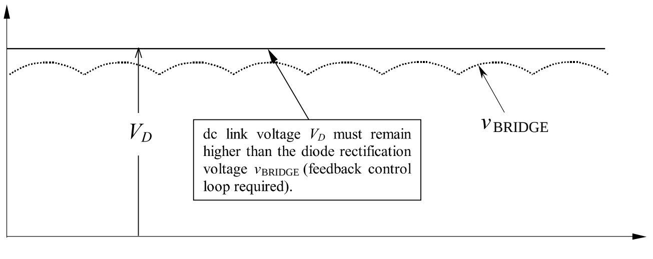


FIGURE 12.41 Direct current link voltage condition for operation of the PWM rectifier.

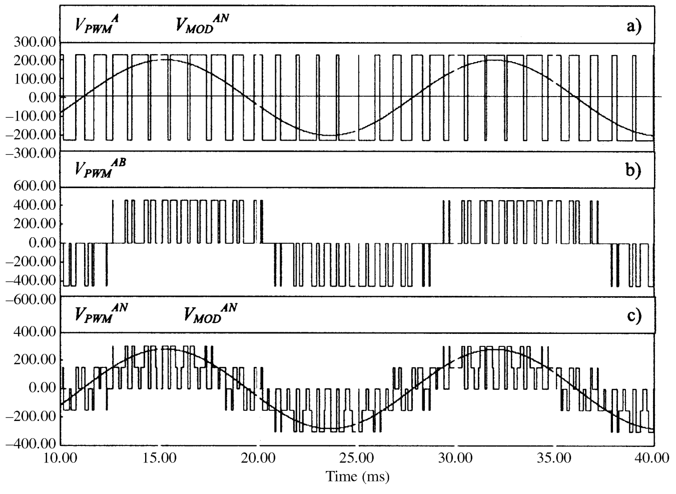


FIGURE 12.42 PWM phase voltages: (a) PWM phase modulation; (b) PWM phase-to-phase voltage; and (c) PWM phase-to-neutral voltage.

respectively. In a less straightforward fashion, the phase-to-neutral voltage can be evaluated with the help of Eq. (12.53):

$$V_{\mathrm{PWM}}^{AN} = 1/3(V_{\mathrm{PWM}}^{AB} - V_{\mathrm{PWM}}^{\mathrm{CA}}) \tag{12.53}$$

where V_{PWM}^{AN} is the phase-to-neutral voltage for phase a, and V_{PWM}^{jk} is the phase-to-phase voltage between phase j and phase k. Figure 12.42 shows the PWM patterns for the phase-to-phase and phase-to-neutral voltages.

12.3.4 Control of the DC Link Voltage

Control of dc link voltage requires a feedback control loop. As already explained in Section 12.3.2, the dc voltage V_D is compared with a reference V_{REF}, and the error signal "e" obtained from this comparison is used to generate a template waveform. The template should be a sinusoidal waveform with the same frequency of the mains supply. This template is used to produce the PWM pattern, and allows controlling the rectifier in two different ways: 1) as a voltage-source, current-controlled PWM rectifier; or 2) as a voltage-source, voltage-controlled PWM rectifier. The first method controls the input current, and the second controls the magnitude and phase of the voltage V_{MOD}. The current controlled method is simpler and more stable than the voltage-controlled method, and for these reasons it will be explained first.

12.3.4.1 Voltage-Source Current-Controlled PWM Rectifier

This method of control is shown in the rectifier in Fig. 12.43. Control is achieved by measuring the instantaneous phase currents and forcing them to follow a sinusoidal current reference template I ref. The amplitude of the current reference template $I_{\max}$ is evaluated by using the following equation:

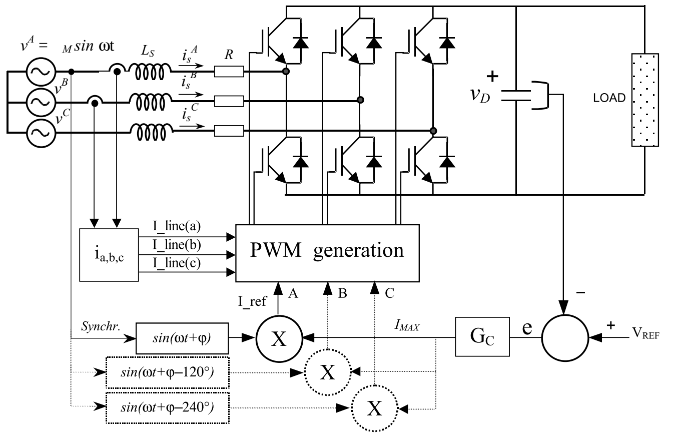


FIGURE 12.43 Voltage-source current-controlled PWM rectifier.

$$I_{\max} = G_C \cdot e = G_C \cdot (V_{\mathrm{REF}} - v_D) \tag{12.54}$$

Where G_C is shown in Fig. 12.43, and represents a controller such as PI, P, Fuzzy or other. The sinusoidal waveform of the template is obtained by multiplying $I_{\max}$ with a *sine* function, with the same frequency of the mains, and with the desired phase-shift angle φ, as shown in Fig. 12.43. Further, the template must be synchronized with the power supply. After that, the template has been created, and it is ready to produce the PWM pattern.

However, one problem arises with the rectifier because the feedback control loop on the voltage $\mathrm{V_C}$ can produce instability. Then it becomes necessary to analyze this problem during rectifier design. Upon introducing the voltage feedback and the G_C controller, the control of the rectifier can be represented in a block diagram in Laplace dominion, as shown in Fig. 12.44. This block diagram represents a linearization of the system around an operating point, given by the rms value of the input current I_S.

The blocks $G_1(S)$ and $G_2(S)$ in Fig. 12.44 represent the transfer function of the rectifier (around the operating point), and the transfer function of the dc link capacitor C_D, respectively

$$G_1(S) = \frac{\Delta P_1(S)}{\Delta I_S(S)} = 3 \cdot (V\cos\varphi - 2RI_S - L_S I_S S) \tag{12.55}$$

$$G_2(S) = \frac{\Delta V_D(S)}{\Delta P_1(S) - \Delta P_2(S)} = \frac{1}{V_D \cdot C_D \cdot S} \tag{12.56}$$

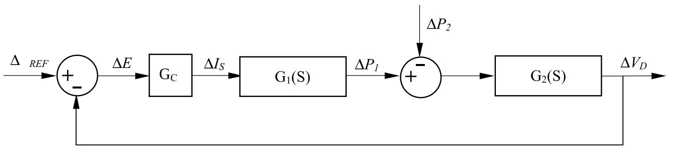


FIGURE 12.44 Close-loop rectifier transfer function.

where $\Delta P_1(S)$ and $\Delta P_2(S)$ represent the input and output power of the rectifier in Laplace dominion, V the rms value of the mains voltage supply (phase-to-neutral), I_S the input current being controlled by the template, L_S the input inductance, and R the resistance between the converter and power supply. According to stability criteria, and assuming a *PI* controller, the following relations are obtained:

$$I_S \leq \frac{C_D \cdot V_D}{3K_P \cdot L_S} \tag{12.57}$$

$$I_S \leq \frac{K_P \cdot V \cdot \cos\varphi}{2R \cdot K_P + L_S \cdot K_I} \tag{12.58}$$

These two relations are useful for the design of the current-controlled rectifier. They relate the values of dc link capacitor, dc link voltage, rms voltage supply, input resistance and inductance, and input power factor, with the rms value of the input current I_S. With these relations the proportional and integral gains K_P and K_I can be calculated to ensure stability of the rectifier. These relations only establish limitations for rectifier operation, because negative currents always satisfy the inequalities.

With these two stability limits satisfied, the rectifier will keep the dc capacitor voltage at the value of V_{REF} (PI controller), for all load conditions, by moving power from the ac to the dc side. Under inverter operation, the power will move in the opposite direction.

Once the stability problems have been solved, and the sinusoidal current template has been generated, a modulation method will be required to produce the PWM pattern for the power valves. The PWM pattern will switch the power valves to force the input currents I line to follow the desired current template I ref. There are many modulation methods in the literature, but three methods for voltage source current controlled rectifiers are the most widely used ones: *periodical sampling* (PS); *hysteresis band* (HB); and *triangular carrier* (TC).

The PS method switches the power transistors of the rectifier during the transitions of a square wave clock of fixed frequency: the *periodical sampling* frequency. In each transition, a comparison between I ref and I line is made, and corrections take place. As shown in Fig. 12.45a, this type of control is very simple to implement: only a comparator and a D-type flip-flop are needed per phase. The main advantage of this method is that the minimum time between switching transitions is limited to the period of the sampling clock. However, the actual switching frequency is not clearly defined.

The HB method switches the transistors when the error between I ref and I line exceeds a fixed magnitude: the *hysteresis band*. As can be seen in Fig. 12.45b, this type of control needs a single comparator with hysteresis per phase. In this case the switching frequency is not determined, but its maximum value can be evaluated through the following equation:

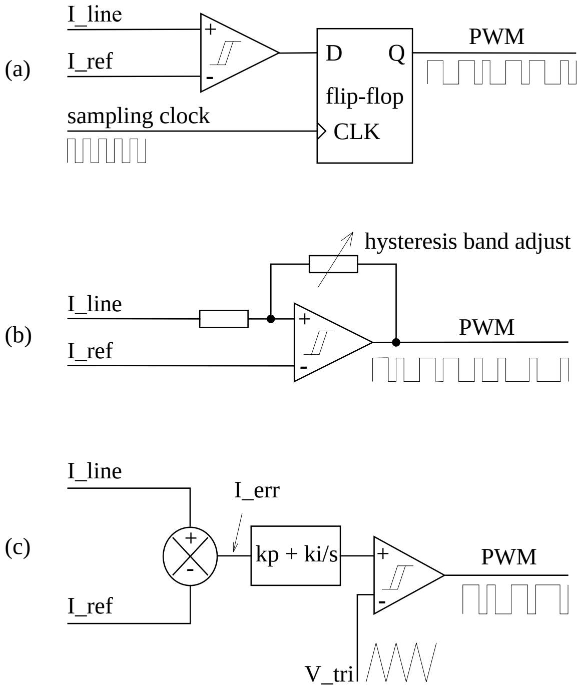


FIGURE 12.45 Modulation control methods: (a) periodical sampling; (b) hysteresis band; and (c) triangular carrier.

$$F_S^{\max} = \frac{V_D}{4h \cdot L_S} \tag{12.59}$$

where h is the magnitude of the hysteresis band.

The TC method shown in Fig. 12.45c, compares the error between I ref and I line with a triangular wave. This triangular wave has fixed amplitude and frequency and is called the *triangular carrier.* The error is processed through a proportional-integral (PI) gain stage before comparison with the triangular carrier takes place. As can be seen, this control scheme is more complex than PS and HB. The values for *kp* and *ki* determine the transient response and steady-state error of the TC method. It has been found empirically that the values for *kp* and *ki* shown in Eqs. (12.60) and (12.61) give a good dynamic performance under several operating conditions:

$$kp = \frac{L_S \cdot \omega_c}{2 \cdot V_D} \tag{12.60}$$

$$ki = \omega_c \cdot kp^* \tag{12.61}$$

where L_S is the total series inductance seen by the rectifier, ω_c is the triangular carrier frequency, and V_D is the dc link voltage of the rectifier.

In order to measure the level of distortion (or undesired harmonic generation) introduced by these three control methods, Eq. (12.62) is defined:

$$\% \text{ Distortion} = \frac{100}{I_{\text{rms}}}\sqrt{\frac{1}{T}\int_T (i_{\text{line}} - i_{\text{ref}})^2\, dt} \tag{12.62}$$

In Eq. (12.62), the term Irms is the effective value of the desired current. The term inside the square root gives the rms value of the error current, which is undesired. This formula measures the percentage of error (or distortion) of the generated waveform. This definition considers the ripple, amplitude, and phase errors of the measured waveform, as opposed to the THD, which does not take into account offsets, scalings, and phase shifts.

Figure 12.46 shows the current waveforms generated by the three forementioned methods. The example uses an average switching frequency of 1.5 kHz. The PS is the worst, but its implementation is digitally simpler. The HB method and TC with PI control are quite similar, and the TC with only proportional control gives a current with a small phase shift. However, Fig. 12.47 shows that the higher the switching frequency, the closer the results obtained with the different modulation methods. Over 6 kHz of switching frequency, the distortion is very small for all methods.

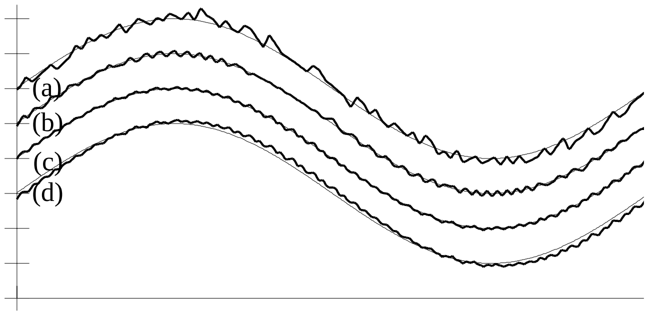


FIGURE 12.46 Waveforms obtained using 1.5 kHz switching frequency and $L_S = 13$ mH: (a) PS method; (b) HB method; (c) TC method ($kp + ki$); and (d) TC method (kp only).

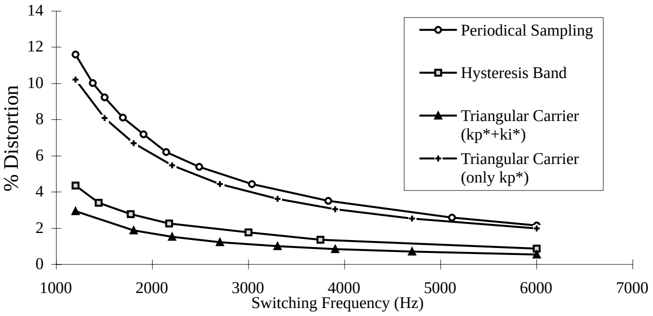


FIGURE 12.47 Distortion comparison for a sinusoidal current reference.

12.3.4.2 Voltage-Source Voltage-Controlled PWM Rectifier

Figure 12.48 shows a one-phase diagram from which the control system for a voltage-source voltage-controlled rectifier is derived. This diagram represents an equivalent circuit of the fundamentals, that is, pure sinusoidal at the mains side, and pure dc at the dc link side. The control is achieved by creating a sinusoidal voltage template V_{MOD}, which is modified in amplitude and angle to interact with the mains voltage V. In this way the input currents are controlled without measuring them. The template V_{MOD} is generated using the differential equations that govern the rectifier.

The following differential equation can be derived from Fig. 12.48:

$$v(t) = L_S \frac{di_s}{dt} + Ri_s + v_{\text{MOD}}(t) \tag{12.63}$$

Assuming that $v(t) = V\sqrt{2}\sin\omega t$, then the solution for $i_s(t)$, to acquire a template V_{MOD} able to make the rectifier work at constant power factor should be of the form:

$$i_s(t) = I_{\max}(t)\sin(\omega t + \varphi) \tag{12.64}$$

Equations (12.63), (12.64), and $v(t)$ allow a function of time able to modify V_{MOD} in amplitude and phase that will make the rectifier work at a fixed power factor. Combining these equations with $v(t)$ yields

$$\begin{aligned} v_{\text{MOD}}(t) &\\ = &\left[V\sqrt{2} + X_S I_{\max}\sin\varphi - \left(RI_{\max} + L_S\frac{dI_{\max}}{dt}\right)\cos\varphi\right]\sin\omega t \\ &- \left[X_S I_{\max}\cos\varphi + \left(RI_{\max} + L_S\frac{dI_{\max}}{dt}\right)\sin\varphi\right]\cos\omega t \end{aligned} \tag{12.65}$$

Equation (12.65) provides a template for V_{MOD}, which is controlled through variations of the input current amplitude $I_{\max}$. The derivatives of $I_{\max}$ into Eq. (12.65) make sense, because $I_{\max}$ changes every time the dc load is modified. The term X_S in Eq. (12.65) is ωL_S. This equation can also be

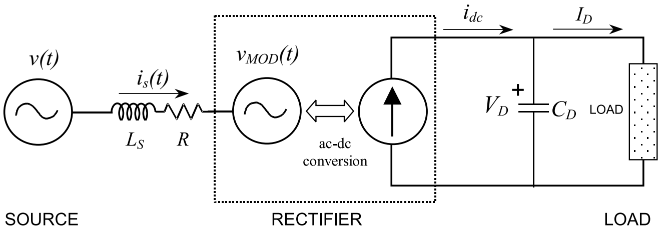


FIGURE 12.48 One-phase fundamental diagram of the voltage-source rectifier.

written for unity power factor operation. In such a case $\cos\varphi = 1$, and $\sin\varphi = 0$:

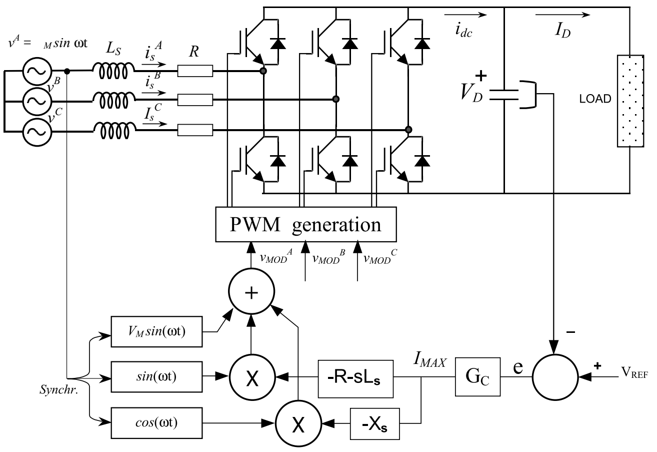
$$v_{\mathrm{MOD}}(t) = \left(V\sqrt{2} - RI_{\max} - L_S\frac{dI_{\max}}{dt}\right)\sin\omega t - X_S I_{\max})\cos\omega t \qquad (12.66)$$

With this last equation, a unity power factor, voltage source, voltage controlled PWM rectifier can be implemented as shown in Fig. 12.49. It can be observed that Eqs. (12.65) and (12.66) have an *in-phase* term with the mains supply ($\sin\omega t$), and an *in-quadrature* term ($\cos\omega t$). These two terms allow the template V_{MOD} to change in magnitude and phase so as to have full unity power factor control of the rectifier.

Compared with the control block of Fig. 12.43, in the voltage-source voltage-controlled rectifier of Fig. 12.49, there is no need to sense the input currents. However, to ensure stability limits as good as the limits of the current-controlled rectifier, blocks "—R—sL$_s$" and "—x$_S$" in Fig. 12.49 have to emulate and reproduce exactly the real values of R, X_S, and L_S of the power circuit. However, these parameters do not remain constant, and this fact affects the stability of this system, making it less stable than the system shown in Fig. 12.43. In theory, if the impedance parameters are reproduced exactly, the stability limits of this rectifier are given by the same equations as used for the current-controlled rectifier seen in Fig. 12.43 (Eqs. (12.57) and (12.58).

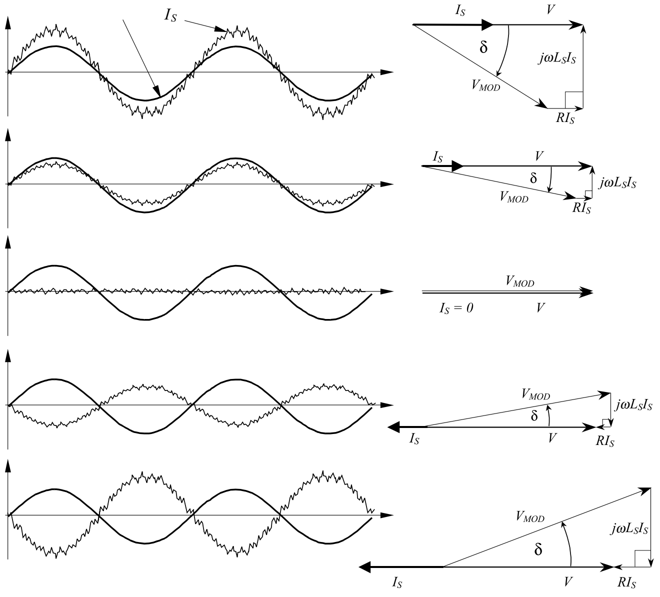
Under steady-state, $I_{\max}$ is constant, and Eq. (12.66) can be written in terms of phasor diagram, resulting in Eq. (12.67). As shown in Fig. 12.50, different operating conditions for the unity power factor rectifier can be displayed with this equation:

$$\vec{V}_{\mathrm{MOD}} = \vec{V} - R\vec{I}_S - jX_s\vec{I}_S \qquad (12.67)$$



$v^A = _M\sin\omega t$
L_S
i_s^A
R
v^B
i_s^B
v^C
i_s^C
i_{dc}
I_D
V_D
+
LOAD
PWM generation
v_{MOD}^A
v_{MOD}^B
v_{MOD}^C
+
$V_M sin(\omega t)$
$sin(\omega t)$
$cos(\omega t)$
Synchr.
X
X
-R-sL$_s$
-X$_s$
I_{MAX}
G$_C$
e
−
+
V$_{REF}$

FIGURE 12.49 Implementation of the voltage-controlled rectifier for unity power factor operation.



I_S
I_S
V
δ
$j\omega L_S I_S$
V_{MOD}
RI_S
I_S
V
δ
$j\omega L_S I_S$
V_{MOD}
RI_S
V_{MOD}
$I_S = 0$
V
V_{MOD}
δ
$j\omega L_S I_S$
I_S
V
RI_S
V_{MOD}
$j\omega L_S I_S$
δ
I_S
V
RI_S

FIGURE 12.50 Steady-state operation of the unity power factor rectifier, under different load conditions.

With the sinusoidal template V_{MOD} already created, a modulation method to commutate the transistors will be required. As in the case of the current-controlled rectifier, there are many methods to modulate the template, with the most well known the so-called *sinusoidal pulse width modulation* (SPWM), which uses a triangular carrier to generate the PWM as shown in Fig. 12.51. Only this method will be described in this chapter.

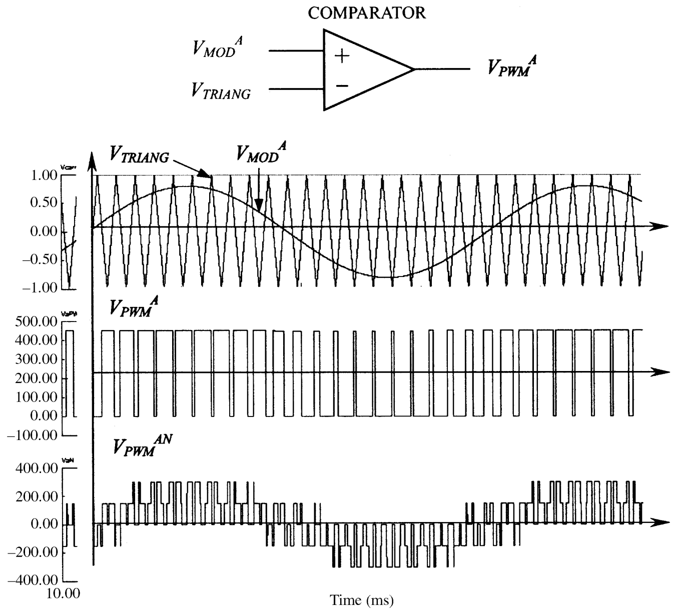


FIGURE 12.51 Sinusoidal modulation method based on triangular carrier.

In this method, there are two important parameters to define: the amplitude modulation ratio, or modulation index m, and the frequency modulation ratio p. Definitions are given by

$$m = \frac{V_{\mathrm{MOD}}{}^{\max}}{V_{\mathrm{TRIANG}}{}^{\max}} \tag{12.68}$$

$$p = \frac{f_T}{f_S} \tag{12.69}$$

Where $V_{\mathrm{MOD}}^{\max}$ and $V_{\mathrm{TRIANG}}^{\max}$ are the amplitudes of V_{MOD} and V_{TRIANG}, respectively. On the other hand, f_S is the frequency of the mains supply and f_T the frequency of the triangular carrier. In Fig. 12.51, $m = 0.8$ and $p = 21$. When $m > 1$ overmodulation is defined.

The modulation method described in Fig. 12.51 has a harmonic content that changes with p and m. When $p < 21$, it is recommended that synchronous PWM be used, which means that the triangular carrier and the template should be synchronized. Furthermore, to avoid subharmonics, it is also desired that p be an integer. If p is an odd number, even harmonics will be eliminated. If p is a multiple of 3, then the PWM modulation of the three phases will be identical. When m increases, the amplitude of the fundamental voltage increases proportionally, but some harmonics decrease. Under overmodulation, the fundamental voltage does not increase linearly, and more harmonics appear. Figure 12.52 shows the harmonic spectrum of the three-phase PWM voltage waveforms for different values of m, and $p = 3k$ where k is an odd number.

Due to the presence of the input inductance L_S, the harmonic currents that result are proportionally attenuated with the harmonic number. This characteristic is shown in the current waveforms of Fig. 12.53, where larger p numbers generate cleaner currents. The rectifier that originated the currents of Fig. 12.53 has the following characteristics: $V_D = 450\ V_{\mathrm{dc}}$, $V_{f-f}^{\mathrm{rms}} = 220\ V_{\mathrm{ac}}$, $L_S = 3$ mH, and input current $I_s = 80$ A rms. It can be observed that with $p > 21$ the current distortion is quite small. The value of $p = 81$ in Fig. 12.53 produces an almost pure sinusoidal waveform, and it means 4860 Hz of switching frequency at 60 Hz or only 4.050 Hz in a rectifier operating in a 50-Hz supply. This switching frequency can be managed by MOSFETs, IGBTs, and even power Darlingtons. Then $p = 81$ is feasible for today's low and medium power rectifiers.

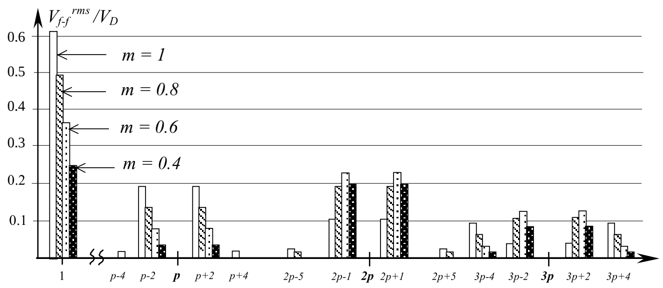


FIGURE 12.52 Harmonic spectrum for SPWM modulation.

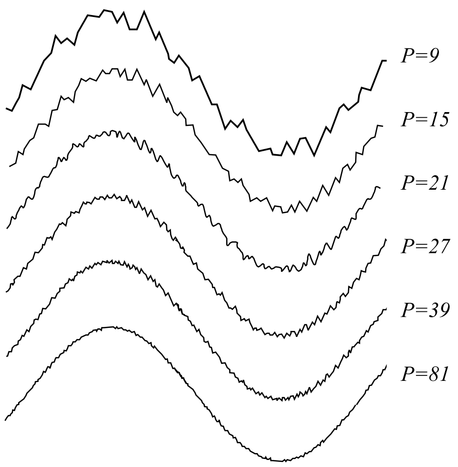


FIGURE 12.53 Current waveforms for different values of p.

12.3.4.3 Voltage-Source Load-Controlled PWM Rectifier

A simple method of control for small PWM rectifiers (up to 10–20 kW) is based on direct control of the dc current. Figure 12.54 shows the schematic of this control system. The fundamental voltage V_{MOD} modulated by the rectifier is produced by a fixed and unique PWM pattern, which can be carefully selected to eliminate most undesirable harmonics. As the PWM does not change, it can be stored in a permanent digital memory (ROM).

The control is based on changing the power angle δ between the mains voltage V and fundamental PWM voltage V_{MOD}. When δ changes, the amount of power flow transferred from the ac to the dc side also changes. When the power angle is negative (V_{MOD} lags V), the power flow goes from the ac to the dc side. When the power angle is positive, the power flows

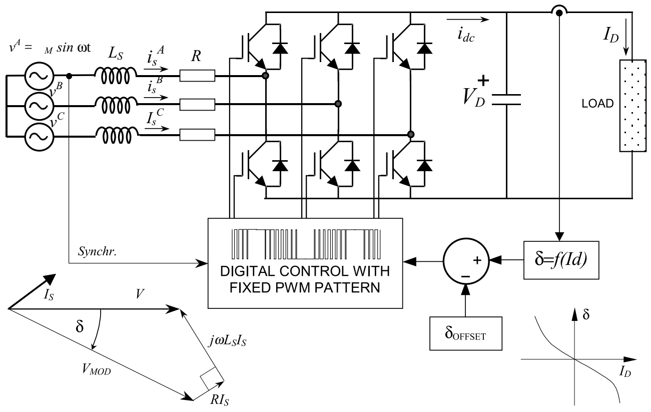


FIGURE 12.54 Voltage-source load-controlled PWM rectifier.

in the opposite direction. Then, the power angle can be controlled through the current I_D. The voltage V_D does not need to be sensed, because this control establishes a stable dc voltage operation for each dc current and power angle. With these characteristics, it is possible to find a relation between I_D and δ so as to obtain constant dc voltage for all load conditions. This relation is given by

$$I_D = f(\delta) = \frac{V(\cos\delta - \omega L_S/R\sin\delta - 1)}{R[1 + (\omega L_S/R)^2]} \tag{12.70}$$

From Eq. (12.70) a plot and a reciprocal function $\delta = f(I_D)$ are obtained to control the rectifier. The relation between I_D and δ allows for leading power factor operation and null regulation. The leading power factor operation is shown in the phasor diagram of Fig. 12.54.

The control scheme of the voltage source load-controlled rectifier is characterized by the following: i) there are neither input current sensors nor dc voltage sensor; ii) it works with a fixed and predefined PWM pattern; iii) it presents very good stability; iv) its stability does not depend on the size of the dc capacitor; v) it can work at leading power factor for all load conditions; and vi) it can be adjusted with Eq. (12.70) to work at zero regulation. The drawback appears when R in Eq. 12.70 becomes negligible, because in such a case the control system is unable to find an equilibrium point for the dc link voltage. This is why this control method is not applicable to large systems.

12.3.5 New Technologies and Applications of Force-Commutated Rectifiers

The additional advantages of force-commutated rectifiers with respect to line-commutated rectifiers make them better candidates for industrial requirements. They permit new applications such as rectifiers with harmonic elimination capability (active filters), power factor compensators, machine drives with four-quadrant operation, frequency links to connect 50-Hz with 60-Hz systems, and regenerative converters for traction power supplies. Modulation with very fast valves such as IGBTs permit almost sinusoidal currents to be obtained. The dynamics of these rectifiers is so fast that they can reverse power almost instantaneously. In machine drives, current source PWM rectifiers, like the one shown in Fig. 12.35a, can be used to drive dc machines from the three-phase supply. Four-quadrant applications, using voltage-source PWM rectifiers, are extended for induction machines, synchronous machines with starting control, and special machines such as brushless-dc motors. Back-to-back systems are being used in Japan to link power systems of different frequencies.

12.3.5.1 Active Power Filter

Force-commutated PWM rectifiers can work as active power filters. The voltage-source current-controlled rectifier has the capability to eliminate harmonics produced by other polluting loads. It only needs to be connected as shown in Fig. 12.55.

The current sensors are located at the input terminals of the power source, and these currents (instead of the rectifier currents) are forced to be sinusoidal. As there are polluting loads in the system, the rectifier is forced to deliver the harmonics that loads need, because the current sensors do not allow the harmonics going to the mains. As a result, the rectifier currents become distorted, but an adequate dc capacitor C_D can keep the dc link voltage in good shape. In this way the rectifier can do its duty, and also eliminate harmonics to the source. In addition, it also can compensate power factor and unbalanced load problems.

12.3.5.2 Frequency Link Systems

Frequency link systems permit power to be transferred from one frequency to another one. They are also useful for linking unsynchronized networks. Line-commutated converters are widely used for this application, but they have some drawbacks that force-commutated converters can eliminate. For example, the harmonic filters requirement, the poor power factor, and the necessity to count with a synchronous compensator when generating machines at the load side are absent. Figure 12.56 shows a typical line-commutated system in which a 60-Hz load is fed by a 50-Hz supply. As the 60-Hz side needs excitation to commutate the valves, a synchronous compensator has been required.

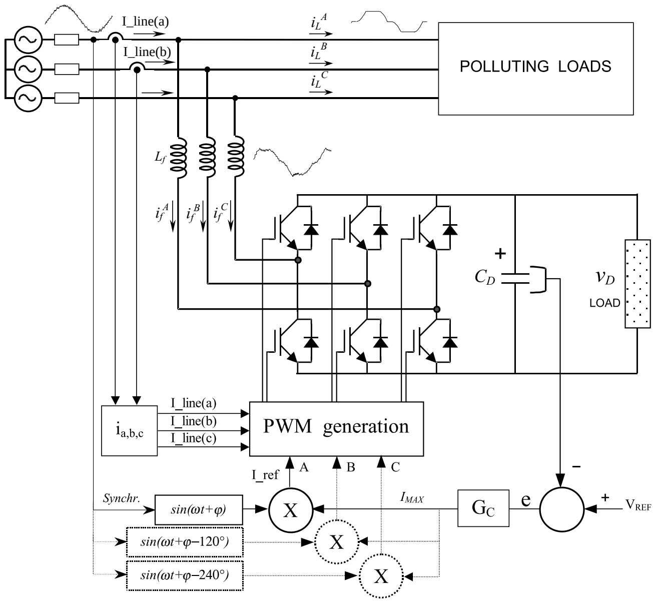


FIGURE 12.55 Voltage-source rectifier with harmonic elimination capability.

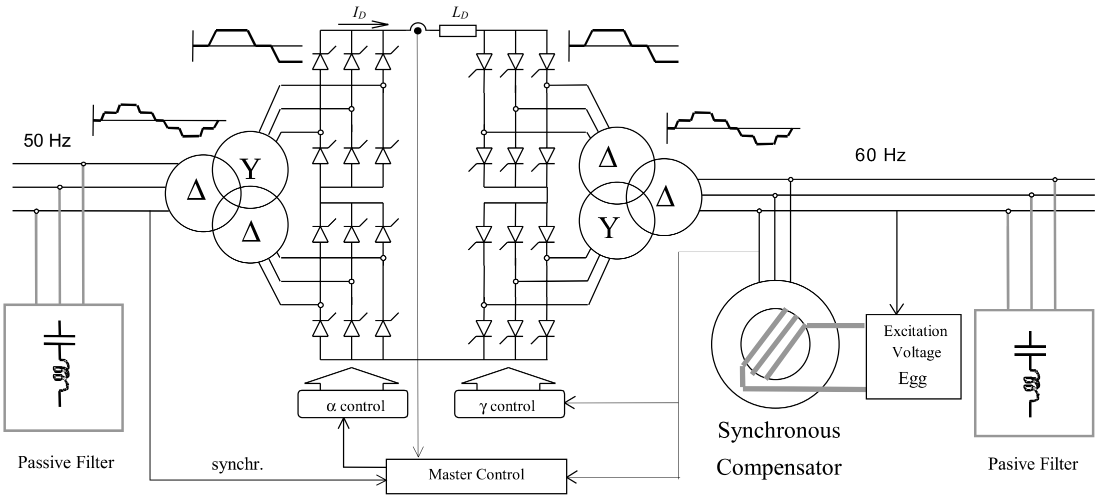


FIGURE 12.56 Frequency link systems with line-commutated converters.

In contrast, an equivalent system with force-commutated converters is simpler, cleaner, and more reliable. It is implemented with a dc voltage-controlled rectifier, and another identical converter working in the inversion mode. The power factor can be adjusted independently at the two ac terminals, and filters or synchronous compensators are not required. Figure 12.57 shows a frequency link system with force-commutated converters.

12.3.5.3 Special Topologies for High-Power Applications

High-power applications require series- and/or parallel-connected rectifiers. Series and parallel operation with force-commutated rectifiers allow improving the power quality because harmonic cancellation can be applied to these topologies. Figure 12.58 shows a series connection of force-commutated rectifiers, where the modulating carriers of the valves in each bridge are shifted to cancel harmonics. The example uses sinusoidal PWM that are with triangular carrier shifted.

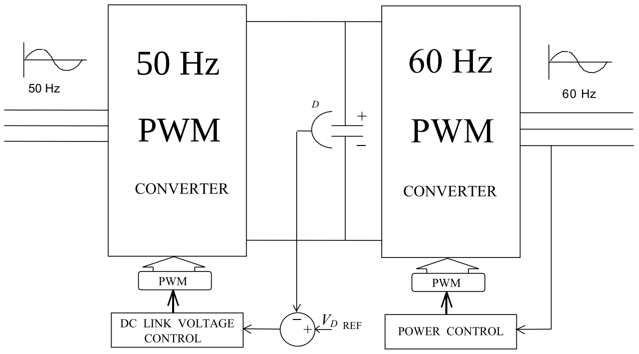


FIGURE 12.57 Frequency link systems with force-commutated converters.

The waveforms of the input currents for the series connection system are shown in Fig. 12.59. The frequency modulation ratio shown in this figure is for $p = 9$. The carriers are shifted by 90° each to obtain harmonics cancellation. Shifting of the carriers δ_T depends on the number of converters in series (or in parallel), and is given by

$$\delta_T = \frac{2\pi}{n} \tag{12.71}$$

where n is the number of converters in series or in parallel. It can be observed that despite the low value of p, the total current becomes quite clean, and clearly better than the current of one of the converters in the chain.

The harmonic cancellation with series- or parallel-connected rectifiers, using the same modulation but the carriers shifted, is quite effective. The resultant current is better with n converters and frequency modulation $p = p_1$ than with one converter and $p = n \cdot p_1$. This attribute is verified in Fig. 12.60, where the total current of four converters in series with $p = 9$ and carriers shifted is compared with the current of only one converter and $p = 36$. This technique also allows for the use of valves with slow commutation times, such as high-power GTOs. Generally, high-power valves have low commutation times and hence the parallel and/or series options remain very attractive.

Another special topology for high power was implemented for ABB (Asea Brown Boveri) in Bremen. A 100-MW power converter supplies energy to the railways at $1\frac{2}{3}$ Hz. It uses basic "H" bridges like the one shown in Fig. 12.61, connected to the load through power transformers. These transformers are

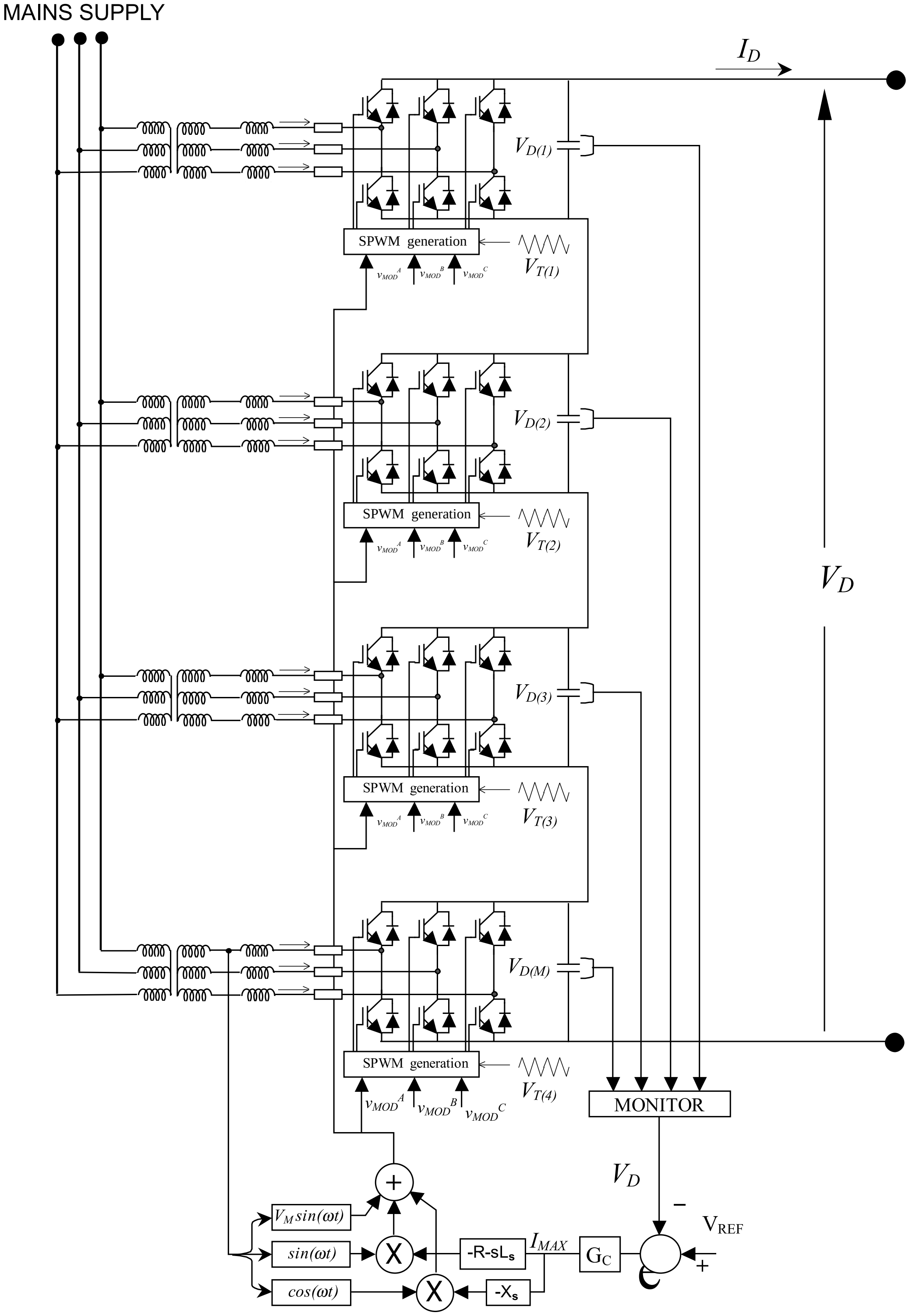

MAINS SUPPLY
I_D
$V_{D(1)}$
SPWM generation
v_{MOD}^A
v_{MOD}^B
v_{MOD}^C
$V_{T(1)}$
$V_{D(2)}$
SPWM generation
$V_{T(2)}$
V_D
$V_{D(3)}$
SPWM generation
$V_{T(3)}$
$V_{D(M)}$
SPWM generation
$V_{T(4)}$
MONITOR
V_D
−
V_{REF}
+
+
$V_M sin(\omega t)$
$sin(\omega t)$
$cos(\omega t)$
X
X
-R-sL$_s$
I_{MAX}
-X$_s$
G$_C$

FIGURE 12.58 Series connection system with force-commutated rectifiers.

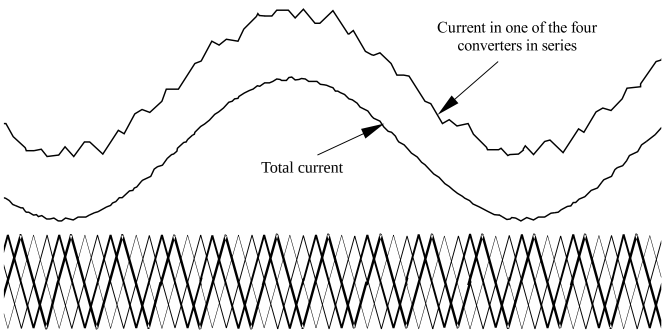


FIGURE 12.59 Input currents and carriers of the series connection system of Fig. 12.58.

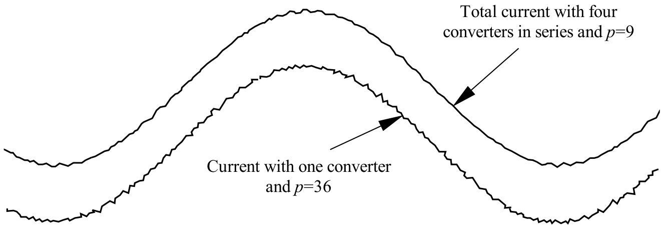


FIGURE 12.60 Four converters in series and $p = 9$, compared with one converter and $p = 36$.

connected in parallel at the converter side, and in series at the load side.

The system uses SPWM with triangular carriers shifted, and depending on the number of converters connected in the chain of bridges, the voltage waveform becomes more and more sinusoidal. Figure 12.62 shows a back-to-back system using a chain of 12 "H" converters connected as shown in Fig. 12.61b.

The ac voltage waveform obtained with the topology of Fig. 12.62 is displayed in Fig. 12.63. It can be observed that the voltage is formed by small steps that depend on the number of converters in the chain (12 in this case). The current is almost perfectly sinusoidal.

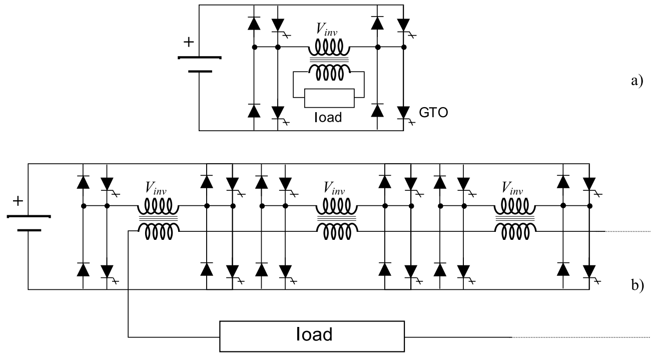


FIGURE 12.61 The "H" modulator: (a) one bridge; and (b) bridge connected in series at load side through isolation transformers.

Figure 12.64 shows the voltage waveforms for different number of converters connected in the bridge. It is clear that the larger the number of converters, the better the voltage. Another interesting result with this converter is that the ac voltages become modulated by both pulsewidth and amplitude (PWM and AM). This is because when the pulse modulation changes, the steps of the amplitude change. The maximum number of steps of the resultant voltage is equal to the number of converters. When the voltage decreases, some steps disappear, and then the amplitude modulation becomes a discrete function. Figure 12.65 shows the amplitude modulation of the voltage.

12.3.5.4 Machine Drives Applications

One of the most important applications of force-commutated rectifiers is in machine drives. Line-commutated thyristor converters have limited applications because they need excitation to extinguish the valves. This limitation do not allow the use of line-commutated converters in induction machine drives. On the other hand, with force-commutated converters four-quadrant operation is achievable. Figure 12.66 shows a typical frequency converter with a force-commutated rectifier-inverter link. The rectifier side controls the dc link, and the inverter side controls the machine. The machine can be a synchronous, brushless dc, or induction machine. The reversal of both speed and power are possible with this topology. At the rectifier side, the power factor can be controlled, and even with an inductive load such as an induction machine, the source can "see" the load as capacitive or resistive. Changing the frequency of the inverter controls the machine speed, and the torque is controlled through the stator currents and torque angle. The inverter will become a rectifier during regenerative braking, which is possible by making slip negative in an induction machine, or by making the torque angle negative in synchronous and brushless dc machines.

A variation of the drive of Fig. 12.66 is found in electric traction applications. Battery-powered vehicles use the inverter as a rectifier during regenerative braking, and sometimes the inverter is also used as a battery charger. In this case, the rectifier can be fed by a single-phase or by a three-phase system. Figure 12.67 shows a battery-powered electric bus system. This system uses the power inverter of the traction motor as a rectifier for two purposes: regenerative braking; and as a battery charger fed by a three-phase power source.

12.3.5.5 Variable Speed Power Generation

Power generation at 50 or 60 Hz requires constant speed machines. In addition, induction machines are not currently used in power plants because of magnetization problems. With the use of frequency-link force-commutated converters, variable-speed constant-frequency generation becomes possible,

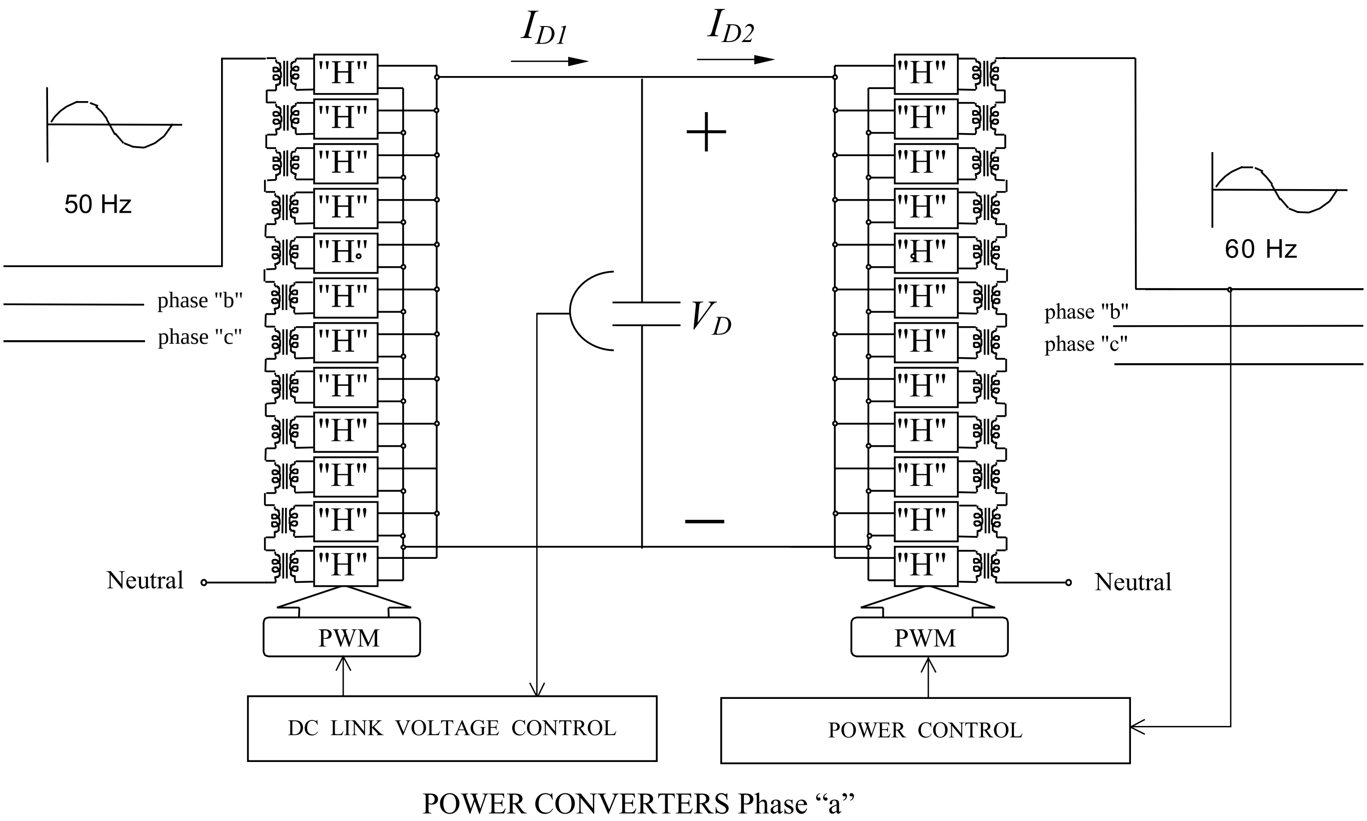

I_{D1}
I_{D2}
"H"
50 Hz
phase "b"
phase "c"
+
V_D
−
60 Hz
phase "b"
phase "c"
Neutral
Neutral
PWM
PWM
DC LINK VOLTAGE CONTROL
POWER CONTROL
POWER CONVERTERS Phase "a"

FIGURE 12.62 Frequency link with force-commutated converters and sinusoidal voltage modulation.

even with induction generators. The power plant in Fig. 12.68 shows a wind generator implemented with an induction machine, and a rectifier-inverter frequency link connected to the utility. The dc link voltage is kept constant with the converter located at the mains side. The converter connected at the machine side controls the slip of the generator and adjusts it according to the speed of wind or power requirements. The utility is not affected by the power factor of the generator, because the two converters keep the cos φ of the machine independent of the mains supply. The last one can even be adjusted to operate at leading power factor.

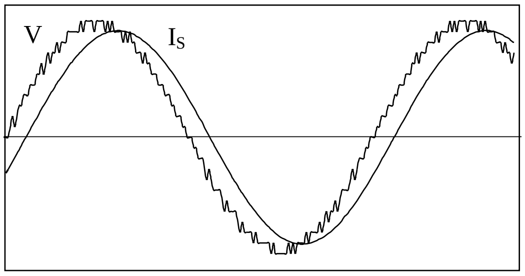


FIGURE 12.63 Voltage and current waveforms with 12 converters.

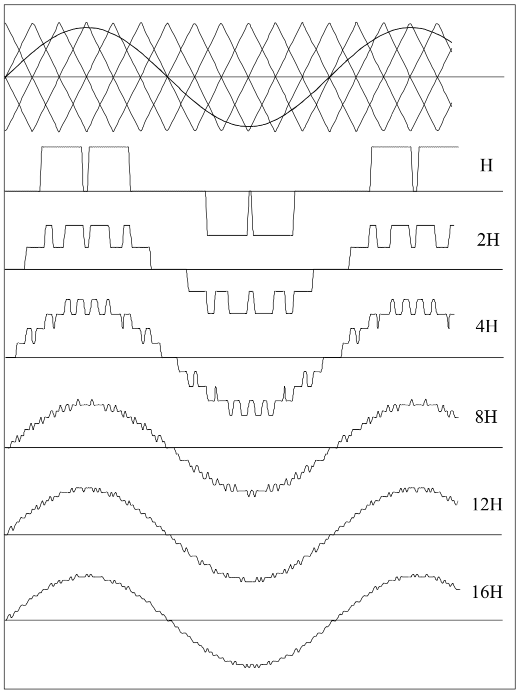


FIGURE 12.64 Voltage waveforms with different numbers of "H" bridges in series.

Variable-speed constant-frequency generation also can be used in either hydraulic or thermal plants. This allows for optimal adjustment of the efficiency-speed characteristics of the machines. In Japan, wound rotor induction generators working as variable speed synchronous machines are being used as constant frequency generators. They operate in hydraulic plants that are able to store water during low demand periods. A power converter is connected at the slip rings of the generator. The rotor is then fed with variable

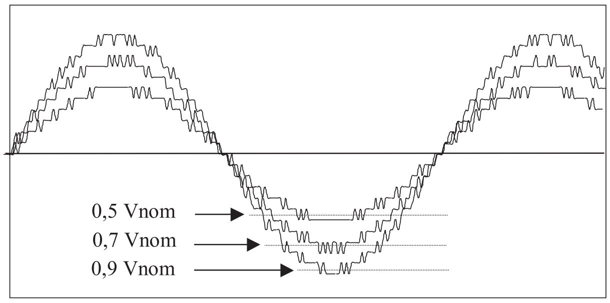


FIGURE 12.65 Amplitude modulation of the "H" bridges of Fig. 12.62.

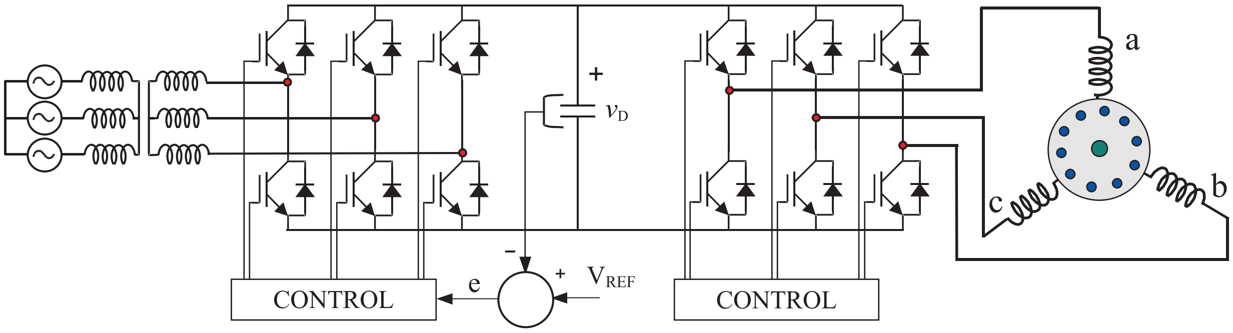

+
v_D
-
+
V_{REF}
e
CONTROL
CONTROL
a
b
c

FIGURE 12.66 Frequency converter with force-commutated converters.

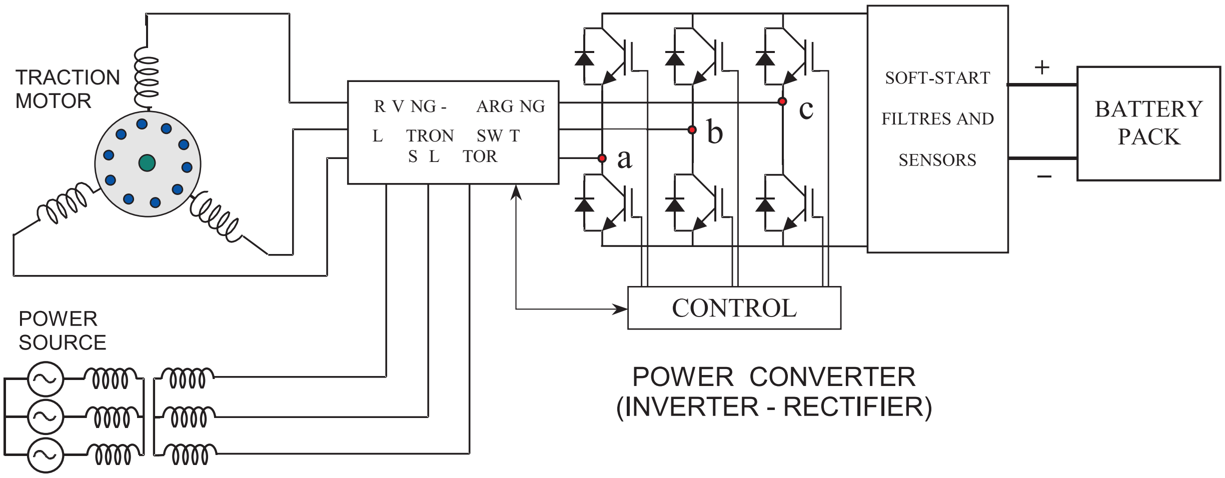

TRACTION MOTOR
DRIVING - CHARGING
ELECTRONIC SWITCH
SELECTOR
a
b
c
SOFT-START
FILTRES AND
SENSORS
+
–
BATTERY PACK
CONTROL
POWER SOURCE
POWER CONVERTER
(INVERTER - RECTIFIER)

FIGURE 12.67 Electric bus system with regenerative braking and battery charger.

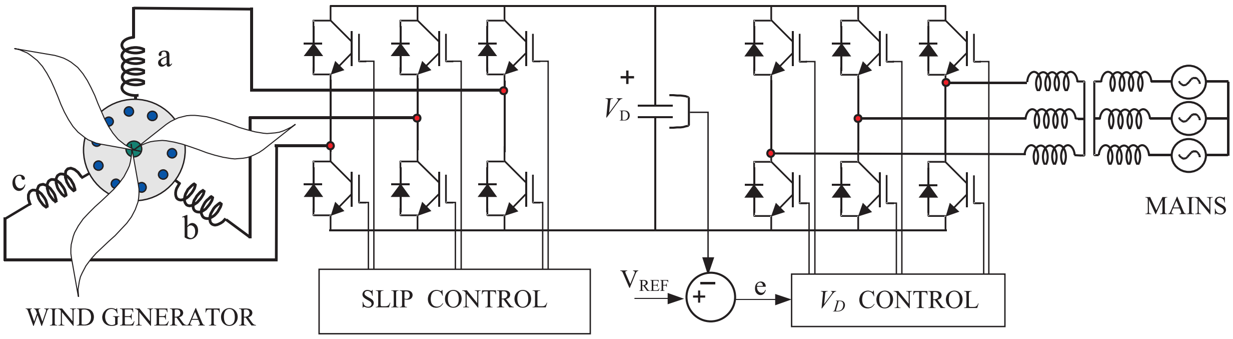

a
b
c
WIND GENERATOR
+
V_D
SLIP CONTROL
V_{REF}
+
–
e
V_D CONTROL
MAINS

FIGURE 12.68 Variable-speed constant-frequency wind generator.

frequency excitation. This allows the generator to generate at different speeds around the synchronous rotating flux.

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13

DC DC Converters

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13.1 Introduction

Modern electronic systems require high-quality, small, lightweight, reliable, and efficient power supplies. Linear power regulators, whose principle of operation is based on a voltage or current divider, are inefficient. This is because they are limited to output voltages smaller than the input voltage, and also their power density is low because they require low-frequency (50 or 60 Hz) line transformers and filters. Linear regulators can, however, provide a very high-quality output voltage. Their main area of application is at low power levels. Electronic devices in linear regulators operate in their active (linear) modes, but at higher power levels switching regulators are used. Switching regulators use power electronic semiconductor switches in *on* and *off* states. Because there is a small power loss in those states (low voltage across a switch in the *on* state, zero current through a switch in the *off* state), switching regulators can achieve high energy conversion efficiencies. Modern power electronic switches can operate at high frequencies. The higher the operating frequency, the smaller and lighter the transformers, filter inductors, and capacitors. In addition, the dynamic characteristics of converters improve with increasing operating frequencies. The bandwidth of a control loop is usually determined by the corner frequency of the output filter. Therefore, high operating frequencies allow for achieving a faster dynamic response to rapid changes in the load current and/or the input voltage.

High-frequency electronic power processors are used in dc-dc power conversion. The functions of dc-dc converters are:

- to convert a dc input voltage V_S into a dc output voltage V_O;
- to regulate the dc output voltage against load and line variations;
- to reduce the ac voltage ripple on the dc output voltage below the required level;
- to provide isolation between the input source and the load (isolation is not always required);
- to protect the supplied system and the input source from electromagnetic interference (EMI); and
- to satisfy various international and national safety standards.

The dc-dc converters can be divided into two main types: hard-switching pulsewidth modulated (PWM) converters, and resonant and soft-switching converters. This chapter deals with PWM dc-dc converters, which have been very popular for the last three decades, and that are widely used at all power levels. Topologies and properties of PWM converters are well

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understood and described in the literature. Advantages of PWM converters include low component count, high efficiency, constant frequency operation, relatively simple control and commercial availability of integrated circuit controllers, and ability to achieve high conversion ratios for both step-down and step-up application. A disadvantage of PWM dc-dc converters is that PWM rectangular voltage and current waveforms cause turn-on and turn-off losses in semiconductor devices, which limit practical operating frequencies to hundreds of kilohertz. Rectangular waveforms also inherently generate EMI.

This chapter begins with a section on dc choppers that are used primarily in dc drives. The output voltage of dc choppers is controlled by adjusting the *on* time of a switch, which in turn adjusts the width of a voltage pulse at the output. This is the so-called pulse width modulation (PWM) control. The dc choppers with additional filtering components form PWM dc-dc converters. Four basic dc-dc converter topologies are presented in Sections 13.3–13.6—buck, boost, buck-boost, and Čuk converters. Popular isolated versions of these converters are also discussed. The operation of converters is explained under ideal component and semiconductor device assumptions. Section 13.7 discusses the effects of nonidealities in PWM converters; Section 13.8 presents topologies for increased efficiency at low output voltages and for bidirectional power flow; Section 13.9 reviews control principles of PWM dc-dc converters, and describes two main control schemes, namely, voltage-mode control and current-mode control. A summary of application areas of PWM dc-dc converters is given in Section 13.10. Finally, a list of modern textbooks on power electronics is provided [1–8]. These books are excellent resources for deeper exploration of the area of dc-dc power conversion.

13.2 DC Choppers

A step-down dc chopper with a resistive load is shown in Fig. 13.1a. It is a series connection of a dc input voltage source V_S, controllable switch S, and load resistance R. In most cases, switch S has unidirectional voltage-blocking capabilities and unidirectional current-conduction capabilities. Power electronic switches are usually implemented with power MOSFETs, IGBTs, MCTs, power BJTs, or GTOs. If an antiparallel diode is used or embedded in a switch, the switch exhibits a bidirectional current conduction property. Figure 13.1b depicts waveforms in a step-down chopper. The switch is being operated with a duty ratio D defined as a ratio of the switch *on* time to the sum of the *on* and *off* times. For a constant frequency operation

$$D \equiv \frac{t_{\text{on}}}{t_{\text{on}} + t_{\text{off}}} = \frac{t_{\text{on}}}{T} \tag{13.1}$$

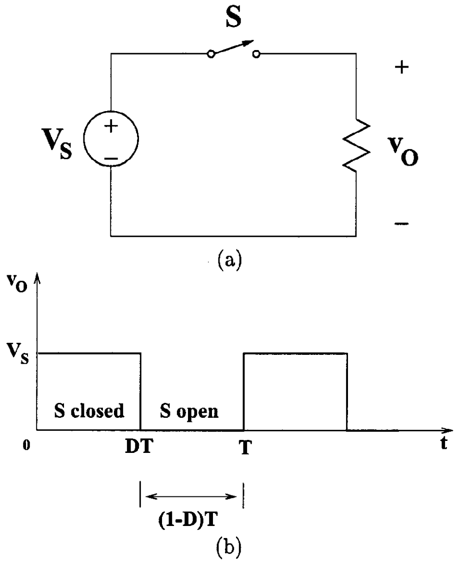


FIGURE 13.1 DC chopper with resistive load: (a) circuit diagram; (b) output voltage waveform.

where $T = 1/f$ is the period of the switching frequency f. The average value of the output voltage is

$$V_O = DV_S \tag{13.2}$$

and can be regulated by adjusting the duty ratio D. The average output voltage is always smaller than the input voltage, hence the name of the converter.

The dc step-down choppers are commonly used in dc drives. In such a case, the load is represented as a series combination of inductance L, resistance R, and back-emf E as shown in Fig. 13.2a. To provide a path for a continuous inductor current flow when the switch is in the *off* state, an antiparallel diode D must be connected across the load. Because the chopper of Fig. 13.2a provides a positive voltage and a positive current to the load, it is called a first-quadrant chopper. The load voltage and current are graphed in Fig. 13.2b under assumptions that the load current never reaches zero and the load time constant $\tau = L/R$ is much greater than the period T. Average values of the output voltage and current can be adjusted by changing the duty ratio D.

The dc choppers can also provide peak output voltages higher than the input voltage. Such a step-up configuration is presented in Fig. 13.3. It consists of dc input source V_S, inductor L connected in series with the source, switch S connecting the inductor to ground, and a series combination of diode D and load. If the switch operates with a duty ratio D, the output voltage is a series of pulses of duration $(1 - D)T$ and amplitude $V_S/(1 - D)$. Therefore, neglecting losses, the average value of the output voltage is V_S. To obtain an average value of the output voltage greater than V_S, a capacitor must be connected in parallel with the load. This results in a topology of a boost dc-dc converter that is described in Section 13.4.

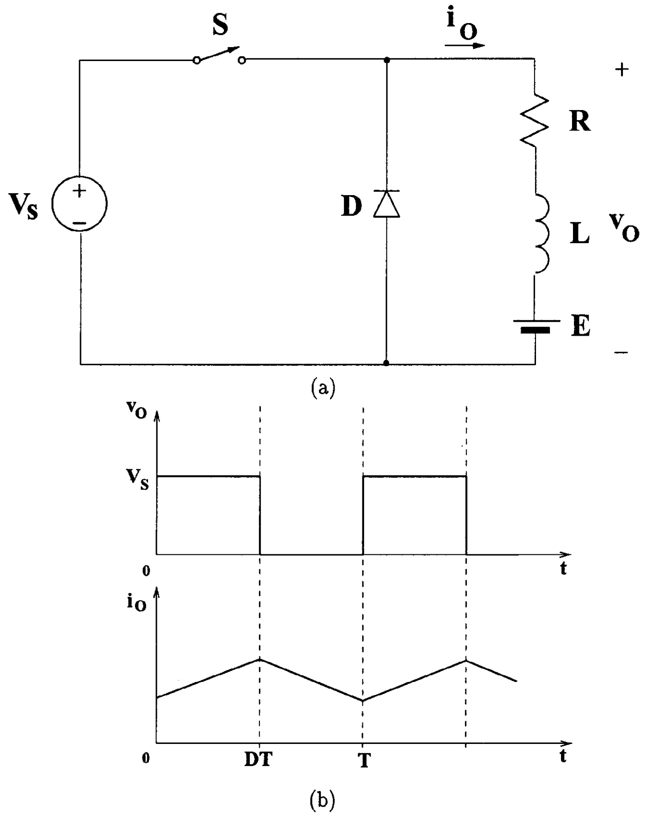


FIGURE 13.2 DC chopper with *RLE* load: (a) circuit diagram; (b) waveforms.

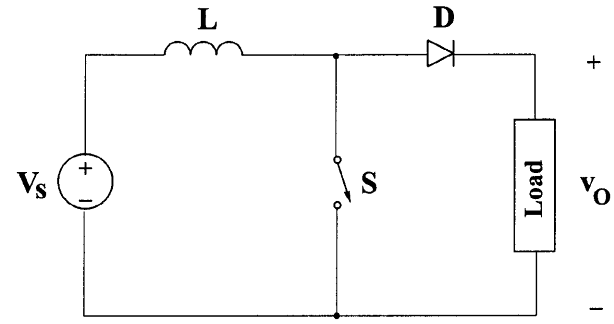


FIGURE 13.3 The dc step-up chopper.

13.3 Step-Down Buck Converter

13.3.1 Basic Converter

The step-down dc-dc converter, commonly known as a buck converter, is shown in Fig. 13.4a. It consists of dc input voltage source V_S, controlled switch S, diode D, filter inductor L, filter capacitor C, and load resistance R. Typical waveforms in the converter are shown in Fig. 13.4b under the assumption that the inductor current is always positive. The state of the converter in which the inductor current is never zero for any period of time is called the *continuous conduction mode* (CCM). It can be seen from the circuit that when the switch S is commanded to the *on* state, the diode D is reverse-biased. When the switch S is *off*, the diode conducts to support an uninterrupted current in the inductor.

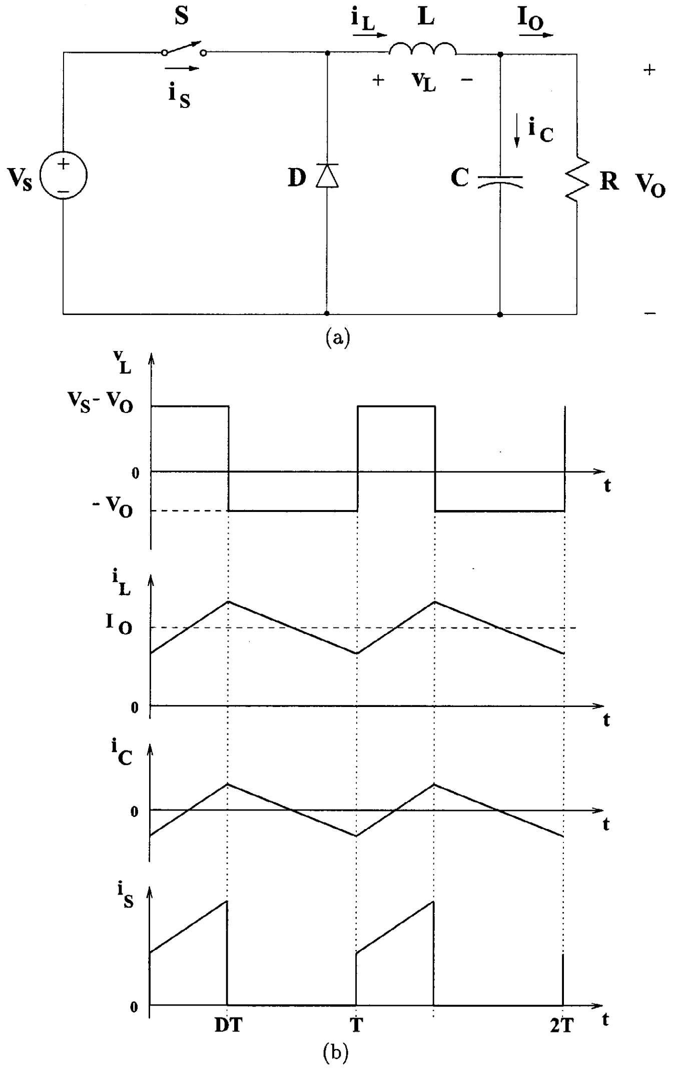


FIGURE 13.4 Buck converter: (a) circuit diagram; (b) waveforms.

The relationship among the input voltage, output voltage, and the switch duty ratio D can be derived, for instance, from the inductor voltage v_L waveform (see Fig. 13.4b). According to Faraday's law, the inductor volt-second product over a period of steady-state operation is zero. For the buck converter

$$(V_S - V_O)DT = -V_O(1 - D)T \tag{13.3}$$

Hence, the dc voltage transfer function, defined as the ratio of the output voltage to the input voltage, is

$$M_V \equiv \frac{V_O}{V_S} = D \tag{13.4}$$

It can be seen from Eq. (13.4) that the output voltage is always smaller that the input voltage.

The dc-dc converters can operate in two distinct modes with respect to the inductor current i_L. Figure 13.4b depicts the CCM in which the inductor current is always greater than zero. When the average value of the output current is low (high R) and/or the switching frequency f is low, the converter may enter the *discontinuous conduction mode* (DCM). In the DCM, the inductor current is zero during a portion of the switching period. The CCM is preferred for high efficiency and good utilization of semiconductor switches and passive components. The DCM may be used in applications with special control requirements because the dynamic order of the converter is reduced (the energy stored in the inductor is zero at the beginning and at the end of each switching period). It is uncommon to mix these two operating modes because of different control algorithms. For the buck converter, the value of the filter inductance that determines the boundary between CCM and DCM is given by

$$L_b = \frac{(1-D)R}{2f} \tag{13.5}$$

For typical values of $D = 0.5$, $R = 10\,\Omega$, and $f = 100$ kHz, the boundary is $L_b = 25\ \mu\text{H}$. For $L > L_b$, the converter operates in the CCM.

The filter inductor current i_L in the CCM consists of a dc component I_O with a superimposed triangular ac component. Almost all of this ac component flows through the filter capacitor as a current i_c. Current i_c causes a small voltage ripple across the dc output voltage V_O. To limit the peak-to-peak value of the ripple voltage below a certain value V_r, the filter capacitance C must be greater than

$$C_{\min} = \frac{(1-D)V_O}{8V_r L f^2} \tag{13.6}$$

At $D = 0.5$, $V_r/V_O = 1\%$, $L = 25\ \mu\text{H}$, and $f = 100$ kHz, the minimum capacitance is $C_{\min} = 25\ \mu\text{F}$.

Equations (13.5) and (13.6) are the key design equations for the buck converter. The input and output dc voltages (hence, the duty ratio D), and the range of load resistances R are usually determined by preliminary specifications. The designer needs to determine values of passive components L and C, and of the switching frequency f. The value of the filter inductor L is calculated from the CCM/DCM condition using Eq. (13.5). The value of the filter capacitor C is obtained from the voltage ripple condition Eq. (13.6). For the compactness and low conduction losses of a converter, it is desirable to use small passive components. Equations (13.5) and (13.6) show that it can be accomplished by using a high switching frequency f. The switching frequency is limited, however, by the type of semiconductor switches used and by switching losses. It should also be noted that values of L and C may be altered by the effects of parasitic components in the converter, especially by the equivalent series resistance of the capacitor. Parasitic components in dc-dc converters are discussed in Section 13.7.

13.3.2 Transformer Versions of Buck Converter

In many dc power supplies, a galvanic isolation between the dc or ac input and the dc output is required for safety and reliability. An economical means of achieving such an isolation is to employ a transformer version of a dc-dc converter. High-frequency transformers are of a small size and low weight and provide high efficiency. Their turns ratio can be used additionally to adjust the output voltage level. Among buck-derived dc-dc converters, the most popular are the forward converter, the push-pull converter, the half-bridge converter, and the full-bridge converter.

13.3.2.1 Forward Converter

The circuit diagram of a forward converter is depicted in Fig. 13.5. When the switch S is *on*, diode D_1 conducts and diode D_2 is *off*. The energy is transferred from the input, through the transformer, to the output filter. When the switch is *off*, the state of diodes D_1 and D_2 is reversed. The dc voltage transfer function of the forward converter is

$$M_V = \frac{D}{n} \tag{13.7}$$

where $n = N_1/N_2$.

In the forward converter, the energy-transfer current flows through the transformer in one direction. Hence, an additional winding with diode D_3 is needed to bring the magnetizing current of the transformer to zero, which prevents transformer saturation. The turns ratio N_1/N_3 should be selected in such a way that the magnetizing current decreases to zero during a fraction of the time interval when the switch is *off*.

Equations (13.5) and (13.6) can be used to design the filter components. The forward converter is very popular for low-power applications. For medium-power levels, converters with bidirectional transformer excitation (push-pull, half-bridge, and full-bridge) are preferred due to better utilization of magnetic components.

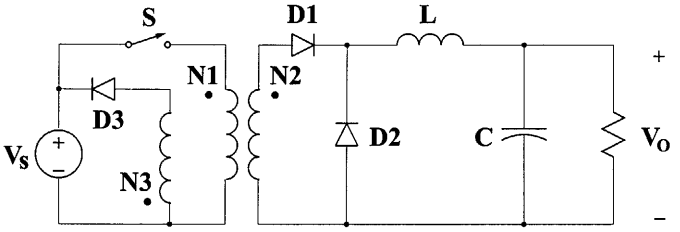


FIGURE 13.5 Forward converter.

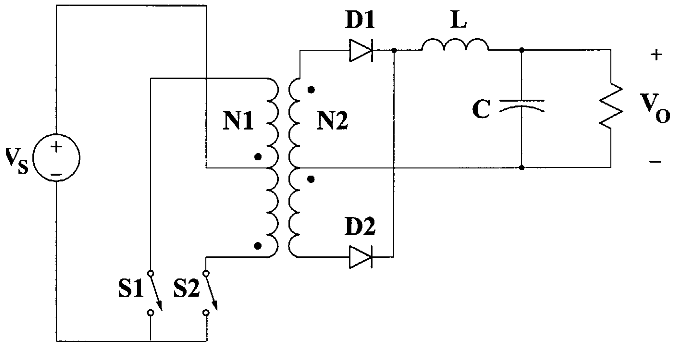


FIGURE 13.6 Push-pull converter.

13.3.2.2 Push-Pull Converter

The PWM dc-dc push-pull converter is shown in Fig. 13.6. The switches S_1 and S_2 operate shifted in phase by $T/2$ with the same duty ratio D, however, the duty ratio must be smaller than 0.5. When switch S_1 is *on*, diode D_1 conducts and diode D_2 is *off*; the diode states are reversed when switch S_2 is *on*. When both controllable switches are *off*, the diodes are *on* and share equally the filter inductor current. The dc voltage transfer function of the push-pull converter is

$$M_V = \frac{2D}{n} \tag{13.8}$$

where $n = N_1/N_2$. The boundary value of the filter inductor is

$$L_b = \frac{(1-2D)R}{4f} \tag{13.9}$$

The filter capacitor can be obtained from

$$C_{\min} = \frac{(1-2D)V_O}{32V_rLf^2} \tag{13.10}$$

13.3.2.3 alf-Bridge Converter

Figure 13.7 shows the dc-dc half-bridge converter. The operation of the PWM half-bridge converter is similar to that of the push-pull converter. In comparison to the push-pull converter, the primary switch of the transformer is simplified at the expense of two voltage-sharing input capacitors. The half-bridge converter dc voltage transfer function is

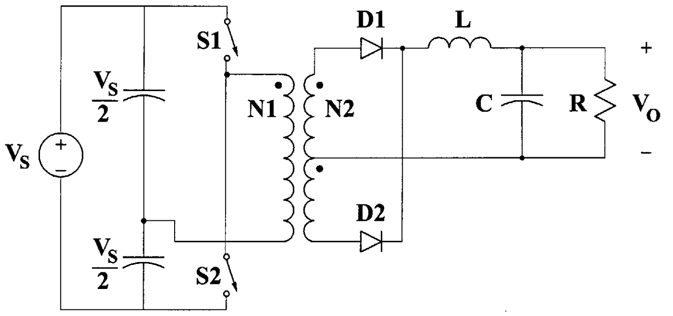


FIGURE 13.7 Half-bridge converter.

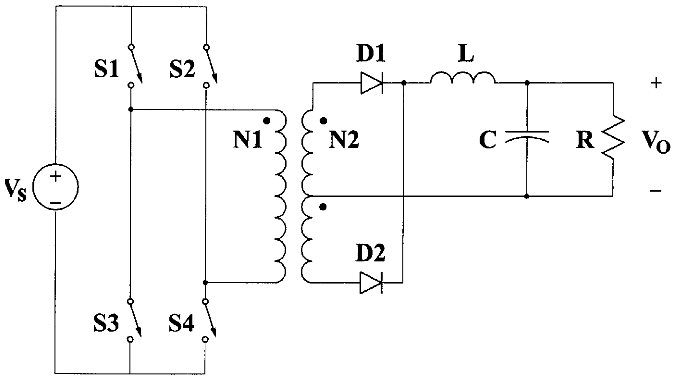


FIGURE 13.8 Full-bridge converter.

$$M_V \equiv \frac{V_D}{V_S} = \frac{D}{n} \tag{13.11}$$

where $D \leq 0.5$. Equations (13.9) and (13.10) apply to the filter components.

13.3.2.4 ull-Bridge Converter

Comparing the PWM dc-dc full-bridge converter of Fig. 13.8 to the half-bridge converter, it can be seen that the input capacitors have been replaced by two controllable switches that are operated in pairs. When S_1 and S_4 are *on*, voltage V_S is applied to the primary switch of the transformer and diode D_1 conducts. With S_2 and S_3 *on*, there is voltage $-V_S$ across the transformer primary switch and diode D_2 is *on*. With all controllable switches *off*, both diodes conduct in the same way as in the push-pull and half-bridge converters. The dc voltage transfer function of the full-bridge converter is

$$M_V \equiv \frac{V_O}{V_S} = \frac{2D}{n} \tag{13.12}$$

where $D \leq 0.5$. The values of filter components can be obtained from Eqs. (13.9) and (13.10).

It should be stressed that the full-bridge topology is a very versatile one. With different control algorithms, it is very popular in dc-ac conversion (square-wave and PWM single-phase inverters), and it is also used in four-quadrant dc drives.

13.4 Step-Up Boost Converter

Figure 13.9a depicts a step-up or a PWM boost converter. It consists of dc input voltage source V_S, boost inductor L, controlled switch S, diode D, filter capacitor C, and load resistance R. The converter waveforms in the CCM are

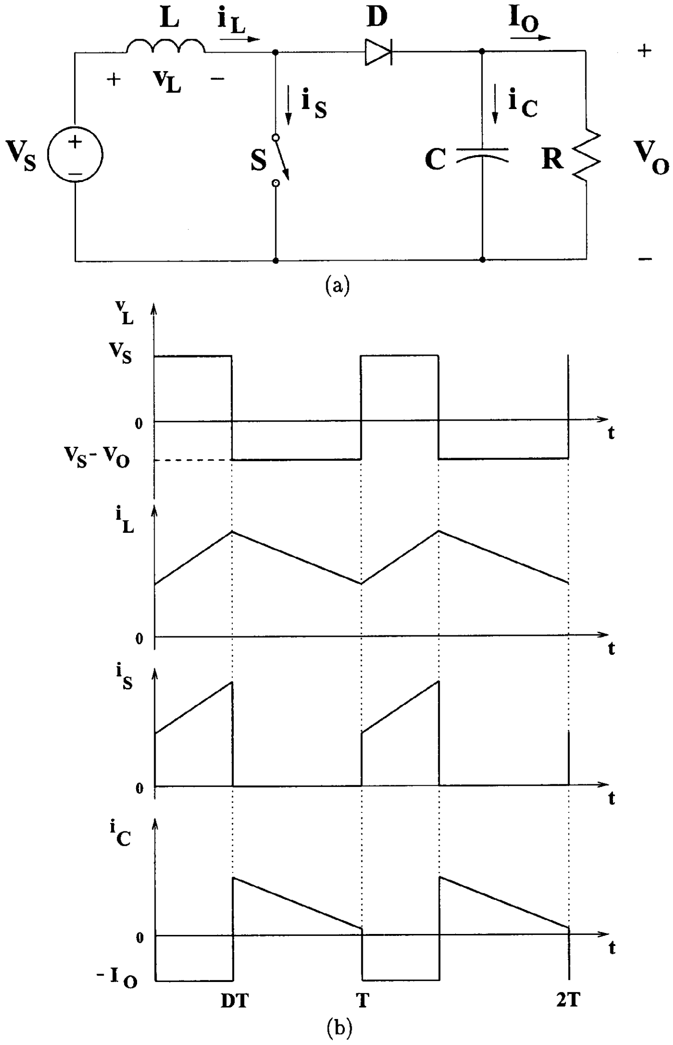


FIGURE 13.9 Boost converter: (a) circuit diagram; (b) waveforms.

presented in Fig. 13.9b. When the switch S is in the *on* state, the current in the boost inductor increases linearly and the diode D is *off* at that time. When the switch S is turned *off*, the energy stored in the inductor is released through the diode to the output RC circuit.

Using Faraday's law for the boost inductor

$$V_S DT = (V_O - V_S)(1 - D)T \tag{13.13}$$

from which the dc voltage transfer function turns out to be

$$M_V \equiv \frac{V_O}{V_S} = \frac{1}{1 - D} \tag{13.14}$$

As the name of the converter suggests, the output voltage is always greater than the input voltage.

The boost converter operates in the CCM for $L > L_b$ where

$$L_b = \frac{(1 - D)^2 DR}{2f} \tag{13.15}$$

For $D = 0.5$, $R = 10\ \Omega$, and $f = 100$ kHz, the boundary value of the inductance is $L_b = 6.25\ \mu$H.

As shown in Fig. 13.9b, the current supplied to the output RC circuit is discontinuous. Thus, a larger filter capacitor is required in comparison to that in the buck-derived converters to limit the output voltage ripple. The filter capacitor must provide the output dc current to the load when the diode D is *off*. The minimum value of the filter capacitance that results in the voltage ripple V_r is given by

$$C_{\min} = \frac{DV_O}{V_r Rf} \tag{13.16}$$

At $D = 0.5$, $V_r/V_O = 1\%$, $R = 10\ \Omega$, and $f = 100$ kHz, the minimum capacitance for the boost converter is $C_{\min} = 50\ \mu$F.

The boost converter does not have a popular transformer (isolated) version.

13.5 Buck-Boost Converter

13.5.1 Basic Converter

A nonisolated (transformerless) topology of the buck-boost converter is shown in Fig. 13.10a. The converter consists of dc input voltage source V_S, controlled switch S, inductor L, diode D, filter capacitor C, and load resistance R. With the switch *on*, the inductor current increases while the diode is maintained *off*. When the switch is turned *off*, the diode provides a path for the inductor current. Note the polarity of the diode that results in its current being *drawn from* the output.

The buck-boost converter waveforms are depicted in Fig. 13.10b. The condition of a zero volt-second product for the inductor in steady state yields

$$V_S DT = -V_O(1 - D)T \tag{13.17}$$

Hence, the dc voltage transfer function of the buck-boost converter is

$$M_V \equiv \frac{V_O}{V_S} = -\frac{D}{1 - D} \tag{13.18}$$

The output voltage V_O is negative with respect to the ground. Its magnitude can be either greater or smaller (equal at $D = 0.5$) than the input voltage as the name of the converter implies.

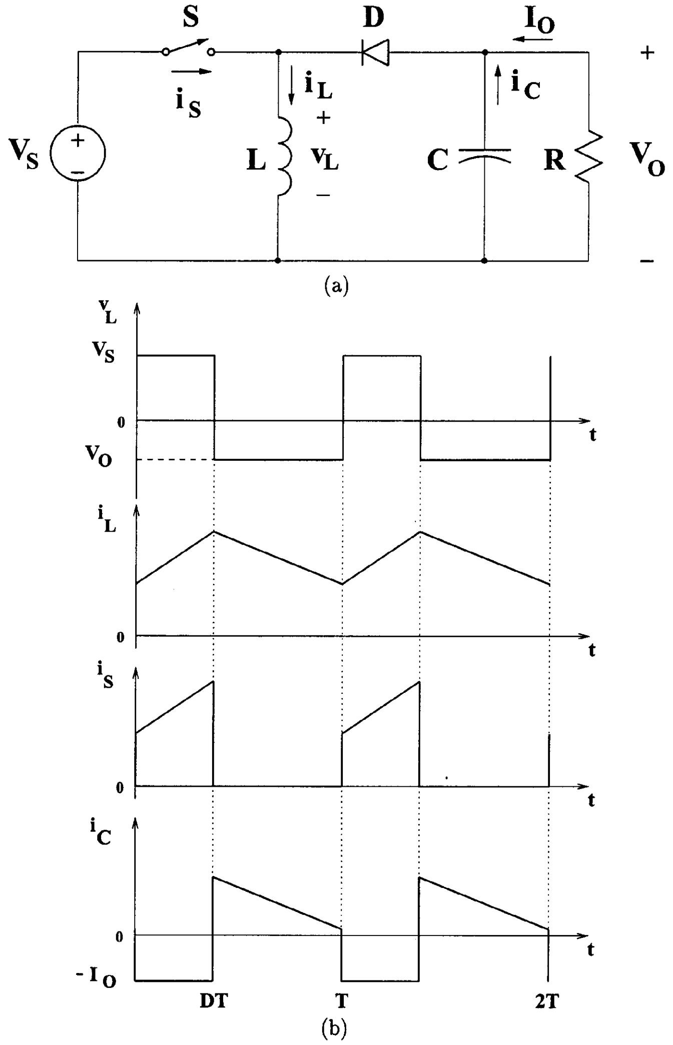


FIGURE 13.10 Buck-boost converter: (a) circuit diagram; (b) waveforms.

The value of the inductor that determines the boundary between the CCM and DCM is

$$L_b = \frac{(1 - D)^2 R}{2f} \tag{13.19}$$

The structure of the output part of the converter is similar to that of the boost converter (reversed polarities are the only difference). Thus, the value of the filter capacitor can be obtained from Eq. (13.16).

13.5.2 lyback Converter

A PWM flyback converter is a very practical isolated version of the buck-boost converter. The circuit of the flyback converter is presented in Fig. 13.11a. The inductor of the buck-boost converter has been replaced by a flyback transformer. The input dc source V_S and switch S are connected in series with the transformer primary. The diode D and the RC output circuit are connected in series with the secondary of the flyback transformer. Figure 13.11b shows the converter with a simple flyback transformer model that includes a magnetizing inductance L_m and an ideal transformer with a turns ratio $n = N_1/N_2$. The flyback transformer leakage inductances and losses are neglected in the model. It should be noted that leakage inductances, although not important from the viewpoint of the principle of operation, affect adversely switch and diode transitions. Therefore, snubbers are usually required in flyback converters Refer to Fig. 13.11b for the converter operation.

When the switch S is *on*, the current in the magnetizing inductance increases linearly, the diode D is *off* and there is no current in the ideal transformer windings. When the switch is turned *off*, the magnetizing inductance current is diverted into the ideal transformer, the diode turns *on*, and the transformed magnetizing inductance current is supplied to the RC load. The dc voltage transfer function of the flyback converter is

$$M_V \equiv \frac{V_O}{V_S} = \frac{D}{n(1 - D)} \tag{13.20}$$

It differs from the buck-boost converter voltage transfer function by the turns ratio factor n. A positive sign has been obtained by an appropriate coupling of the transformer windings.

Unlike in transformer buck-derived converters, the magnetizing inductance L_m of the flyback transformer is an important design parameter. The value of the magnetizing inductance that determines the boundary between the CCM and DCM is given by

$$L_{mb} = \frac{n^2(1 - D)^2 R}{2f} \tag{13.21}$$

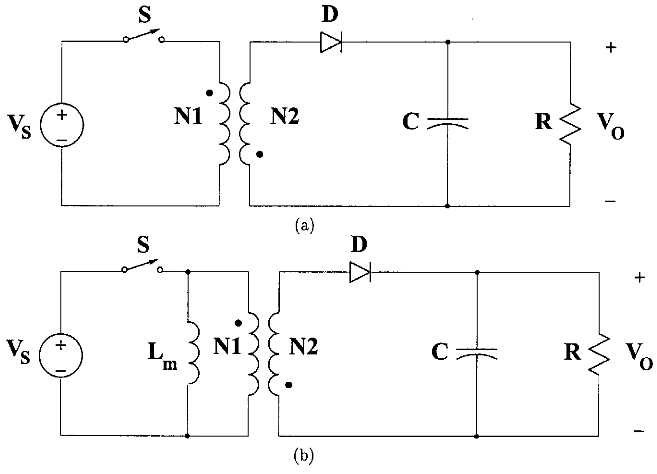
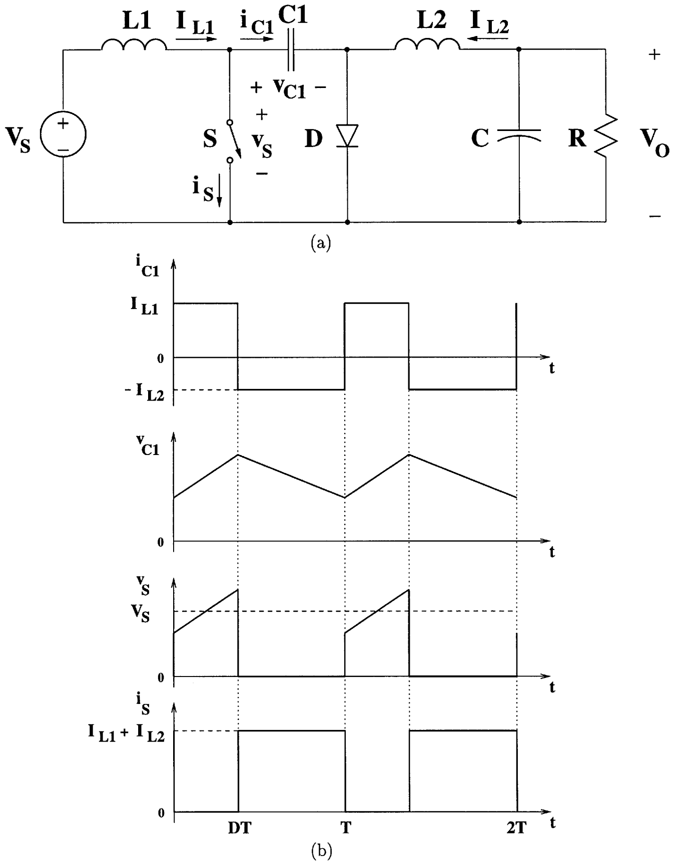


FIGURE 13.11 Flyback conveter: (a) circuit diagram; (b) circuit with a transformere model showing the magnetizing inductance L_m.

The value of the filter capacitance can be calculated using Eq. (13.16).

13.6 Cuk Converter

The circuit of the C̀uk converter is shown in Fig. 13.12a. It consists of dc input voltage source V_S, input inductor L_1, controllable switch S, energy transfer capacitor C_1, diode D, filter inductor L_2, filter capacitor C, and load resistance R. An important advantage of this topology is a continuous current at both the input and the output of the converter. Disadvantages of the C̀uk converter are a high number of reactive components and high current stresses on the switch, the diode, and the capacitor C_1. The main waveforms in the converter are presented in Fig. 13.12b. When the switch is *on*, the diode is *off* and the capacitor C_1 is discharged by the inductor L_2 current. With the switch in the *off* state, the diode conducts currents of the inductors L_1 and L_2, whereas capacitor C_1 is charged by the inductor L_1 current.



(b)

FIGURE 13.12 C̀uk converter: (a) circuit diagram; (b) waveforms.

To obtain the dc voltage transfer function of the converter, we shall use the principle that the average current through a capacitor is zero for steady-state operation. Let us assume that inductors L_1 and L_2 are large enough that their ripple current can be neglected. Capacitor C_1 is in steady state if

$$I_{L2}DT = I_{L1}(1-D)T \tag{13.22}$$

For a lossless converter

$$P_S = V_S I_{L1} = -V_O I_{L2} = P_O \tag{13.23}$$

Combining these two equations, the dc voltage transfer function of the C̀uk converter is

$$M_V \equiv \frac{V_O}{V_S} = -\frac{D}{1-D} \tag{13.24}$$

This voltage transfer function is the same as that for the buck-boost converter.

The boundaries between the CCM and DCM are determined by

$$L_{b1} = \frac{(1-D)R}{2Df} \tag{13.25}$$

for L_1 and

$$L_{b2} = \frac{(1-D)R}{2f} \tag{13.26}$$

for L_2.

The output part of the C̀uk converter is similar to that of the buck converter. Hence, the expression for the filter capacitor C is

$$C_{\min} = \frac{(1-D)V_O}{8V_r L_2 f^2} \tag{13.27}$$

The peak-to-peak ripple voltage in the capacitor C_1 can be estimated as

$$V_{r1} = \frac{DV_O}{C_1 R_f} \tag{13.28}$$

A transformer (isolated) version of the C̀uk converter can be obtained by splitting capacitor C_1 and inserting a high-frequency transformer between the split capacitors.

13.7 Effects of Parasitics

The analysis of converters in Sections 13.2 through 13.6 has been performed under ideal switch, diode, and passive component assumptions. Nonidealities or parasitics of practical devices and components may, however, greatly affect some performance parameters of dc-dc converters. In this section, the effects of parasitics on output voltage ripple, efficiency, and voltage transfer function of converters will be illustrated.

A more realistic model of a capacitor than simply a capacitance *C*, consists of a series connection of capacitance *C* and resistance r_C. The resistance r_C is called an equivalent series resistance (ESR) of the capacitor and is due to losses in the dielectric and physical resistance of leads and connections. Recall Eq. (13.6) that provided a value of the filter capacitance in a buck converter that limits the peak-to-peak output voltage ripple to V_r. Equation (13.6) was derived under an assumption that the entire triangular ac component of the inductor current flows through a capacitance *C*. It is, however, closer to reality to maintain that this triangular component flows through a series connection of capacitance *C* and resistance r_C.

The peak-to-peak ripple voltage is independent of the voltage across the filter capacitor and is determined only by the ripple voltage of the ESR if the following condition is satisfied:

$$C \geq C_{\min} = \max\left\{\frac{1 - D_{\min}}{2r_C f}, \frac{D_{\max}}{2r_C f}\right\} \tag{13.29}$$

If condition Eq. (13.29) is satisfied, the peak-to-peak ripple voltage of the buck and forward converters is

$$V_r = r_C \Delta i_{L\max} = \frac{r_C V_O (1 - D_{\min})}{fL} \tag{13.30}$$

For push-pull, half-bridge, and full-bridge converters,

$$C \geq C_{\min} = \max\left\{\frac{0.5 - D_{\min}}{2r_C f}, \frac{D_{\max}}{2r_C f}\right\} \tag{13.31}$$

where $D_{\max} \leq 0.5$. If Eq. (13.31) is met, the peak-to-peak ripple voltage V_r of these converters is given by

$$V_r = r_C \Delta i_{L\max} = \frac{r_C V_O (0.5 - D_{\min})}{fL} \tag{13.32}$$

Waveforms of voltage acroos the ESR v_{rC}, voltage across the capacitance v_C, and total ripple voltage v_r are depicted in Fig. 13.13 for three values of the filter capacitances. For the case of the top graph in Fig. 13.13, the peak-to-peak value of v_r is higher than the peak-to-peak value of v_{rC} because $C < C_{\min}$. The middle and bottom graphs in Fig. 13.13 show the waveforms for $C = C_{\min}$ and $C > C_{\min}$, respectively. For both these cases, the peak-to-peak voltages of v_r and v_{rC} are equal to each other.

Note that when the resistance r_C sets the ripple voltage V_r, the minimum value of inductance *L* is determined either by the boundary between the CCM and DCM according to Eq. (13.5) (buck and forward converters) or Eq. (13.9) (push-pull, half-bridge, and full-bridge converters), or by the voltage ripple condition Eq. (13.30) or (13.32).

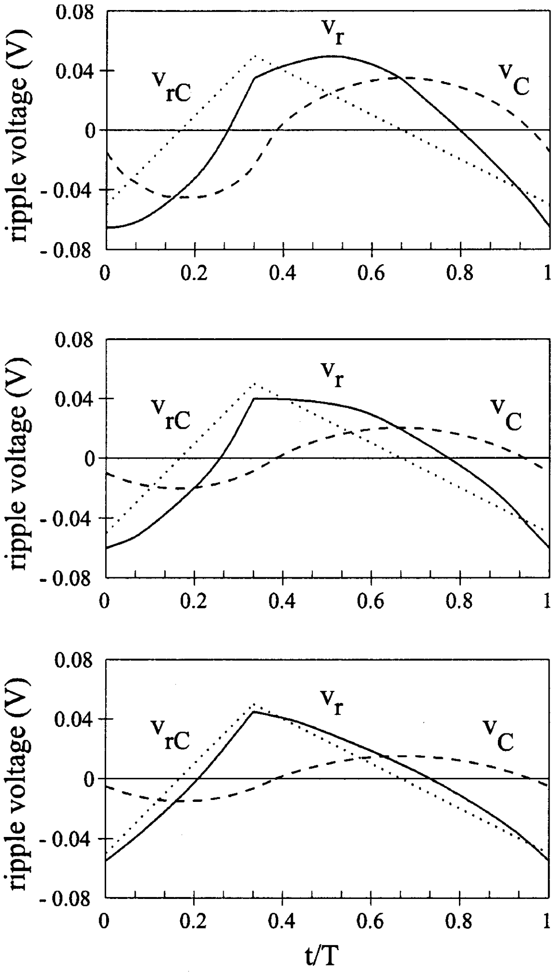


FIGURE 13.13 Voltage ripple waveforms v_rC, v_C, and v_r for a buck converter at $V_O = 12$ V, $f = 100$ kHz, $L = 40$ μH, $r_C = 0.05$ Ω and various values of *C*: $C = 33$ μF (top graph); $C = C_{min} = 65$ μF (middle graph); and $C = 100$ μF (bottom graph).

In buck-boost and boost converters, the peak-to-peak capacitor current I_{Cpp} is equal to the peak-to-peak diode current and is given by

$$I_{Cpp} = \frac{I_O}{1 - D} \tag{13.33}$$

under the condition that the inductor current ripple is much lower than the average value of the inductor current. The peak-to-peak voltage across the ESR is

$$V_{rc} = r_C I_{Cpp} = \frac{r_C I_O}{1 - D} \tag{13.34}$$

Assuming that the total ripple voltage V_r is approximately equal to the sum of the ripple voltages across the ESR and the capacitance, the maximum value of the peak-to-peak ripple voltage across the capacitance is

$$V_{C\max} \approx V_r - V_{rc} \tag{13.35}$$

Finally, by analogy to Eq. (13.16), when the ESR of the filter capacitor is taken into account in the boost-type output filter, the filter capacitance should be greater than

$$C_{\min} = \frac{DV_O}{V_{C\max} Rf} \tag{13.36}$$

Parasitic resistances, capacitances, and voltage sources also affect the energy conversion efficiency of dc-dc converters. The efficiency η is defined as a ratio of output power to the input power

$$\eta \equiv \frac{P_O}{P_S} = \frac{V_O I_O}{V_S I_S} \tag{13.37}$$

Thus as efficiencies are usually specified in percent, let us consider the boost converter as an example. Under the low ripple assumption, the boost converter efficiency can be estimated as

$$\eta = \frac{R(1-D)^2}{\begin{array}{c} R(1-D)^2(1 + V_D/V_O + fC_oR) \\ + r_L + Dr_S + (1-D)r_D + D(1-D)r_C \end{array}} \tag{13.38}$$

where V_D is the forward conduction voltage drop of the diode, C_o is the output capacitance of the switch, r_L is the ESR of the inductor, and r_D is the forward *on* resistance of the diode. The term fC_oR in Eq. (13.38) represents switching losses in the converter; other terms account for conduction losses. Losses in a dc-dc converter contribute also to a decrease in the dc voltage transfer function. The nonideal dc voltage transfer function M_{Vn} is a product of the ideal one and the efficiency

$$M_{Vn} = \eta M_V \tag{13.39}$$

Sample graphs for the boost converter that correspond to Eqs. (13.38) and (13.39) are presented in Fig. 13.14.

13.8 Synchronous and Bidirectional Converters

It can be observed in Eq. (13.38) that the forward voltage of a diode V_D contributes to a decrease in efficiency. This contribution is especially significant in low-output voltage power supplies, for example, 3.3-V power supplies for microprocessors or power supplies for portable telecommunication equipment. Even with a Schottky diode, which has V_D in the range of 0.4 V, the power loss in the diode can easily exceed 10 of the total power delivered to the load. To reduce conduction losses in the diode, a low on-resistance switch can be added in parallel as shown in Fig. 13.15 for a buck converter. The input switch and the switch parallel to the diode must be turned on and off alternately. The arrangement of Fig. 13.15 is called a synchronous converter or a synchronous rectifier. Modern low-voltage MOSFETs have *on* resistances of only several milliohms. Hence, a synchronous converter may exhibit higher efficiency than a conventional one at output currents as large as tens of amperes. The efficiency is increased at the expense of a more complicated driving circuitry for the switches. In particular, a special care must be exercised to avoid having both switches *on* at the same time as this would

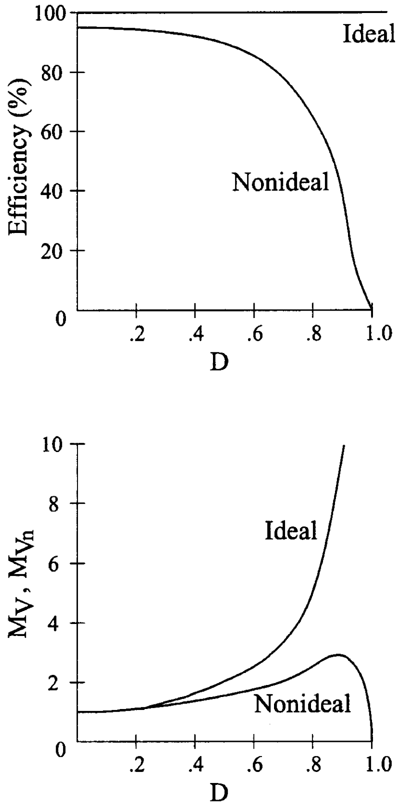


FIGURE 13.14 Effects of parasitics on characteristics of a boost converter: efficiency (top graph) and dc voltage transfer function (bottom graph).

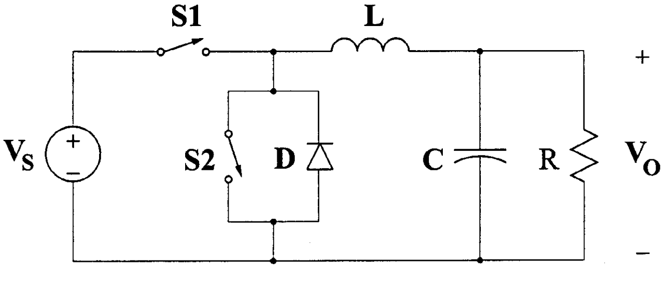


FIGURE 13.15 Synchronous buck converter.

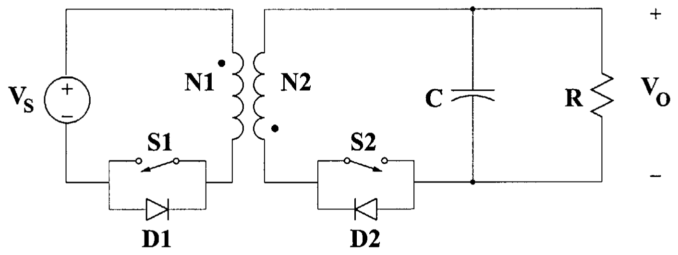


FIGURE 13.16 Bidirectional flyback converter.

short the input voltage source. As power semiconductor devices usually have longer turn-off times than turn-on times, a dead time (sometimes called a blanking time) must be introduced in PWM driving signals.

The parallel combination of a controllable switch and a diode is also used in converters, which allow for a current flow in both directions from the input source to the load and from the load back to the input source. Such converters are called bidirectional power-flow or simply bidirectional converters. As an example, a flyback bidirectional converter is shown in Fig. 13.16. It contains unipolar voltage and bidirectional current switch-diode combinations at both the primary switch and the secondary switch of the flyback transformer. When the primary switch and secondary diode operate, the current flows from the input source to the load. The converter current can also flow from the output to the input through the secondary switch and primary diode. Bidirectional arrangements can be made for both buck and boost converters. A bidirectional buck converter operates as a boost converter when the current flow is from the output to the input. A bidirectional boost converter operates as a buck converter with a reversed current flow. If for any reason (for instance, to avoid the DCM) the controllable switches are driven at the same time, they must be driven alternately with a sufficient dead time.

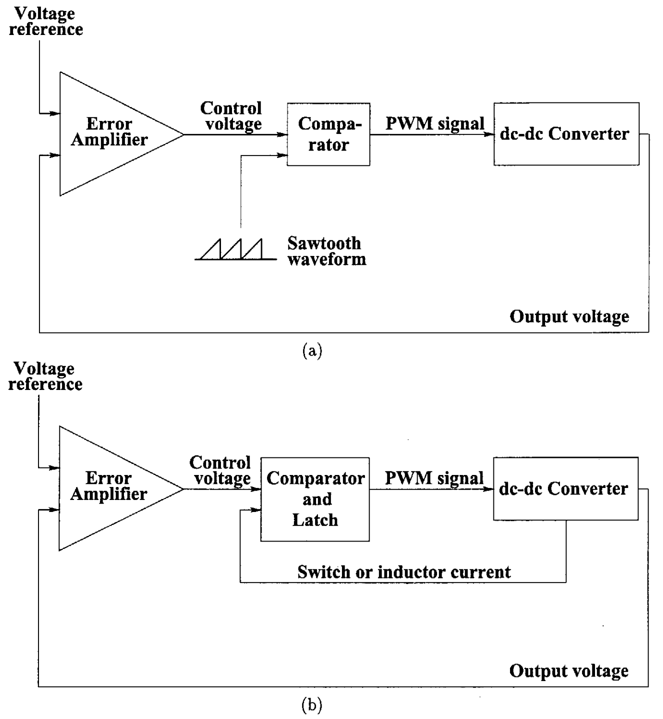
13. Control Principles

A dc-dc converter must provide a regulated dc output voltage under varying load and input voltage conditions. The converter component values are also changing with time, temperature, pressure, and so forth. Hence, the control of the output voltage should be performed in a closed-loop manner using principles of negative feedback. The two most common closed-loop control methods for PWM dc-dc converters, namely, the voltage-mode control and the current-mode control, are presented schematically in Fig. 13.17.

In the voltage-mode control scheme shown in Fig. 13.17a, the converter output voltage is sensed and subtracted from an external reference voltage in an error amplifier. The error amplifier produces a control voltage that is compared to a constant-amplitude sawtooth waveform. The comparator produces a PWM signal that is fed to drivers of controllable switches in the dc-dc converter. The duty ratio of the PWM signal depends on the value of the control voltage. The frequency of the PWM signal is the same as the frequency of the sawtooth waveform. An important advantage of the voltage-mode control is its simple hardware implementation and flexibility.

The error amplifier in Fig. 13.17a reacts fast to changes in the converter output voltage. Thus, the voltage-mode control provides good load regulation, that is, regulation against variations in the load. Line regulation (regulation against variations in the input voltage) is, however, delayed because changes in the input voltage must first manifest themselves in the converter output before they can be corrected. To alleviate this problem, the voltage-mode control scheme is sometimes augmented by a so-called voltage-feedforward path. The feedforward path affects directly the PWM duty ratio according to variations in the input voltage. As will be explained in what follows, the input voltage feedforward is an inherent feature of current-mode control schemes.

The current-mode control scheme is presented in Fig. 13.7b. An additional inner control loop feeds back an inductor current signal, and this current signal, converted into its voltage analog, is compared to the control voltage. This modification of replacing the sawtooth waveform of the voltage-mode control scheme by a converter current signal significantly alters the dynamic behavior of the converter, which then takes on some characteristics of a current source.



(a)

(b)

FIGURE 13.17 Main control schemes for dc-dc converters: (a) voltage-mode control; (b) current-mode control.

The output current in PWM dc-dc converters is either equal to the *average* value of the output inductor current (buck-derived and Čuk converters) or is a product of an *average* inductor current and a function of the duty ratio. In practical implementations of the current-mode control, it is feasible to sense the peak inductor current instead of the average value. As the peak inductor current is equal to the peak switch current, the latter can be used in the inner loop, which often simplifies the current sensor. Note that the peak inductor (switch) current is proportional to the input voltage. Hence, the inner loop of the current-mode control naturally accomplishes the input voltage-feedforward technique. Among several current-mode control versions, the most popular is the constant-frequency one that requires a clock signal. Advantages of the current-mode control are the input voltage feedforward, the limit on the peak switch current, the equal current sharing in modular converters, and the reduction in the converter dynamic order. The main disadvantage of the current-mode control is its complicated hardware, which includes a need to compensate the control voltage by ramp signals (to avoid converter instability).

Among other control methods of dc-dc converters, a hysteretic (or bang-bang) control is very simple for hardware implementation. However, the hysteretic control results in variable frequency operation of semiconductor switches. Generally, a constant switching frequency is preferred in power electronic circuits for easier elimination of electromagnetic interference and better utilization of magnetic components.

Application specific integrated circuits (ASICs) are commercially available that contain the main elements of voltage- or current-mode control schemes. On a single 14- or 16-pin chip, there is an error amplifier, comparator, sawtooth generator or sensed current input, latch, and PWM drivers. The switching frequency is usually set by an external *RC* network and can be varied from tens to hundreds of kilohertz. The controller has an oscillator output for synchronization with other converters in modular power supply systems, and a constant voltage reference is generated on the chip as well. Additionally, the ASIC controller may be equipped with various diagnostic and protection features; for example, current limiting, overvoltage and undervoltage protection, soft start, dead time in case of multiple PWM outputs, and duty ratio limiting. In several dc-dc converter topologies, for example, buck and buck-boost, neither control terminal of semiconductor switches is grounded (so-called high-side switches). The ASIC controllers are usually designed for a particular topology and their PWM drivers may be able to drive high-side switches in low-voltage applications. However, in high-voltage applications, external PWM drivers must be used. External PWM drivers are also used for switches with high input capacitances. To take full advantage of the input-output isolation in transformer versions of dc-dc converters, such an isolation must be also provided in the control loop. Signal transformers or optocouplers are used for isolating feedback signals.

Dynamic characteristics of closed-loop dc-dc converters must fulfill certain requirements. To simplify analysis, these requirements are usually translated into desired properties of the open loop. The open loop should provide a sufficient (typically, at least 45°) phase margin for stability, high bandwidth (about one-tenth of the switching frequency) for good transient response, and high gain (several tens of decibels) at low frequencies for small steady-state error.

The open-loop dynamic characteristics are shaped by compensating networks of passive components around the error amplifier. Second- or third-order *RC* networks are commonly used. Because the converter itself is a part of the control loop, the design of compensating networks requires a knowledge of small-signal characteristics of the converter. There are several methods of small-signal characterization of PWM dc-dc converters, and the most popular ones provide average models of converters under the assumptions of high switching frequency. The averaged models are then linearized at an operating point to obtain small-signal transfer functions. Among analytical averaging methods, state-space averaging has been popular since the late 1970s. Circuit-based averaging is usually performed using PWM switch or direct replacement of semiconductor switches by controlled current and voltage sources. All these methods can take into account converter parasitics.

The most important small-signal characteristic is the *control-to-output* transfer function T_p. Other converter characteristics that are investigated are: the *input-to-output* (or *line-to-output*) voltage transfer function, also called the *open-loop dynamic line regulation* or the *audio susceptibility*, which describes the input-output disturbance transmission; the *open-loop input impedance*; and the *open-loop dynamic load regulation*. Buck-derived, boost, and buck-boost converters are second-order dynamic systems; the Čuk converter is a fourth-order system. Characteristics of buck and buck-derived converters are similar to each other. Another group of converters with similar small-signal characteristics is formed by boost, buck-boost, and flyback converters. Among parasitic components, the ESR of the filter capacitor r_C introduces additional dynamic terms into transfer functions. Other parasitic resistances usually modify slightly the effective value of the load resistance. Sample characteristics in what follows are given for nonzero r_C, neglecting other parasitics.

The control-to-output transfer function of the forward converter is

$$\begin{aligned} T_p(s) &\equiv \left.\frac{v_o(s)}{d(s)}\right|_{v_s(s)=0} \\ &= \frac{V_I R r_C}{nL(R+r_C)} \frac{s+1/Cr_c}{s^2+s(CR_C+L)/LC(R+r_C)+R/LC(R+r_C)} \end{aligned} \tag{13.40}$$

It can be seen that this transfer function has two poles and one zero. The zero is due to the filter capacitor ESR. Buck-derived converters can easily be compensated for stability with second-order controllers.

The control-to-output transfer function of the boost converter is given by

$$T_p(s) = -\frac{V_O r_C}{(1-D)(R+r_C)} \times \frac{(s+1/Cr_C)(s-(1-D)^2R/L)}{s^2+s((1-D)^2CRr_C+L)/LC(R+r_C)+(1-D)^2R/LC(R+r_C)}. \tag{13.41}$$

The zero $-(1-D)^2R/L$ is located in the right-half of the s-plane Therefore, the boost converter (as well as buck-boost and flyback converters) is a nonminimum phase system. Nonminimum phase dc-dc converters are typically compensated with third-order controllers. Step-by-step procedures for the design of compensating networks are usually given by manufacturers of ASIC controllers in application notes.

This section ends with a word on the behavior of dc-dc converters in distributed power supply systems. An important feature of closed-loop regulated dc-dc converters is that they exhibit a negative input resistance. As the load voltage is kept constant by the controller, the output power changes with the load. With slow load changes, an increase (decrease) in the input voltage results in a decrease (increase) in the input power. This negative resistance property must be carefully examined during the system design to avoid resonances.

13.1 Applications of DC-DC Converters

Step-down choppers find most of their applications in high-performance dc drive systems, for example, electric traction, electric vehicles, and machine tools. The dc motors with their winding inductances and mechanical inertia act as filters resulting in high-quality armature currents. The average output voltage of step-down choppers is a linear function of the switch duty ratio. Step-up choppers are used primarily in radar and ignition systems. The dc choppers can be modified for two-quadrant and four-quadrant operation. Two-quadrant choppers may be a part of autonomous power supply systems that contain battery packs and such renewable dc sources as photovoltaic arrays, fuel cells, or wind turbines. Four-quadrant choppers are applied in drives in which regenerative breaking of dc motors is desired, for example, transportation systems with frequent stops. The dc choppers with inductive outputs serve as inputs to current-driven inverters.

The addition of filtering reactive components to dc choppers results in PWM dc-dc converters. The dc-dc converters can be viewed as dc transformers that deliver to the load a dc voltage or current at a different level than the input source. This dc transformation is performed by electronic switching means, not by electromagnetic means such as in conventional transformers. The output voltages of dc-dc converters range from one volt for special VLSI circuits to tens of kilovolts in X-ray lamps. The most common output voltages are: 3.3 V for modern microprocessors; 5 and 12 V for logic circuits; 48 V for telecommunication equipment; and 270 V for main dc bus on airplanes. Typical input voltages include 48 V, 170 V (the peak value of a 120-V rms line), and 270 V.

Selection of a topology of dc-dc converters is determined not only by input/output voltages, which can be additionally adjusted with the turns ratio in isolated converters, but also by power levels, voltage and current stresses of semiconductor switches, and utilization of magnetic components. The low part-count flyback converter is popular in low power applications (up to 200 W). Its main deficiencies are a large size of the flyback transformer core and high voltage stress on the semiconductor switch. The forward converter is also a single switch converter. Because its core size requirements are smaller, it is popular in low-medium- (up to several hundreds of watts) power applications. Disadvantages of the forward converter are the need for demagnetizing winding, and a high voltage stress on the semiconductor switch. The push-pull converter is also used at medium-power levels. Due to bidirectional excitation, the transformer size is small. An advantage of the push-pull converter is also a possibility to refer driving terminals of both switches to the ground, which greatly simplifies the control circuitry. A disadvantage of the push-pull converter is a potential core saturation in the case of asymmetry. The half-bridge converter has a similar range of applications as the push-pull converter. There is no danger of transformer saturation in the half-bridge converter. It requires, however, two additional input capacitors to split in half the input dc source. The full-bridge converter is used at high (several kilowatts) power and voltage levels. The voltage stress on power switches is limited to the input voltage source value. A disadvantage of the full-bridge converter is a high number of semiconductor devices.

The dc-dc converters are building blocks of distributed power supply systems in which a common dc bus voltage is converted to various other voltages according to requirements of particular loads. Such distributed dc systems are common in space stations, ships and airplanes, as well as in computer and telecommunication equipment. It is expected that modern portable wireless communication and signal processing systems will use variable supply voltages to minimize power consumption and to extend battery life. Low-output voltage converters in these applications utilize the synchronous rectification arrangement.

Another major area of dc-dc converter applications is related to the utility ac grid. For critical loads, if the utility grid fails, there must be a backup source of energy, for example, a battery pack. This need for continuous power delivery gave rise to various types of uninterruptible power supplies (UPSs). Thus dc-dc converters are used in UPSs to adjust the level of a rectified grid voltage to that of the backup source. Because during normal operation the energy flows from the grid to the backup source and during emergency conditions the backup source must supply the load, bidirectional dc-dc converters are often used. Moreover dc-dc converters are also used in dedicated battery chargers.

Power electronic loads, especially those with front-end rectifiers, pollute the ac grid with odd harmonics. Thus dc-dc converters are used as intermediate stages, just after a rectifier and before the load-supplying dc-dc converter, for shaping the input ac current to improve power factor and decrease the harmonic content. The boost converter is especially popular in such power factor correction (PFC) applications. Another utility grid-related application of dc-dc converters is in interfaces between ac networks and dc renewable energy sources such as fuel cells and photovoltaic arrays.

In isolated dc-dc converters, multiple outputs are possible with additional secondary windings of transformers. Only one output is regulated with a feedback loop, but other outputs depend on the duty ratio of the regulated one and on their loads. A multiple-output dc-dc converter is a convenient solution in applications where there is a need for one closely regulated output voltage and for one or more other noncritical output voltage levels.

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Inverters

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14.1 Introduction

The main objective of static power converters is to produce an ac output waveform from a dc power supply. These are the types of waveforms required in adjustable speed drives (ASDs), uninterruptible power supplies (UPS), static var compensators, active filters, flexible ac transmission systems (FACTS), and voltage compensators, which are only a few applications. For sinusoidal ac outputs, the magnitude, frequency, and phase should be controllable. According to the type of ac output waveform, these topologies can be considered as voltage source inverters (VSIs), where the independently controlled ac output is a voltage waveform. These structures are the most widely used because they naturally behave as voltage sources as required by many industrial applications, such as adjustable speed drives (ASDs), which are the most popular application of inverters; see Fig. 14.1a. Similarly, these topologies can be found as current source inverters (CSIs), where the independently controlled ac output is a current waveform. These structures are still widely used in medium-voltage industrial applications, where high-quality voltage waveforms are required.

Static power converters, specifically inverters, are constructed from power switches and the ac output waveforms are therefore made up of discrete values. This leads to the generation of waveforms that feature fast transitions rather than smooth ones. For instance, the ac output voltage produced by the VSI of a standard ASD is a three-level

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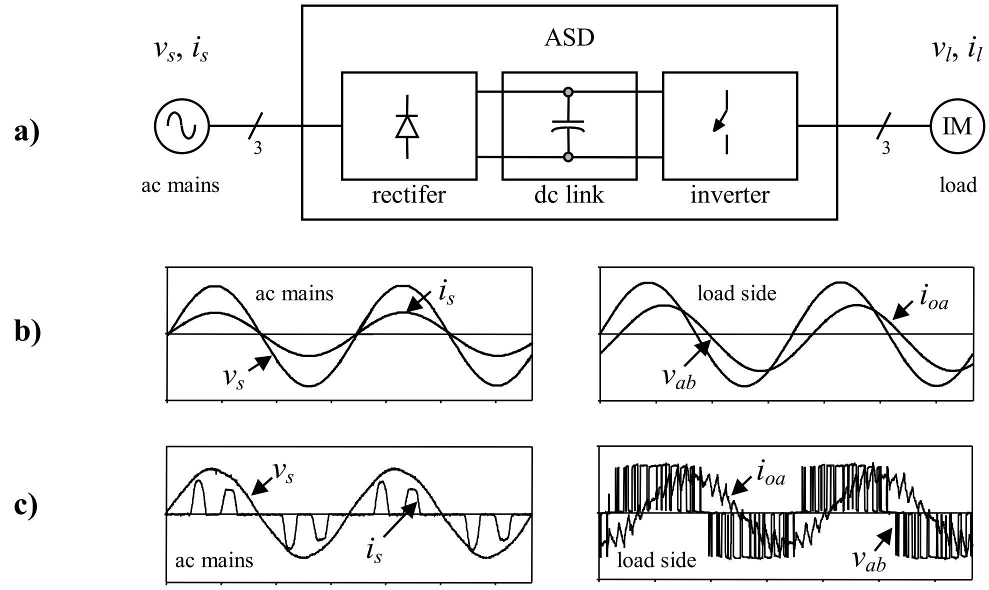


FIGURE 14.1 A standard adjustable speed drive scheme and associated waveforms: (a) the electrical power conversion topology; (b) the ideal input (ac mains) and output (load) waveforms; and (c) the actual input (ac mains) and output (load) waveforms.

waveform (Fig. 14.1c). Although this waveform is not sinusoidal as expected (Fig. 14.1b), its fundamental component behaves as such. This behavior should be ensured by a modulating technique that controls the amount of time and the sequence used to switch the power valves on and off. The modulating techniques most used are the carrier-based technique (e.g., sinusoidal pulsewidth modulation, SPWM), the space-vector (SV) technique, and the selective-harmonic-elimination (SHE) technique.

The discrete shape of the ac output waveforms generated by these topologies imposes basic restrictions on the applications of inverters. The VSI generates an ac output voltage waveform composed of discrete values (high dv/dt); therefore, the load should be inductive at the harmonic frequencies in order to produce a smooth current waveform. A capacitive load in the VSIs will generate large current spikes. If this is the case, an inductive filter between the VSI ac side and the load should be used. On the other hand, the CSI generates an ac output current waveform composed of discrete values (high di/dt); therefore, the load should be capacitive at the harmonic frequencies in order to produce a smooth voltage waveform. An inductive load in CSIs will generate large voltage spikes. If this is the case, a capacitive filter between the CSI ac side and the load should be used.

A three-level voltage waveform is not recommended for medium-voltage ASDs due to the high dv/dt that would apply to the motor terminals. Several negative side effects of this approach have been reported (bearing and isolation problems). As alternatives to improve the ac output waveforms in VSIs are the multistage topologies (multilevel and multicell). The basic principle is to construct the required ac output waveform from various voltage levels, which achieves medium-voltage waveforms at reduced dv/dt. Although these topologies are well developed in ASDs, they are also suitable for static var compensators, active filters, and voltage compensators. Specialized modulating techniques have been developed to switch the higher number of power valves involved in these topologies. Among others, the carrier-based (SPWM) and SV-based techniques have been naturally extended to these applications.

In many applications, it is required to take energy from the ac side of the inverter and send it back into the dc side. For instance, whenever ASDs need to either brake or slow down the motor speed, the kinetic energy is sent into the voltage dc link (Fig. 14.1a). This is known as the regenerative mode operation and, in contrast to the motoring mode, the dc link current direction is reversed due to the fact that the dc link voltage is fixed. If a capacitor is used to maintain the dc link voltage (as in standard ASDs) the energy must either be dissipated or fed back into the distribution system, otherwise, the dc link voltage gradually increases. The first approach requires the dc link capacitor be connected in parallel with a resistor, which must be properly switched only when the energy flows from the motor load into the dc link. A better alternative is to feed back such energy into the distribution system. However, this alternative requires a reversible-current topology connected between the distribution system and the dc link capacitor. A modern approach to such a requirement is to use the active front-end rectifier technologies, where the regeneration mode is a natural operating mode of the system.

In this chapter, single and three-phase inverters in their voltage and current source alternatives will be reviewed. The dc link will be assumed to be a perfect dc, either voltage or current source that could be fixed as the dc link voltage in standard ASDs, or variable as the dc link current in some medium-voltage current source drives. Specifically, the topologies, modulating techniques, and control aspects, oriented to standard applications, are analyzed. In order to simplify the analysis, the inverters are considered lossless topologies, which are composed of ideal power valves. Nevertheless, some practical nonideal conditions are also considered.

14.2 Single-Phase Voltage Source Inverters

Single-phase voltage source inverters (VSIs) can be found as half-bridge and full-bridge topologies. Although the power range they cover is the low one, they are widely used in power supplies, single-phase UPSs, and currently to form elaborate high-power static power topologies, such as for instance, the multicell configurations that are reviewed in Section 14.7. The main features of both approaches are reviewed and presented in the following.

14.2.1 Half-Bridge VSI

Figure 14.2 shows the power topology of a half-bridge VSI, where two large capacitors are required to provide a neutral point N, such that each capacitor maintains a constant voltage $v_i/2$. Because the current harmonics injected by the operation of the inverter are low-order harmonics, a set of large capacitors (C_+ and C_-) is required. It is clear that both switches S_+ and S_- cannot be on simultaneously because a short circuit across the dc link voltage source v_i would be produced. There are two defined (states 1 and 2) and one undefined (state 3) switch state as shown in Table 14.1. In order to avoid the short circuit across the dc bus and the undefined ac output voltage condition, the modulating technique should always enure that at any instant either the top or the bottom switch of the inverter leg is on.

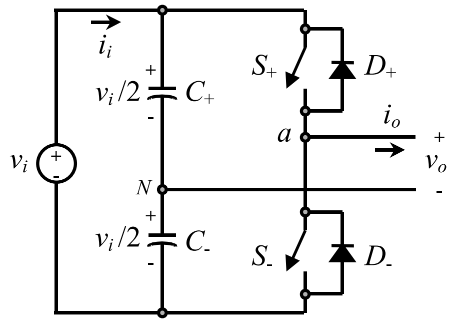


FIGURE 14.2 Single-phase half-bridge VSI.

TABLE 14.1 Switch states for a half-bridge single-phase VSI

State	State	v_o	Components Conducting
S_+ is on and S_- is off	1	$v_i/2$	S_+ if $i_o > 0$ D_+ if $i_o < 0$
S_- is on and S_+ is off	2	$-v_i/2$	D_- if $i_o > 0$ S_- if $i_o < 0$
s_+ and S_- are all off	3	$-v_i/2$ $v_i/2$	D_- if $i_o > 0$ D_+ if $i_o < 0$

Figure 14.3 shows the ideal waveforms associated with the half-bridge inverter shown in Fig. 14.2. The states for the switches S_+ and S_- are defined by the modulating technique, which in this case is a carrier-based PWM.

14.2.1.1 The Carrier-Based Pulsewidth Modulation (PWM) Technique

As mentioned earlier, it is desired that the ac output voltage $v_o = v_{aN}$ follow a given waveform (e.g., sinusoidal) on a continuous basis by properly switching the power valves. The carrier-based PWM technique fulfils such a requirement as it defines the on and off states of the switches of one leg of a VSI by comparing a modulating signal v_c (desired ac output voltage) and a triangular waveform v_Δ (carrier signal). In practice, when $v_c > v_\Delta$ the switch S_+ is on and the switch S_- is off; similarly, when $v_c < v_\Delta$ the switch S_+ is off and the switch S_- is on.

A special case is when the modulating signal v_c is a sinusoidal at frequency f_c and amplitude $\hat{v}_c$, and the triangular signal v_Δ is at frequency f_Δ and amplitude $\hat{v}_\Delta$. This is the sinusoidal PWM (SPWM) scheme. In this case, the modulation index m_a (also known as the amplitude-modulation ratio) is defined as

$$m_a = \frac{\hat{v}_c}{\hat{v}_\Delta} \tag{14.1}$$

and the normalized carrier frequency m_f (also known as the frequency-modulation ratio) is

$$m_f = \frac{f_\Delta}{f_c} \tag{14.2}$$

Figure 14.3(e) clearly shows that the ac output voltage $v_o = v_{aN}$ is basically a sinusoidal waveform plus harmonics, which features: (a) the amplitude of the fundamental component of the ac output voltage $\hat{v}_{o1}$ satisfying the following expression:

$$\hat{v}_{o1} = \hat{v}_{aN1} = \frac{v_i}{2} m_a \tag{14.3}$$

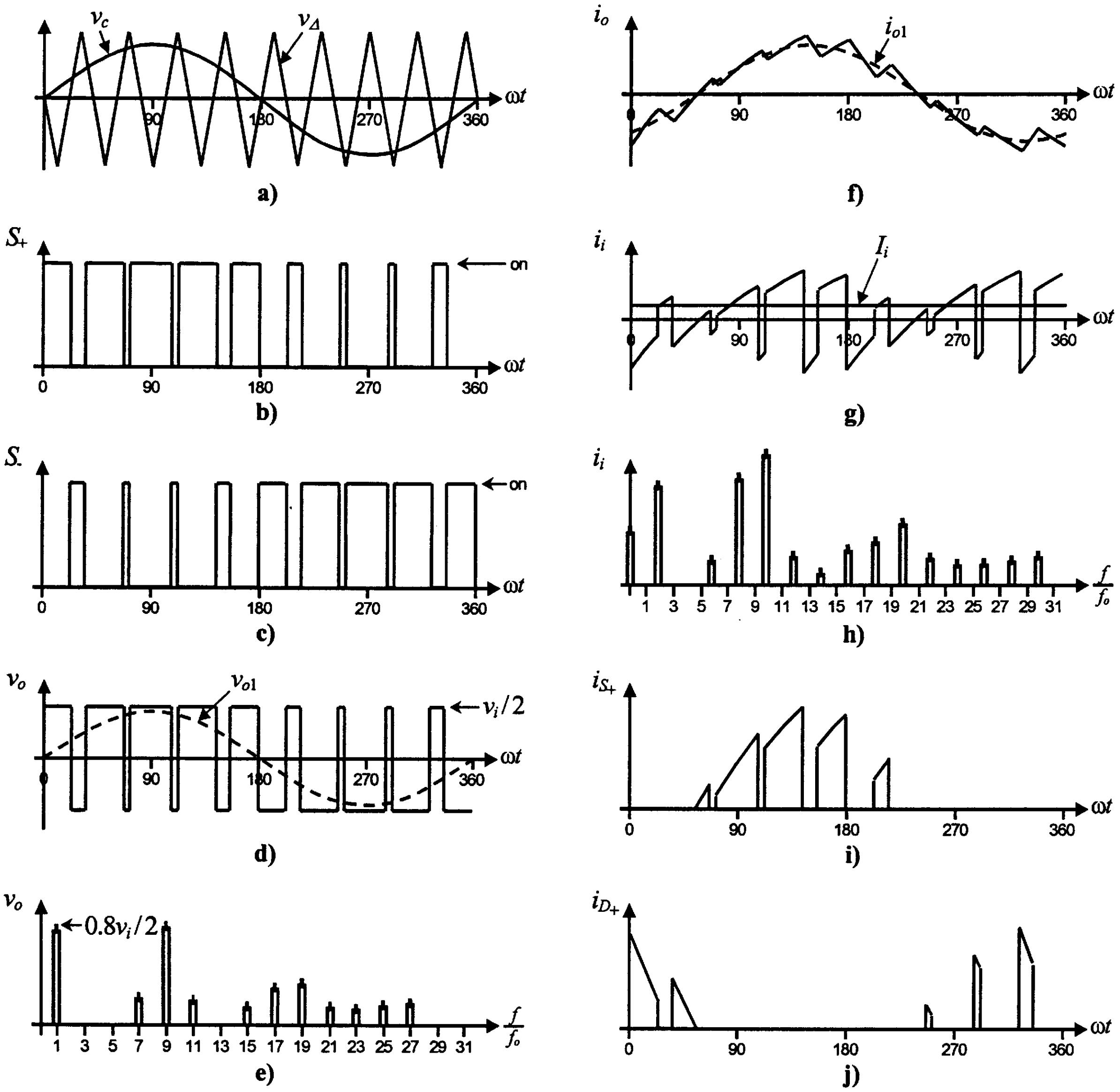


FIGURE 14.3 The half-bridge VSI. Ideal waveforms for the SPWM ($m_a = 0.8$, $m_f = 9$): (a) carrier and modulating signals; (b) switch S_+ state; (c) Switch S_- state; (d) ac output voltage; (e) ac output voltage spectrum; (f) ac output current; (g) dc current; (h) dc current spectrum; (i) switch S_+ current; (j) diode D_+ current.

will be discussed later); (b) for odd values of the normalized carrier frequency m_f the harmonics in the ac output voltage appear at normalized frequencies f_h centered around m_f and its multiples, specifically,

$$h = lm_f \pm k \qquad l = 1, 2, 3, \ldots \tag{14.4}$$

where $k = 2, 4, 6, \ldots$ for $l = 1, 3, 5, \ldots$; and $k = 1, 3, 5, \ldots$ for $l = 2, 4, 6, \ldots$; (c) the amplitude of the ac output voltage harmonics is a function of the modulation index m_a and is independent of the normalized carrier frequency m_f for $m_f > 9$; (d) the harmonics in the dc link current (due to the modulation) appear at normalized frequencies f_p centered around the normalized carrier frequency m_f and its multiples, specifically,

$$p = lm_f \pm k \pm 1 \qquad l = 1, 2, \ldots \tag{14.5}$$

where $k = 2, 4, 6, \ldots$ for $l = 1, 3, 5, \ldots$; and $k = 1, 3, 5, \ldots$ for $l = 2, 4, 6, \ldots$. Additional important issues are: (a) for small values of m_f ($m_f < 21$), the carrier signal v_Δ and the modulating signal v_c should be synchronized to each other (m_f integer), which is required to hold the previous features; if this is not the case, subharmonics will be present in the ac output voltage; (b) for large values of m_f ($m_f > 21$), the subharmonics are negligible if an asynchronous PWM

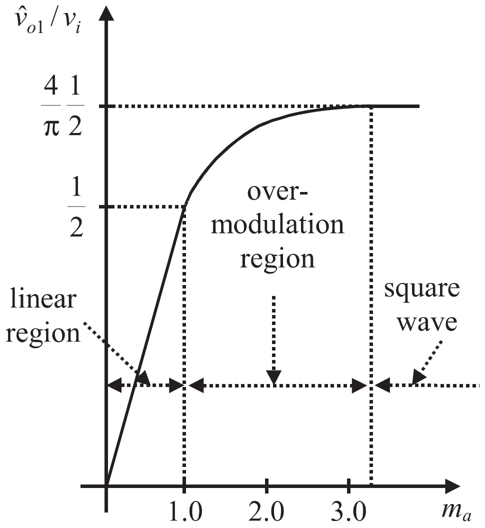


FIGURE 14.4 Fundamental ac component of the output voltage in a half-bridge VSI SPWM modulated.

technique is used, however, due to potential very low-order subharmonics, its use should be avoided; finally (c) in the overmodulation region ($m_a > 1$) some intersections between the carrier and the modulating signal are missed, which leads to the generation of low-order harmonics but a higher fundamental ac output voltage is obtained; unfortunately, the linearity between m_a and $\hat{v}_{o1}$achieved in the linear region Eq. (14.3) does not hold in the overmodulation region, moreover, a saturation effect can be observed (Fig. 14.4).

The PWM technique allows an ac output voltage to be generated that tracks a given modulating signal. A special case is the SPWM technique (the modulating signal is a sinusoidal) that provides in the linear region an ac output voltage that varies linearly as a function of the modulation index and the harmonics are at well-defined frequencies and amplitudes. These features simplify the design of filtering components. Unfortunately, the maximum amplitude of the fundamental ac voltage is $v_i/2$ in this operating mode. Higher voltages are obtained by using the overmodulation region ($m_a > 1$); however, low-order harmonics appear in the ac output voltage. Very large values of the modulation index ($m_a > 3.24$) lead to a totally square ac output voltage that is considered as the square-wave modulating technique that is discussed in the next section.

14.2.1.2 Square-Wave Modulating Technique

Both switches S_+ and S_- are on for one-half cycle of the ac output period. This is equivalent to the SPWM technique with an infinite modulation index m_a. Figure 14.5 shows the following: (a) the normalized ac output voltage harmonics are at frequencies $h = 3, 5, 7, 9, \ldots$, and for a given dc link voltage; (b) the fundamental ac output voltage features an amplitude given by

$$\hat{v}_{o1} = \hat{v}_{aN1} = \frac{4}{\pi}\frac{v_i}{2}, \tag{14.6}$$

and the harmonics feature an amplitude given by

$$\hat{v}_{oh} = \frac{\hat{v}_{o1}}{h} \tag{14.7}$$

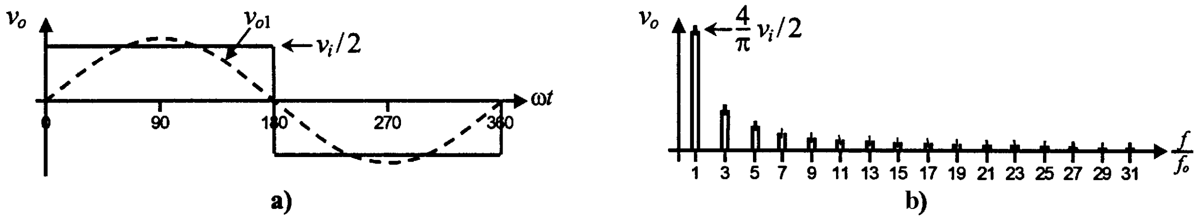
It can be seen that the ac output voltage cannot be changed by the inverter. However, it could be changed by controlling the dc link voltage v_i. Other modulating techniques that are applicable to half-bridge configurations (e.g., selective harmonic elimination) are reviewed here as they can easily be extended to modulate other topologies.

14.2.1.3 Selective Harmonic Elimination

The main objective is to obtain a sinusoidal ac output voltage waveform where the fundamental component can be adjusted arbitrarily within a range and the intrinsic harmonics selectively eliminated. This is achieved by mathematically generating the exact instant of the turn-on and turn-off of the power valves. The ac output voltage features odd half- and quarter-wave symmetry; therefore, even harmonics are not present ($v_{oh} = 0, h = 2, 4, 6, \ldots$). Moreover, the per-phase voltage waveform ($v_o = v_{aN}$ in Fig. 14.2), should be chopped N times per half-cycle in order to adjust the fundamental and eliminate $N - 1$ harmonics in the ac output voltage waveform. For instance, to eliminate the third and fifth harmonics and to perform fundamental magnitude control ($N = 3$), the equations to be solved are the following:

$$\begin{aligned}
&\cos(1\alpha_1) - \cos(1\alpha_2) + \cos(1\alpha_3) = (2 + \pi\hat{v}_{o1}/v_i)/4 \\
&\cos(3\alpha_1) - \cos(3\alpha_2) + \cos(3\alpha_3) = 1/2 \\
&\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) = 1/2
\end{aligned} \tag{14.8}$$

where the angles α_1, α_2, and α_3 are defined as shown in Fig. 14.6a. The angles are found by means of iterative algorithms as no analytical solutions can be derived. The angles α_1, α_2, and



a) b)

FIGURE 14.5 The half-bridge VSI. Ideal waveforms for the square-wave modulating technique: (a) ac output voltage; (b) ac output voltage spectrum.

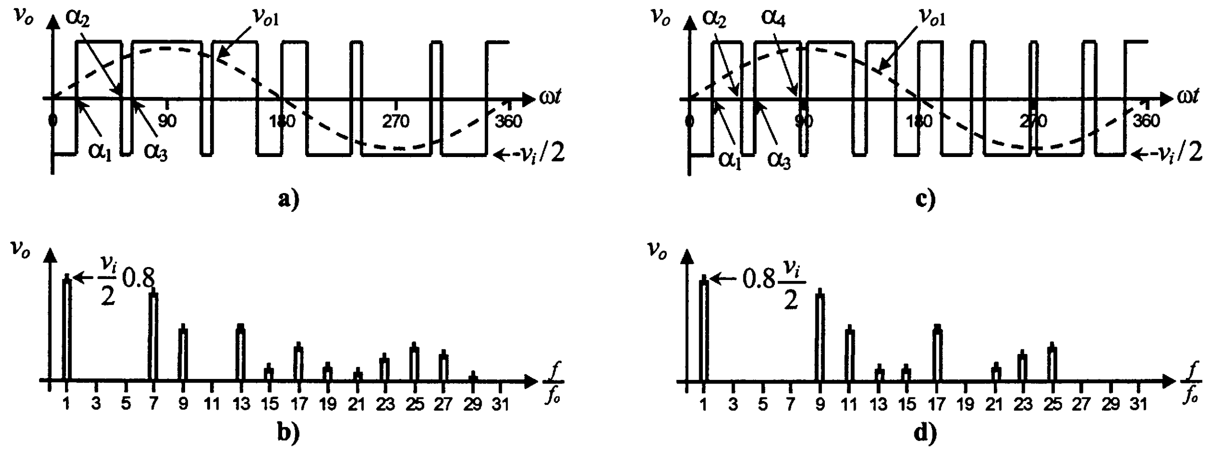


FIGURE 14.6 The half-bridge VSI. Ideal waveforms for the SHE technique: (a) ac output voltage for third and fifth harmonic elimination; (b) spectrum of (a); (c) ac output voltage for third, fifth, and seventh harmonic elimination; (d) spectrum of (c).

α_3 are plotted for different values of $\hat{v}_{o1}/v_i$ in Fig. 14.7a. The general expressions to eliminate an even $N-1$ $(N-1 = 2, 4, 6, \ldots)$ number of harmonics are

$$-\sum_{k=1}^{N}(-1)^k\cos(\alpha_k) = \frac{2+\pi\hat{v}_{o1}/v_i}{4}$$
$$-\sum_{k=1}^{N}(-1)^k\cos(n\alpha_k) = \frac{1}{2} \qquad \text{for } n = 3, 5, \ldots, 2N-1 \tag{14.9}$$

where α_1, $\alpha_2, \ldots, \alpha_N$ should satisfy $\alpha_1 < \alpha_2 < \cdots < \alpha_N < \pi/2$. Similarly, to eliminate an odd number of harmonics, for instance, the third, fifth and seventh, and to perform fundamental magnitude control $(N-1=3)$, the equations to be solved are:

$$\begin{aligned}
\cos(1\alpha_1) - \cos(1\alpha_2) + \cos(1\alpha_3) - \cos(1\alpha_4) &= (2-\pi\hat{v}_{o1}/v_i)/4\\
\cos(3\alpha_1) - \cos(3\alpha_2) + \cos(3\alpha_3) - \cos(3\alpha_4) &= 1/2\\
\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) - \cos(5\alpha_4) &= 1/2\\
\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) - \cos(7\alpha_4) &= 1/2
\end{aligned} \tag{14.10}$$

where the angles $\alpha_1, \alpha_2, \alpha_3$, and α_4 are defined as shown in Fig. 14.6b. The angles α_1, α_2, α_3 and α_4 are plotted for different values of $\hat{v}_{o1}/v_i$ in Fig. 14.7b. The general expressions to

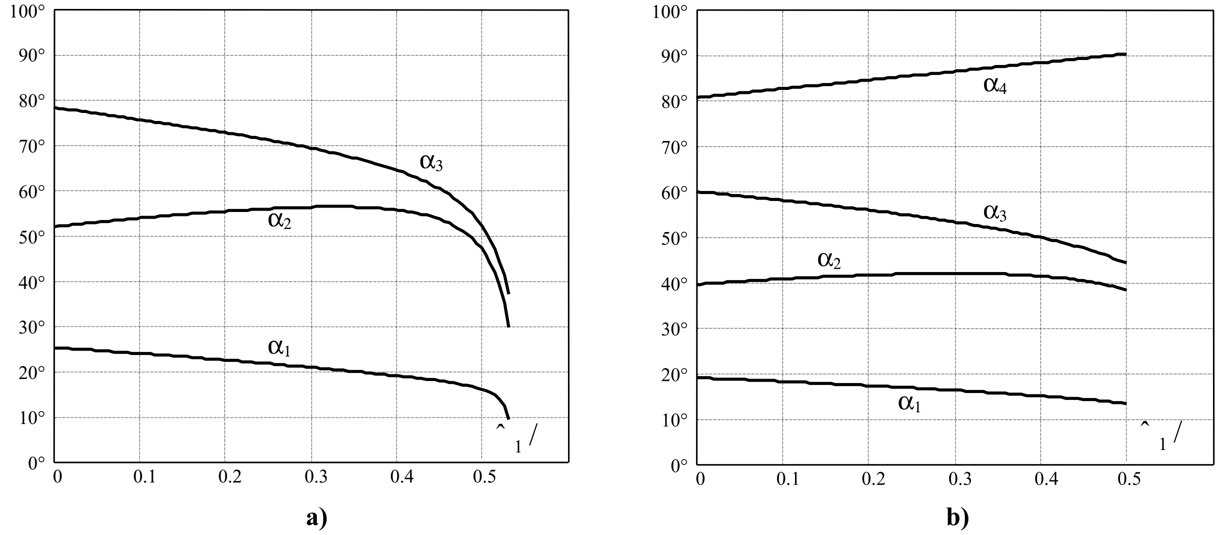


FIGURE 14.7 Chopping angles for SHE and fundamental voltage control in half-bridge VSIs: (a) third and fifth harmonic elimination; (b) third, fifth, and seventh harmonic elimination.

eliminate an odd $N-1$ $(N-1=3,5,7,\ldots)$ number of harmonics are given by

$$-\sum_{k=1}^{N}(-1)^k\cos(n\alpha_k)=\frac{2-\pi\hat{v}_{o1}/v_i}{4}$$
$$-\sum_{k=1}^{N}(-1)^k\cos(n\alpha_k)=\frac{1}{2}\qquad\text{for } n=3,5,\ldots,2N-1 \tag{14.11}$$

where $\alpha_1,\alpha_2,\ldots,\alpha_N$ should satisfy $\alpha_1<\alpha_2<\cdots<\alpha_N<\pi/2$.

To implement the SHE modulating technique, the modulator should generate the gating pattern according to the angles as shown in Fig. 14.7. This task is usually performed by digital systems that normally store the angles in look-up tables.

14.2.1.4 DC Link Current

The split capacitors are considered part of the inverter and therefore an instantaneous power balance cannot be considered due to the storage energy components (C_+ and C_-). However, if a lossless inverter is assumed, the average power absorbed in one period by the load must be equal to the average power supplied by the dc source. Thus, we can write

$$\int_0^T v_i(t)\cdot i_i(t)\cdot dt=\int_0^T v_o(t)\cdot i_o(t)\cdot dt \tag{14.12}$$

where T is the period of the ac output voltage. For an inductive load and a relatively high switching frequency, the load current i_o is nearly sinusoidal and therefore only the fundamental component of the ac output voltage provides power to the load. On the other hand, if the dc link voltage remains constant $v_i(t)=V_i$, Eq. (14.12) can be simplified to

$$\int_0^T i_i(t)\cdot dt=\frac{1}{V_i}\int_0^T\sqrt{2}V_{o1}\sin(\omega t)\cdot\sqrt{2}I_o\sin(\omega t-\phi)\cdot dt=I_i \tag{14.13}$$

where V_{o1} is the fundamental rms ac output voltage, I_o is the rms load current, ϕ is an arbitrary inductive load power factor, and I_i is the dc link current that can be further simplified to

$$I_i=\frac{V_{o1}}{V_i}I_o\cos(\phi) \tag{14.14}$$

14.2.2 ull-Bridge VSI

Figure 14.8 shows the power topology of a full-bridge VSI. This inverter is similar to the half-bridge inverter; however, a second leg provides the neutral point to the load. As expected, both switches S_{1+} and S_{1-} (or S_{2+} and S_{2-}) cannot be on simultaneously because a short circuit across the dc link voltage source v_i would be produced. There are four defined (states 1, 2, 3, and 4) and one undefined (state 5) switch states as shown in Table 14.2.

The undefined condition should be avoided so as to be always capable of defining the ac output voltage. In order to avoid the short circuit across the dc bus and the undefined ac output voltage condition, the modulating technique should ensure that either the top or the bottom switch of each leg is on at any instant. It can be observed that the ac output voltage can take values up to the dc link value v_i, which is twice that obtained with half-bridge VSI topologies.

Several modulating techniques have been developed that are applicable to full-bridge VSIs. Among them are the PWM (bipolar and unipolar) techniques.

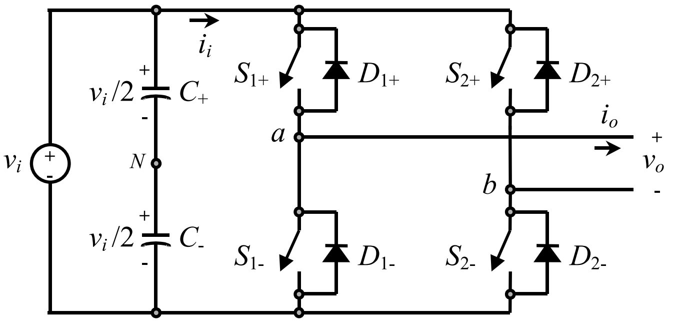


FIGURE 14.8 Single-phase full-bridge VSI.

TABLE 14.2 Switch states for a full-bridge single-phase VSI

State	State	v_{aN}	v_{bN}	v_o	Components Conducting	
S_{1+} and S_{2-} are on and S_{1-} and S_{2+} are off	1	$v_i/2$	$-v_i/2$	v_i	S_{1+} and S_{2-} D_{1+} and D_{2-}	if $i_o>0$ if $i_o<0$
S_{1-} and S_{2+} are on and S_{1+} and S_{2-} are off	2	$-v_i/2$	$v_i/2$	$-v_i$	D_{1-} and D_{2+} S_{1-} and S_{2+}	if $i_o>0$ if $i_o<0$
S_{1+} and S_{2+} are on and S_{1-} and S_{2-} are off	3	$v_i/2$	$v_i/2$	0	S_{1+} and D_{2+} D_{1+} and S_{2+}	if $i_o>0$ if $i_o<0$
s_{1-} and S_{2-} are on and S_{1+} and S_{2+} are off	4	$-v_i/2$	$-v_i/2$	0	D_{1-} and S_{2-} S_{1-} and D_{2-}	if $i_o>0$ if $i_o<0$
S_{1-}, S_{2-}, S_{1+}, and S_{2+} are all off	5	$-v_i/2$ $v_i/2$	$v_i/2$ $-v_i/2$	$-v_i$ v_i	D_{1-} and D_{2+} D_{1+} and D_{2-}	if $i_o>0$ if $i_o<0$

14.2.2.1 Bipolar PWM Technique

States 1 and 2 (Table 14.2) are used to generate the ac output voltage in this approach. Thus, the ac output voltage waveform features only two values, which are v_i and $-v_i$. To generate the states, a carrier-based technique can be used as in half-bridge configurations (Fig. 14.3), where only one sinusoidal modulating signal has been used. It should be noted that the on state in switch S_+ in the half-bridge corresponds to both switches S_{1+} and S_{2-} being in the on state in the full-bridge configuration. Similarly, S_- in the on state in the half-bridge corresponds to both switches S_{1-} and S_{2+} being in the on state in the full-bridge configuration. This is called bipolar carrier-based SPWM. The ac output voltage waveform in a full-bridge VSI is basically a sinusoidal waveform that features a fundamental component of amplitude $\hat{v}_{o1}$ that satisfies the expression

$$\hat{v}_{o1} = \hat{v}_{ab1} = v_i m_a \tag{14.15}$$

in the linear region of the modulating technique ($m_a \leq 1$), which is twice that obtained in the half-bridge VSI. Identical conclusions can be drawn for the frequencies and amplitudes of the harmonics in the ac output voltage and dc link current, and for operations at smaller and larger values of odd m_f (including the overmodulation region ($m_a > 1$)), than in half-bridge VSIs, but considering that the maximum ac output voltage is the dc link voltage v_i. Thus, in the overmodulation region the fundamental component of amplitude $\hat{v}_{o1}$ satisfies the expression

$$v_i < \hat{v}_{o1} = \hat{v}_{ab1} < \frac{4}{\pi} v_i \tag{14.16}$$

14.2.2.2 Unipolar PWM Technique

In contrast to the bipolar approach, the unipolar PWM technique uses the states 1, 2, 3, and 4 (Table 14.2) to generate the ac output voltage. Thus, the ac output voltage waveform can instantaneously take one of three values, namely, v_i, $-v_i$, and 0. To generate the states, a carrier-based technique can be used as shown in Fig. 14.9, where two sinusoidal modulating signals (v_c and $-v_c$) are used. The signal v_c is used to generate v_{aN}, and $-v_c$ is used to generate v_{bN}; thus $v_{bN1} = -v_{aN1}$. On the other hand, $v_{o1} = v_{aN1} - v_{bN1} = 2 \cdot v_{aN1}$; thus $\hat{v}_{o1} = 2 \cdot \hat{v}_{aN1} = m_a \cdot v_i$. This is called unipolar carrier-based SPWM.

Identical conclusions can be drawn for the amplitude of the fundamental component and harmonics in the ac output voltage and dc link current, and for operations at smaller and larger values of m_f, (including the overmodulation region ($m_a > 1$)), than in full-bridge VSIs modulated by the bipolar SPWM. However, because the phase voltages (v_{aN} and v_{bN}) are identical but 180° out of phase, the output voltage ($v_o = v_{ab} = v_{aN} - v_{bN}$) will not contain even harmonics. Thus, if m_f is taken even, the harmonics in the ac output voltage appear at normalized odd frequencies f_h centered around twice the normalized carrier frequency m_f and its multiples. Specifically,

$$h = l m_f \pm k \qquad l = 2, 4, \ldots \tag{14.17}$$

where $k = 1, 3, 5, \ldots$ and the harmonics in the dc link current appear at normalized frequencies f_p centered around twice the normalized carrier frequency m_f and its multiples. Specifically,

$$p = l m_f \pm k \pm 1 \qquad l = 2, 4, \ldots \tag{14.18}$$

where $k = 1, 3, 5, \ldots$. This feature is considered to be an advantage because it allows the use of smaller filtering components to obtain high-quality voltage and current waveforms while using the same switching frequency as in VSIs modulated by the bipolar approach.

14.2.2.3 Selective Harmonic Elimination

In contrast to half-bridge VSIs, this approach is applied in a per-line fashion for full-bridge VSIs. The ac output voltage features odd half- and quarter-wave symmetry; therefore, even harmonics are not present ($\hat{v}_{oh} = 0$, $h = 2, 4, 6, \ldots$). Moreover, the ac output voltage waveform ($v_o = v_{ab}$ in Fig. 14.8), should feature N pulses per half-cycle in order to adjust the fundamental component and eliminate $N - 1$ harmonics. For instance, to eliminate the third, fifth and seventh harmonics and to perform fundamental magnitude control ($N = 4$), the equations to be solved are:

$$\begin{aligned}
&\cos(1\alpha_1) - \cos(1\alpha_2) + \cos(1\alpha_3) - \cos(1\alpha_4) = \pi \hat{v}_{o1}/(v_i 4)\\
&\cos(3\alpha_1) - \cos(3\alpha_2) + \cos(3\alpha_3) - \cos(3\alpha_4) = 0\\
&\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) - \cos(5\alpha_4) = 0\\
&\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) - \cos(7\alpha_4) = 0
\end{aligned} \tag{14.19}$$

where the angles α_1, α_2, α_3, and α_4 are defined as shown in Fig. 14.10(a). The angles α_1, α_2, α_3, and α_4 are plotted for different values of $\hat{v}_{o1}/v_i$ in Fig. 14.11a. The general expressions to eliminate an arbitrary $N - 1$ ($N - 1 = 3, 5, 7, \ldots$) number of harmonics are given by

$$\begin{aligned}
&-\sum_{k=1}^{N} (-1)^k \cos(n\alpha_k) = \frac{\pi}{4} \frac{\hat{v}_{o1}}{v_i}\\
&-\sum_{k=1}^{N} (-1)^k \cos(n\alpha_k) = 0 \qquad \text{for } n = 3, 5, \ldots, 2N - 1
\end{aligned} \tag{14.20}$$

where $\alpha_1, \alpha_2, \ldots, \alpha_N$ should satisfy $\alpha_1 < \alpha_2 < \cdots < \alpha_N < \pi/2$.

Figure 14.10c shows a special case where only the fundamental ac output voltage is controlled. This is known as output control by voltage cancellation, which derives from the fact that its implementation is easily attainable by using two phase-shifted square-wave switching signals as shown in

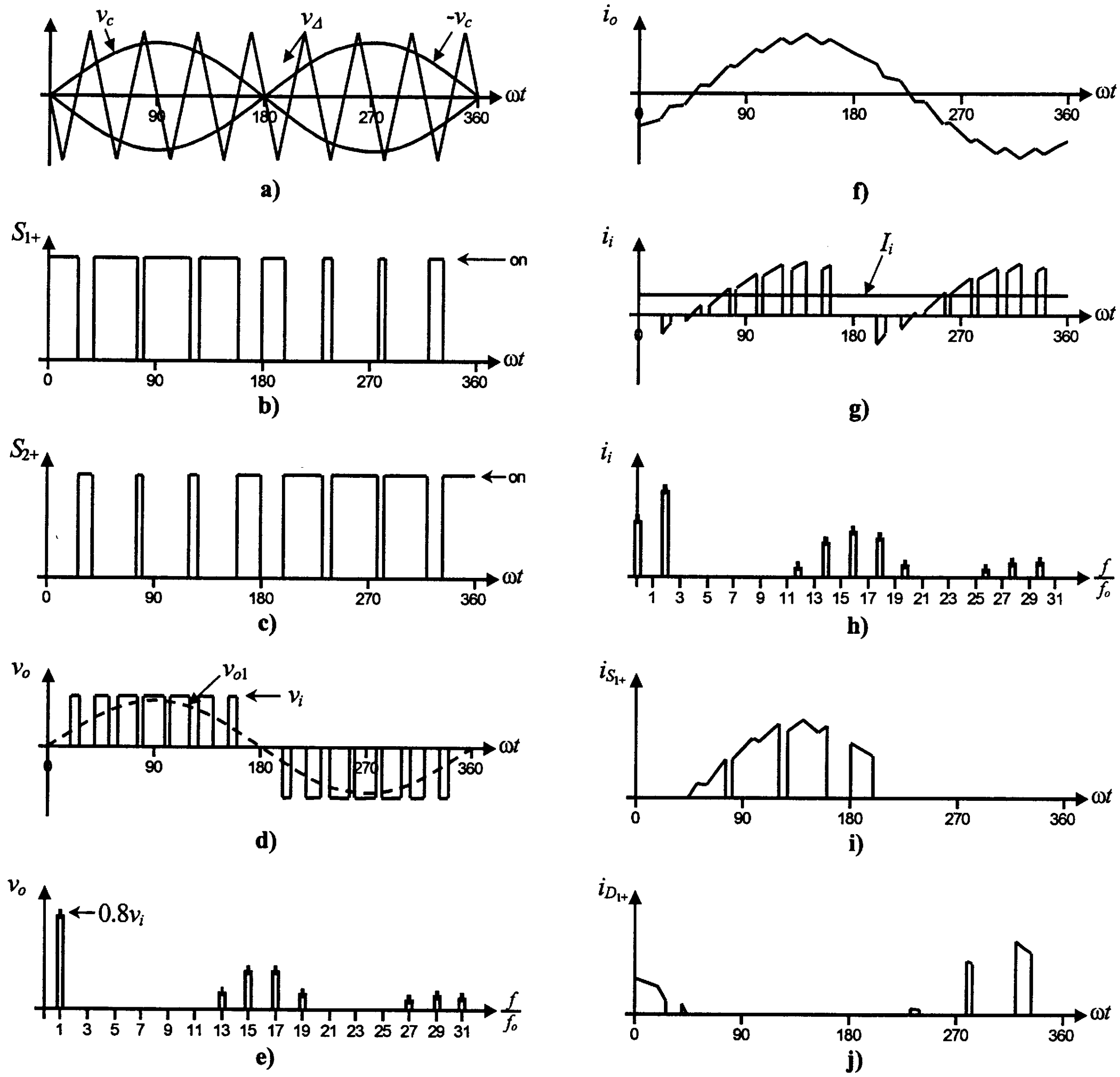


FIGURE 14.9 The full-bridge VSI. Ideal waveforms for the unipolar SPWM ($m_a = 0.8$, $m_f = 8$): (a) carrier and modulating signals; (b) switch S_{1+} state; (c) switch S_{2+} state; (d) ac output voltage; (e) ac output voltage spectrum; (f) ac output current; (g) dc current; (h) dc current spectrum; (i) switch S_{1+} current; (j) diode D_{1+} current.

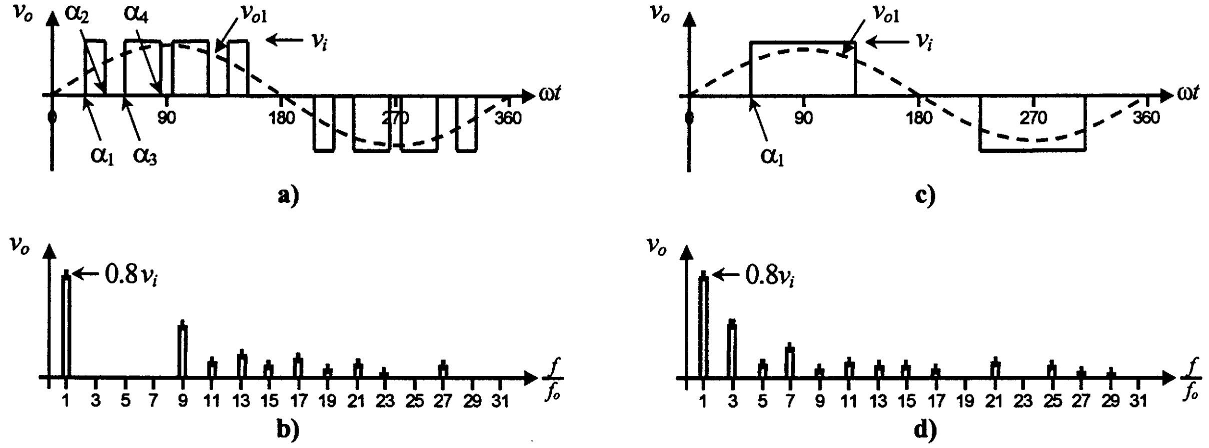


FIGURE 14.10 The half-bridge VSI. Ideal waveforms for the SHE technique: (a) ac output voltage for third, fifth, and seventh harmonic elimination; (b) spectrum of (a); (c) ac output voltage for fundamental control; (d) spectrum of (c).

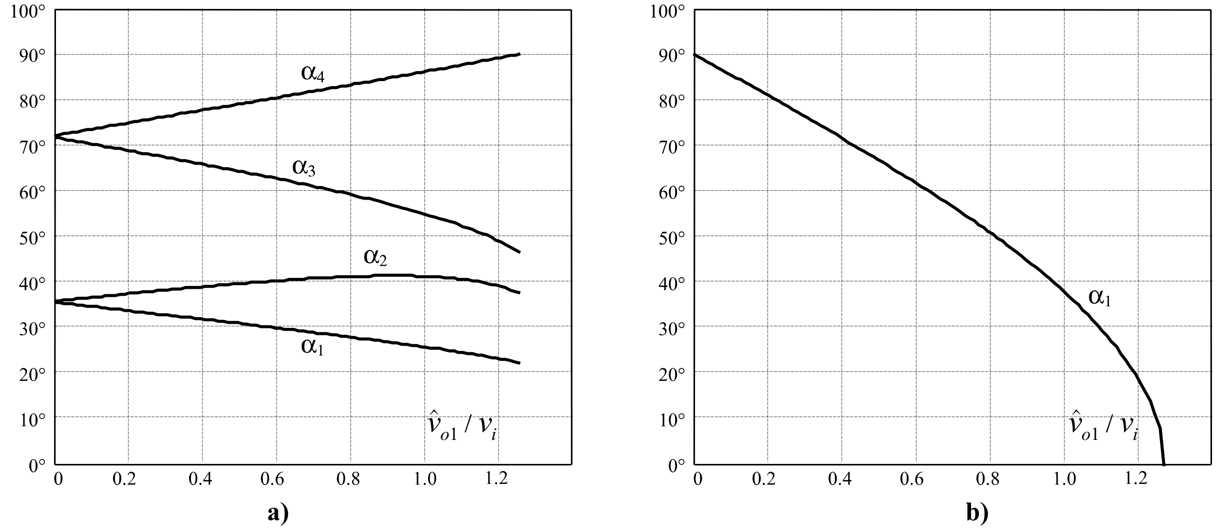


FIGURE 14.11 Chopping angles for SHE and fundamental voltage control in half-bridge VSIs: (a) fundamental control and third, fifth, and seventh harmonic elimination; (b) fundamental control.

Fig. 14.12. The phase-shift angle becomes $2 \cdot \alpha_1$ (Fig. 14.11b). Thus, the amplitude of the fundamental component and harmonics in the ac output voltage are given by

$$\hat{v}_{oh} = \frac{4}{\pi} v_i \frac{1}{h} \cos(h\alpha_1), \qquad h = 1, 3, 5, \ldots \tag{14.21}$$

It can also be observed in Fig. 14.12c that for $\alpha_1 = 0$ square-wave operation is achieved. In this case, the fundamental ac output voltage is given by

$$\hat{v}_{o1} = \frac{4}{\pi} v_i \tag{14.22}$$

where the fundamental load voltage can be controlled by the manipulation of the dc link voltage.

14.2.2.4 DC Link Current

Due to the fact that the inverter is assumed lossless and constructed without storage energy components, the instantaneous power balance indicates that

$$v_i(t) \cdot i_i(t) = v_o(t) \cdot i_o(t) \tag{14.23}$$

For inductive load and relatively high switching frequencies, the load current i_o is nearly sinusoidal. As a first approximation, the ac output voltage can also be considered sinusoidal. On the other hand, if the dc link voltage remains constant $v_i(t) = V_i$, Eq. (14.23) can be simplified to

$$i_i(t) = \frac{1}{V_i} \sqrt{2} V_{o1} \sin(\omega t) \cdot \sqrt{2} I_o \sin(\omega t - \phi) \tag{14.24}$$

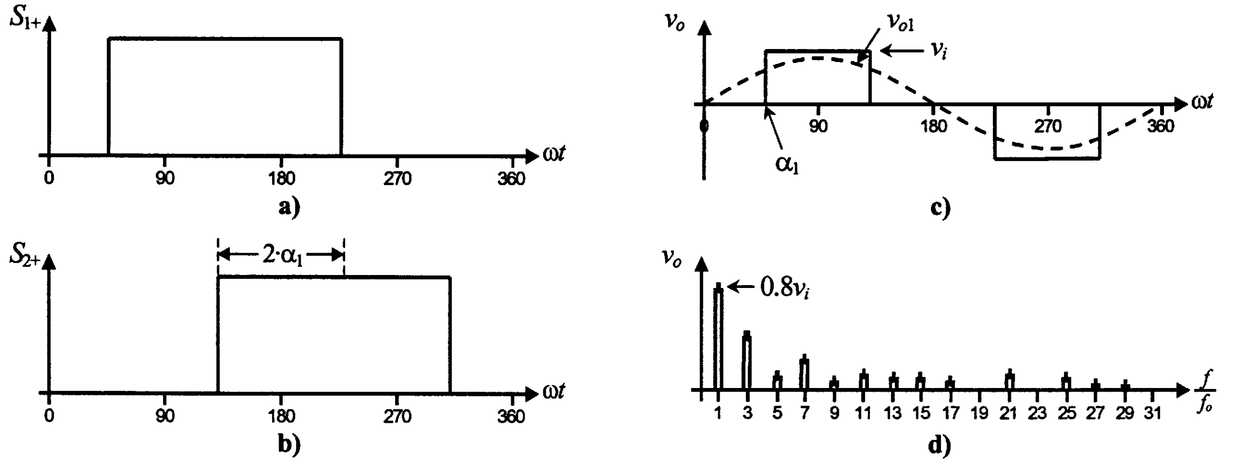


FIGURE 14.12 The full-bridge VSI. Ideal waveforms for the output control by voltage cancellation: (a) switch S_{1+} state; (b) switch S_{2+} state; (c) ac output voltage; (d) ac output voltage spectrum.

where V_{o1} is the fundamental rms ac output voltage, I_o is the rms load current, and ϕ is an arbitrary inductive load power factor. Thus, the dc link current can be further simplified to

$$i_i(t) = \frac{V_{o1}}{V_i} I_o \cos(\phi) - \frac{V_{o1}}{V_i} I_o \cos(2\omega t - \phi) \tag{14.25}$$

The preceding expression reveals an important issue, that is, the presence of a large second-order harmonic in the dc link current (its amplitude is similar to the dc link current). This second harmonic is injected back into the dc voltage source, thus its design should consider it in order to guarantee a nearly constant dc link voltage. In practical terms, the dc voltage source is required to feature large amounts of capacitance, which is costly and demands space, both undesirable features, especially in medium- to high-power supplies.

14.3 Three-Phase Voltage Source Inverters

Single-phase VSIs cover low-range power applications and three-phase VSIs cover the medium- to high-power applications. The main purpose of these topologies is to provide a three-phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable. Although most of the applications require sinusoidal voltage waveforms (e.g., ASDs, UPSs, FACTS, var compensators), arbitrary voltages are also required in some emerging applications (e.g., active filters, voltage compensators).

The standard three-phase VSI topology is shown in Fig. 14.13 and the eight valid switch states are given in Table 14.3. As in single-phase VSIs, the switches of any leg of the inverter (S_1 and S_4, S_3 and S_6, or S_5 and S_2) cannot be switched on simultaneously because this would result in a short circuit across the dc link voltage supply. Similarly, in order to avoid undefined states in the VSI, and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously as this will result in voltages that will depend upon the respective line current polarity.

Of the eight valid states, two of them (7 and 8 in Table 14.3) produce zero ac line voltages. In this case, the ac line currents freewheel through either the upper or lower components. The remaining states (1 to 6 in Table 14.3) produce nonzero ac output voltages. In order to generate a given voltage waveform, the inverter moves from one state to another. Thus the resulting ac output line voltages consist of discrete values of voltages that are v_i, 0, and $-v_i$ for the topology shown in Fig. 14.13. The selection of the states in order to generate the given waveform is done by the modulating technique that should ensure the use of only the valid states.

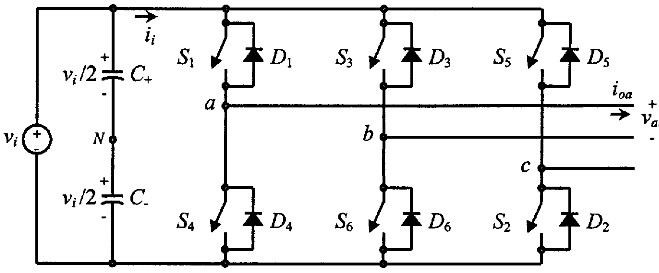


FIGURE 14.13 Three-phase VSI topology.

14.3.1 Sinusoidal PWM

This is an extension of the one introduced for single-phase VSIs. In this case and in order to produce 120° out-of-phase load voltages, three modulating signals that are 120° out of phase are used. Figure 14.14 shows the ideal waveforms of three-phase VSI SPWM. In order to use a single carrier signal and preserve the features of the PWM technique, the normalized carrier frequency m_f should be an odd multiple of 3. Thus, all phase voltages (v_{aN}, v_{bN}, and v_{cN}) are identical but 120° out of phase without even harmonics; moreover, harmonics at frequencies a multiple of 3 are identical in amplitude and phase in all phases. For instance, if the ninth harmonic in phase aN is

$$v_{aN9}(t) = \hat{v}_9 \sin(9\omega t) \tag{14.26}$$

the ninth harmonic in phase bN will be

$$\begin{aligned} v_{bN9}(t) &= \hat{v}_9 \sin(9(\omega t - 120^\circ)) \\ &= \hat{v}_9 \sin(9\omega t - 1080^\circ) \\ &= \hat{v}_9 \sin(9\omega t) \end{aligned} \tag{14.27}$$

TABLE 14.3 Valild switch states for a three-phase VSI

State	State	v_{ab}	v_{bc}	v_{ca}	Space Vector
S_1, S_2, and S_6 are on and S_4, S_5, and S_3 are off	1	v_i	0	$-v_i$	$\mathbf{V}_1 = 1 + j0.577$
S_2, S_3, and S_1 are on and S_5, S_6, and S_4 are off	2	0	v_i	$-v_i$	$\mathbf{V}_2 = j1.155$
S_3, S_4, and S_2 are on and S_6, S_1, and S_5 are off	3	$-v_i$	v_i	0	$\mathbf{V}_3 = -1 + j0.577$
S_4, S_5, and S_3 are on and S_1, S_2, and S_6 are off	4	$-v_i$	0	v_i	$\mathbf{V}_4 = -1 - j0.577$
S_5, S_6, and S_4 are on and S_2, S_3, and S_1 are off	5	0	$-v_i$	v_i	$\mathbf{V}_5 = -j1.155$
S_6, S_1, and S_5 are on and S_3, S_4, and S_2 are off	6	v_i	$-v_i$	0	$\mathbf{V}_6 = 1 - j0.577$
S_1, S_3, and S_5 are on and S_4, S_6, and S_2 are off	7	0	0	0	$\mathbf{V}_7 = 0$
S_4, S_6, and S_2 are on and S_1, S_3, and S_5 are off	8	0	0	0	$\mathbf{V}_8 = 0$

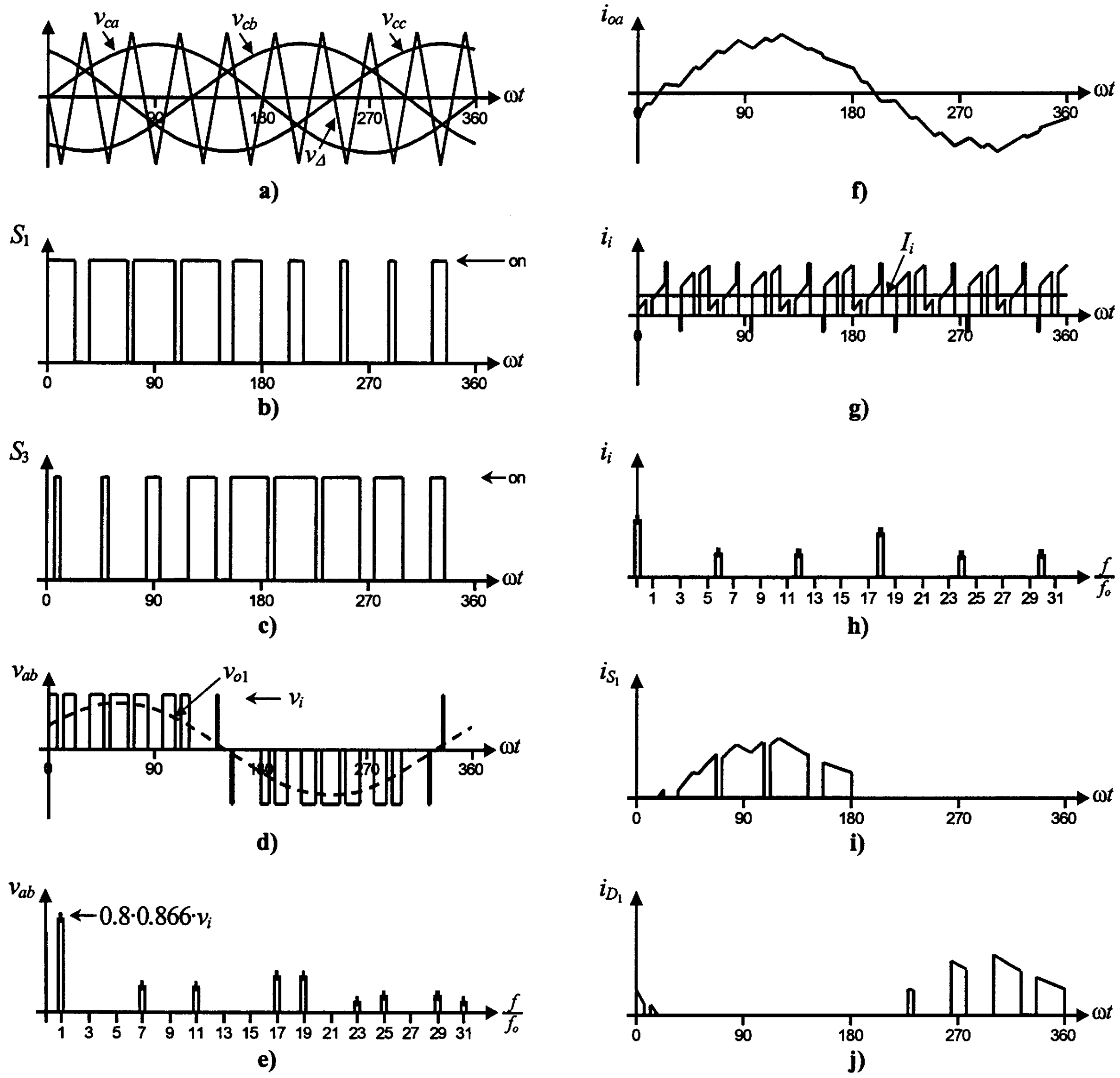


FIGURE 14.14 The three-phase VSI. Ideal waveforms for the SPWM ($m_a = 0.8$, $m_f = 9$): (a) carrier and modulating signals; (b) switch S_1 state; (c) switch S_3 state; (d) ac output voltage; (e) ac output voltage spectrum; (f) ac output current; (g) dc current; (h) dc current spectrum; (i) switch S_1 current; (j) diode D_1 current.

Thus, the ac output line voltage $v_{ab} = v_{aN} - v_{bN}$ will not contain the ninth harmonic. Therefore, for odd multiple of 3 values of the normalized carrier frequency m_f, the harmonics in the ac output voltage appear at normalized frequencies f_h centered around m_f and its multiples, specifically, at

$$h = lm_f \pm k \qquad l = 1, 2, \ldots \tag{14.28}$$

where $l = 1, 3, 5, \ldots$ for $k = 2, 4, 6, \ldots$, and $l = 2, 4, \ldots$ for $k = 1, 5, 7, \ldots$, such that h is not a multiple of 3. Therefore, the harmonics will be at $m_f \pm 2$, $m_f \pm 4, \ldots$, $2m_f \pm 1$, $2mf \pm 5, \ldots$, $3m_f \pm 2$, $3m_f \pm 4, \ldots$, $4m_f \pm 1$, $4m_f \pm 5, \ldots$.

For nearly sinusoidal ac load current, the harmonics in the dc link current are at frequencies given by

$$h = lm_f \pm k \pm 1 \qquad l = 1, 2, \ldots \tag{14.29}$$

where $l = 0, 2, 4, \ldots$ for $k = 1, 5, 7, \ldots$, and $l = 1, 3, 5, \ldots$ for $k = 2, 4, 6, \ldots$, such that $h = l \cdot m_f \pm k$ is positive and not a multiple of 3. For instance, Fig. 14.14h shows the sixth harmonic ($h = 6$), which is due to $h = 1 \cdot 9 - 2 - 1 = 6$.

The identical conclusions can be drawn for the operation at small and large values of m_f as for the single-phase configurations. However, because the maximum amplitude of the fundamental phase voltage in the linear region ($m_a \leq 1$) is

$v_i/2$, the maximum amplitude of the fundamental ac output line voltage is $\hat{v}_{ab1} = \sqrt{3}v_i/2$. Therefore, one can write

$$\hat{v}_{ab1} = m_a\sqrt{3}\frac{v_i}{2}, \qquad 0 < m_a \leq 1 \tag{14.30}$$

To further increase the amplitude of the load voltage, the amplitude of the modulating signal $\hat{v}_c$ can be made higher than the amplitude of the carrier signal $\hat{v}_\Delta$, which leads to overmodulation. The relationship between the amplitude of the fundamental ac output line voltage and the dc link voltage becomes nonlinear as in single-phase VSIs. Thus, in the overmodulation region, the line voltages range in

$$\sqrt{3}\frac{v_i}{2} < \hat{v}_{ab1} = \hat{v}_{bc1} = \hat{v}_{ca1} < \frac{4}{\pi}\sqrt{3}\frac{v_i}{2} \tag{14.31}$$

14.3.2 Square-Wave Operation of Three-Phase VSIs

Large values of m_a in the SPWM technique lead to full overmodulation. This is known as square-wave operation as illustrated in Fig. 14.15, where the power valves are on for 180°. In this operation mode, the VSI cannot control the load voltage except by means of the dc link voltage v_i. This is based on the fundamental ac line-voltage expression

$$\hat{v}_{ab1} = \frac{4}{\pi}\sqrt{3}\frac{v_i}{2} \tag{14.32}$$

The ac line output voltage contains the harmonics f_h, where $h = 6 \cdot k \pm 1$ $(k = 1, 2, 3, \ldots)$ and they feature amplitudes that are inversely proportional to their harmonic order (Fig. 14.15d). Their amplitudes are

$$\hat{v}_{abh} = \frac{1}{h}\frac{4}{\pi}\sqrt{3}\frac{v_i}{2} \tag{14.33}$$

14.3.3 Selective Harmonic Elimination in Three-Phase VSIs

As in single-phase VSIs, the SHE technique can be applied to three-phase VSIs. In this case, the power valves of each leg of the inverter are switched so as to eliminate a given number of harmonics and to control the fundamental phase-voltage amplitude. Considering that in many applications the required line output voltages should be balanced and 120° out of phase, the harmonics multiple of three $(h = 3, 9, 15, \ldots)$, which could be present in the phase voltages (v_{aN}, v_{bN}, and v_{cN}), will not be present in the load voltages (v_{ab}, v_{bc}, and v_{ca}). Therefore, these harmonics are not required to be eliminated, thus the chopping angles are used to eliminate only the harmonics at frequencies $h = 5, 7, 11, 13, \ldots$ as required.

The expressions to eliminate a given number of harmonics are the same as those used in single-phase inverters. For instance, to eliminate the fifth and seventh harmonics and perform fundamental magnitude control $(N = 3)$, the equations to be solved are

$$\begin{aligned} \cos(1\alpha_1) - \cos(1\alpha_2) + \cos(1\alpha_3) &= (2 + \pi\hat{v}_{aN1}/v_i)/4 \\ \cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) &= 1/2 \\ \cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) &= 1/2 \end{aligned} \tag{14.34}$$

where the angles α_1, α_2, and α_3 are defined as shown in Fig. 14.16a and plotted in Fig. 14.17. Figure 14.16b shows that the third, ninth, fifteenth, … harmonics are all present in the phase voltages; however, they are not in the line voltages (Fig. 14.16d).

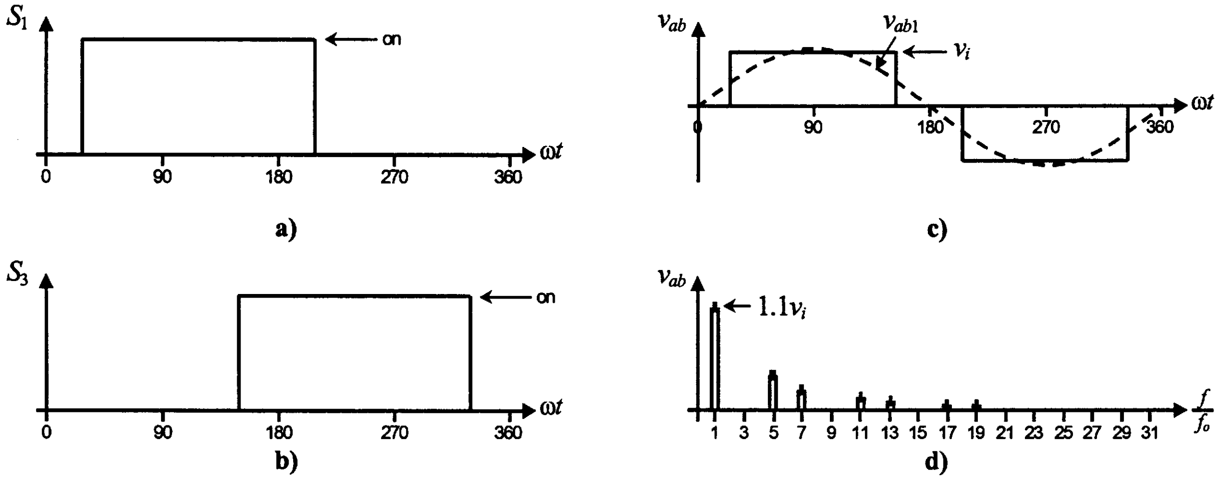


FIGURE 14.15 The three-phase VSI. Square-wave operation: (a) switch S_1 state; (b) switch S_3 state; (c) ac output voltage; (d) ac output voltage spectrum.

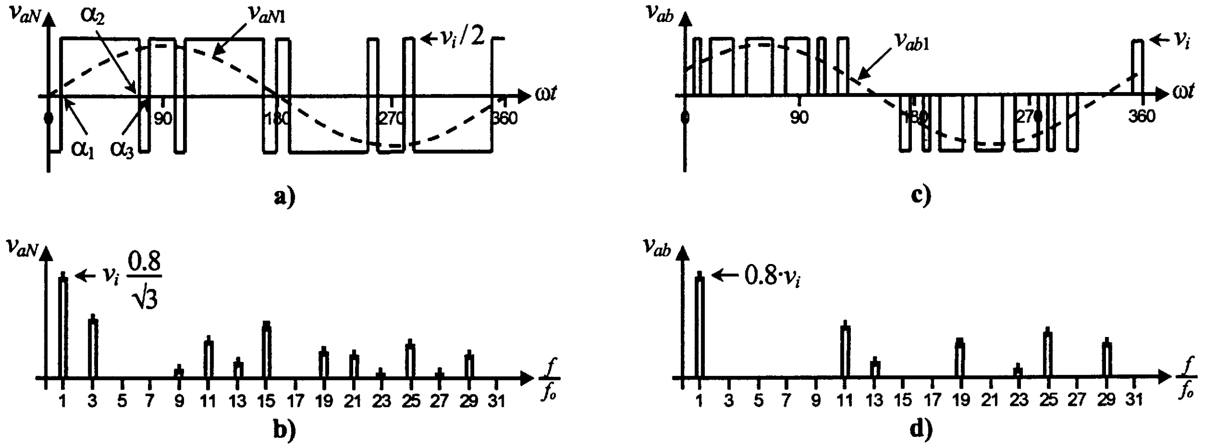


FIGURE 14.16 The three-phase VSI. Ideal waveforms for the SHE technique: (a) phase voltage v_{aN} for fifth and seventh harmonic elimination; (b) spectrum of (a); (c) line voltage v_{ab} for fifth and seventh harmonic elimination; (d) spectrum of (c).

14.3.4 Space-Vector-based Modulating Techniques

At present, the control strategies are implemented in digital systems, and therefore digital modulating techniques are also available. The SV-based modulating technique is a digital technique in which the objective is to generate PWM load line voltages that are on average equal to given load line voltages. This is done in each sampling period by properly selecting the switch states from the valid ones of the VSI (Table 14.3) and by proper calculation of the period of times they are used. The selection and calculation times are based upon the space-vector transformation.

14.3.4.1 Space-Vector Transformation

Any three-phase set of variables that add up to zero in the stationary *abc* frame can be represented in a complex plane by a complex vector that contains a real (α) and an imaginary (β) component. For instance, the vector of three-phase line-modulating signals $[v_c]_{\text{abc}} = [v_{ca} v_{cb} v_{cc}]^T$ can be represented by the complex vector $\mathbf{V_c} = [v_c]_{\alpha\beta} = [v_{c\alpha} v_{c\beta}]^T$ by means of the following transformation:

$$v_{c\alpha} = \frac{2}{3}[v_{ca} - 0.5(v_{cb} + v_{cc})] \qquad (14.35)$$

$$v_{c\beta} = \frac{\sqrt{3}}{3}(v_{cb} - v_{cc}) \qquad (14.36)$$

If the line-modulating signals $[v_c]_{\text{abc}}$ are three balanced sinusoidal waveforms that feature an amplitude $\hat{v}_c$ and an angular frequency ω, the resulting modulating signals in the $\alpha\beta$ stationary frame $\mathbf{V_c} = [v_c]_{\alpha\beta}$ become a vector of fixed module $\hat{v}_c$, which rotates at frequency ω (Fig. 14.18). Similarly, the SV transformation is applied to the line voltages of

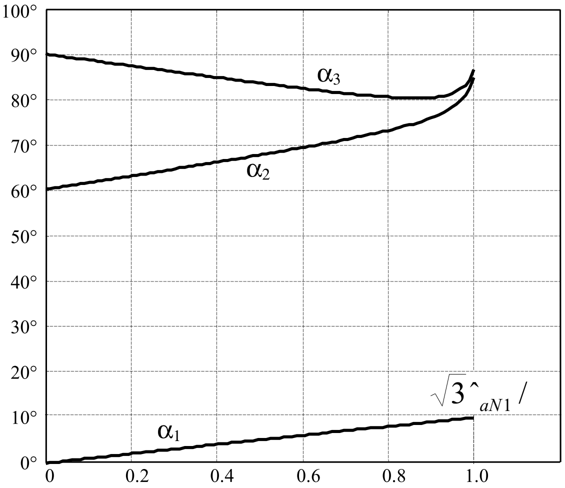


FIGURE 14.17 Chopping angles for SHE and fundamental voltage control in three-phase VSIs: fifth and seventh harmonic elimination.

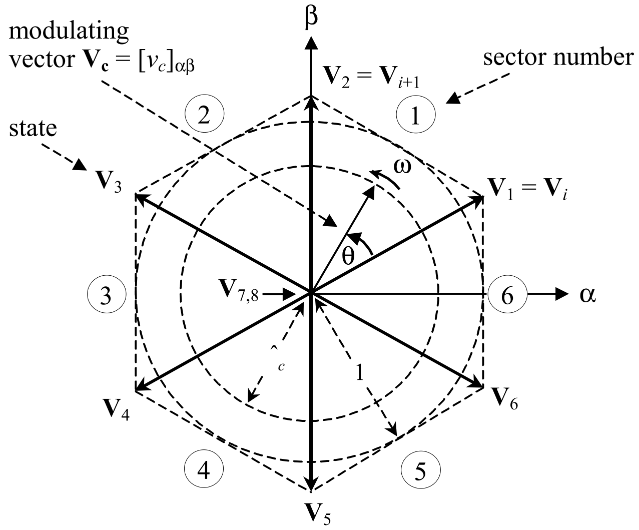


FIGURE 14.18 The space-vector representation.

the eight states of the VSI normalized with respect to v_i (Table 14.3), which generates the eight space vectors ($\mathbf{V}_i$, $i = 1, 2, \ldots, 8$) in Fig. 14.18. As expected, $\mathbf{V}_1$ to $\mathbf{V}_6$ are nonnull line voltage vectors and $\mathbf{V}_7$ and $\mathbf{V}_8$ are null line-voltage vectors.

The objective of the SV technique is to approximate the line-modulating signal space $\mathbf{V_c}$ with the eight space vectors ($\mathbf{V}_i$, $i = 1, 2, \ldots, 8$) available in VSIs. However, if the modulating signal $\mathbf{V_c}$ is laying between the arbitrary vectors $\mathbf{V}_i$ and $\mathbf{V}_{i+1}$, only the nearest two nonzero vectors ($\mathbf{V}_i$ and $\mathbf{V}_{i+1}$) and one zero SV ($\mathbf{V}_z = \mathbf{V}_7$ or $\mathbf{V}_8$) should be used. Thus, the maximum load line voltage is maximized and the switching frequency is minimized. To ensure that the generated voltage in one sampling period T_s (made up of the voltages provided by the vectors $\mathbf{V}_i$, $\mathbf{V}_{i+1}$, and $\mathbf{V}_z$ used during times T_i, T_{i+1}, and T_z) is on average equal to the vector $\mathbf{V_c}$, the following expression should hold:

$$\mathbf{V_c} \cdot T_s = \mathbf{V}_i \cdot T_i + \mathbf{V}_{i+1} \cdot T_{i+1} + \mathbf{V}_z \cdot T_z \tag{14.37}$$

The solution of the real and imaginary parts of Eq. (14.37) for a line-load voltage that features an amplitude restricted to $0 \leq \hat{v}_c \leq 1$ gives

$$T_i = T_s \cdot \hat{v}_c \cdot \sin(\pi/3 - \theta) \tag{14.38}$$

$$T_{i+1} = T_s \cdot \hat{v}_c \cdot \sin(\theta) \tag{14.39}$$

$$T_z = T_s - T_i - T_{i+1} \tag{14.40}$$

The preceding expressions indicate that the maximum fundamental line-voltage amplitude is unity as $0 \leq \theta \leq \pi/3$. This is an advantage over the SPWM technique which achieves a $\sqrt{3}/2$ maximum fundamental line-voltage amplitude in the linear operating region. Although, the SVM technique selects the vectors to be used and their respective on-times, the sequence in which they are used, the selection of the zero space vector, and the normalized sampled frequency remain undetermined.

For instance, if the modulating line-voltage vector is in sector 1 (Fig. 14.18), the vectors $\mathbf{V}_1$, $\mathbf{V}_2$, and $\mathbf{V}_z$ should be used within a sampling period by intervals given by T_1, T_2, and T_z, respectively. The question that remains is whether the sequence (i) $\mathbf{V}_1 - \mathbf{V}_2 - \mathbf{V}_z$, (ii) $\mathbf{V}_z - \mathbf{V}_1 - \mathbf{V}_2 - \mathbf{V}_z$, (iii) $\mathbf{V}_z - \mathbf{V}_1 - \mathbf{V}_2 - \mathbf{V}_1 - \mathbf{V}_z$, (iv) $\mathbf{V}_z - \mathbf{V}_1 - \mathbf{V}_2 - \mathbf{V}_z - \mathbf{V}_2 - \mathbf{V}_1 - \mathbf{V}_z$, or any other sequence should actually be used. Finally, the technique does not indicate whether $\mathbf{V}_z$ should be $\mathbf{V}_7$, $\mathbf{V}_8$, or a combination of both.

14.3.4.2 Space-Vector Sequences and Zero Space-Vector Selection

The sequence to be used should ensure load line voltages that feature quarter-wave symmetry in order to reduce unwanted harmonics in their spectra (even harmonics). Additionally, the zero SV selection should be done in order to reduce the switching frequency. Although there is not a systematic approach to generate a SV sequence, a graphical representation shows that the sequence $\mathbf{V}_i$, $\mathbf{V}_{i+1}$, $\mathbf{V}_z$ (where $\mathbf{V}_z$ is alternately chosen among $\mathbf{V}_7$ and $\mathbf{V}_8$) provides high performance in terms of minimizing unwanted harmonics and reducing the switching frequency.

14.3.4.3 The Normalized Sampling Frequency

The normalized carrier frequency m_f in three-phase carrier-based PWM techniques is chosen to be an odd integer number multiple of 3 ($m_f = 3 \cdot n$, $n = 1, 3, 5, \ldots$). Thus, it is possible to minimize parasitic or nonintrinsic harmonics in the PWM waveforms. A similar approach can be used in the SVM technique to minimize uncharacteristic harmonics. Hence, it is found that the normalized sampling frequency f_{sn} should be an integer multiple of 6. This is due to the fact that in order to produce symmetrical line voltages, all the sectors (a total of 6) should be used equally in one period. As an example, Fig. 14.19 shows the relevant waveforms of a VSI SVM for $f_{sn} = 18$ and $\hat{v}_c = 0.8$. Figure 14.19 confirms that the first set of relevant harmonics in the load line voltage are at f_{sn}, which is also the switching frequency.

14.3.5 DC Link Current in Three-Phase VSIs

Due to the fact that the inverter is assumed to be lossless and constructed without storage energy components, the instantaneous power balance indicates that

$$v_i(t) \cdot i_i(t) = v_{ab}(t) \cdot i_a(t) + v_{bc}(t) \cdot i_b(t) + v_{ca}(t) \cdot i_c(t) \tag{14.41}$$

where $i_a(t)$, $i_b(t)$, and $i_c(t)$ are the phase-load currents as shown in Fig. 14.20. If the load is balanced and inductive, and a relatively high switching frequency is used, the load currents become nearly sinusoidal balanced waveforms. On the other hand, if the ac output voltages are considered sinusoidal and the dc link voltage is assumed constant $v_i(t) = V_i$, Eq. (14.41) can be simplified to

$$i_i(t) = \frac{1}{V_i}\left\{\begin{array}{l} \sqrt{2}V_{o1}\sin(\omega t) \cdot \sqrt{2}I_o \sin(\omega t - \phi) \\ +\sqrt{2}V_{o1}\sin(\omega t - 120^\circ) \cdot \sqrt{2}I_o \sin(\omega t - 120^\circ - \phi) \\ +\sqrt{2}V_{o1}\sin(\omega t - 240^\circ) \cdot \sqrt{2}I_o \sin(\omega t - 240^\circ - \phi) \end{array}\right\} \tag{14.42}$$

where V_{o1} is the fundamental rms ac output line voltage, I_o is the rms load-phase current, and ϕ is an arbitrary inductive load power factor. Hence, the dc link current expression can be further simplified to

$$i_i(t) = 3\frac{V_{o1}}{V_i} I_o \cos(\phi) = \sqrt{3}\frac{V_{o1}}{V_i} I_l \cos(\phi) \tag{14.43}$$

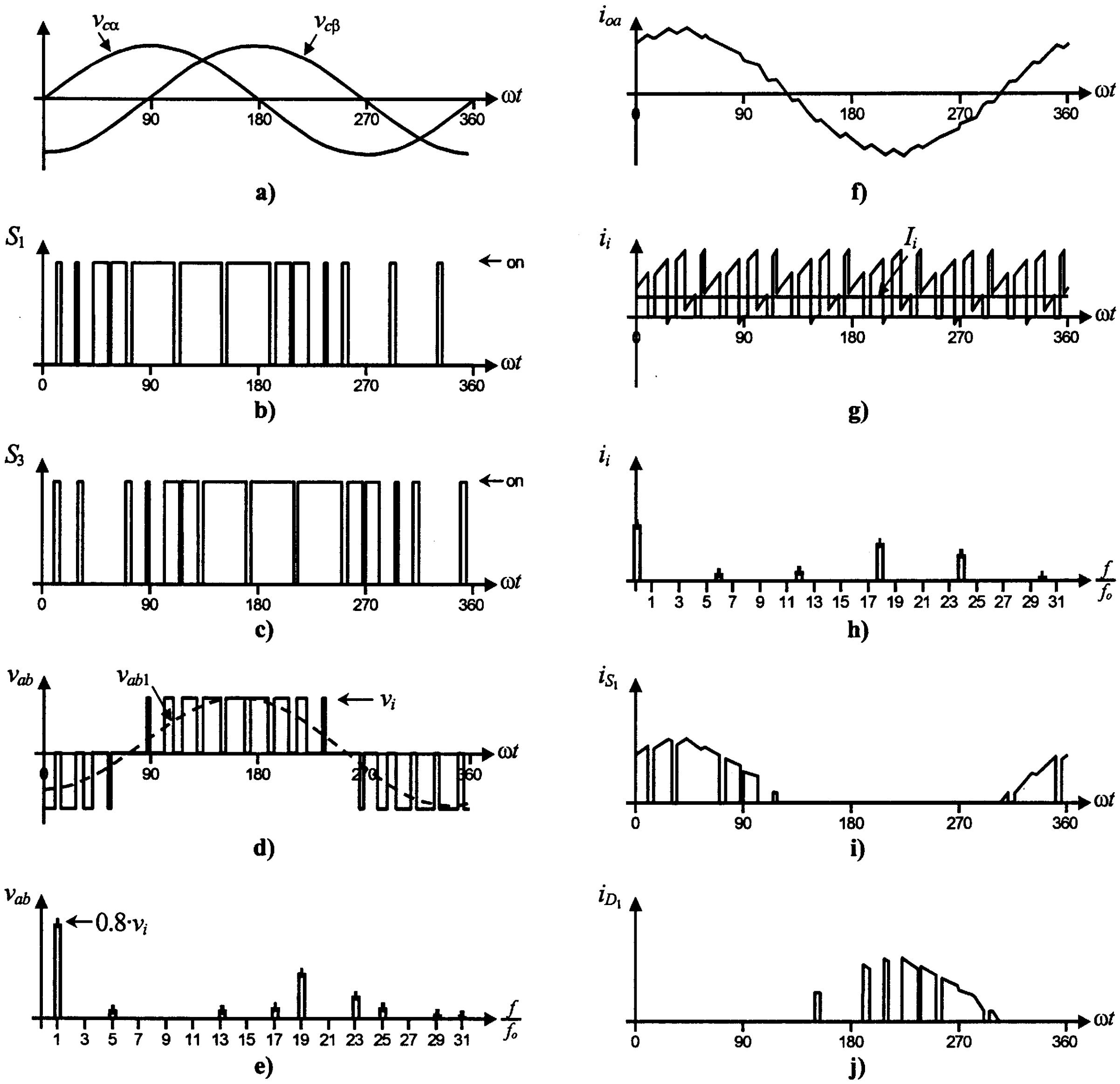


FIGURE 14.19 The three-phase VSI. Ideal waveforms for space-vector modulation ($\hat{v}_c = 0.8, f_{sn} = 18$): (a) modulating signals; (b) switch S_1 state; (c) switch S_3 state; (d) ac output voltage; (e) ac output voltage spectrum; (f) ac output current; (g) dc current; (h) dc current spectrum; (i) switch S_1 current; (j) diode D_1 current.

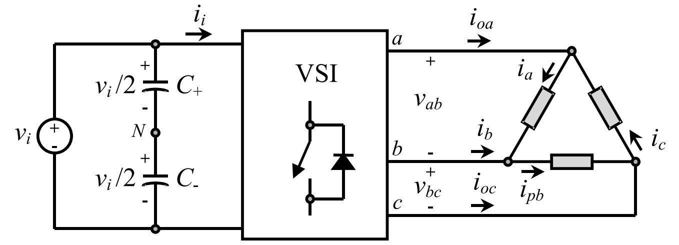


FIGURE 14.20 Phase-load currents definition in a delta-connected load.

where $I_l = \sqrt{I_o}$ is the rms load line current. The resulting dc link current expression indicates that under harmonic-free load voltages, only a clean dc current should be expected in the dc bus and, compared to single-phase VSIs, there is no presence of second harmonic. However, as the ac load line voltages contain harmonics around the normalized sampling frequency f_{sn}, the dc link current will contain harmonics but around f_{sn} as shown in Fig. 14.19h.

14.3.6 Load-Phase Voltages in Three-Phase VSIs

The load is sometimes wye-connected and the phase-load voltages v_{an}, v_{bn}, and v_{cn} may be required (Fig. 14.21). To

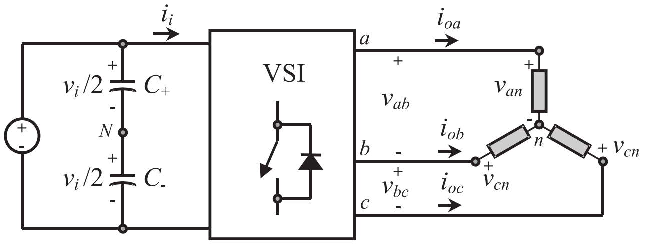


FIGURE 14.21 Phase-load voltages definition in a wye-connected load.

obtain them, it should be considered that the line-voltage vector is

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} v_{an} - v_{bn} \\ v_{bn} - v_{cn} \\ v_{cn} - v_{an} \end{bmatrix} \tag{14.44}$$

which can be written as a function of the phase-voltage vector $[v_{an}\ v_{bn}\ v_{cn}]^T$ as,

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{14.45}$$

Expression (14.45) represents a linear system where the unknown quantity is the vector $[v_{an}\ v_{bn}\ v_{cn}]^T$. Unfortunately, the system is singular as the rows add up to zero (line voltages add up to zero), therefore, the phase-load voltages cannot be obtained by matrix inversion. However, if the phase-load voltages add up to zero, Eq. (14.45) can be rewritten as

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{14.46}$$

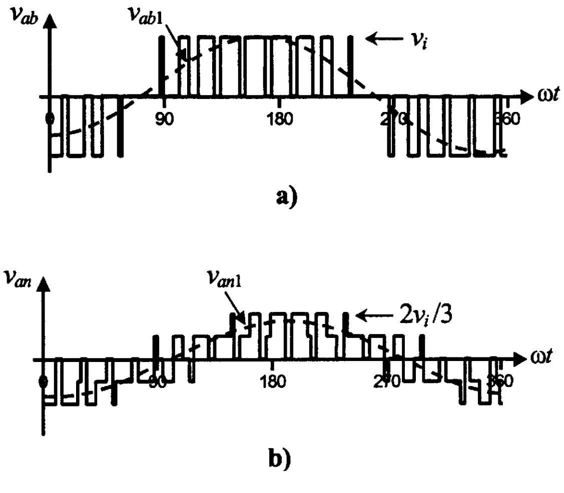


FIGURE 14.22 The three-phase VSI. Line- and phase-load voltages: (a) line-load voltage v_{ab}; (b) phase-load voltage v_{an}.

which is not singular and hence

$$\begin{aligned} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} &= \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_{ab} \\ v_{bc} \\ 0 \end{bmatrix} \\ &= \frac{1}{3} \begin{bmatrix} 2 & 1 & 1 \\ -1 & 1 & 1 \\ -1 & -2 & 1 \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \\ 0 \end{bmatrix} \end{aligned} \tag{14.47}$$

that can be further simplified to

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & 1 \\ -1 & 1 \\ -1 & -2 \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \end{bmatrix} \tag{14.48}$$

The final expression for the phase-load voltages is only a function of v_{ab} and v_{bc}, which is due to fact that the last row in Eq. (14.45) is chosen to be only ones. Figure 14.22 shows the line and phase-voltages obtained using Eq. (14.48).

14.4 Current Source Inverters

The main objective of these static power converters is to produce ac output current waveforms from a dc current power supply. For sinusoidal ac outputs, its magnitude, frequency, and phase should be controllable. Due to the fact that the ac line currents i_{oa}, i_{ob}, and i_{oc} (Fig. 14.23) feature high di/dt, a capacitive filter should be connected at the ac terminals in inductive load applications (such as ASDs). Thus, nearly sinusoidal load voltages are generated that justifies the use of these topologies in medium-voltage industrial applications, where high-quality voltage waveforms are required. Although single-phase CSIs can in the same way as three-phase CSIs topologies be developed under similar principles, only three-phase applications are of practical use and are analyzed in the following.

In order to properly gate the power switches of a three-phase CSI, two main constraints must always be met: (a) the ac side is mainly capacitive, thus, it must not be short-circuited; this implies that, at most one top switch (1, 3, or 5 (Fig. 14.23)) and one bottom switch (4, 6, or 2 (Fig. 14.23))

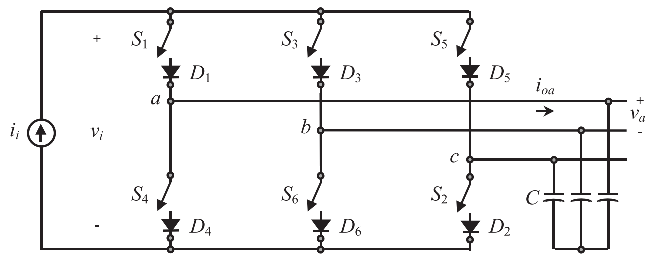


FIGURE 14.23 Three-phase CSI topology.

TABLE 14.4 Valid switch states for a three-phase CSI

State	State	i_{oa}	i_{ob}	i_{oc}	Space Vector
S_1 and S_2 are on and S_3, S_4, S_5, and S_6 are off	1	i_i	0	$-i_i$	$\mathbf{I}_1 = 1 + j0.577$
S_2 and S_3 are on and S_4, S_5, S_6, and S_1 are off	2	0	i_i	$-i_i$	$\mathbf{I}_2 = j1.155$
S_3 and S_4 are on and S_5, S_6, S_1, and S_2 are off	3	$-i_i$	i_i	0	$\mathbf{I}_3 = -1 + j0.577$
S_4 and S_5 are on and S_6, S_1, S_2, and S_3 are off	4	$-i_i$	0	i_i	$\mathbf{I}_4 = -1 - j0.577$
S_5 and S_6 are on and S_1, S_2, S_3, and S_4 are off	5	0	$-i_i$	i_i	$\mathbf{I}_5 = -j1.155$
S_6 and S_1 are on and S_2, S_3, S_4, and S_5 are off	6	i_i	$-i_i$	0	$\mathbf{I}_6 = 1 - j0.577$
S_1 and S_4 are on and S_2, S_3, S_5, and S_6 are off	7	0	0	0	$\mathbf{I}_7 = 0$
S_3 and S_6 are on and S_1, S_2, S_4, and S_5 are off	8	0	0	0	$\mathbf{I}_8 = 0$
S_5 and S_2 are on and S_6, S_1, S_3, and S_4 are off	9	0	0	0	$\mathbf{I}_9 = 0$

should be closed at any time; and (b) the dc bus is of the current-source type and thus it cannot be opened; therefore, there must be at least one top switch (1, 3, or 5) and one bottom switch (4, 6, or 2) closed at all times. Note that both constraints can be summarized by stating that at any time, only one top switch and one bottom switch must be closed.

There are nine valid states in three-phase CSIs. The states 7, 8, and 9 (Table 14.4) produce zero ac line currents. In this case, the dc link current freewheels through either the switches S_1 and S_4, switches S_3 and S_6, or switches S_5 and S_2. The remaining states (1 to 6 in Table 14.4) produce nonzero ac output line currents. In order to generate a given set of ac line current waveforms, the inverter must move from one state to another. Thus, the resulting line currents consist of discrete values of current, which are i_i, 0, and $-i_i$. The selection of the states in order to generate the given waveforms is done by the modulating technique that should ensure the use of only the valid states.

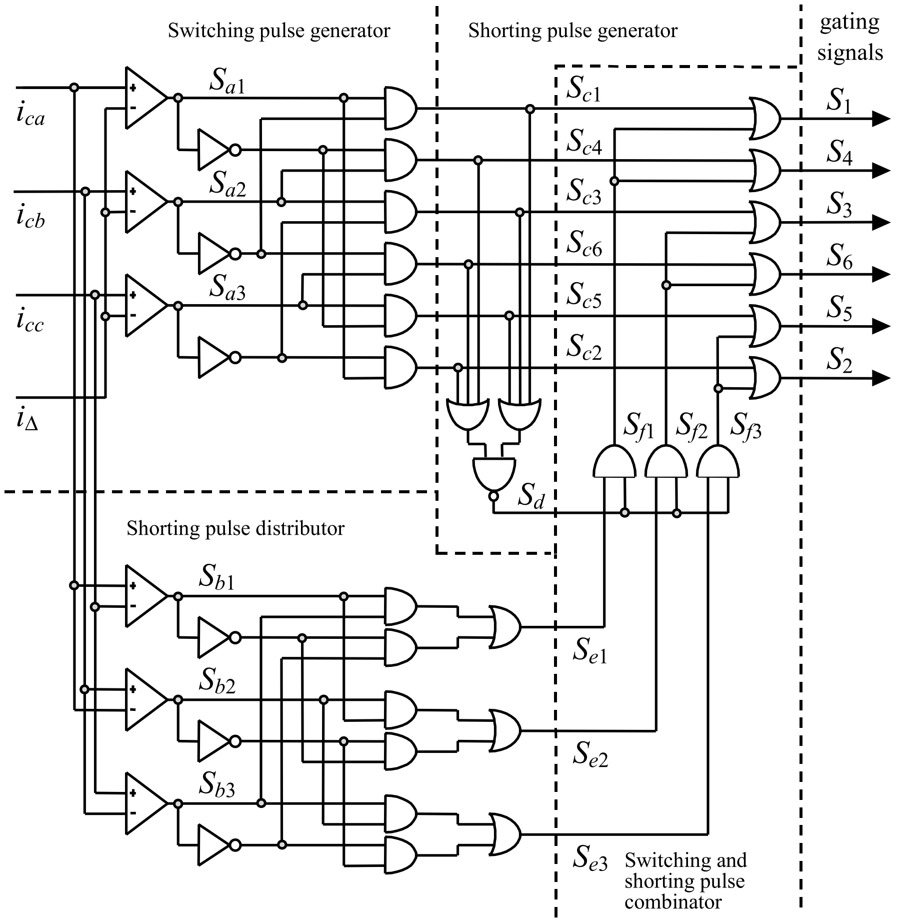

Switching pulse generator
Shorting pulse generator
gating signals
i_{ca}
i_{cb}
i_{cc}
i_{Δ}
S_{a1}
S_{a2}
S_{a3}
S_{c1}
S_{c4}
S_{c3}
S_{c6}
S_{c5}
S_{c2}
S_1
S_4
S_3
S_6
S_5
S_2
S_{f1}
S_{f2}
S_{f3}
S_d
Shorting pulse distributor
S_{b1}
S_{b2}
S_{b3}
S_{e1}
S_{e2}
S_{e3}
Switching and shorting pulse combinator

FIGURE 14.24 The three-phase CSI. Gating pattern generator for analog on-line carrier-based PWM.

There are several modulating techniques that deal with the special requirements of CSIs and can be implemented on line. These techniques are classified into three categories (a) the carrier, (b) the selective harmonic elimination, and (c) the space-vector-based techniques. Although they are different, they generate gating signals that satisfy the special requirements of CSIs. To simplify the analysis, a constant dc link current source is considered ($i_i = I_i$).

14.4.1 Carrier-based PWM Techniques in CSIs

It has been shown that carrier-based PWM techniques that were initially developed for three-phase VSIs can be extended to three-phase CSIs. The circuit shown in Fig. 14.24 obtains the gating pattern for a CSI from the gating pattern developed for a VSI. As a result, the line current appears to be identical to the line voltage in a VSI for similar carrier and modulating signals.

It is composed of a *switching pulse generator*, a *shorting pulse generator*, a *shorting pulse distributor*, and a *switching and shorting pulse combinator*. The circuit basically produces the gating signals ($[S]_{1\ldots6} = [S_1 \ldots S_6]^T$) according to a carrier i_Δ and three modulating signals $[i_c]_{\text{abc}} = [i_{ca}\ i_{cb}\ i_{ca}]^T$. Therefore, any set of modulating signals which when combined result in a sinusoidal line-to-line set of signals, will satisfy the requirement for a sinusoidal line current pattern. Examples of such a modulating signals are the standard sinusoidal, sinusoidal with third harmonic injection, trapezoidal, and deadband waveforms.

The first component of this stage (Fig. 14.24) is the *switching pulse generator*, where the signals $[S_a]_{123}$ are generated according to:

$$[S_a]_{123} = \begin{cases} \text{HIGH} = 1 & \text{if } [i_c]_{\text{abc}} > v_c \\ \text{LOW} \ = 0 & \text{otherwise} \end{cases} \tag{14.49}$$

The outputs of the *switching pulse generator* are the signals $[S_c]_{1\ldots6}$, which are basically the gating signals of the CSI without the shorting pulses. These are necessary to freewheel the dc link current i_i when zero ac output currents are required. Table 14.5 shows the truth table of $[S_c]_{1\ldots6}$ for all combinations of their inputs $[S_a[_{123}$. It can be clearly seen that at most one top switch and one bottom switch is on, which satisfies the first constraint of the gating signals as stated before.

In order to satisfy the second constraint, the shorting pulse ($S_d = 1$) is generated (*shorting pulse generator* (Fig. 14.24)) when none of the top switches ($S_{c1} = S_{c3} = S_{c5} = 0$) or none of the bottom switches ($S_{c4} = S_{c6} = S_{c2} = 0$) are gated. Then, this pulse is added (using OR gates) to only one leg of the CSI (either to the switches 1 and 4, 3 and 6, or 5 and 2) by means of the *switching and shorting pulse combinator* (Fig. 14.24). The signals generated by the *shorting pulse generator* $[S_e]_{123}$ ensure that: (a) only one leg of the CSI is shorted, as only one of the signals is high at any time; and (b) there is an even distribution of the shorting pulse, as $[S_e]_{123}$ is HIGH for 120° in each period. This ensures that the rms currents are equal in all legs.

TABLE 14.5 Truthtable for the switching pulse generator stage (Fig. 14.24)

			Top Switches			Bottom Switches		
S_{a1}	S_{a2}	S_{a3}	S_{c1}	S_{c3}	S_{c5}	S_{c4}	S_{c6}	S_{c2}
0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	1	0
0	1	0	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0
1	0	0	1	0	0	0	0	1
1	0	1	1	0	0	0	1	0
1	1	0	0	1	0	0	0	1
1	1	1	0	0	0	0	0	0

Figure 14.25 shows the relevant waveforms if a triangular carrier i_Δ and sinusoidal modulating signals $[i_c]_{\text{abc}}$ are used in combination with the gating pattern generator circuit (Fig. 14.24); this is SPWM in CSIs. It can be observed that some of the waveforms (Fig. 14.25) are identical to those obtained in three-phase VSIs, where a SPWM technique is used (Fig. 14.14). Specifically: (i) the load line voltage (Fig. 14.14d) in the VSI is identical to the load line current (Fig. 14.25d) in the CSI; and (ii) the dc link current (Fig. 14.14g) in the VSI is identical to the dc link voltage (Fig. 14.25g) in the CSI.

This brings up the duality issue between both topologies when similar modulation approaches are used. Therefore, for odd multiple of 3 values of the normalized carrier frequency m_f, the harmonics in the ac output current appear at normalized frequencies f_h centered around m_f and its multiples, specifically, at

$$h = lm_f \pm k \qquad l = 1, 2, \ldots \tag{14.50}$$

where $l = 1, 3, 5, \ldots$ for $k = 2, 4, 6, \ldots$ and $l = 2, 4, \ldots$ for $k = 1, 5, 7, \ldots$, such that h is not a multiple of 3. Therefore, the harmonics will be at $m_f \pm 2$, $m_f \pm 4, \ldots$, $2m_f \pm 1$, $2m_f \pm 5, \ldots$, $3m_f \pm 2$, $3m_f \pm 4, \ldots$, $4m_f \pm 1$, $4m_f \pm 5, \ldots$. For nearly sinusoidal ac load voltages, the harmonics in the dc link voltage are at frequencies given by

$$h = lm_f \pm k \pm 1 \qquad l = 1, 2, \ldots \tag{14.51}$$

where $l = 0, 2, 4, \ldots$ for $k = 1, 5, 7, \ldots$, and $l = 1, 3, 5, \ldots$ for $k = 2, 4, 6, \ldots$, such that $h = l \cdot m_f \pm k$ is positive and not a multiple of 3. For instance, Fig. 14.25h shows the sixth harmonic ($h = 6$), which is due to $h = 1 \cdot 9 - 2 - 1 = 6$. Identical conclusions can be drawn for the operation at small and large values of m_f in the same way as for three-phase VSI configurations. Thus, the maximum amplitude of

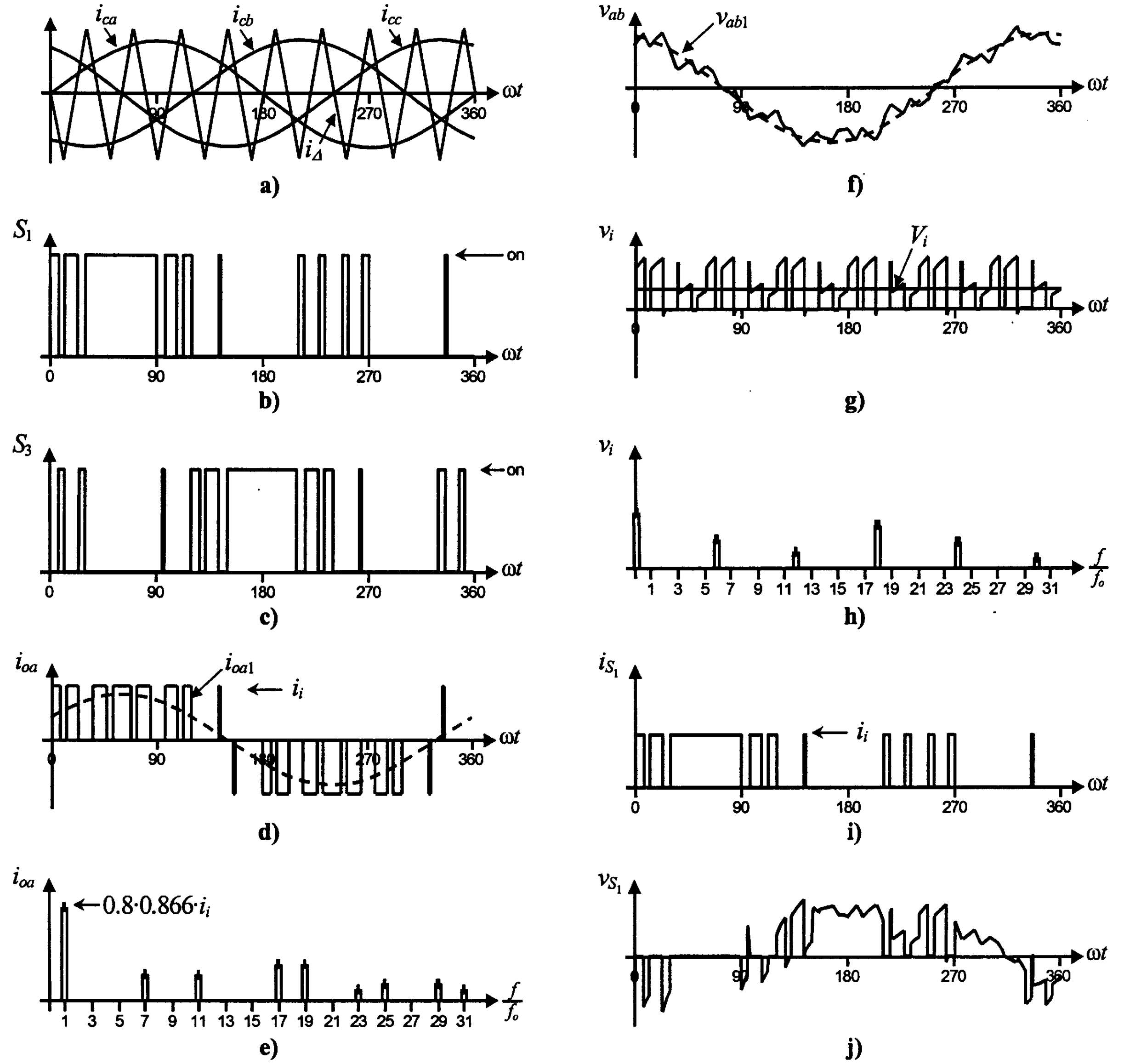


FIGURE 14.25 The three-phase CSI. Ideal waveforms for the SPWM ($m_a = 0.8$, $m_f = 9$): (a) carrier and modulating signals; (b) switch S_1 state; (c) switch S_3 state; (d) ac output current; (e) ac output current spectrum; (f) ac output voltage; (g) dc voltage; (h) dc voltage spectrum; (i) switch S_1 current; (j) Switch S_1 voltage.

the fundamental ac output line current is $\hat{i}_{oa1} = \sqrt{3}i_i/2$ and therefore one can write

$$\hat{i}_{oa1} = m_a \frac{\sqrt{3}}{2} i_i, \qquad 0 < m_a \leq 1 \tag{14.52}$$

To further increase the amplitude of the load current, the overmodulation approach can be used. In this region, the fundamental line currents range in

$$\frac{\sqrt{3}}{2} i_i < \hat{i}_{oa1} = \hat{i}_{ob1} = \hat{i}_{oc1} < \frac{4}{\pi} \frac{\sqrt{3}}{2} i_i. \tag{14.53}$$

To further test the gating signal generator circuit (Fig. 14.24), a sinusoidal set with third and ninth harmonic injection modulating signals are used. Figure 14.26 shows the relevant waveforms.

14.4.2 Square-Wave Operation of Three-Phase CSIs

As in VSIs, large values of m_a in the SPWM technique lead to full overmodulation. This is known as square-wave operation. Figure 14.27 depicts this operating mode in a three-phase CSI, where the power valves are on for 120°. As presumed, the CSI cannot control the load current except by means of the dc link

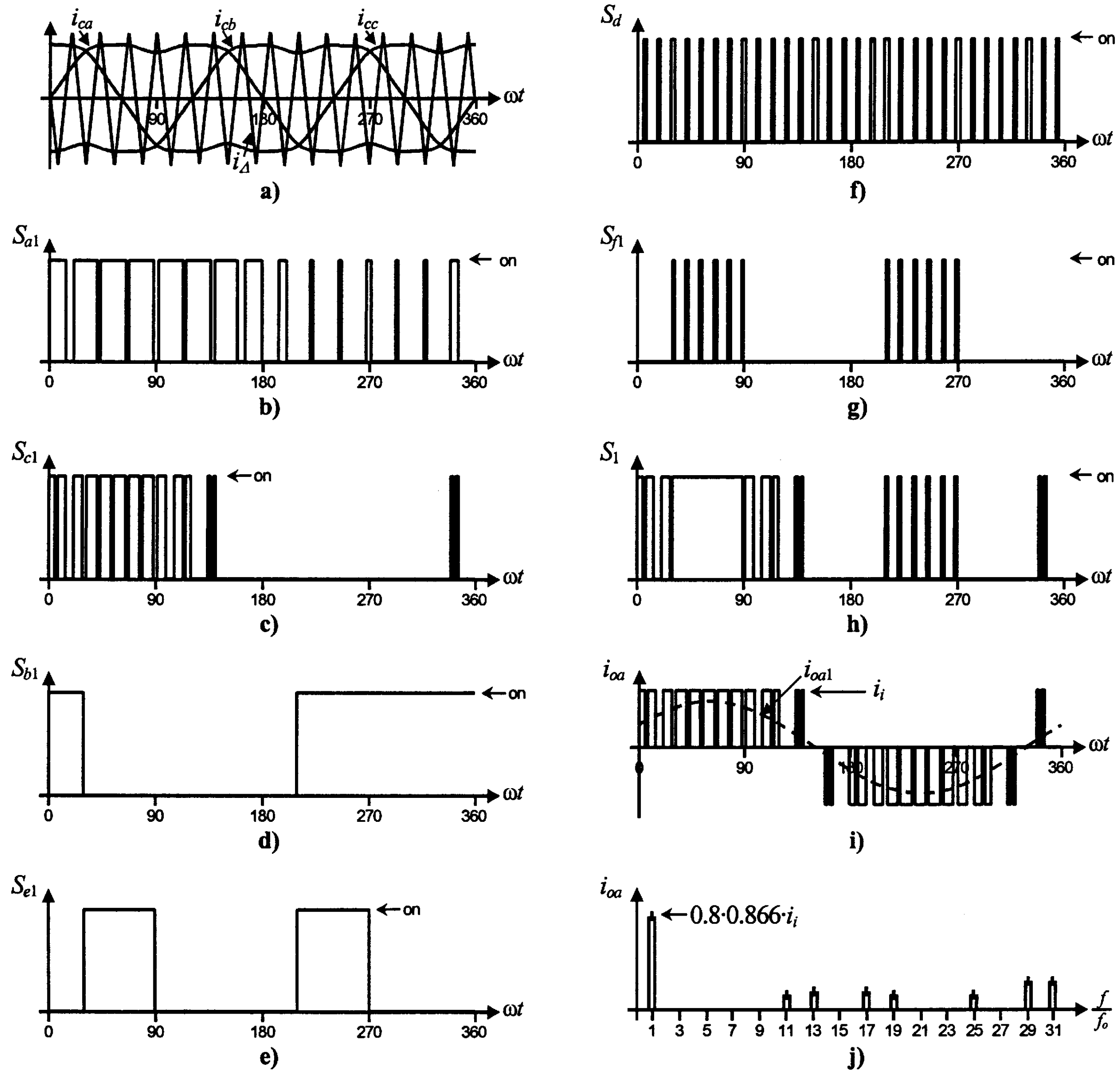


FIGURE 14.26 Gating pattern generator. Waveforms for third and ninth harmonic injection PWM ($m_a = 0.8$, $m_f = 15$): signals as described in Figure 14.24.

current i_i. This is due to the fact that the fundamental ac line current expression is

$$\hat{i}_{oa1} = \frac{4}{\pi}\frac{\sqrt{3}}{2} i_i \tag{14.54}$$

The ac line current contains the harmonics f_h, where $h = 6 \cdot k \pm 1$ $(k = 1, 2, 3, \ldots)$, and they feature amplitudes that are inversely proportional to their harmonic order (Fig. 14.27d). Thus,

$$\hat{i}_{oah} = \frac{1}{h}\frac{4}{\pi}\frac{\sqrt{3}}{2} i_i \tag{14.55}$$

The duality issue among both the three-phase VSI and CSI should be noted especially in terms of the line-load waveforms. The line-load voltage produced by a VSI is identical to the load line current produced by the CSI when both are modulated using identical techniques. The next section will show that this also holds for SHE-based techniques.

14.4.3 Selective armonic Elimination in Three-Phase CSIs

The SHE-based modulating techniques in VSIs define the gating signals such that a given number of harmonics are eliminated and the fundamental phase-voltage amplitude is

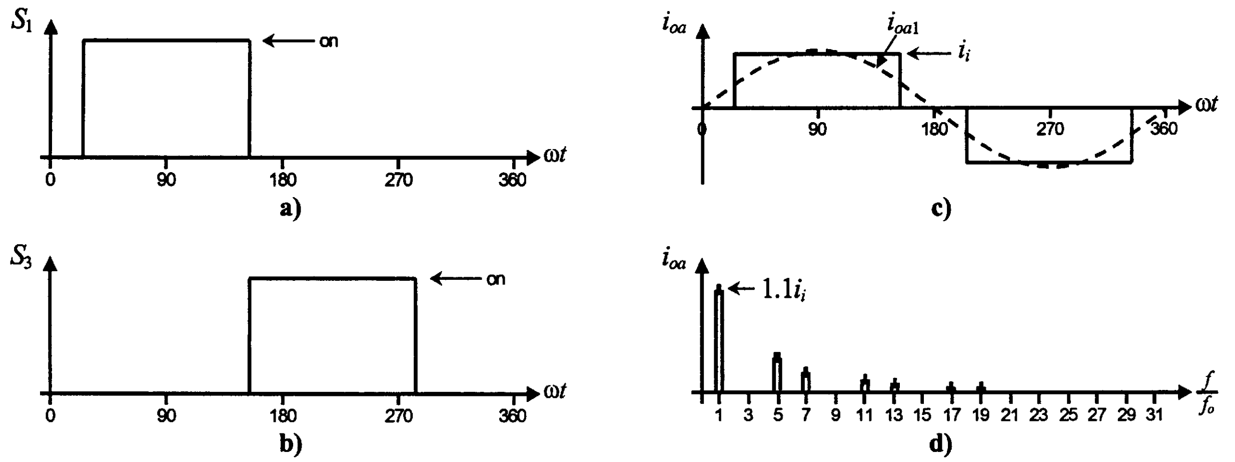


FIGURE 14.27 The three-phase CSI. Square-wave operation: (a) switch S_1 state; (b) switch S_3 state; (c) ac output current; (d) ac output current spectrum.

controlled. If the required line output voltages are balanced and 120° out of phase, the chopping angles are used to eliminate only the harmonics at frequencies $h = 5, 7, 11, 13, \ldots$ as required.

The circuit shown in Fig. 14.28 uses the gating signals $[S_a]_{123}$ developed for a VSI and a set of synchronizing signals $[i_c]_{\text{abc}}$ to obtain the gating signals $[S]_{1\ldots6}$ for a CSI. The synchronizing signals $[i_c]_{\text{abc}}$ are sinusoidal balanced waveforms that are

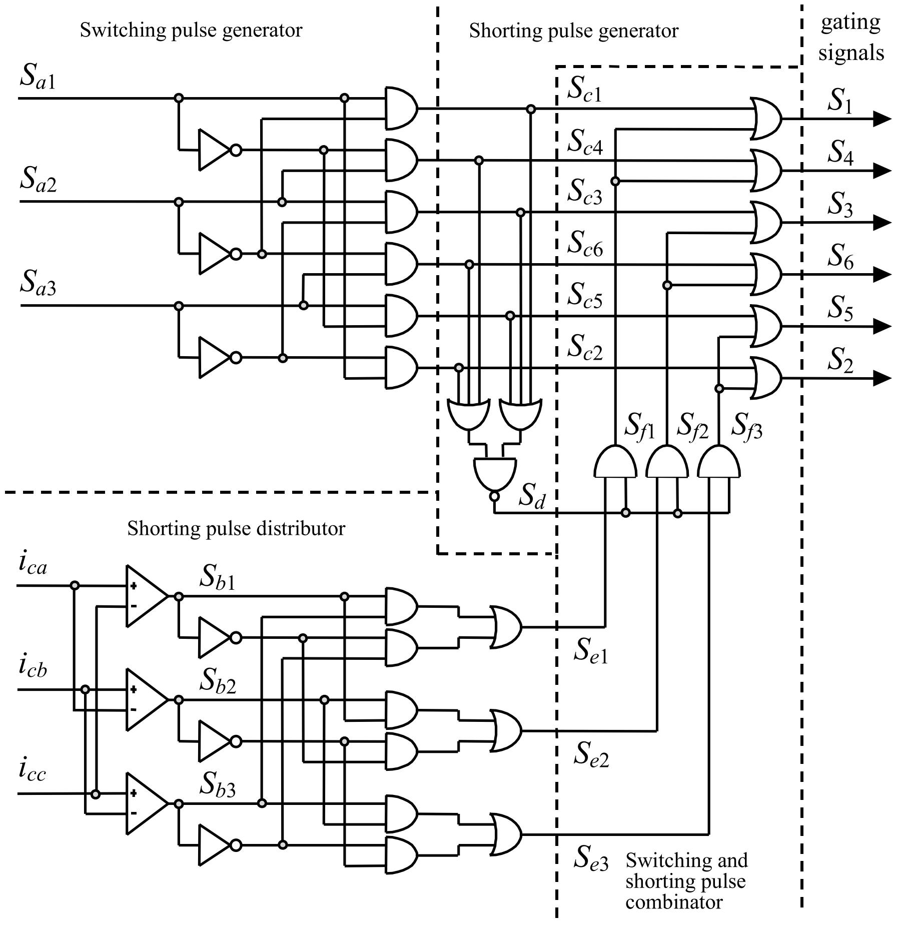

Switching pulse generator
Shorting pulse generator
gating signals
S_{a1}
S_{a2}
S_{a3}
S_{c1}
S_{c4}
S_{c3}
S_{c6}
S_{c5}
S_{c2}
S_1
S_4
S_3
S_6
S_5
S_2
S_{f1}
S_{f2}
S_{f3}
S_d
Shorting pulse distributor
i_{ca}
i_{cb}
i_{cc}
S_{b1}
S_{b2}
S_{b3}
S_{e1}
S_{e2}
S_{e3}
Switching and shorting pulse combinator

FIGURE 14.28 The three-phase CSI. Gating pattern generator for SHE PWM techniques.

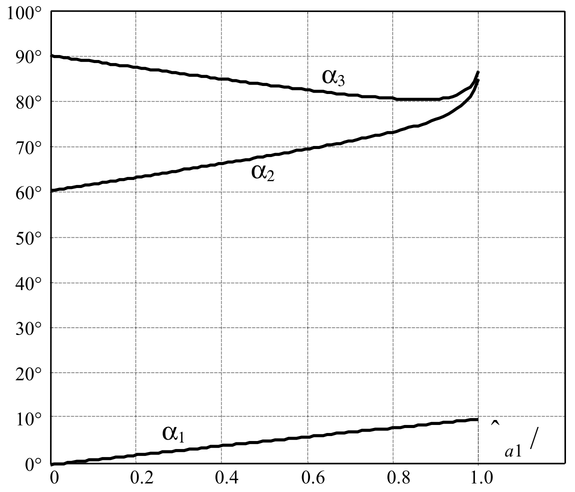


FIGURE 14.29 Chopping angles for SHE and fundamental current control in three-phase CSIs: fifth and seventh harmonic elimination.

synchronized with the signals $[S_a]_{123}$ in order to symmetrically distribute the shorting pulse and thus generate symmetrical gating patterns. The circuit ensures line current waveforms as the line voltages in a VSI. Therefore, any arbitrary number of harmonics can be eliminated and the fundamental line current can be controlled in CSIs. Moreover, the same chopping angles obtained for VSIs can be used in CSIs.

For instance, to eliminate the fifth and seventh harmonics, the chopping angles are shown in Fig. 14.29, which are identical to that obtained for a VSI using Eq. (14.9). Figure 14.30 shows that the line current does not contain the fifth and the seventh harmonics as expected. Hence, any number of harmonics can be eliminated in three-phase CSIs by means of the circuit (Fig. 14.28) without the hassle of how to satisfy the gating signal constrains.

14.4.4 Space-Vector-based Modulating Techniques in CSIs

The objective of the space vector (SV)-based modulating technique is to generate PWM load line currents that are on average equal to given load line currents. This is done digitally in each sampling period by properly selecting the switch states from the valid ones of the CSI (Table 14.4) and the proper calculation of the period of times they are used. As in VSIs, the selection and time calculations are based upon the space-vector transformation.

14.4.4.1 Space-Vector Transformation in CSIs

Similarly to VSIs, the vector of three-phase line-modulating signals $[i_c[_{\text{abc}}= [i_{ca}\ i_{cb}\ i_{cc}]^T$ can be represented by the complex vector $\mathbf{I_c} = [i_c]_{\alpha\beta} = [i_{c\alpha}\ i_{c\beta}]^T$ by means of Eqs. (14.35) and (14.36). For three-phase balanced sinusoidal modulating waveforms, which feature an amplitude $\hat{i}_c$ and an angular frequency ω, the resulting modulating signals complex vector $\mathbf{I_c} = [i_c]_{\alpha\beta}$ becomes a vector of fixed module $\hat{i}_c$, which rotates at frequency ω (Fig. 14.31). Similarly, the SV transformation is applied to the line currents of the nine states of the CSI normalized with respect to i_i, which generates nine space vectors ($\mathbf{I}_i$, $i = 1, 2, \ldots, 9$ in Fig. 14.31). As expected, $\mathbf{I}_1$ to $\mathbf{I}_6$ are nonnull line current vectors and $\mathbf{I}_7$, $\mathbf{I}_8$, and $\mathbf{I}_9$ are null line current vectors.

The SV technique approximates the line-modulating signal space vector $\mathbf{I_c}$ by using the nine space vectors ($\mathbf{I}_i$, $i = 1, 2, \ldots, 9$) available in CSIs. If the modulating signal vector $\mathbf{I_c}$ is between the arbitrary vectors $\mathbf{I}_i$ and $\mathbf{I}_{i+1}$, then $\mathbf{I}_i$ and $\mathbf{I}_{i+1}$ combined with one zero SV ($\mathbf{I}_z = \mathbf{I}_7$ or $\mathbf{I}_8$ or $\mathbf{I}_9$) should be used to generate $\mathbf{I_c}$. To ensure that the generated current in one sampling period T_s (made up of the currents provided by the vectors $\mathbf{I}_i$, $\mathbf{I}_{i+1}$, and $\mathbf{I}_z$ used during times T_i, T_{i+1}, and T_z)

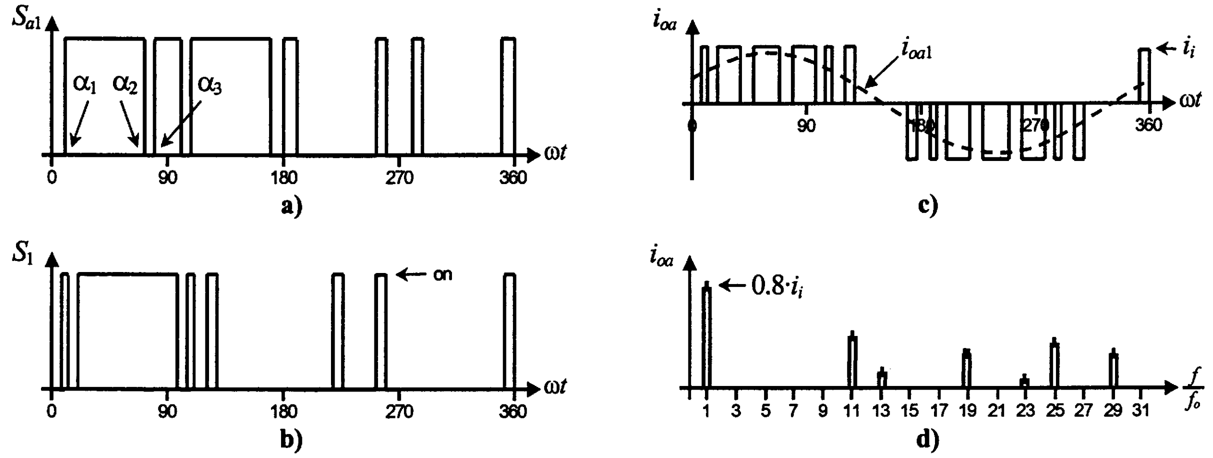


FIGURE 14.30 The three-phase CSI ideal waveforms for the SHE technique: (a) VSI gating pattern for fifth and seventh harmonic elimination; (b) CSI gating pattern for fifth and seventh harmonic elimination; (c) line current i_{oa} for fifth and seventh harmonic elimination; (d) spectrum of (c).

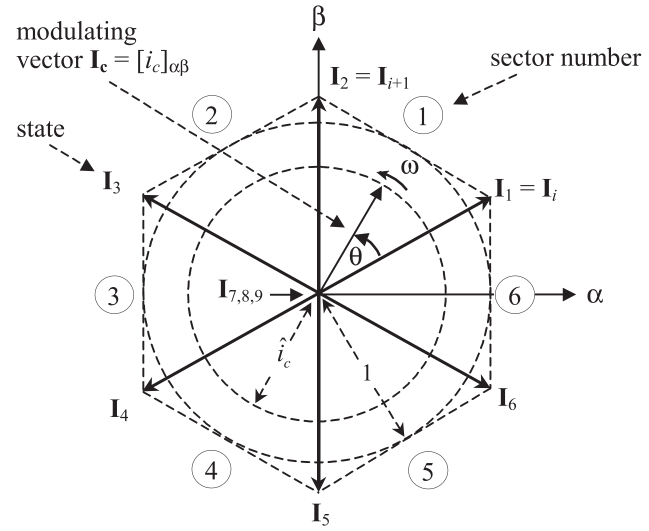

β
modulating vector $\mathbf{I_c} = [i_c]_{\alpha\beta}$
sector number
state
$\mathbf{I}_2 = \mathbf{I}_{i+1}$
$\mathbf{I}_1 = \mathbf{I}_i$
$\mathbf{I}_3$
$\mathbf{I}_4$
$\mathbf{I}_5$
$\mathbf{I}_6$
$\mathbf{I}_{7,8,9}$
ω
θ
$\hat{i}_c$
1
①
②
③
④
⑤
⑥
α

FIGURE 14.31 The space-vector representation in CSIs.

is on average equal to the vector $\mathbf{I_c}$, the following expressions should hold:

$$T_i = T_s \cdot \hat{i}_c \cdot \sin(\pi/3 - \theta) \tag{14.56}$$

$$T_{i+1} = T_s \cdot \hat{i}_c \cdot \sin(\theta) \tag{14.57}$$

$$T_z = T_s - T_i - T_{i+1} \tag{14.58}$$

where $0 \leq \hat{i}_c \leq 1$. Although, the SVM technique selects the vectors to be used and their respective on-times, the sequence in which they are used, the selection of the zero space vector, and the normalized sampled frequency remain undetermined.

14.4.4.2 Space-Vector Sequences and Zero Space-Vector Selection

Although there is no systematic approach to generate a SV sequence, a graphical representation shows that the sequence $\mathbf{I}_i$, $\mathbf{I}_{i+1}$, $\mathbf{I}_z$ (where the chosen $\mathbf{I}_z$ depends upon the sector) provides high performance in terms of minimizing unwanted harmonics and reducing the switching frequency. To obtain the zero SV that minimizes the switching frequency, it is assumed that $\mathbf{I_c}$ lays in Sector ②. Then Fig. 14.32 shows all the possible transitions that could be found in Sector 2. It can be seen that the zero vector $\mathbf{I_9}$ should be chosen to minimize the switching frequency. Table 14.6 gives a summary of the zero space vector to be used in each sector in order to minimize the switching frequency. However, it should be noted that Table 14.6 is valid only for the sequence $\mathbf{I}_i$, $\mathbf{I}_{i+1}$, $\mathbf{I}_z$. Another sequence will require reformulating the zero space-vector selection algorithm.

14.4.4.3 The Normalized Sampling Frequency

As in VSIs modulated by a space-vector approach, the normalized sampling frequency f_{sn} should be an integer multiple of 6 to minimize uncharacteristic harmonics. As an example, Fig. 14.33 shows the relevant waveforms of a CSI SVM for $f_{sn} = 18$ and $\hat{i}_c = 0.8$. Figure 14.33 also shows that the first set of relevant harmonics in the load line current are at f_{sn}.

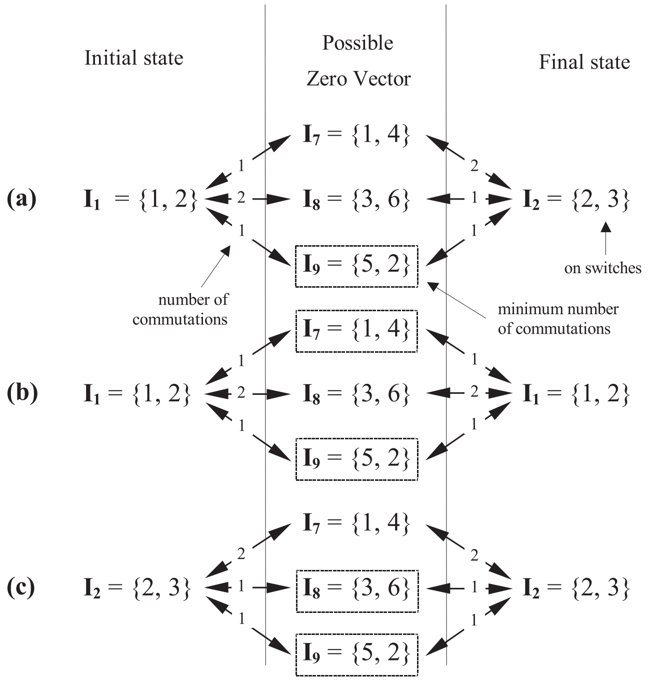

Initial state
Possible Zero Vector
Final state
(a)
$\mathbf{I}_1 = \{1, 2\}$
$\mathbf{I}_7 = \{1, 4\}$
$\mathbf{I}_8 = \{3, 6\}$
$\mathbf{I}_9 = \{5, 2\}$
$\mathbf{I}_2 = \{2, 3\}$
1
2
1
2
1
1
on switches
number of commutations
minimum number of commutations
(b)
$\mathbf{I}_1 = \{1, 2\}$
$\mathbf{I}_7 = \{1, 4\}$
$\mathbf{I}_8 = \{3, 6\}$
$\mathbf{I}_9 = \{5, 2\}$
$\mathbf{I}_1 = \{1, 2\}$
1
2
1
1
2
1
(c)
$\mathbf{I}_2 = \{2, 3\}$
$\mathbf{I}_7 = \{1, 4\}$
$\mathbf{I}_8 = \{3, 6\}$
$\mathbf{I}_9 = \{5, 2\}$
$\mathbf{I}_2 = \{2, 3\}$
2
1
1
2
1
1

FIGURE 14.32 Possible state transitions in Sector ② involving a zero SV. (a) Transition: $\mathbf{I}_1 \Leftrightarrow \mathbf{I}_z \Leftrightarrow \mathbf{I}_2$ or $\mathbf{I}_2 \Leftrightarrow \mathbf{I}_z \Leftrightarrow \mathbf{I}_1$; (b) transition: $\mathbf{I}_1 \Leftrightarrow \mathbf{I}_z \Leftrightarrow \mathbf{I}_1$; (c) transition: $\mathbf{I}_2 \Leftrightarrow \mathbf{I}_z \Leftrightarrow \mathbf{I}_2$.

14.4.5 DC Link Voltage in Three-Phase CSIs

An instantaneous power balance indicates that

$$v_i(t) \cdot i_i(t) = v_{an}(t) \cdot i_{oa}(t) + v_{bn}(t) \cdot i_{ob}(t) + v_{cn}(t) \cdot i_{oc}(t) \tag{14.59}$$

where $v_{an}(t)$, $v_{bn}(t)$, and $v_{cn}(t)$ are the phase filter voltages as shown in Fig. 14.34. If the filter is large enough and a relatively

TABLE 14.6 Zero SV for minimum switching frequency in CSI and sequence I_i, I_{i+1}, I_z

Sector	$\mathbf{I}_i$	$\mathbf{I}_{i+1}$	$\mathbf{I}_z$
1	$\mathbf{I}_6$	$\mathbf{I}_1$	$\mathbf{I}_7$
2	$\mathbf{I}_1$	$\mathbf{I}_2$	$\mathbf{I}_9$
3	$\mathbf{I}_2$	$\mathbf{I}_3$	$\mathbf{I}_8$
4	$\mathbf{I}_3$	$\mathbf{I}_4$	$\mathbf{I}_7$
5	$\mathbf{I}_4$	$\mathbf{I}_5$	$\mathbf{I}_9$
6	$\mathbf{I}_5$	$\mathbf{I}_6$	$\mathbf{I}_8$

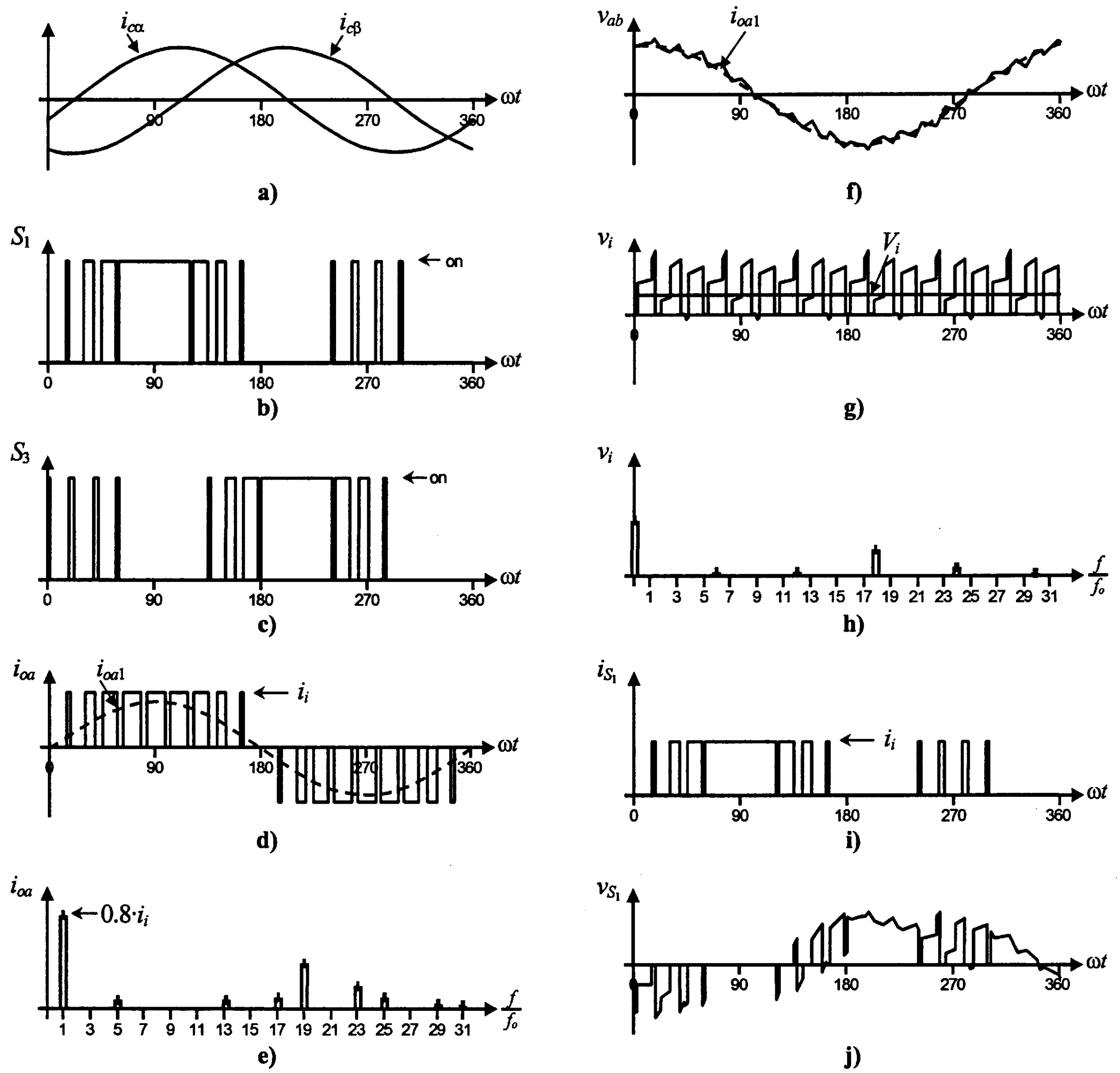


FIGURE 14.33 The three-phase CSI. Ideal waveforms for space-vector Modulation ($\hat{i}_c = 0.8, f_{sn} = 18$): (a) modulating signals; (b) switch S_1 state; (c) switch S_3 state; (d) ac output current; (e) ac output current spectrum; (f) ac output voltage; (g) dc voltage; (h) dc voltage spectrum; (i) switch S_1 current; (j) Switch S_1 voltage.

high switching frequency is used, the phase voltages become nearly sinusoidal balanced waveforms. On the other hand, if the ac output currents are considered sinusoidal and the dc link current is assumed constant $i_i(t) = I_i$, Eq. (14.59) can be simplified to

$$v_i(t) = \frac{1}{I_i}\left\{\begin{array}{l} \sqrt{2}V_{on}\sin(\omega t)\cdot\sqrt{2}I_{o1}\sin(\omega t-\phi) \\ +\sqrt{2}V_{on}\sin(\omega t-120^\circ)\cdot\sqrt{2}I_{o1}\sin(\omega t-120^\circ-\phi) \\ +\sqrt{2}V_{on}\sin(\omega t-240^\circ)\cdot\sqrt{2}I_{o1}\sin(\omega t-240^\circ-\phi) \end{array}\right\} \tag{14.60}$$

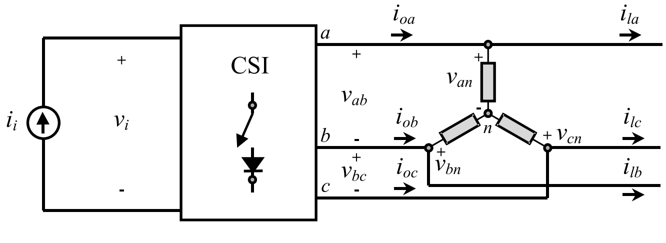


FIGURE 14.34 Phase voltage definition in a wye-connected filter.

where V_{on} is the rms ac output phase voltage, I_{o1} is the rms fundamental line current, and ϕ is an arbitrary filter-load angle. Hence, the dc link voltage expression can be further simplified to the following:

$$v_i(t) = 3\frac{I_{o1}}{I_i}V_{on}\cos(\phi) = \sqrt{3}\frac{I_{o1}}{I_i}V_o\cos(\phi) \tag{14.61}$$

where $V_o = \sqrt{3}V_{on}$ is the rms load line voltage. The resulting dc link voltage expression indicates that the first line-current harmonic I_{o1} generates a clean dc current. However, as the load line currents contain harmonics around the normalized sampling frequency f_{sn}, the dc link current will contain harmonics but around f_{sn} as shown in Fig. 14.33h. Similarly, in carrier-based PWM techniques, the dc link current will contain harmonics around the carrier frequency m_f (Fig. 14.25).

In practical implementations, a CSI requires a dc current source that should behave as a constant (as required by PWM CSIs) or variable (as square-wave CSIs) current source. Such current sources should be implemented as separate units and they are described earlier in this book.

14.5 Closed-Loop Operation of Inverters

Inverters generate variable ac waveforms from a dc power supply to feed, for instance, ASDs. As the load conditions usually change, the ac waveforms should be adjusted to these new conditions. Also, as the dc power supplies are not ideal and the dc quantities are not fixed, the inverter should compensate for such variations. Such adjustments can be done automatically by means of a closed-loop approach. Inverters also provide an alternative to changing the load operating conditions (i.e., speed in an ASD).

There are two alternatives for closed-loop operation the feedback and the feedforward approaches. It is known that the feedback approach can compensate for both perturbations (dc power variations) and load variations (load torque changes). However, the feedforward strategy is more effective in mitigating perturbations as it prevents its negative effects at the load side. These cause-effect issues are analyzed in three-phase inverters in the following, although similar results are obtained for single-phase VSIs.

14.5.1 Feedforward Techniques in Voltage Source Inverters

The dc link bus voltage in VSIs is usually considered a constant voltage source v_i. Unfortunately, and due to the fact that most practical applications generate the dc bus voltage by means of a diode rectifier (Fig. 14.35), the dc bus voltage contains low-order harmonics such as the sixth, twelfth,... (due to six-pulse diode rectifiers), and the second if the ac voltage supply features an unbalance, which is usually the case. Additionally, if the three-phase load is unbalanced, as in UPS applications, the dc input current in the inverter i_i also contains the second harmonic, which in turn contributes to the generation of a second voltage harmonic in the dc bus.

The basic principle of feedforward approaches is to sense the perturbation and then modify the input in order to compensate for its effect. In this case, the dc link voltage should be sensed and the modulating technique should accordingly be modified. The fundamental ab line voltage in a VSI SPWM can be written as

$$v_{ab1}(t) = \left\{\frac{v_{ca1}(t)}{\hat{v}_\Delta} - \frac{v_{cb1}(t)}{\hat{v}_\Delta}\right\}\frac{\sqrt{3}}{2}v_i(t), \qquad \hat{v}_\Delta > \hat{v}_{ca1}, \hat{v}_{cb1} \tag{14.62}$$

where $\hat{v}_\Delta$ is the carrier signal peak, $\hat{v}_{ca1}$ and $\hat{v}_{cb1}$ are the modulating signal peaks, and $v_{ca}(t)$ and $v_{cb}(t)$ are the modulating signals. If the dc bus voltage v_i varies around a nominal V_i value, then the fundamental line voltage varies proportionally; however, if the carrier signal peak $\hat{v}_\Delta$ is redefined as

$$\hat{v}_\Delta = \hat{v}_{\Delta m}\frac{v_i(t)}{V_i} \tag{14.63}$$

where $\hat{v}_{\Delta m}$ is the carrier signal peak (Fig. 14.36), then the resulting fundamental ab line voltage in a VSI SPWM is

$$v_{ab1}(t) = \left\{\frac{v_{ca1}(t)}{\hat{v}_{\Delta m}} - \frac{v_{cb1}(t)}{\hat{v}_{\Delta m}}\right\}\frac{\sqrt{3}}{2}V_i \tag{14.64}$$

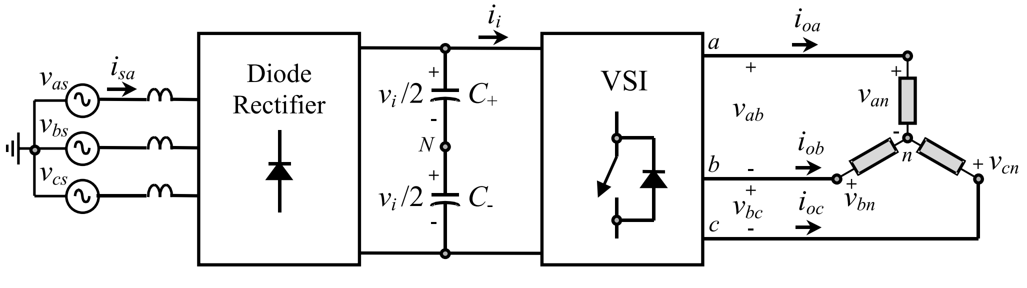


FIGURE 14.35 Three-phase topology with a diode-based front-end rectifier.

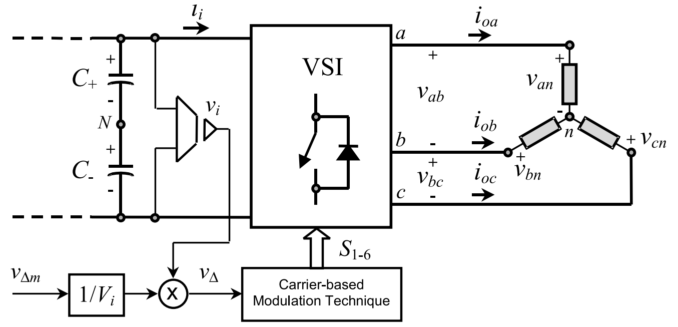


FIGURE 14.36 The three-phase VSI. Feedforward control technique to reject dc bus voltage variations.

where clearly the result does not depend upon the variations of the dc bus voltage.

Fig. 14.37 shows the waveforms generated by the SPWM under a severe dc bus voltage variation (a second harmonic has been added manually to a constant V_i). As a consequence, the ac line voltage generated by the VSI is distorted as it contains low-order harmonics (Fig. 14.37e). These operating conditions may not be acceptable in standard applications such as ASDs because the load will draw distorted three-phase currents as well. The feedforward loop performance is illustrated in Fig. 14.38. As expected, the carrier signal is modified so as to compensate for the dc bus voltage variation (Fig. 14.38b). This is probed by the spectrum of the ac line voltage that does not contain low-order harmonics (Fig. 14.38e). It should be noted that $\hat{v}_\Delta > \hat{v}_{ca1}, \hat{v}_{cb1}$; therefore, the compensation capabilities are limited by the required ac line voltage.

The performance of the feedforward approach depends upon the frequency of the harmonics present in the dc bus voltage and the carrier signal frequency. Fortunately, the relevant unwanted harmonics to be found in the dc bus voltage are the second due to unbalanced supply voltages, and/or the sixth as the dc bus voltage is generated by means of a six-pulse diode rectifier. Therefore, a carrier signal featuring a 15-pu frequency is found to be sufficient to properly compensate for dc bus voltage variations.

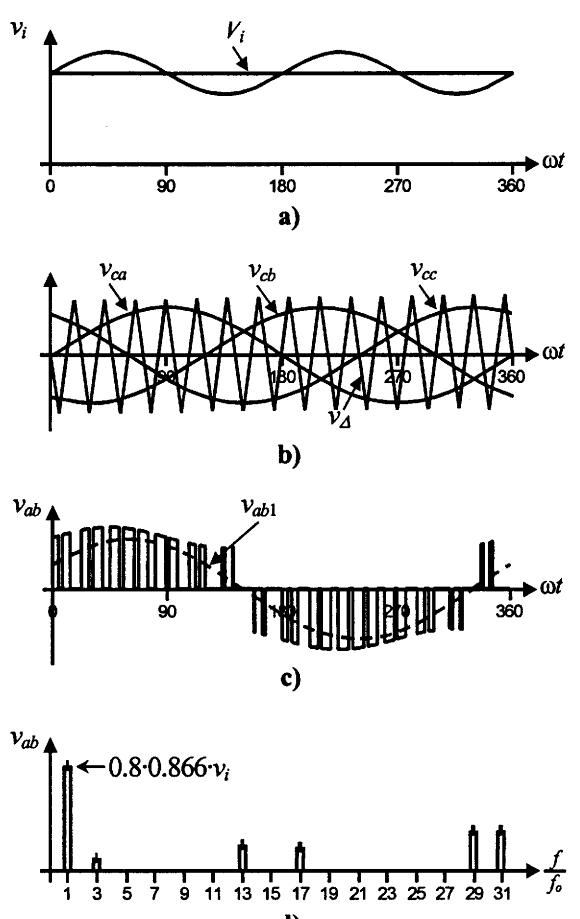


FIGURE 14.37 The three-phase VSI. Ideal waveforms for regular SPWM ($m_a = 0.8$, $m_f = 9$): (a) dc bus voltage; (b) carrier and modulating signals; (c) ac output voltage; (d) ac output voltage spectrum.

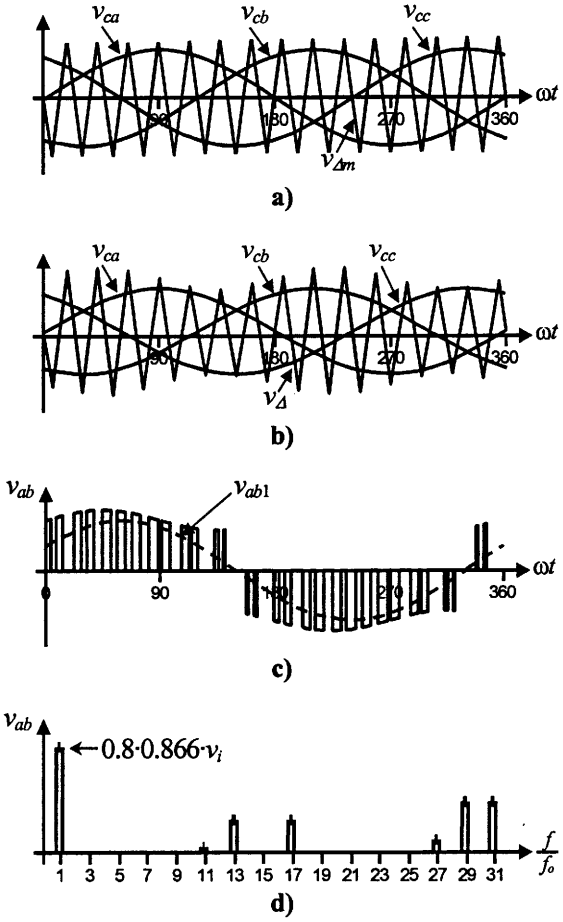


FIGURE 14.38 The three-phase VSI. Ideal waveforms for SPWM including a feedforward loop ($m_a = 0.8$, $m_f = 9$): (a) carrier and modulating signals; (b) Modified carrier and modulating signals; (c) ac output voltage; (d) ac output voltage spectrum.

Unbalanced loads generate a dc input current i_i that contains a second harmonic, which contributes to the dc bus voltage variation. The previous feedforward approach can compensate for such perturbation and maintain balanced ac load voltages.

Digital techniques can also be modified in order to compensate for dc bus voltage variations by means of a feedforward approach. For instance, the SVM techniques indicate that the on-times of the vectors $\mathbf{V}_i$, $\mathbf{V}_{i+1}$, and $\mathbf{V}_z$ are

$$T_i = T_s \cdot \hat{v}_c \cdot \sin(\pi/3 - \theta) \tag{14.65}$$

$$T_{i+1} = T_s \cdot \hat{v}_c \cdot \sin(\theta) \tag{14.66}$$

$$T_z = T_s - T_i - T_{i+1} \tag{14.67}$$

respectively, where $\hat{v}_c$ is the amplitude of the desired ac line voltage, as shown in Fig. 14.18. By redefining this quantity to

$$0 \le \hat{v}_c = \hat{v}_{cm} \frac{V_i}{v_i(t)} \le 1 \tag{14.68}$$

where V_i is the nominal dc bus voltage and $v_i(t)$ is the actual dc bus voltage. Thus, the on-times become

$$T_i = T_s \cdot \hat{v}_{cm} \frac{V_i}{v_i(t)} \cdot \sin(\pi/3 - \theta) \tag{14.69}$$

$$T_{i+1} = T_s \cdot \hat{v}_{cm} \frac{V_i}{v_i(t)} \cdot \sin(\theta) \tag{14.70}$$

$$T_z = T_s - T_i - T_{i+1} \tag{14.71}$$

where $\hat{v}_{cm}$ is the desired maximum ac line voltage. The previous expressions account for dc bus voltage variations and behave as a feedforward loop as it needs to sense the perturbation in order to be implemented. The previous expressions are valid for the linear region, thus $\hat{v}_c$ is restricted to $0 \le \hat{v}_c \le 1$, which indicates that the compensation is indeed limited.

14.5.2 Feedforward Techniques in Current Source Inverters

The duality principle between the voltage and current source inverters indicates that, as described previously, the feedforward approach can be used for CSIs as well as for VSIs. Therefore, low-order harmonics present in the dc bus current can be compensated for before they appear at the load side. This can be done for both analog-based (e.g., carrier-based) and digital-based (e.g., space-vector) modulating techniques.

14.5.3 Feedback Techniques in Voltage Source Inverters

Unlike the feedforward approach, the feedback techniques correct the input to the system (gating signals) depending upon the deviation of the output to the system (e.g., ac load line currents in VSIs). Another important difference is that feedback techniques need to sense the controlled variables. In general, the controlled variables (output to the system) are chosen according to the control objectives. For instance, in ASDs, it is usually necessary to keep the motor line currents equal to a given set of sinusoidal references. Therefore, the controlled variables become the ac line currents. There are several alternatives to implement feedback techniques in VSIs, and three of them are discussed in the following.

14.5.3.1 Hysteresis Current Control

The main purpose here is to force the ac line current to follow a given reference. The status of the power valves S_1 and S_4 are changed whenever the actual i_{oa} current goes beyond a given reference $i_{oa,ref} \pm \Delta i/2$. Figure 14.39 shows the hysteresis current controller for phase *a*. Identical controllers are used in phase *b* and *c*. The implementation of this controller is simple as it requires an op-amp operating in the hysteresis mode, thus the controller and modulator are combined in one unit.

Unfortunately, there are several drawbacks associated with the technique itself. First, the switching frequency cannot be predicted as in carrier-based modulators and therefore the harmonic content of the ac line voltages and currents becomes random (Fig. 14.40d). This could be a disadvantage when designing the filtering components. Second, as three-phase loads do not have the neutral connected as in ASDs, the load currents add up to zero. This means that only two ac line currents can be controlled independently at any given instant. Therefore, one of the hysteresis controllers is redundant at a given time. This explains why the load current goes beyond the limits and introduces limit cycles (Fig. 14.40a). Finally, although the ac load currents add up to zero, the controllers cannot ensure that all load line currents feature a zero dc component in one load cycle.

14.5.3.2 Linear Control of VSIs

Proportional and proportional-integrative controllers can also be used in VSIs. The main purpose is to generate the modulating signals v_{ca}, v_{cb}, and v_{cc} in a closed-loop fashion

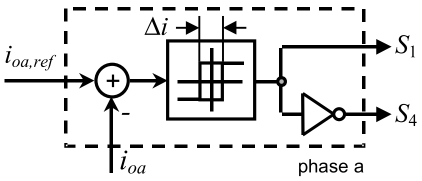


FIGURE 14.39 The three-phase VSI. Hysteresis current control (phase a).

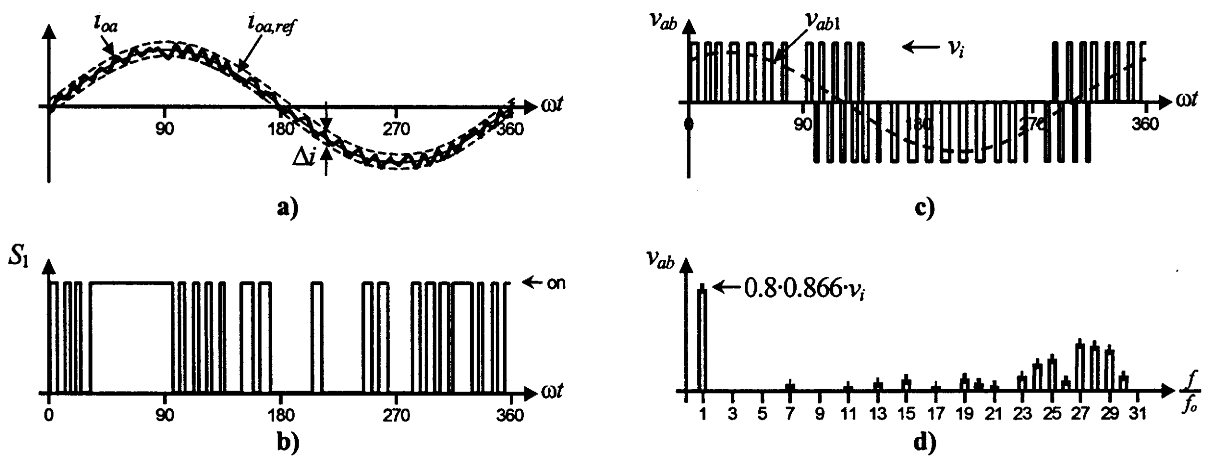


FIGURE 14.40 The three-phase VSI. Ideal waveforms for Hysteresis current control: (a) actual ac load current and reference; (b) Switch S_1 state; (c) ac output voltage; (d) ac output voltage spectrum.

as depicted in Fig. 14.41. The modulating signals can be used by a carrier-based technique such as the SPWM (as depicted in Fig. 14.41) or by space-vector modulation. Because the load line currents add up to zero, the load line current references must add up to zero. Thus, the abc/$\alpha\beta\gamma$ transformation can be used to reduce to two controllers the overall implementation scheme as the γ component is always zero. This avoids limit cycles in the ac load currents.

The transformation of a set of variables in the stationary abc frame $[x]_{\mathrm{abc}}$ into a set of variables in the stationary $\alpha\beta$ frame $[x]_{\alpha\beta}$ is given by

$$[x]_{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}[x]_{\mathrm{abc}} \tag{14.72}$$

The selection of the controller (P, PI, . . .) is done according to control procedures such as steady-state error, settling time, overshoot, and so forth. Figure 14.42 shows the relevant waveforms of a VSI SPWM controlled by means of a PI controller as shown in Fig. 14.41.

Although it is difficult to prove that no limit cycles are generated, the ac line current appears very much sinusoidal. Moreover, the ac line voltage generated by the VSI preserves the characteristics of such waveforms generated by SPWM modulators. This is confirmed by the harmonic spectrum shown in Fig. 14.42d, where the first set of characteristic harmonics are around the normalized carrier frequency $m_f = 15$.

However, an error between the actual i_{oa} and the ac line current reference $i_{oa,ref}$ can be observed (Fig. 14.42a). This error is inherent to linear controllers and cannot be totally eliminated, but it can be minimized by increasing the gain of the controller. However, the noise in the circuit is also increased, which could deteriorate the overall performance of the control scheme. The inherent presence of the error in this type of controllers is due to the fact that the controller needs a sinusoidal error to generate sinusoidal modulating signals v_{ca}, v_{cb}, and v_{cc}, as required by the modulator. Therefore, an error must exist between the actual and the ac line current references.

Nevertheless, as current-controlled VSIs are actually the inner loops in many control strategies, their inherent errors are compensated by the outer loop. This is the case of ASDs, where the outer speed loop compensates the inner current loops. In general, if the outer loop is implemented with dc quantities (such as speed), it can compensate the ac inner loops (such as ac line currents). If it is mandatory that a zero steady-state error be achieved with the ac quantities, then an stationary or rotating transformation is a valid alternative to use.

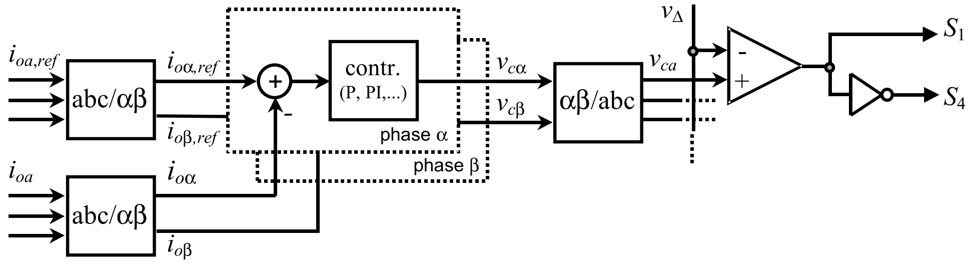


FIGURE 14.41 The three-phase VSI. Feedback control based on linear controllers.

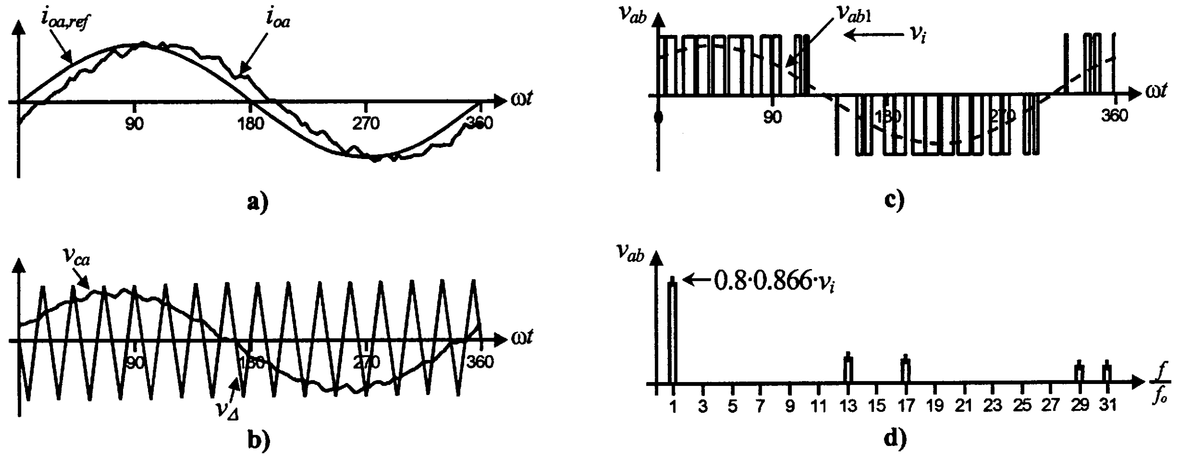


FIGURE 14.42 The three-phase VSI. Ideal waveforms for a PI controller in a feedback loop ($m_a = 0.8$, $m_f = 15$): (a) actual ac load current and reference; (b) Carrier and modulating signals; (c) ac output voltage; (d) ac output voltage spectrum.

14.5.3.3 Linear Control of VSIs in Rotating Coordinates

The direct-quadrature-zero (dq0) transformation allows ac three-phase circuits to be operated as if they were dc circuits. This is based upon a mathematical operation that is the transformation of a set of variables in the stationary abc frame $[x]_{\text{abc}}$ into a set of variables in the rotating dq0 frame $[x]_{\text{dq0}}$. The transformation is given by

$$[x]_{\text{dq0}} = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t - 4\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t - 4\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}[x]_{\text{abc}} \tag{14.73}$$

where ω is the angular frequency of the ac quantities. For instance, the current vector given by

$$[i]_{\text{abc}} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} I\sin(\omega t - \varphi) \\ I\sin(\omega t - 2\pi/3 - \varphi) \\ I\sin(\omega t - 4\pi/3 - \varphi) \end{bmatrix} \tag{14.74}$$

becomes the vector

$$[i]_{\text{dq0}} = \begin{bmatrix} i_{\text{d}} \\ i_{\text{q}} \\ i_0 \end{bmatrix} = \begin{bmatrix} I\cos(\varphi) \\ -I\sin(\varphi) \\ 0 \end{bmatrix} \tag{14.75}$$

where I and φ are the amplitude and phase of the line currents, respectively. It can be observed that: (a) the zero component i_0 is always zero as the three-phase quantities add up to zero; and (b) the d and q components i_{d}, i_{q} are dc quantities. Thus, linear controllers should help to achieve zero steady-state error. The control strategy shown in Fig. 14.43 is an alternative where the zero-component controller has been eliminated due to fact that the line currents at the load side add up to zero.

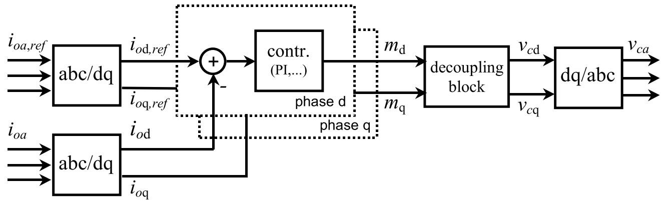


FIGURE 14.43 The three-phase VSI. Feedback control based on dq0 transformation.

The controllers in Fig. 14.43 include an integrator that generates the appropriate dc outputs m_{d} and m_{q} even if the actual and the line current references are identical. This ensures that zero steady-state error is achieved. The decoupling block in Fig. 14.43 is used to eliminate the cross-coupling effect generated by the dq0 transformation and to allow an easier design of the parameters of the controllers.

The dq0 transformation requires the intensive use of multiplications and trigonometric functions. These operations can readily be done by means of digital microprocessors. Also, analog implementations would indeed be involved.

14.5.4 Feedback Techniques in Current Source Inverters

Duality indicates that CSIs should be controlled as equally as VSIs except that voltages become currents and currents become voltages. Thus, hysteresis, linear and dq linear-based control strategies are also applicable to CSIs; however, the controlled variables are the load voltages instead of the load line currents.

For instance, the linear control of a CSI based on a dq transformation is depicted in Fig. 14.44. In this case, a passive balanced load is considered. In order to show that zero steady-

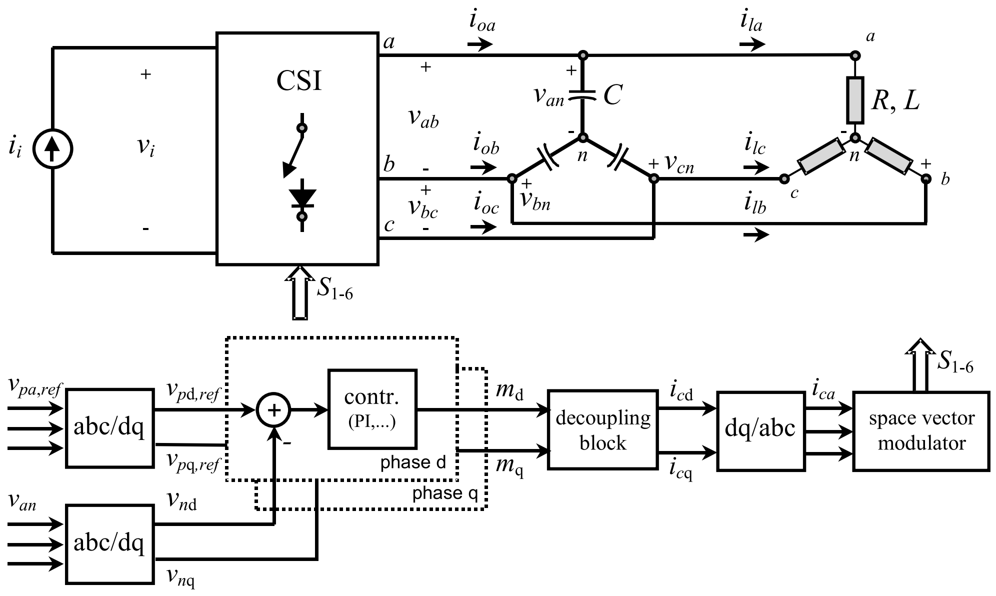


FIGURE 14.44 The three-phase CSI. Feedback control based on dq0 transformation.

state error is achieved, the per phase equations of the converter are written as

$$C\frac{d}{dt}[v_p]_{\text{abc}} = [i_o]_{abc} - [i_l]_{\text{abc}} \tag{14.76}$$

$$L\frac{d}{dt}[i_l]_{\text{abc}} = [v_p]_{\text{abc}} - R[i_l]_{\text{abc}} \tag{14.77}$$

the ac line currents are in fact imposed by the modulator and they satisfy

$$[i_o]_{\text{abc}} = i_i[i_c]_{\text{abc}} \tag{14.78}$$

Replacing Eq. (14.78) into the model of the converter equations (14.76) and (14.77), using the dq0 transformation and assuming null zero component, the model of the converter becomes

$$\frac{d}{dt}[v_p]_{\text{dq}} = -W[v_p]_{\text{dq}} + \frac{i_i}{C}[i_c]_{\text{dq}} - \frac{1}{C}[i_l]_{\text{dq}} \tag{14.79}$$

$$\frac{d}{dt}[i_l]_{\text{dq}} = -W[i_l]_{\text{dq}} + \frac{1}{L}[v_p]_{\text{dq}} - \frac{R}{L}[i_l]_{\text{dq}} \tag{14.80}$$

where W is given by

$$W = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \tag{14.81}$$

A first approximation is to assume that the decoupling block is not there; in other words, $[i_c]_{\text{dq}} = [m]_{\text{dq}}$. On the other hand, the model of the controllers can be written as

$$[m]_{\text{dq}} = k\{[v_{p,ref}]_{\text{dq}} - [v_p]_{\text{dq}}\} + \frac{1}{T}\int_{-\infty}^{t}([v_{p,ref}]_{\text{dq}} - [v_p]_{\text{dq}})dt \tag{14.82}$$

where k and T are the proportional and integrative gains of the PI controller that are chosen to achieve a desired dynamic response. Combining the model of the controllers and the model of the converter in dq coordinates and using the Laplace transform, the following relationship between the reference and actual load-phase voltages is found:

$$\begin{aligned}[v_p]_{\text{dq}} =& \frac{i_i}{C}\left\{sk + \frac{1}{T}\right\}\left\{sI + W + \frac{R}{L}I\right\}\left[\left\{sI + W + \frac{R}{L}I\right\}\right. \\ &\left.\times\left\{s^2I + s\left(W + \frac{i_i}{C}kI\right) + \frac{i_i}{CT}I\right\} + \frac{s}{LC}I\right]^{-1}[v_{p,ref}]_{\text{dq}}\end{aligned} \tag{14.83}$$

In order to finally prove that zero steady-state error is achieved for step inputs in either the d or q component of the load-phase voltage reference, the previous expression is evaluated in $s = 0$. This results in the following:

$$\begin{aligned}[v_p]_{\text{dq}} &= \frac{i_i}{C}\left\{\frac{1}{T}\right\}\left\{W + \frac{R}{L}I\right\}\left[\left\{W + \frac{R}{L}I\right\}\left\{\frac{i_i}{CT}I\right\}\right]^{-1}[v_{p,ref}]_{\text{dq}} \\ &= [v_{p,ref}]_{\text{dq}}\end{aligned} \tag{14.84}$$

As expected, the actual and reference values are identical. Finally, the relationship Eq. (14.83) is a matrix that is not diagonal. This means that both actual and reference load-phase voltages are coupled. In order to obtain a decoupled control, the decoupling block in Fig. 14.44 should be properly chosen.

14.6 Regeneration in Inverters

Industrial applications are usually characterized by a power flow that goes from the ac distribution system to the load. This is, for example, the case of an ASD operating in the motoring mode. In this instance, the active power flows from the dc side to the ac side of the inverter. However, there are an important number of applications in which the load may supply power to the system. Moreover, this could be an occasional condition as well a normal operating condition. This is known as the regenerative operating mode. For example, when an ASD reduces the speed of an electrical machine this can be considered a transient condition. Downhill belt conveyors in mining applications can be considered a normal operating condition. In order to simplify the notation, it could be said that an inverter operates in the motoring mode when the power flows from the dc to the ac side, and in the regenerative mode when the power flows from the ac to the dc side.

14.6.1 Motoring Operating Mode in Three-Phase VSIs

This is the case where the power flows from the dc side to the ac side of the inverter. Figure 14.45 shows a simplified scheme of an ASD where the motor has been modeled by three *RLe* branches, where the sources $[e]_{abc}$ are the back-emf. Because the ac line voltages applied by the inverter are imposed by the pulsewidth-modulation technique being used, they can be adjusted according to specific requirements. In particular,

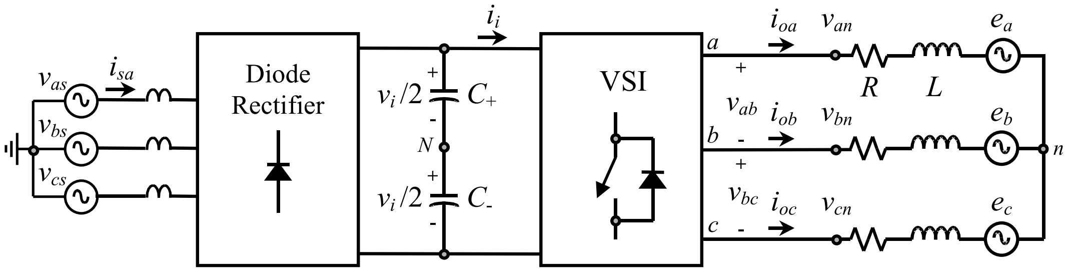


FIGURE 14.45 Three-phase VSI topology with a diode-based front-end rectifier.

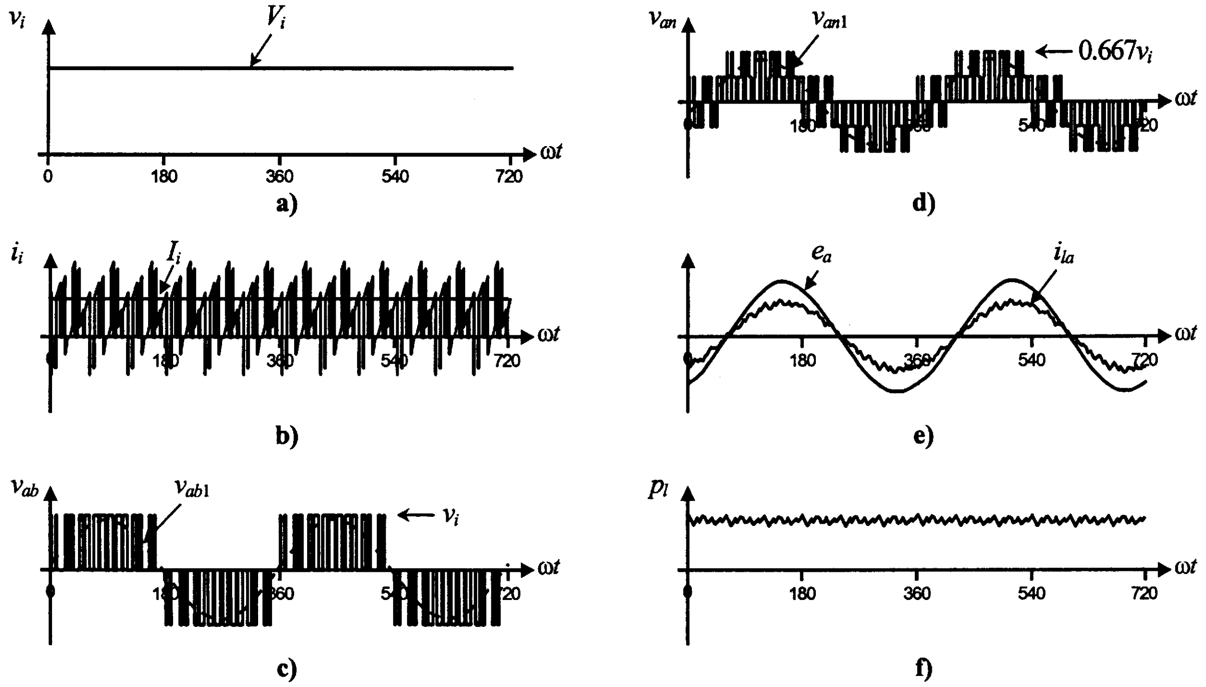


FIGURE 14.46 The ASD based on a VSI. Motoring mode: (a) dc bus voltage; (b) dc bus current; (c) ac line-load voltage; (d) ac phase-load voltage; (e) motor line current and back-emf; (f) shaft power.

Fig. 14.46 shows the relevant waveforms in steady state for the motoring operating mode of the ASD. To simplify the analysis, a constant dc bus voltage $v_i = V_i$ has been considered.

It can be observed that: (i) the dc bus current i_i features a dc value I_i that is positive; and (ii) the motor line current is in phase with the back-emf. Both features confirm that the active power flows from the dc source to the motor. This also is confirmed by the shaft power plot (Fig. 14.46f), which is obtained as:

$$p_l(t) = e_a(t)i_{la}(t) + e_b(t)i_{lb}(t) + e_c(t)i_{lc}(t) \tag{14.85}$$

14.6.2 Regenerative Operating Mode in Three-Phase VSISs

The back-emf sources $[e]_{\text{abc}}$ are functions of the machine speed and as such they ideally change just as the speed changes. The regeneration operating mode can be achieved by properly modifying the ac line voltages applied to the machine. This is done by the speed outer loop that could be based on a scalar (e.g., V/f) or vectorial (e.g., field-oriented) control strategy. As indicated earlier, there are two cases of regenerative operating modes.

14.6.2.1 Occasional Regenerative Operating Mode

This mode is required during transient conditions such as in occasional braking of electrical machines (ASDs). Specifically, the speed needs to be reduced and the kinetic energy is taken into the dc bus. Because the motor line voltage is imposed by the VSI, the speed reduction should be done in such a way that the motor line currents do not exceed the maximum values. This boundary condition will limit the ramp-down speed to a minimum, but shorter braking times will require a mechanical braking system.

Figure 14.47 shows a transition from the motoring to regenerative operating mode for an ASD as shown in Fig. 14.45. Here, a stiff dc bus voltage has been used. Zone I in Fig. 14.47 is the motoring mode, Zone II is a transition condition, and Zone III is the regeneration mode. The line voltage is adjusted dynamically to obtain nominal motor line currents during regeneration (Fig. 14.47d). Zone III clearly shows that the shaft power gets reversed.

Occasional regeneration means that the drive rarely goes into this operating mode. Therefore, such energy can be: (a) left uncontrolled; or (b) burned in resistors that are paralleled to the dc bus. The first option is used in low- to medium-power applications that use diode-based front-end rectifiers. Therefore, the dc bus current flows into the dc bus capacitor and the dc bus voltage rises accordingly to

$$\Delta v_i = \frac{1}{C} I_i \Delta t \tag{14.86}$$

where Δv_i is the dc bus voltage variation, C is the dc bus voltage capacitor, I_i is the average dc bus current during regeneration, and Δt is the duration of the regeneration operating mode. Usually, the drives have the capacitor C designed to allow a 10 overvoltage in the dc bus.

The second option uses burning resistors R_R that are paralleled in the dc bus as shown in Fig. 14.48 by means of the switch S_R. A closed-loop strategy based on the actual dc bus voltage modifies the duty cycle of the turn-on/turn-off of the switch S_R in order to keep such voltage under to a given reference. This alternative is used when the energy recovered by the VSI would result in an acceptable dc bus voltage variation if an uncontrolled alternative is used.

There are some special cases where the regeneration operating mode is frequently used. For instance, electrical shovels in mining companies have repetitive working cycles and $\approx$15% of the energy is sent back into the dc bus. In this case, a valid alternative is to send back the energy into the ac distribution system.

The schematic shown in Fig. 14.49 is capable of taking the kinetic energy and sending it into the ac grid. As reviewed earlier, the regeneration operating mode reverses the polarity of the dc current i_i, and because the diode-based front-end converter cannot take negative currents, a thyristor-based front-end converter is added. Similarly to the burning-resistor approach, a closed-loop strategy based on the actual dc bus voltage v_i modifies the commutation angle α of the thyristor rectifier in order to keep such voltage under a given reference.

14.6.2.2 Regenerative Operating Mode as Normal Operating Mode

Fewer industrial applications are capable of returning energy into the ac distribution system on a continuous basis. For instance, mining companies usually transport their product downhill for few kilometers before processing it. In such cases, the drive maintains the transportation belt conveyor at constant speed and takes the kinetic energy. Due to the large amount of energy and the continuous operating mode, the drive should be capable of taking the kinetic energy, transforming it into electrical energy, and sending it into the ac distribution system. This would make the drive a generator that would compensate for the active power required by other loads connected to the electrical grid.

The schematic shown in Fig. 14.50 is a modern alternative for adding regeneration capabilities to the VSI-based drive on a continuous basis. In contrast to the previous alternatives, this scheme uses a VSI topology as an active front-end converter, which is generally called a voltage-source rectifier VSR. The VSR operates in two quadrants, that is positive dc voltages and at positive/negative dc currents as reviewed earlier. This feature makes it a perfect match for ASDs based on a VSI. Some of the advantages of using a VSR topology are: (i) the ac supply current can be as sinusoidal as required (by increasing the switching frequency of the VSR or the ac line inductance); (ii) the operation can be done at a unity displacement power factor in both motoring and regenerative

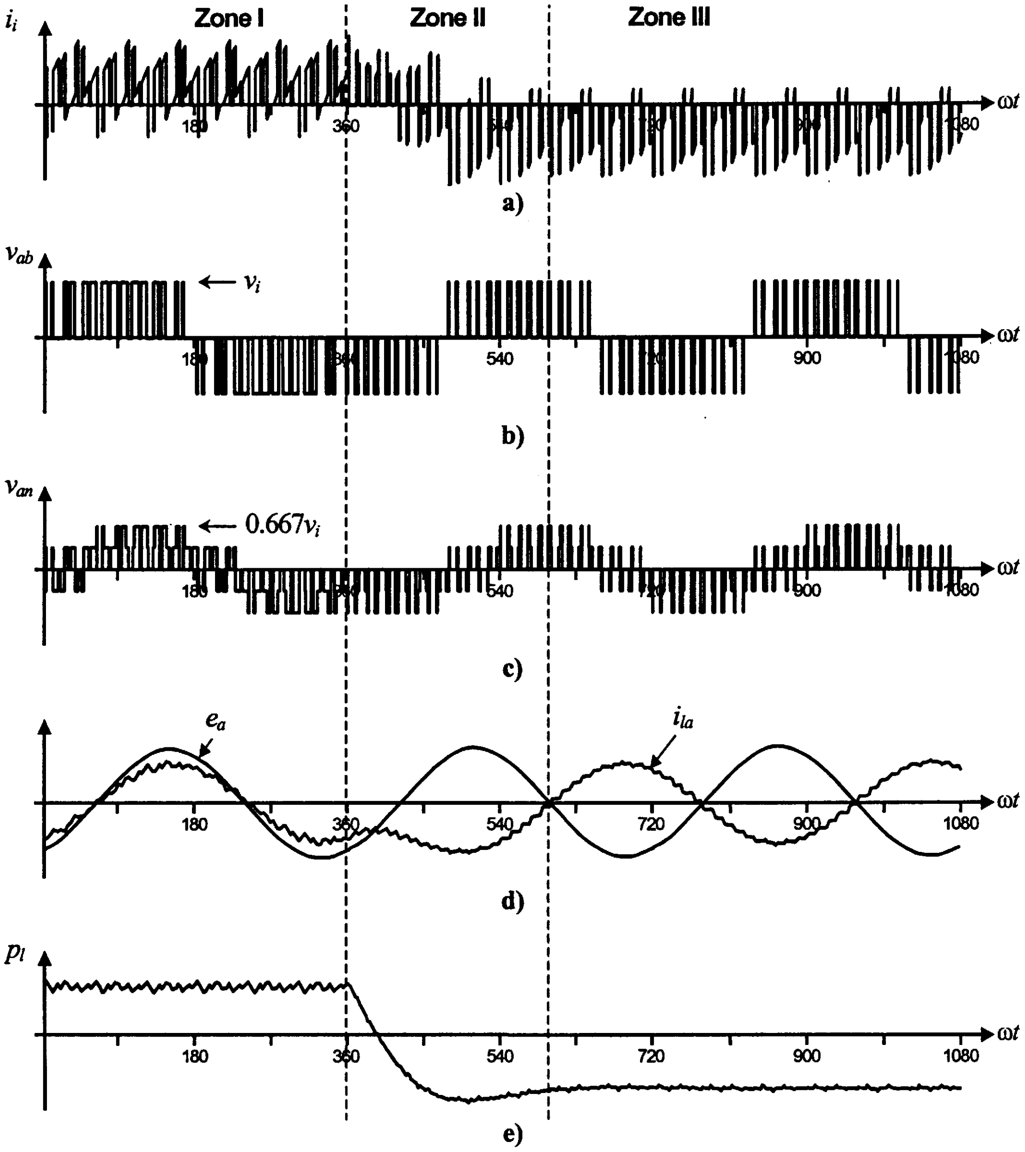


FIGURE 14.47 The ASD based on a VSI. Motoring to regenerative operating mode transition: (a) dc bus current; (b) ac line motor voltage; (c) ac phase motor voltage; (d) motor line current and back emf; (e) shaft power.

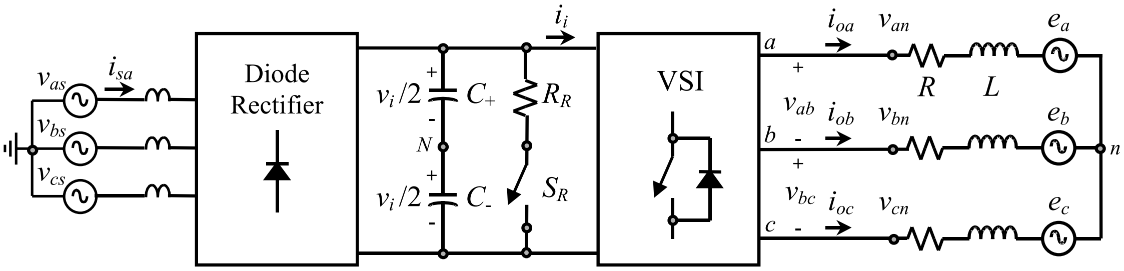

v_{as}
i_{sa}
v_{bs}
v_{cs}
Diode Rectifier
$v_i/2$
C_+
N
$v_i/2$
C_-
i_i
R_R
S_R
VSI
a
b
c
i_{oa}
v_{an}
v_{ab}
i_{ob}
v_{bn}
v_{bc}
i_{oc}
v_{cn}
R
L
e_a
e_b
e_c
n

FIGURE 14.48 The ASD based on a VSI. Burning resistor strategy.

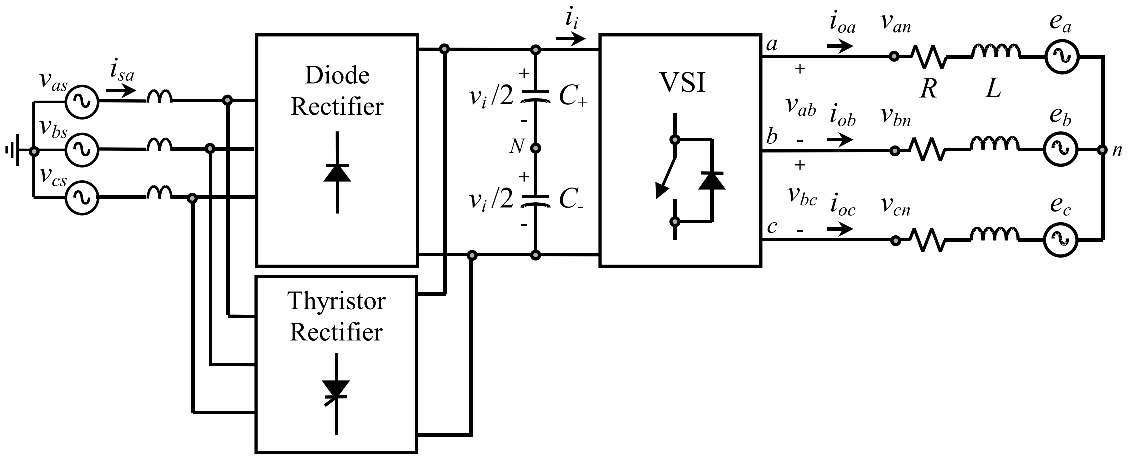

v_{as}
i_{sa}
v_{bs}
v_{cs}
Diode Rectifier
Thyristor Rectifier
i_i
$v_i/2$
C_+
N
C_-
VSI
a
b
c
i_{oa}
v_{an}
v_{ab}
i_{ob}
v_{bn}
v_{bc}
i_{oc}
v_{cn}
R
L
e_a
e_b
e_c
n

FIGURE 14.49 The ASD based on a VSI. Diode-thyristor-based front-end rectifier with regeneration capabilities.

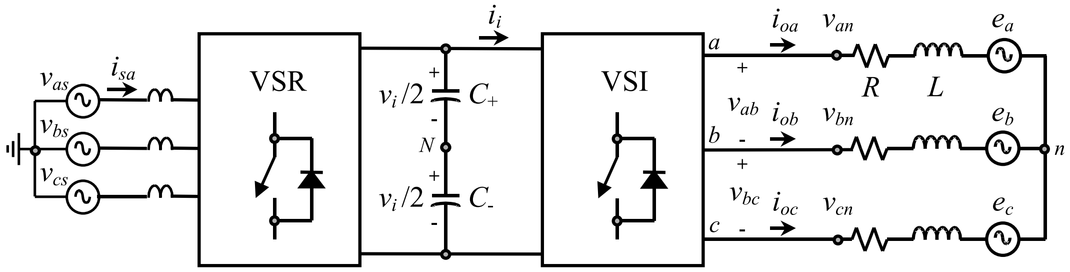

v_{as}
i_{sa}
v_{bs}
v_{cs}
VSR
i_i
$v_i/2$
C_+
N
C_-
VSI
a
b
c
i_{oa}
v_{an}
v_{ab}
i_{ob}
v_{bn}
v_{bc}
i_{oc}
v_{cn}
R
L
e_a
e_b
e_c
n

FIGURE 14.50 The ASD based on a VSI. Active front-end rectifier with regeneration capabilities.

operating modes; and (iii) the control of the VSR is done in both motoring and regenerative operating modes by a single dc bus voltage loop.

14.6.3 Regenerative Operating Mode in Three-Phase CSIs

There are drives where the motor side converter is a CSI. This is usually the case where near sinusoidal motor voltages are needed instead of the PWM type of waveform generated by VSIs. This is normally the case for medium-voltage applications. Such inverters require a dc current source that is constructed by means of a controlled rectifier.

Figure 14.51 shows a CSI-based ASD where the dc current source is generated by means of a thyristor-based rectifier in combination with a dc link inductor L_{dc}. In order to maintain a constant dc link current $i_i = I_i$, the thyristor-based rectifier adjusts the commutation angle α by means of a closed-loop control strategy. Assuming a constant dc link current, the regenerating operating mode is achieved when the dc link voltage v_i reverses its polarity. This can be done by modifying the PWM pattern applied to the CSI as in the VSI-based drive. To maintain the dc link current constant, the thyristor-based rectifier also reverses its dc link voltage v_r. Fortunately, the thyristor rectifier operates in two quadrants, that is, positive dc link currents and positive/negative dc link voltages. Thus, no

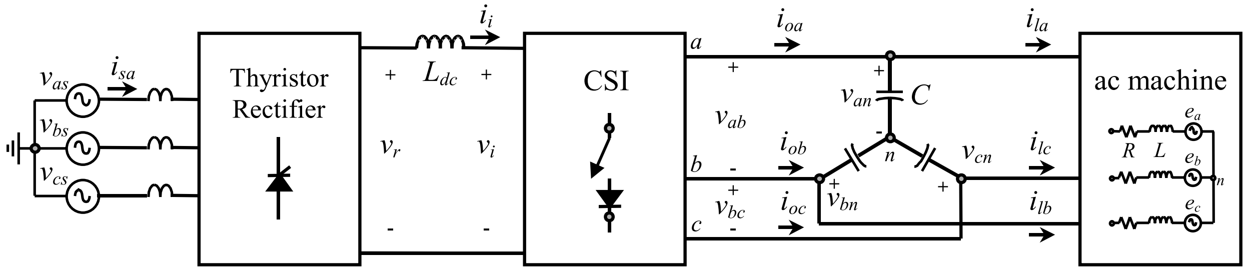

v_{as}
i_{sa}
v_{bs}
v_{cs}
Thyristor Rectifier
i_i
L_{dc}
v_r
v_i
CSI
a
b
c
i_{oa}
v_{ab}
i_{ob}
v_{bc}
i_{oc}
v_{an}
C
n
v_{bn}
v_{cn}
i_{la}
i_{lc}
i_{lb}
ac machine
R
L
e_a
e_b
e_c
n

FIGURE 14.51 The ASD based on a CSI. Thyristor-based rectifier.

additional equipment is required to include regeneration capabilities in CSI-based drives.

Similarly, an active front-end rectifier could be used to improve the overall performance of the thyristor-based rectifier. A PWM current-source rectifier CSR could replace the thyristor-based rectifier with the following added advantages: (i) the ac supply current can be as sinusoidal as required (e.g., by increasing the switching frequency of the CSR); (ii) the operation can be done at a unity displacement power factor in both motoring and regenerative operating modes; and (iii) the control of the CSR is done in both motoring and regenerative operating modes by a single dc bus current loop.

14.7 Multistage Inverters

The most popular three-phase voltage source inverter VSI consists of a six-switch topology (Fig. 14.52a). The topology can generate a three-phase set of ac line voltages such that each line voltage v_{ab} (Fig. 14.52b) features a fundamental ac line voltage v_{ab1} and unwanted harmonics Fig. 14.52c. The fundamental ac line voltage is usually required as a sinusoidal waveform at variable amplitude and frequency, and the unwanted harmonics are located at high frequencies. These requirements are met by means of a modulating technique as shown earlier. Among the applications in low-voltage ranges of six-switch VSIs are the adjustable speed drives (ASDs). The range is in low voltages due to: (a) the high dv/dt present in the PWM ac line voltages (Fig. 14.52b), which will be unacceptable in the medium- to high-voltage ranges; and (b) the load power would be shared only among six switches. This may require paralleling and series-connected power valves, an option usually avoided as symmetrical sharing of the power is not natural in these arrangements.

Two solutions are available to generate near-sinusoidal voltage waveforms while using six-switch topologies. The first is a topology based on a CSI in combination with a capacitive filter. The second solution is a topology based on a VSI including an inductive or inductive/capacitive filter at the load terminals. Although both alternatives generate near-sinusoidal voltage waveforms, both continue sharing the load power only among six power valves.

Solutions based on multistage voltage source topologies have been proposed. They provide medium voltages at the ac terminals while keeping low dv/dts and a large number of power valves that symmetrically share the total load power. The multistage VSIs can be classified in multicell and multilevel topologies.

14.7.1 Multicell Topologies

The goal is to develop a new structure with improved performance based on standard structures that are known as cells. For instance, Fig. 14.53a shows a cell featuring a three-phase input and a single-phase output. The front-end converter is a six-diode-based rectifier, and a single-phase VSI generates a single-phase ac voltage v_o. Figure 14.53b,c shows characteristic waveforms where a sinusoidal unipolar PWM ($m_f = 6$, $m_a = 0.8$) has been used to modulate the inverter.

Standard cells are meant to be used at low voltages, thus they can use standard components that are less expensive and widely available. The new structure should generate near-sinusoidal ac load voltages, draw near-sinusoidal ac line currents, and more importantly the load voltages should feature moderate dv/dts.

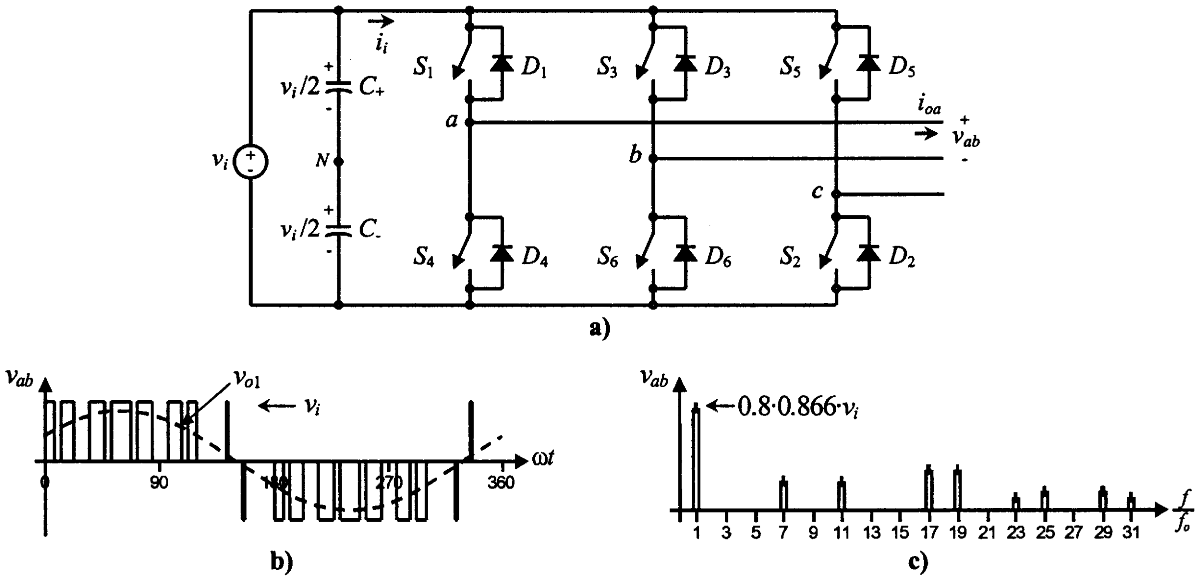


FIGURE 14.52 Six-switch voltage source inverter ($m_f = 9$, $m_a = 0.8$): (a) power topology; (b) ac output voltage; (c) ac output voltage spectrum.

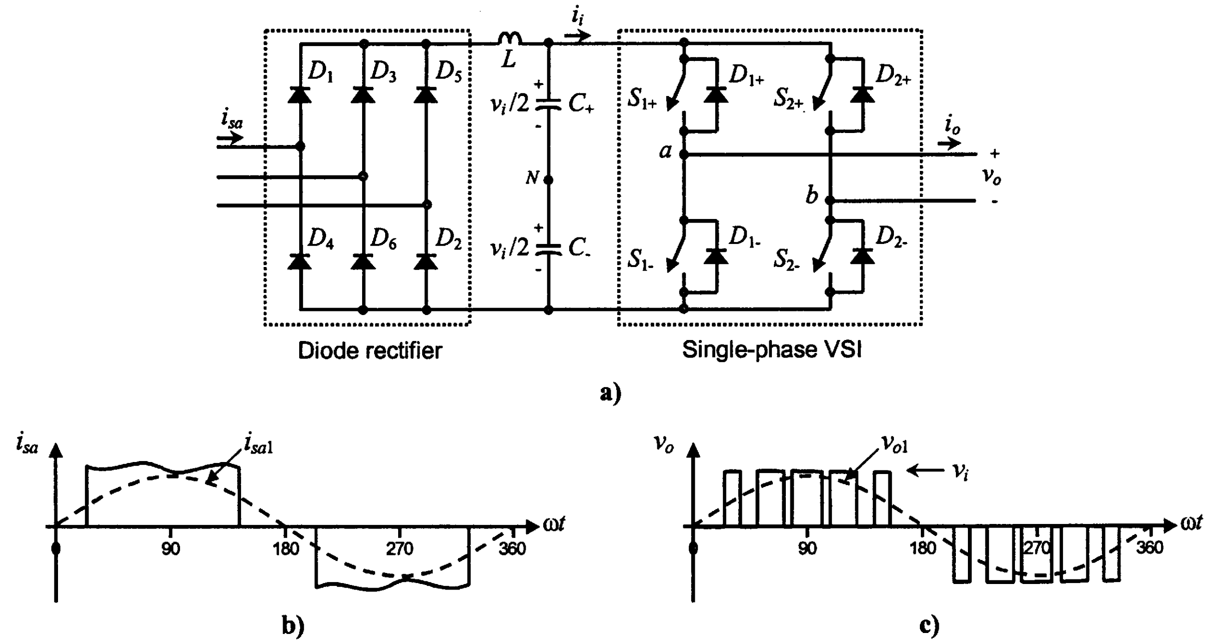


FIGURE 14.53 Three-phase-input single-phase output cell: (a) power topology; (b) ac input current, phase a; (c) ac output voltage ($m_f = 6$, $m_a = 0.8$).

Figure 14.54 shows a multicell converter that generates a three-phase output voltage out of a three-phase ac distribution system. The structure uses three standard cells (as shown in Fig. 14.53) connected in series to form one phase; thus the phase-load voltages are the sum of the single-phase voltages generated by each cell. For instance, the phase voltage a is given by

$$v_{an} = v_{o11} + v_{o21} + v_{o31} \tag{14.87}$$

In order to maximize the load-phase voltages, the ac voltages generated by the cells should feature identical fundamental components. On the other hand, each cell generates a PWM voltage waveform at the ac side, which contains unwanted voltage harmonics. If a carrier-based modulating technique is used, the harmonics generated by each cell are at well-defined frequencies (Fig. 14.53c). Some of these harmonics are not present in the phase-load voltage if the carrier signals of each cell are properly phase shifted.

In fact, Fig. 14.55 shows the voltages generated by cells c_{11}, c_{21}, and c_{31}, which are v_{o11}, $_{o21}$, and v_{o31}, respectively, and form the load-phase voltage a. They are generated using the unipolar SPWM approach, that is, one modulating signal v_{ca} and three carrier signals $v_{\Delta 1}$, $v_{\Delta 2}$, and $v_{\Delta 3}$ that are used by cells c_{11}, c_{21}, and c_{31}, respectively (Fig. 14.55a). The carrier signals have a normalized frequency m_f, which ensures an m_f switching frequency in each power valve and the lowest unwanted set of harmonics $\approx 2 \cdot m_f (m_f$ even) in the ac cell voltages v_{o11}, v_{o21}, and v_{o31}. More importantly, the carrier signals are $\psi = 120°$ out of phase, which ensures the lowest unwanted set of voltage harmonics $\approx 6 \cdot m_f$ in the load-phase voltage v_{an}, that is, the lowest set of harmonics in Fig. 14.55f) is $6 \cdot m_f = 6 \cdot 6 = 36$.

This can be explained as follows. The voltage harmonics present in the PWM voltage of each cell are at $l \cdot m_f \pm k$, $l = 2, 4, \ldots$ (where $k = 1, 3, 5, \ldots$); for instance, for $m_f = 6$, the first set of harmonics is at $12 \pm 1, 12 \pm 3, \ldots$ in all cells. Because the cells in one phase use carrier signals that are 120° out of phase, all the voltage harmonics $\approx l \cdot m_f$ in all cells are $l \cdot 120°$ out of phase. Therefore, for $l = 2$, the cell c_{11} generates the harmonics $l \cdot m_f \pm k = 2 \cdot m_f \pm k$ at a given phase φ, the cell c_{21} generates the harmonics $2 \cdot m_f \pm k$ at a phase $\varphi + l \cdot 120° = \varphi + 2 \cdot 120° = \varphi + 240° = \varphi - 120°$, and the cell c_{21} generates the harmonics $2 \cdot m_f \pm k$ at a phase $\varphi - l \cdot 120° = \varphi - 2 \cdot 120° = \varphi - 240° = \varphi + 120°$; thus, if the voltages have identical amplitudes, the harmonics $\approx 2 \cdot m_f$ add up to zero. Similarly, for $l = 4$, the cell c_{11} generates the harmonics $l \cdot m_f \pm k = 4 \cdot m_f \pm k$ at a given phase φ, the cell c_{21} generates the harmonics $4 \cdot m_f \pm k$ at a phase $\varphi + l \cdot 120° = \varphi + 4 \cdot 120° = \varphi + 480° = \varphi + 120°$, and the cell c_{21} generates the harmonics $4 \cdot m_f \pm k$ at a phase $\varphi - l \cdot 120° = \varphi - 4 \cdot 120° = \varphi - 480° = \varphi - 120°$; thus, if the voltages have identical amplitudes, the harmonics $\approx 4 \cdot m_f$ add up to zero. However, for $l = 6$, the cell c_{11} generates the harmonics $l \cdot m_f \pm k = 6 \cdot m_f \pm k$ at a given phase φ, the cell c_{21} generates the harmonics $6 \cdot m_f \pm k$ at a phase $\varphi + l \cdot 120° = \varphi + 6 \cdot 120° = \varphi + 720° = \varphi$, and the cell c_{21} generates the harmonics $6 \cdot m_f \pm k$ at a phase $\varphi - l \cdot 120° = \varphi - 6 \cdot 120° = \varphi - 720°$; thus, if the voltages have identical amplitudes, the harmonics $\approx 6 \cdot m_f$ become triplicated rather than cancelled out.

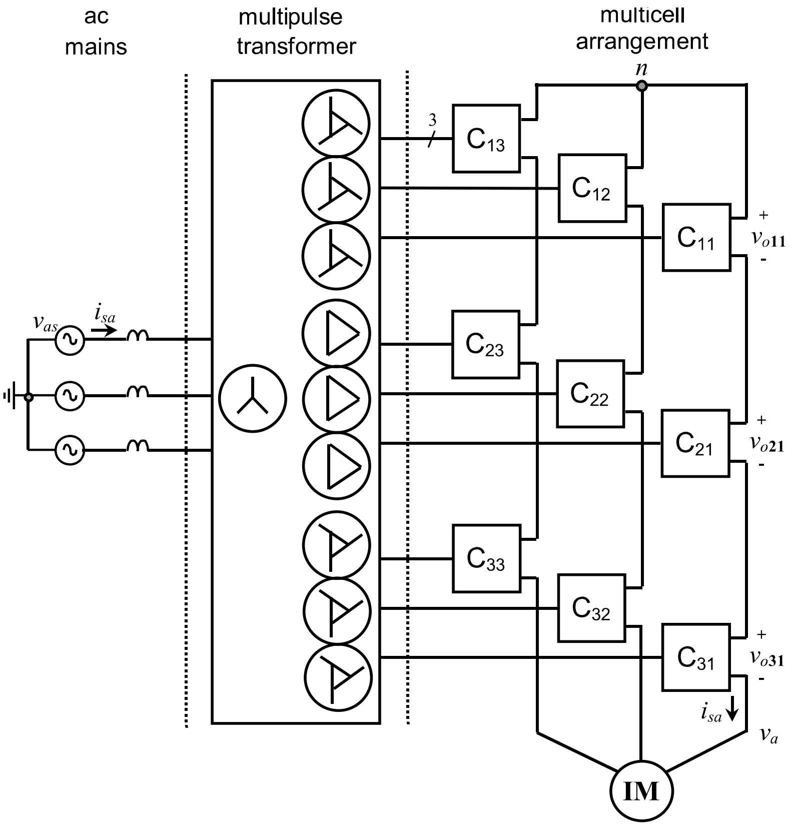

ac mains
multipulse transformer
multicell arrangement
n
3
C13
C12
C11
+
v_{o11}
-
C23
C22
C21
+
v_{o21}
-
C33
C32
C31
+
v_{o31}
-
v_{as}
i_{sa}
i_{sa}
v_a
IM

FIGURE 14.54 Multistage converter based on a multicell arrangement.

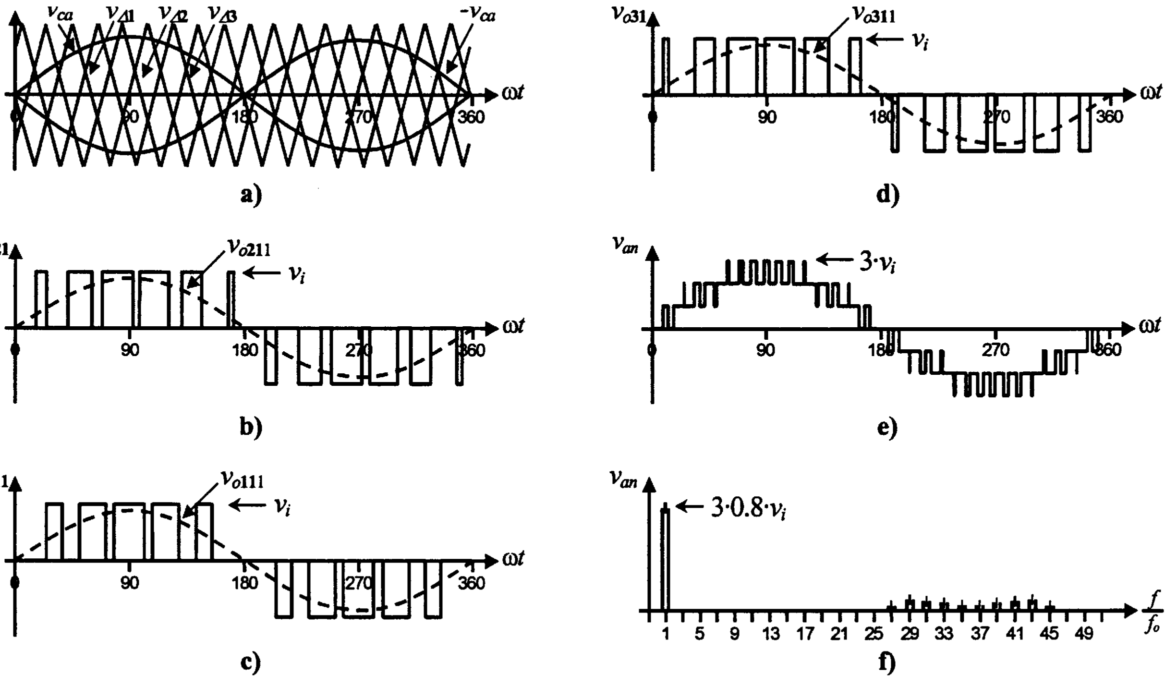


FIGURE 14.55 Multicell topology. Cell voltages in phase *a* using a unipolar SPWM ($m_f = 6$, $m_a = 0.8$): (a) Modulating and carrier signals; (b) cell c_{11} ac output voltage; (c) cell c_{21} ac output voltage; (d) cell c_{31} ac output voltage; (e) phase *a* load voltage. (f) phase *a* load-voltage spectrum.

In general, due to the fact that $n_c = 3$ cells are connected in series in each phase, n_c carriers are required, which should be $\psi = 360^\circ/n_c$ out of phase. The number of cells per phase n_c depends on the required phase voltage. For instance, a 600-V dc cell generates an ac voltage of $\approx 600/\sqrt{2} = 424$ V. Then three cells connected in series generate a phase voltage of $3 \cdot 424 = 1.27$ kV, which in turn generates a $1.27 \cdot \sqrt{3} = 2.2$-kV line-to-line voltage.

Phases b and c are generated similarly to phase a. However, the modulating signals v_{cb} and v_{cc} should be 120° out of phase. In order to use identical carrier signals in phases b and c, the carrier-normalized frequency m_f should be a multiple of 3. Thus, three modulating signals and n_c carrier signals are required to generate three phase voltages by means of a multicell approach, where n_c depends upon the required load line voltage and the dc bus voltage of each cell.

The ac supply current of each cell is a six-pulse type of current as shown in Fig. 14.56, which feature harmonics at $6 \cdot k \pm 1$ $(k = 1, 2, \ldots)$. Similarly to the load side, the ac supply currents of each cell are combined so as to achieve high-performance overall supply currents. Because the front-end converter of each cell is a six-pulse diode rectifier, a multipulse approach is used. This is based on the natural harmonic cancellation when, for instance, a wye to delta/wye transformer is used to form an $N = 12$ pulse configuration from two six-pulse diode rectifiers. In this case, the fifth and seventh harmonics are cancelled out because the supply voltages applied to each six-pulse rectifier become 30° out of phase. In general, to form an $N = 6 \cdot n_s$ pulse configuration, n_s set of supply voltages that should be $60^\circ/n_s$ out of phase is required. This would ensure the first set of unwanted current harmonics at $6 \cdot n_s \pm 1$.

The configuration depicted in Fig. 14.54 contains $n_c = 9$ cells, and a transformer capable of providing $n_s = 9$ sets of three-phase voltages that should be $60^\circ/n_s = 60^\circ/9$ out of phase to form an $N = 6 \cdot n_s = 6 \cdot 9 = 54$-pulse configuration is required. Although this alternative would provide a near-sinusoidal overall supply current, a fewer number of pulses is also acceptable that would reduce the transformer complexity. An $N = 18$-pulse configuration usually satisfies all the requirements. In the example, this configuration can be achieved by means of a transformer with $n_c = 9$ isolated secondaries; however, only $n_s = 3$ set of three-phase voltages that are $60^\circ/n_s = 60^\circ/3 = 20^\circ$ out of phase are generated (Fig. 14.54). The configuration of the transformer restricts the connection of the cells in groups of three as shown in Fig. 14.54. In this case, the fifth, seventh, eleventh, and thirteenth harmonics are cancelled out and thus the first set of harmonics in the supply currents are the seventeenth and the nineteenth. Figure 14.56d shows the resulting supply current that is near-sinusoidal and Fig. 14.56f shows the corresponding spectrum. The fifth, seventh, eleventh, and thirteenth harmonics are still there, which is due to the fact that the ac input currents in each cell are not exactly the six-pulse type of waveforms as seen in Fig. 14.56a,b and c. This is mainly because: (i) the dc link in the cells contains a small inductor L, which does not smooth out sufficiently the dc bus current (Fig. 14.53a); and (ii) the transformer leakage inductance (or added line induc-

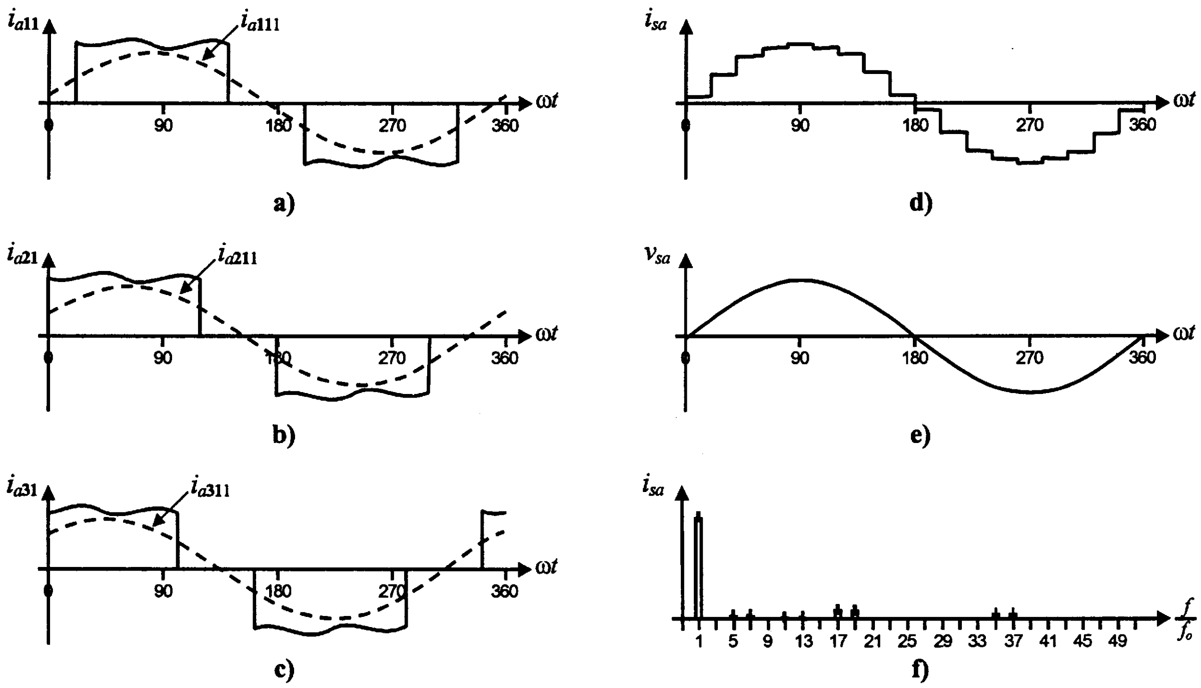


FIGURE 14.56 Multicell topology. Ac input current, phase a: (a) cell c_{11}; (b) cell c_{21}; (c) cell c_{31}; (d) Overall supply current; (e) supply phase voltage; (f) overall current spectrum.

tance) smoothes out the edges of the current, which also contributes to the reactive power required by the cells. This last effect is not shown in Fig. 14.56a,b and c.

14.7.2 Multilevel Topologies

The six-switch VSI is usually called a two-level VSI due to the fact that the inverter phase voltages v_{aN}, v_{bN}, and v_{cN} (Fig. 14.52a) are instantaneously either $v_i/2$ or $-v_i/2$. In other words, the phase voltages can take one of two voltage levels. Multilevel topologies provide an alternative to these voltages to take one value out of N levels. For instance, Fig. 14.57 shows an $N = 3$-level topology, where the values of the inverter phase voltage are either $v_i/2$, 0, or $-v_i/2$ (Fig. 14.58d). An interesting problem is how to obtain the gating pattern for the 12 switches required in an $N = 3$-level topology. There are several modulating techniques to overcome this problem, which can be classified as analog (e.g., carrier-based) and digital (space-vector-based). Both approaches have to deal with the valid switch states of the inverter.

14.7.2.1 Valid Switch States in a Three-Level VSI

The easiest way of obtaining the valid switch states is to analyze each phase separately. Phase a contains the switches S_{1a}, S_{1b}, S_{4a}, and S_{4b}, which cannot be on simultaneously because a short circuit across the dc bus would be produced, and cannot be off simultaneously because an undefined phase voltage v_{aN} would be produced. A summary of the valid switch combinations is given in Table 14.7. It is important to note that all valid switch combinations satisfy the condition that switch S_{1a} state is always the opposite to switch S_{4a} state, and that switch S_{1b} state is always the opposite to switch S_{4b} state.

TABLE 14.7 Valid switch states for a three-level VSI, phase *a*

S_{1a}	S_{1b}	S_{4a}	S_{4b}	v_o	Components Conducting
1	1	0	0	$v_i/2$	S_{1a}, S_{1b} if $i_{oa} > 0$ D_{1a}, D_{1b} if $i_{oa} < 0$
0	1	1	0	0	S_{1b}, D_{a+} if $i_{oa} > 0$ S_{4a}, D_{a-} if $i_{oa} < 0$
0	0	1	1	$-v_i/2$	D_{4a}, D_{4b} if $i_{oa} > 0$ S_{4a}, S_{4b} if $i_{oa} < 0$

Any other switch-state combination would result in an undefined inverter phase a voltage because it will depend upon the load-phase current i_{oa} polarity. The switch states for phases *b* and *c* are identical to that of phase *a*; moreover, because they are paralleled, they can operate in an independent manner.

14.7.2.2 The SPWM Technique in Three-Level VSIs

The main objective is to generate the appropriate 12 gating signals so as to obtain fundamental inverter phase voltages equal to a given set of modulating signals. Specifically, the SPWM in three-level inverters uses a sinusoidal set of modulating signals (v_{ca}, v_{cb}, and v_{cc} for phases *a*, *b*, and *c*, respectively) and $N - 1 = 2$ triangular type of carrier signals ($v_{\Delta 1}$ and $v_{\Delta 2}$ as illustrated in Fig. 14.58a. The best results are obtained if the carrier signals are in-phase and feature an odd normalized frequency $m_f = 15$. According to Fig. 14.58a, switch S_{1a} is either turned on if $v_{ca} > v_{\Delta 1}$ or off if $v_{ca} < v_{\Delta 1}$, and switch S_{1b} is either turned on if $v_{ca} > v_{\Delta 2}$ or off if $v_{ca} < v_{\Delta 2}$. Additionally, the switch S_{4a} status is obtained as the opposite to switch S_{1a}, and the switch S_{4b} status is obtained as the opposite to switch S_{1b}. In order to use the same set of

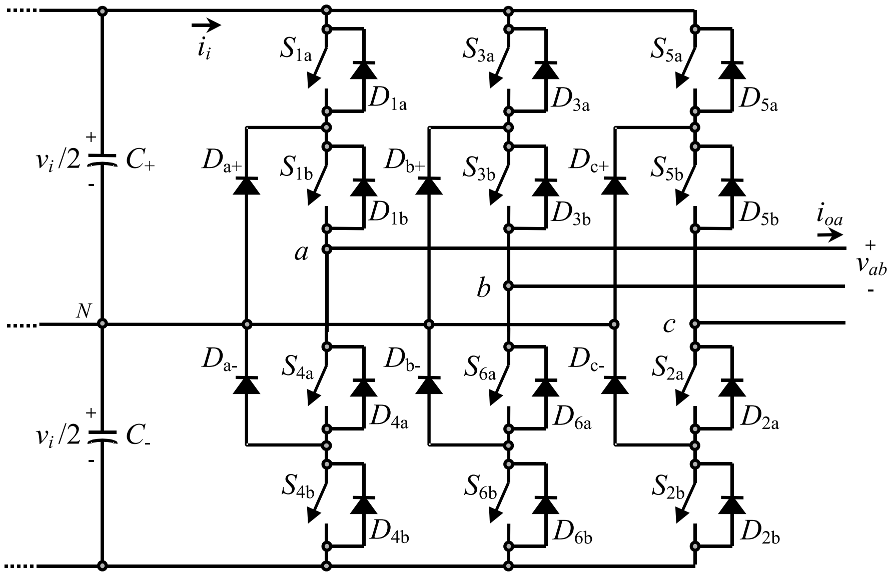


FIGURE 14.57 Three-phase three-level VSI topology.

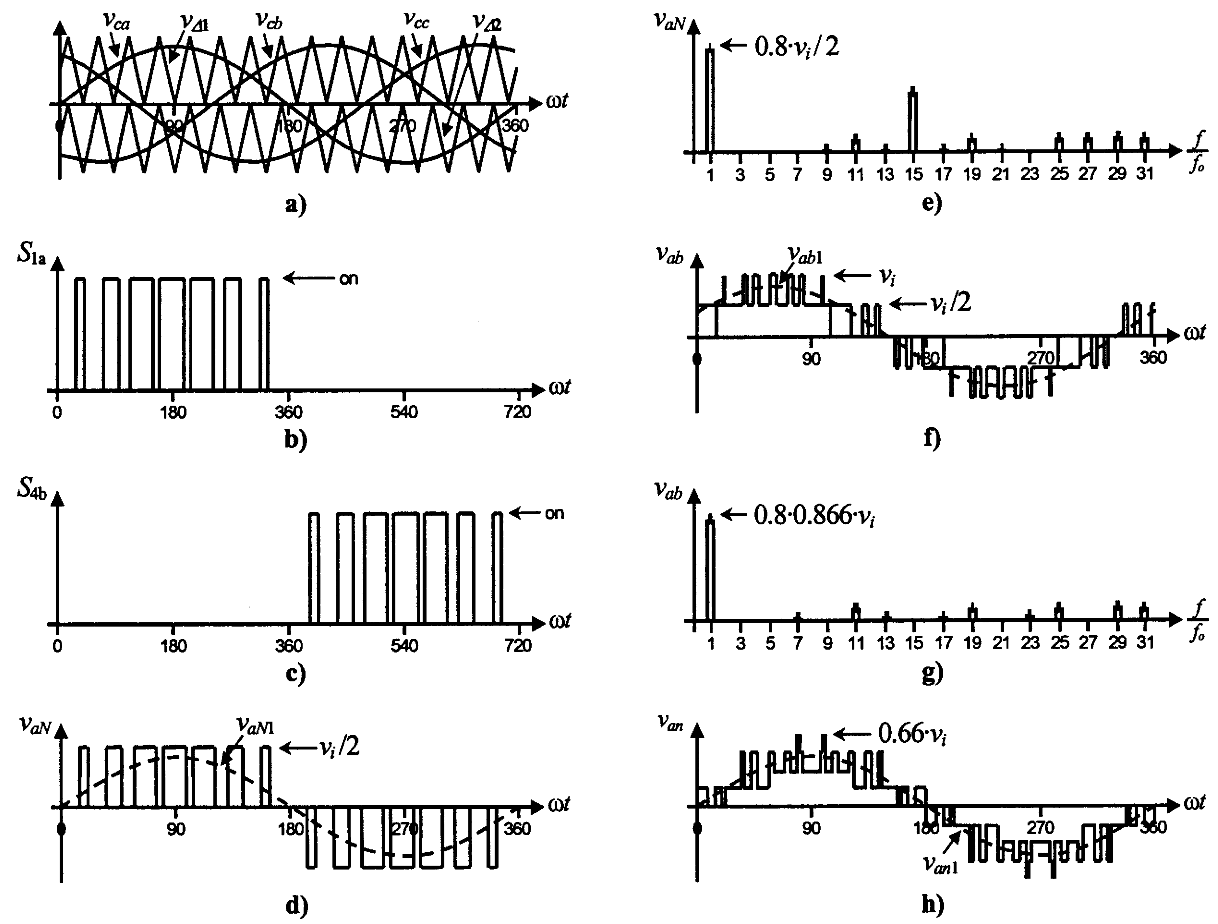


FIGURE 14.58 Three-level VSI topology. Relevant waveforms using a SPWM ($m_f = 15$, $m_a = 0.8$); (a) modulating and carrier signals; (b) switch S_{1a} status; (c) switch S_{4b} status; (d) inverter phase a voltage; (e) inverter phase a voltage spectrum; (f) load line voltage; (g) load line voltage spectrum; (h) load phase a voltage.

carrier signals to generate the gating signals for phases b and c, the normalized frequency of the carrier signal m_f should be a multiple of 3. Thus, the possible values are $m_f = 3, 9, 15, 21, \ldots$.

Figure 14.58 shows the relevant waveforms for a three-level inverter modulated by means of a SPWM technique ($m_f = 15$, $m_a = 0.8$). Specifically, Fig. 14.58d shows the inverter phase voltage, which is clearly a three-level type of voltage, and Fig. 14.58f shows the load line voltage, which shows that the step voltages are at most $v_i/2$. More importantly, the inverter phase voltage (Fig. 14.58e) contains harmonics at $l \cdot m_f \pm k$ with $l = 1, 3, \ldots$ and $k = 0, 2, 4, \ldots$, and at $l \cdot m_f \pm k$ with $l = 2, 4, \ldots$ and $k = 1, 3, \ldots$. For instance, the first set of harmonics ($l = 1$, $m_f = 15$) are at 15, 15 ± 2, $15 \pm 4, \ldots$. The inverter line voltage (Fig. 14.58g) contains harmonics at $l \cdot m_f \pm k$ with $l = 1, 3, \ldots$ and $k = 2, 4, \ldots$, and at $l \cdot m_f \pm k$ with $l = 2, 4, \ldots$ and $k = 1, 2, \ldots$. For instance, the first set of harmonics in the line voltages ($l = 1$, $m_f = 15$) are at 15 ± 2, $15 \pm 4, \ldots$.

All the other features of carrier-based PWM techniques also apply in multilevel inverters. For instance: (I) the fundamental component of the inverter phase voltages satisfy

$$\hat{v}_{aN1} = \hat{v}_{bN1} = \hat{v}_{cN1} = m_a \frac{v_i}{2}, \qquad 0 < m_a \le 1 \tag{14.88}$$

and thus the line voltages satisfy

$$\hat{v}_{ab1} = \hat{v}_{bc1} = \hat{v}_{ca1} = m_a \sqrt{3} \frac{v_i}{2}, \qquad 0 < m_a \le 1 \tag{14.89}$$

where $0 < m_a \le 1$ is the linear operating region. To further increase the amplitude of the load voltages, the overmodulation operating region can be used by further increasing the modulating signal amplitudes ($m_a > 1$), where the line voltages range in,

$$\sqrt{3} \frac{v_i}{2} < \hat{v}_{ab1} = \hat{v}_{bc1} = \hat{v}_{ca1} < \frac{4}{\pi} \sqrt{3} \frac{v_i}{2} \tag{14.90}$$

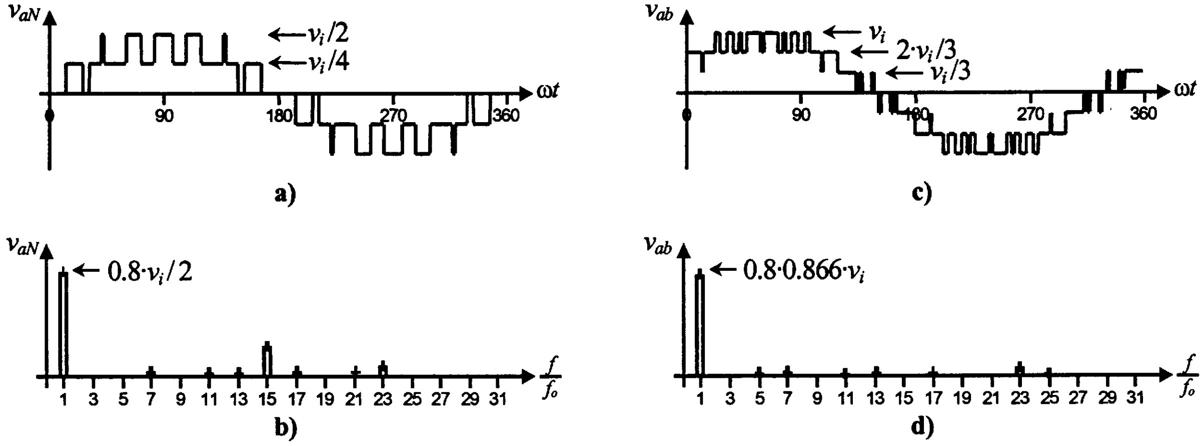


FIGURE 14.59 Five-level VSI topology. Relevant waveforms using a SPWM ($m_f = 15$, $m_a = 0.8$): (a) inverter phase a voltage; (b) inverter phase a voltage spectrum; (c) load line voltage; (d) load line voltage spectrum.

Also: (II) the modulating signals could be improved by adding a third harmonic (zero sequence), which will increase the linear region up to $m_a = 1.15$. This results in a maximum fundamental line-voltage component equal to v_i. (III) a nonsinusoidal set of modulating signals could also be used by the modulating technique. This is the case where nonsinusoidal line voltages are required as in active filter applications; and (IV) because of the two quadrants operation of VSIs, the multilevel inverter could equally be used in applications where the active power flow goes from the dc to the ac side or from the ac to the dc side.

In general, for an N-level inverter modulated by means of a carrier-based technique, the following conclusions can be drawn: (a) three modulating signals 120° out of phase and $N - 1$ carrier signals are required; (b) the phase voltages in the inverters have a peak value of $v_i/2$; (c) the phase voltages in the inverters are discrete waveforms constructed from the values

$$\frac{v_i}{2}, \frac{v_i}{2} - \frac{v_i}{N-1}, \frac{v_i}{2} - \frac{2 \cdot v_i}{N-1}, \ldots, -\frac{v_i}{2} \tag{14.91}$$

(d) the maximum voltage step in the load voltages is

$$\frac{v_i}{N-1} \tag{14.92}$$

for instance, an $N = 5$-level inverter requires four carrier signals, the discrete values of the phase voltages are: $v_i/2$, $v_i/4$, 0, $-v_i/4$, and $-v_i/2$, and the maximum step voltage at the load side is $v_i/4$. Key waveforms are shown in Fig. 14.59.

One of the drawbacks of the multilevel inverter is that the dc link capacitors cannot be supplied by a single dc voltage source. This is due to the fact that the currents required by the inverter in the dc bus are not symmetrical and therefore the capacitors will not equally share the dc supply voltage v_i. To overcome this problem, $N - 1$ independent dc voltage supplies are required. For instance, a three-level inverter will require two supplies that can be constructed by a multipulse transformer; specifically, a wye primary to delta-wye secondaries transformer would fit the requirements. In addition, the supply currents will improve its performance as the fifth and seventh harmonics will be cancelled out.

14.7.2.3 The Space Vector Modulation in Three-Level VSIs

Digital techniques are naturally extended to multilevel inverters. In fact, the space vector modulating technique can be applied using the same principles used in two-level inverters. However, the higher number of voltage levels increases the complexity of the practical implementation of the technique. For instance, in $N = 3$-level inverters, each leg allows $N = 3$ different switch combinations as indicated in Table 14.7. Therefore, there are $N^3 = 27$ total valid switch combinations, which generate $N^3 = 27$ load line voltages that are represented by $N^3 = 27$ space vectors $(\mathbf{V}_1, \mathbf{V}_2, \ldots \mathbf{V}_{27})$ in Fig. 14.60. For

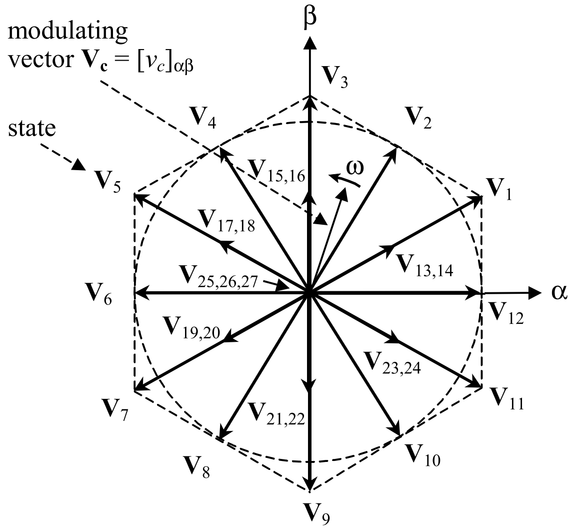


FIGURE 14.60 The space vector representation in a three-level VSI.

instance, $\mathbf{V}_2 = 0.5 + j0.866$ is due to the line voltages $v_{ab} = 0.5$, $v_{bc} = 0.5$, $v_{ca} = -1.0$ in pu. Thus, although the principle of operation is the same, the space vector digital algorithm will have to deal with a higher number of states N^3. Moreover, because some space vectors (e.g., $\mathbf{V}_{13}$ and $\mathbf{V}_{14}$ in Fig. 14.60) produce the same load-voltage terminals, the algorithm will have to decide between the two based on additional criteria and that of the basic space vector approach. Clearly, as the number of level increases, the algorithm becomes more and more elaborate. However, the benefits are not evident as the number of level increases. Five levels is the maximum number used in practical applications. This is based on a compromise between the complexity of the implementation and the benefits of the resulting waveforms.

14.8 Acknowledgments

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15.1 Introduction

Advances in power electronics in the last few decades have led not only to improvements in power devices, but also to new concepts in converter topologies and control. In the 1970s, conventional pulsewidth modulatioin (PWM) power converters were operated in switched mode. Power switches have to cut off the load current within the turn-on and turn-off times under the hard switching conditions. Hard switching refers to the stressful switching behavior of the power electronic devices. The switching trajectory of a hard-switched power device is shown in Fig. 15.1. During the turn-on and turn-off processes, the power device has to withstand high voltage and current simultaneously, which results in high switching losses and stress. Dissipative passive snubbers are usually added to the power circuits so that the dv/dt and di/dt of the power devices can be reduced, and the switching loss and stress can be diverted to the passive snubber circuits. However, switching loss is proportional to switching frequency, thus limiting the maximum switching frequency of the power converters. Typical converter switching frequency was limited to a few tens of kilohertz (typically 20 to 50 kHz) in early 1980s. Stray inductive and capacitive components in the power circuits and power devices still cause considerable transient effects, which in turn give rise to electromagnetic interference (EMI) problems. Figure 15.2 shows both typical ideal switching waveforms and practical switching waveforms of the switch voltage. Transient ringing effects are the major cause of EMI.

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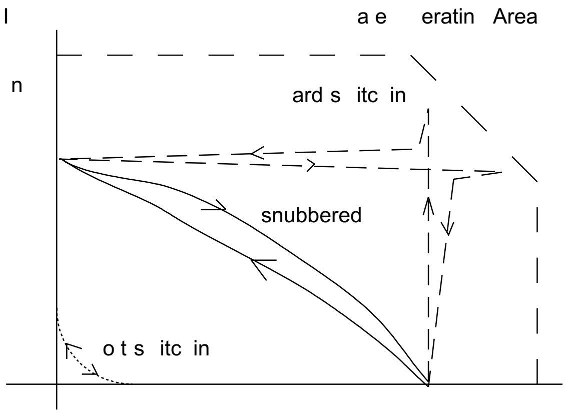
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FIGURE 15.1 Typical switching trajectories of power switches.

In the 1980s, much research was focused on the use of resonant converters. The concept was to incorporate resonant tanks in the converters to create oscillatory (usually sinusoidal) voltage and/or current waveforms so that zero-voltage switching (ZVS) or zero-current switching (ZCS) conditions could be created for the power switches. Reduction of switching loss and continual improvement of power switches allow the switching frequency of the resonant converters to reach hundreds of kilohertz (typically 100 to 500 kHz). Consequently, the size of magnetic components can be reduced and the power density of the converters increased. Various forms of resonant converters have been proposed and developed. However, most of the resonant converters suffer several problems. When compared with conventional PWM converters, the resonant current and voltage of resonant converters have high peak values, leading to higher conduction loss and higher V and I ratings requirements for the power devices. In addition, many resonant converters require frequency modulation (FM) for output regulation. Variable switching frequency operation makes the filter design and control more complicated.

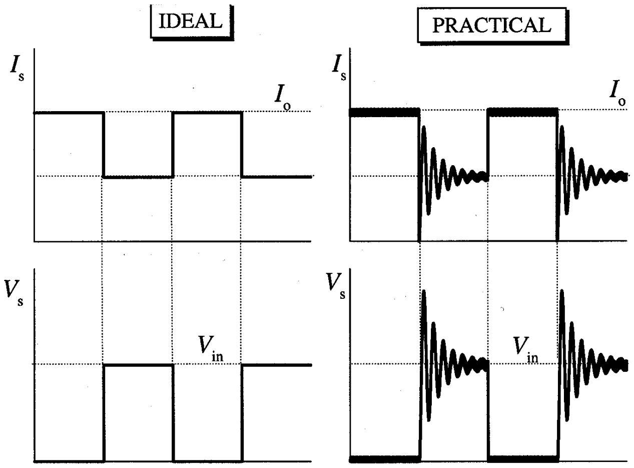
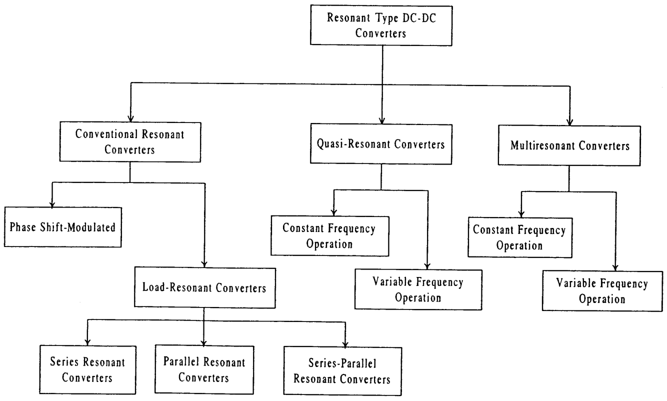


FIGURE 15.2 Typical ideal and practical switching waveforms.

In the late 1980s and throughout the 1990s, further improvements were made in converter technology. New generations of soft-switched converters that combine the advantages of conventional PWM converters and resonant converters were developed. These soft-switched converters have switching waveforms similar to those of conventional PWM converters except that the rising and falling edges of the waveforms are "smoothed" with no transient spikes. Unlike the resonant converters, new soft-switched converters usually utilize the resonance in a controlled manner. Resonance is allowed to occur just before and during the turn-on and turn-off processes so as to create ZVS and ZCS conditions. Other than that, they behave just like conventional PWM converters. With simple modifications, many customized control integrated circuits (IC) designed for conventional converters can be employed for soft-switched converters. Because the switching loss and stress have been reduced, soft-switched converters can be operated at the very high frequency (typically 500 kHz to a few megahertz). Soft-switching converters also provide an effective solution to suppress EMI and have been applied to dc-dc, ac-dc and dc-ac converters. This chapter covers the basic technology of resonant and soft-switching converters. Various forms of soft-switching techniques such as ZVS, ZCS, voltage clamping, zero-voltage transition methods etc. are addressed. The emphasis is placed on the basic operating principle and practicality of the converters with only a small amount of mathematical analysis.

15.2 Classification

This diagram provides at a glance the various types of converters available:


Resonant Type DC-DC Converters
Conventional Resonant Converters
Quasi-Resonant Converters
Multiresonant Converters
Phase Shift-Modulated
Load-Resonant Converters
Series Resonant Converters
Parallel Resonant Converters
Series-Parallel Resonant Converters
Constant Frequency Operation
Variable Frequency Operation
Constant Frequency Operation
Variable Frequency Operation

15.3 Resonant Switch

Prior to the availability of fully controllable power switches, thyristors were the major power devices used in power electronic circuits. Each thyristor requires a commutation

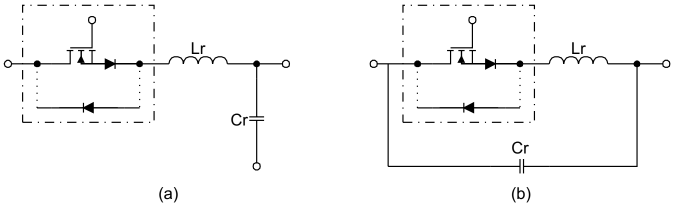


FIGURE 15.3 Two types of zero-current (ZC) resonant switch.

circuit, which usually consists of an *LC* resonant circuit, for forcing the current to zero in the turn-off process [1]. This mechanism is in fact a type of zero-current turn-off process. With recent advancements in semiconductor technology, the voltage and current handling capability and the switching speed of fully controllable switches have improved significantly. In many high-power applications, controllable switches such as GTOs and IGBTs have replaced thyristors [2, 3]. However, the use of a resonant circuit for achieving zero-current-switching (ZCS) and/or zero-voltage-switching (ZVS) [4–8] has also emerged as a new technology for power converters. The concept of resonant switch to replace a conventional power switch is introduced in this section.

A resonant switch is a subcircuit composed of a semiconductor switch *S* and resonant elements L_r and C_r [9–11]. Switch *S* can be implemented by a unidirectional or bidirectional switch, which determines the operation mode of the resonant switch. Two types of resonant switches [12], including zero-current (ZC) resonant switch and zero-voltage (ZV) resonant switches, are shown in Fig. 15.3 and Fig. 15.4, respectively.

15.3.1 C Resonant Switch

In a ZC resonant switch, an inductor L_r is connected in series with a power switch *S* in order to achieve zero-current-switching (ZCS). If the switch *S* is a unidirectional switch, the switch current is allowed to resonate in the positive half-cycle only. The resonant switch is said to operate in *half-wave* mode. If a diode is connected in antiparallel with the unidirectional switch, the switch current can flow in both directions. In this case, the resonant switch can operate in *full-wave* mode. At turn-on, the switch current will rise slowly from zero. It will then oscillate because of the resonance between L_r and C_r. Finally, the switch can be commutated at the next zero current duration. The objective of this type of switch is to shape the switch current waveform during conduction time in order to create a zero-current condition for the switch to turn off [13].

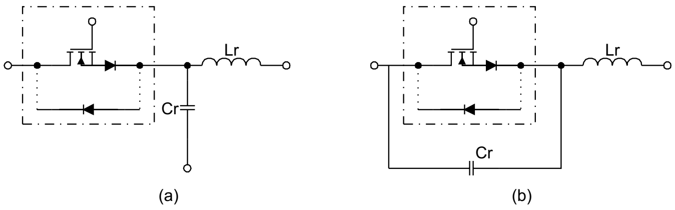


FIGURE 15.4 Two types of zero-voltage (ZV) resonant switch.

15.3.2 V Resonant Switch

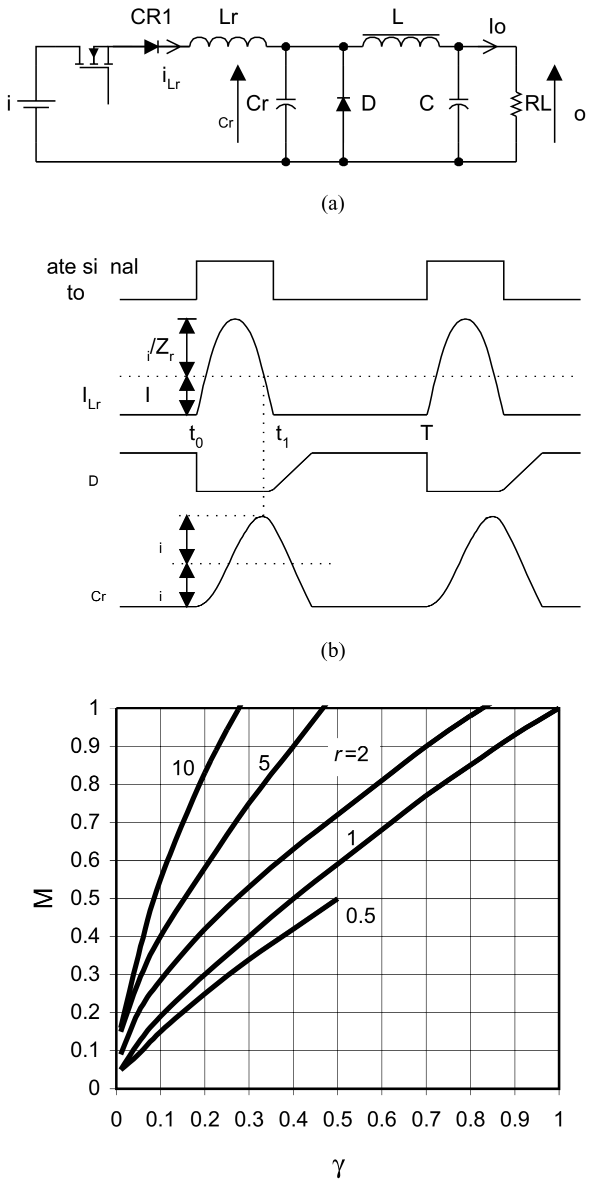
In a ZV resonant switch, a capacitor C_r is connected in parallel with the switch *S* for achieving zero-voltage-switching (ZVS). If the switch *S* is a unidirectional switch, the voltage across the capacitor C_r can oscillate freely in both positive and negative half-cycle. Thus, the resonant switch can operate in *full-wave* mode. If a diode is connected in antiparallel with the unidirectional switch, the resonant capacitor voltage is clamped by the diode to zero during the negative half-cycle. The resonant switch will then operate in *half-wave* mode. The objective of a ZV switch is to use the resonant circuit to shape the switch voltage waveform during off time in order to create a zero-voltage condition for the switch to turn on [13].

15.4 uasi-Resonant Converters

Quasi-resonant converters (QRCs) can be considered a hybrid of resonant and PWM converters. The underlying principle is to replace the power switch in PWM converters with the resonant switch. A large family of conventional converter circuits can be transformed into their resonant converter counterparts. The switch current and/or voltage waveforms are forced to oscillate in a quasi-sinusoidal manner, so that ZCS and/or ZVS can be achieved. Both ZCS-QRCs and ZVS-QRCs have *half-wave* and *full-wave* modes of operation [8–10, 12].

15.4.1 CS- RCs

A ZCS-QRC designed for *half-wave* operation is illustrated with a buck-type dc-dc converter. The schematic is shown in Fig. 15.5a. It is formed by replacing the power switch in a conventional PWM buck converter with the ZC resonant switch in Fig. 15.3a. The circuit waveforms in steady state are shown in Fig. 15.5b. The output filter inductor L_f is sufficiently large so that its current is approximately constant. Prior to turning the switch on, the output current I_o freewheels through the output diode D_f. The resonant capacitor voltage V_{Cr} equals zero. At t_0, the switch is turned on with ZCS. A quasi-sinusoidal current I_S flows through L_r and C_r, the output filter, and the load. Then *S* is softly commutated at t_1 with ZCS again. During and after the gate pulse, the resonant capacitor voltage V_{Cr} rises and then decays at a rate depending on the output current. Output voltage regulation is achieved by controlling the switching frequency. Operation and characteristics of the converter depend mainly on the design of the resonant circuit $L_r - C_r$. The following parameters are defined: voltage conversion ratio *M*, characteristic



(a)

(b)

(c)

FIGURE 15.5 Half-wave, quasi-resonant buck converter with ZCS: (a) Schematic diagram; (b) circuit waveforms; and (c) relationship between M and γ.

impedance Z_r, resonant frequency f_r, normalized load resistance r, and normalized switching frequency γ.

$$M = \frac{V_o}{V_i} \tag{15.1a}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{15.1b}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{15.1c}$$

$$r = \frac{R_L}{Z_r} \tag{15.1d}$$

$$\gamma = \frac{f_s}{f_r} \tag{15.1e}$$

It can be seen from the waveforms that if $I_o > V_i/Z_r$, I_S will not come back to zero naturally and the switch will have to be forced off, thus resulting in turn-off losses. The relationships between M and γ at different r are shown in Fig. 15.5c. It can be seen that M is sensitive to the load variation. At light load conditions, the unused energy is stored in C_r, leading to an increase in the output voltage. Thus, the switching frequency has to be controlled in order to regulate the output voltage.

If an antiparallel diode is connected across the switch, the converter will be operating in *full-wave* mode. The circuit schematic is shown in Fig. 15.6a. The circuit waveforms in steady state are shown in Fig. 15.6b. The operation is similar to the one in *half-wave* mode. However, the inductor current is allowed to reverse through the antiparallel diode and the duration for the resonant stage is lengthened. This permits excess energy in the resonant circuit at light loads to be transferred back to the voltage source V_i. This significantly reduces the dependence of V_o on the output load. The relationships between M and γ at different r are shown in Fig. 15.6c. It can be seen that M is insensitive to load variation.

By replacing the switch in the conventional converters, a family of QRC [9] with ZCS is shown in Fig. 15.7.

15.4.2 VS- RC

In these converters, the resonant capacitor provides a zero-voltage condition for the switch to turn on and off. A quasi-resonant buck converter designed for *half-wave* operation is shown in Fig. 15.8a using a ZV resonant switch in Fig. 15.4b. The steady-state circuit waveforms are shown in Fig. 15.8b. Basic relations of ZVS-QRCs are given in Eqs. (1a)–(1e). When the switch S is turned on, it carries output current I_o. The supply voltage V_i reverse-biases the diode D_f. When the switch is zero-voltage (ZV) turned off, the output current starts to flow through the resonant capacitor C_r. When the resonant capacitor voltage V_{Cr} is equal to V_i, D_f turns on. This starts the resonant stage. When V_{Cr} equals zero, the antiparallel diode turns on. The resonant capacitor is shorted and the source voltage is applied to the resonant inductor L_r. The resonant inductor current I_{Lr} increases linearly until it reaches I_o. Then D_f turns off. In order to achieve ZVS, S should be triggered during the time when the antiparallel diode conducts. It can be seen from the waveforms that the peak amplitude of the resonant capacitor voltage should be greater or equal to the input voltage (i.e., $I_o Z_r > V_{in}$). From Fig. 15.8c,

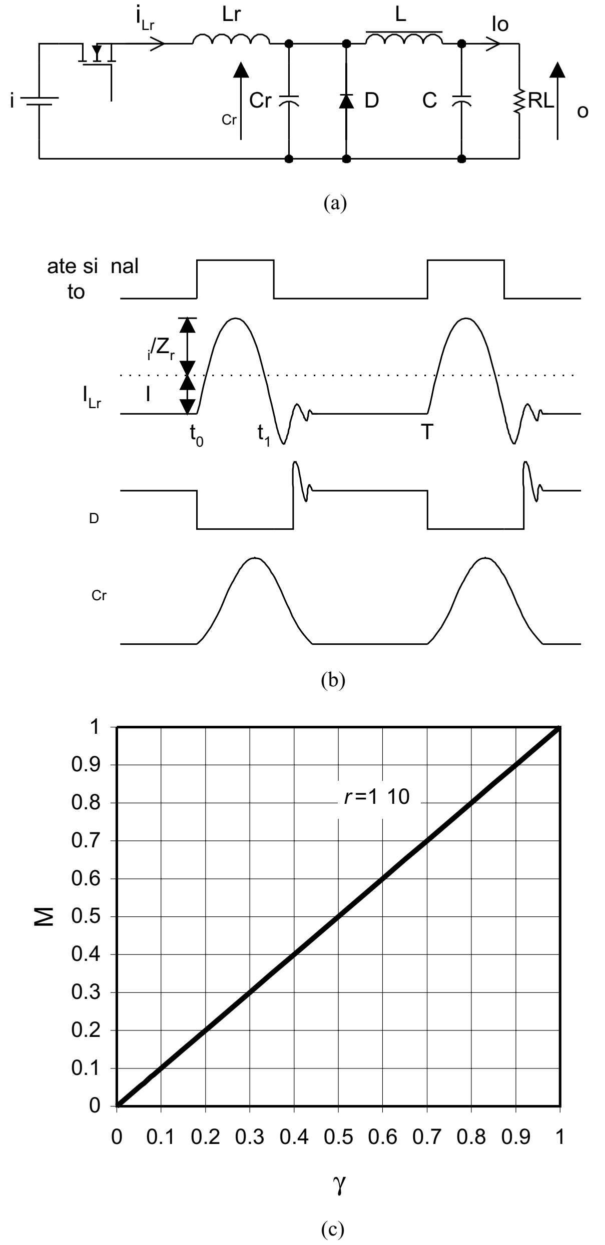


FIGURE 15.6 Full-wave, quasi-resonant buck converter with ZCS: (a) Schematic diagram; (b) circuit waveforms; and (c)relationship between M and γ.

it can be seen that the voltage conversion ratio is load-sensitive. In order to regulate the output voltage for different loads r, the switching frequency should also be changed accordingly.

Zero-voltage-switching converters can be operated in *full-wave* mode. The circuit schematic is shown in Fig. 15.9a. The circuit waveforms in steady state are shown in Fig. 15.9b. The operation is similar to *half-wave* mode of operation, except that V_{Cr} can swing between positive and negative voltages. The relationships between M and γ at different r are shown in Fig. 15.9c.

By comparing Fig. 15.8c with Fig. 15.9c, it can be seen that M is load-insensitive in *full-wave* mode. This is a desirable feature. However, as the series diode limits the direction of the switch current, energy will be stored in the output capacitance of the switch and will dissipate in the switch during turn-on. Hence, the *full-wave* mode has the problem of capacitive turn-on loss, and is less practical in *high-frequency* operation. In practice, ZVS-QRCs are usually operated in *half-wave* mode rather than *full-wave* mode.

By replacing the ZV resonant switch in the conventional converters, various ZVS-QRCs can be derived. They are shown in Fig. 15.10.

15.4.3 Comparisons Between CS and VS

The ZCS can eliminate the switching losses at turn-off and reduce the switching losses at turn-on. As a relatively large capacitor is connected across the output diode during resonance, the converter operation becomes insensitive to the diode's junction capacitance. When power MOSFETs are zero-current switched on, the energy stored in the device's capacitance will be dissipated. This capacitive turn-on loss is proportional to the switching frequency. During turn-on, a considerable rate of change of voltage can be coupled to the gate drive circuit through the Miller capacitor, thus increasing switching loss and noise. Another limitation is that the switches are under high-current stress, resulting in higher conduction loss. However, it should be noted that ZCS is particularly effective in reducing switching loss for power devices (such as IGBT) with large tail current in the turn-off process.

The ZVS eliminates the capacitive turn-on loss. It is suitable for high-frequency operation. For single-ended configuration, the switches could suffer from excessive voltage stress, which is proportional to the load. It will be shown in Section 15.5 that the maximum voltage across switches in half-bridge and full-bridge configurations is clamped to the input voltage.

For both ZCS and ZVS, output regulation of the resonant converters can be achieved by variable frequency control. The ZCS operates with constant on-time control, while ZVS operates with constant off-time control. With a wide input and load range, both techniques have to operate with a wide switching frequency range, making it difficult to design resonant converters optimally.

15.5 VS in igh- re uency Applications

By the nature of the resonant tank and ZCS, the peak switch current in resonant converters is much higher than that in the square-wave counterparts. In addition, a high voltage will be established across the switch in the off state after the resonant

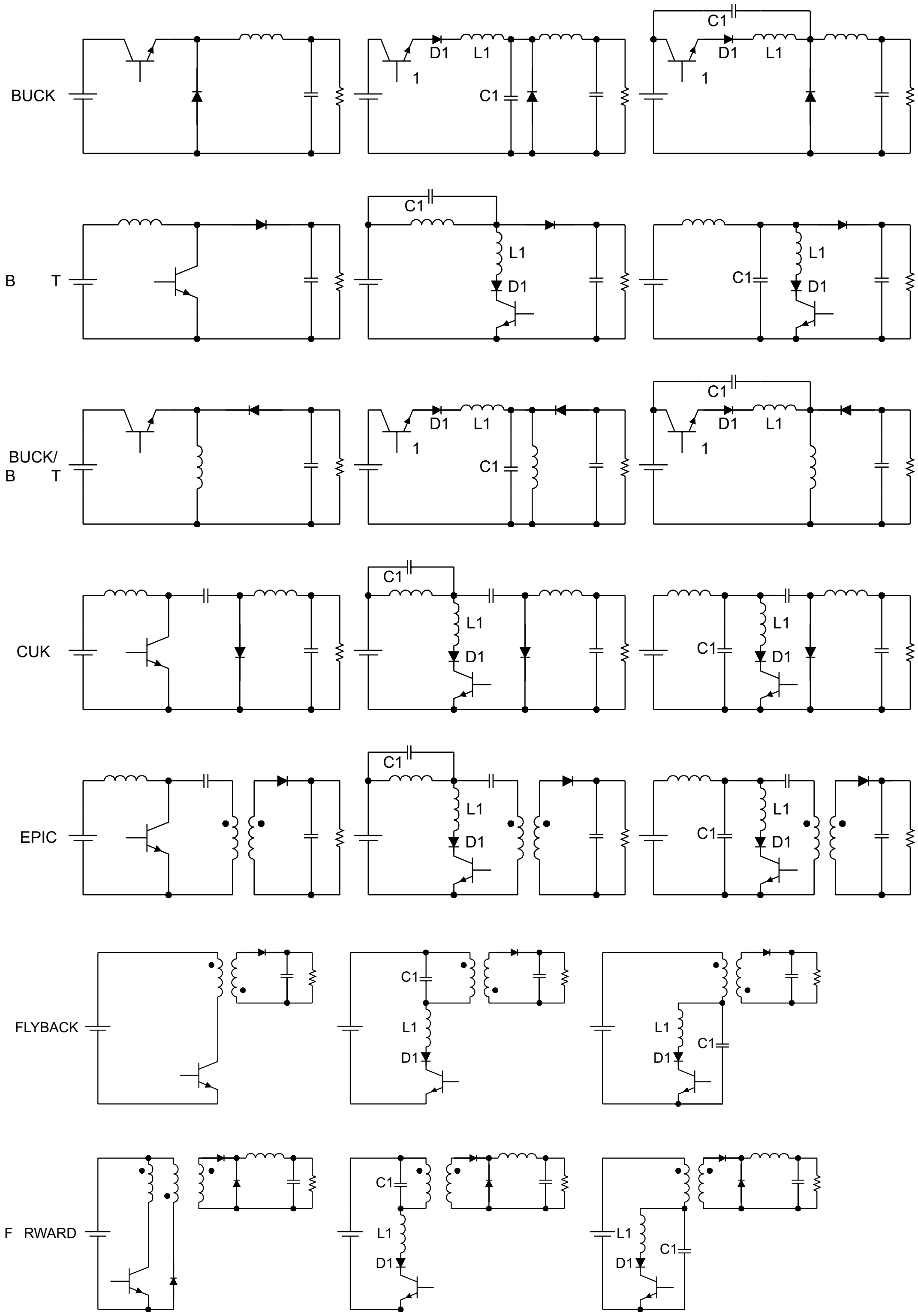

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FIGURE 15.7 A family of quasi-resonant converters with ZCS.

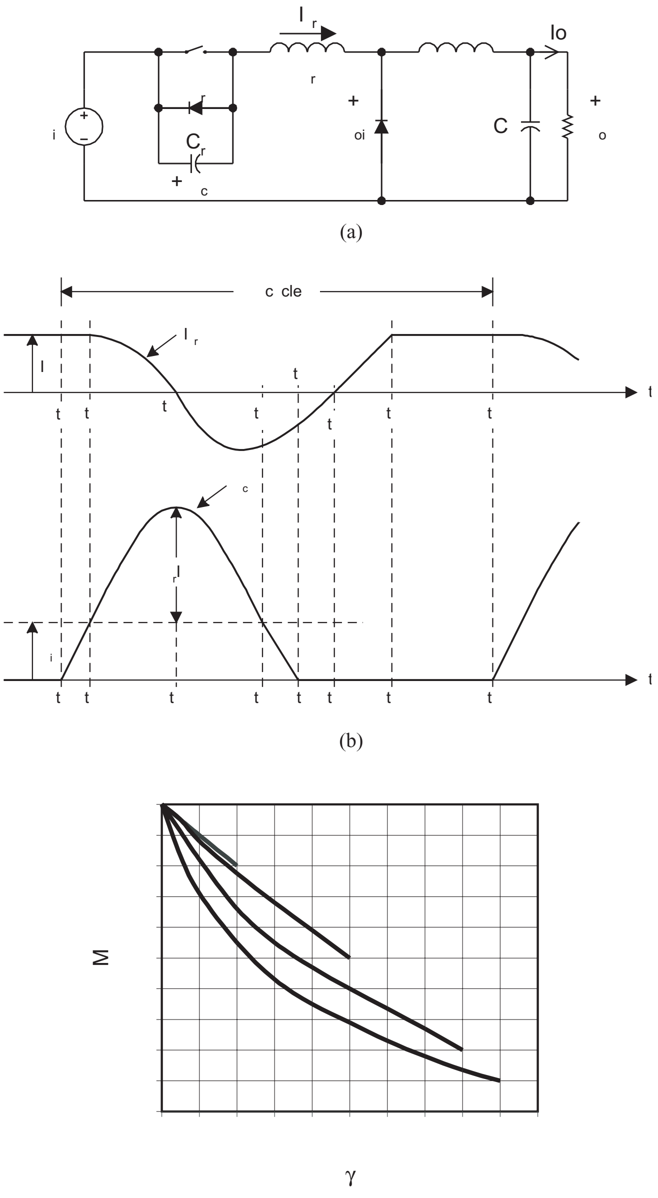
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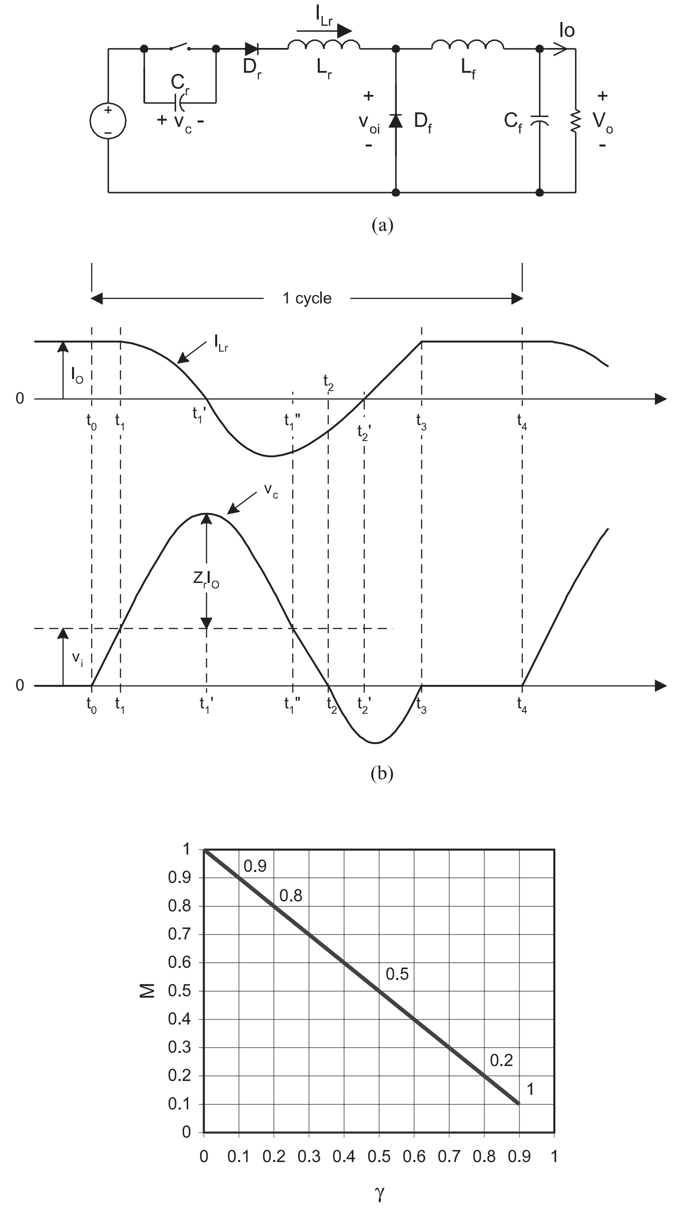
FIGURE 15.8 Half-wave, quasi-resonant buck converter with ZVS: (a) Schematic diagram; (b) circuit waveforms; and (c) relationship between M and γ.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(a)

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FIGURE 15.9 Full-wave, quasi-resonant buck converter with ZVS: (a) Schematic diagram; (b) circuit waveforms; and (c) relationship between M and γ.

stage. When the switch is switched on again, the energy stored in the output capacitor will be discharged through the switch, causing a significant power loss at high frequencies and voltages. This switching loss can be reduced by using ZVS.

The ZVS can be viewed as square-wave power utilizing a constant off-time control. Output regulation is achieved by controlling the on time or switching frequency. During the off time, the resonant tank circuit traverses the voltage across the switch from zero to its peak value and then back to zero again. At that ZV instant, the switch can be reactivated. Apart from conventional single-ended converters, some other examples of converters with ZVS are illustrated in the following section.

15.5.1 VS with Clamped Voltage

The high-voltage stress problem in the single-switch configuration with ZVS can be avoided in half-bridge (HB) and full-bridge (FB) configurations [14]–[17]. The peak switch voltage can be clamped to the dc supply rail, and thus reduces the switch voltage stress. In addition, the series transformer leakage and circuit inductance can form parts of the resonant

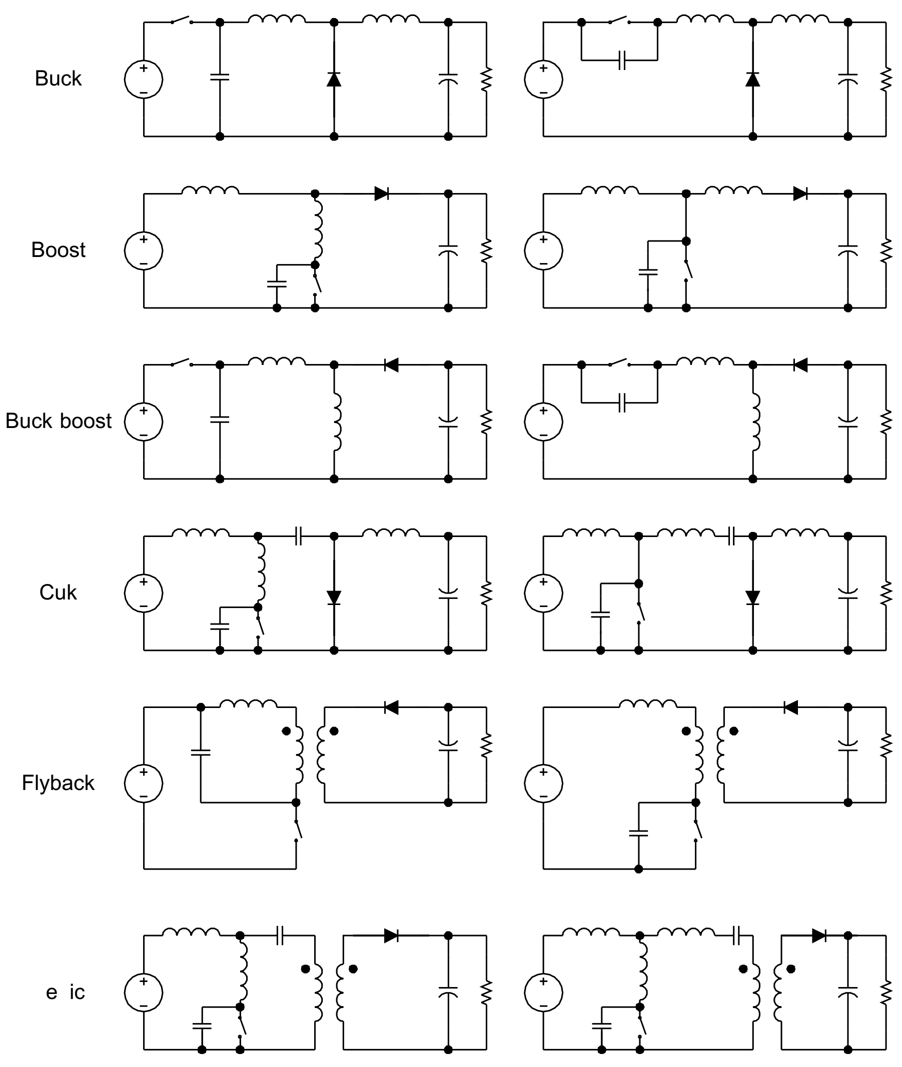

FIGURE 15.10 A family of quasi-resonant converters with ZVS.

path. Therefore, these parasitic components, which are undesirable in hard-switched converters, become useful components in ZVS ones. Figures 15.11 and 15.12 show the ZVS HB and FB circuits, respectively, together with the circuit waveforms. The resonant capacitor is equivalent to the parallel connection of the two capacitors ($C_r/2$) across the switches. The off-state voltage of the switches will not exceed the input voltage during resonance because they will be clamped to the supply rail by the antiparallel diode of the switches.

15.5.2 Phase-Shifted Converter with Zero Voltage Transition

In a conventional FB converter, the two diagonal switch pairs are driven alternatively. The output transformer is fed with an ac rectangular voltage. By applying a phase-shifting approach, a deliberate delay can be introduced between the gate signals to the switches [18]. The circuit waveforms are shown in Fig. 15.13. Two upper or lower switches can be conducting (either through the switch or the antiparallel diode), yet the applied voltage to the transformer is zero. This zero-voltage condition appears in the interval $[t_1, t_2]$ of V_{pri} in Fig. 15.13. This operating stage corresponds to the required off time for that particular switching cycle. When the desired switch is turned off, the primary transformer current flows into the switch output capacitance and this causes the switch voltage to resonate to the opposite input rail. Effects of the parasitic circuit components are used advantageously to facilitate the resonant transitions. This enables a ZVS condition for turning on the opposite switch. Thus, varying the phase shift controls the effective duty cycle and hence the output power. The resonant circuit is necessary to meet the requirement of providing sufficient inductive energy to drive the capacitors to the opposite bus rail. The resonant transition must be achieved within the designed transition time.

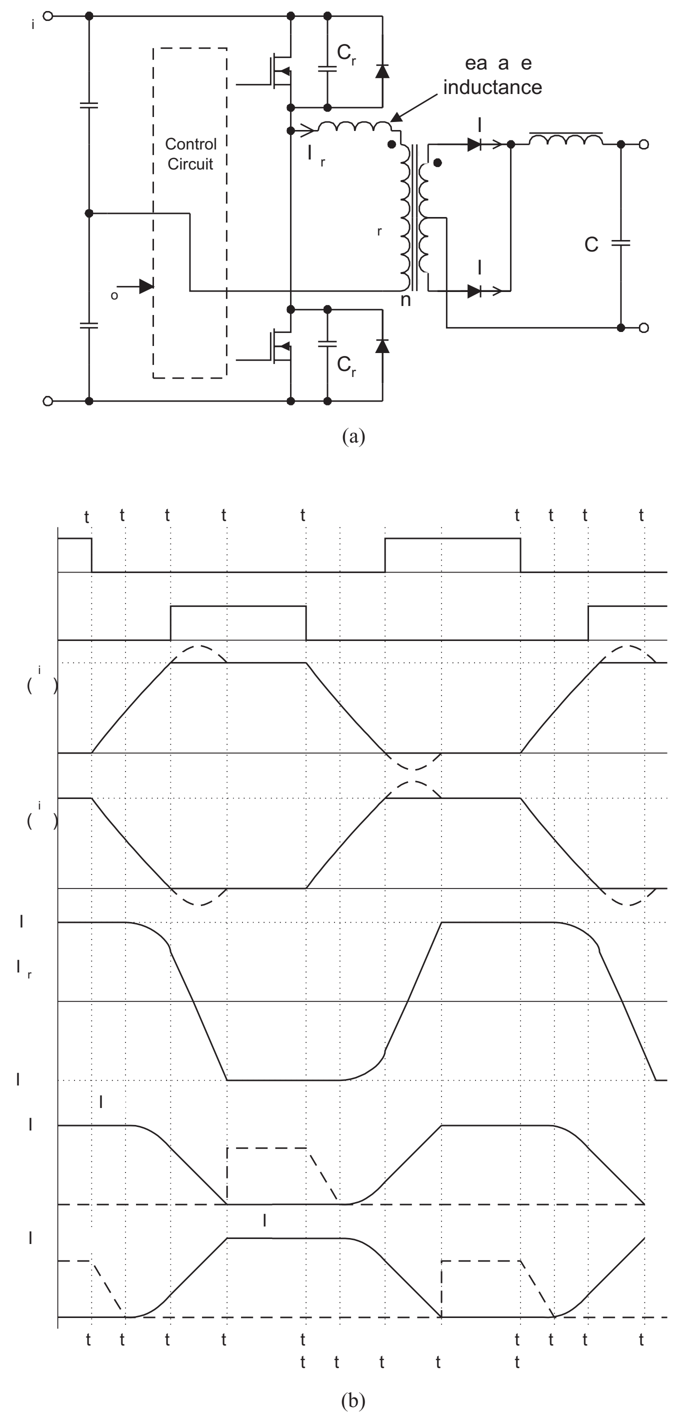
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FIGURE 15.11 Half-bridge converter with ZVS. (a) Circuit diagram; and (b) circuit waveforms.

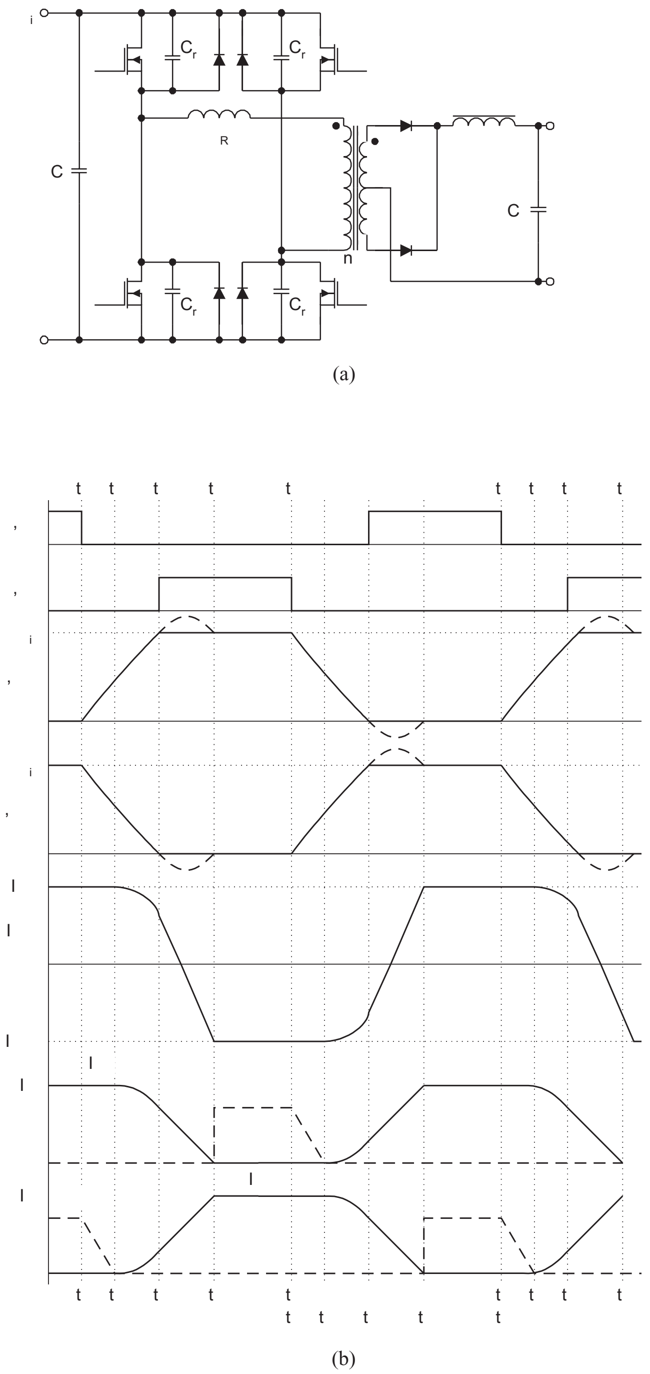
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FIGURE 15.12 Full-bridge converter with ZVS. (a) Circuit schematic; and (b) circuit waveforms.

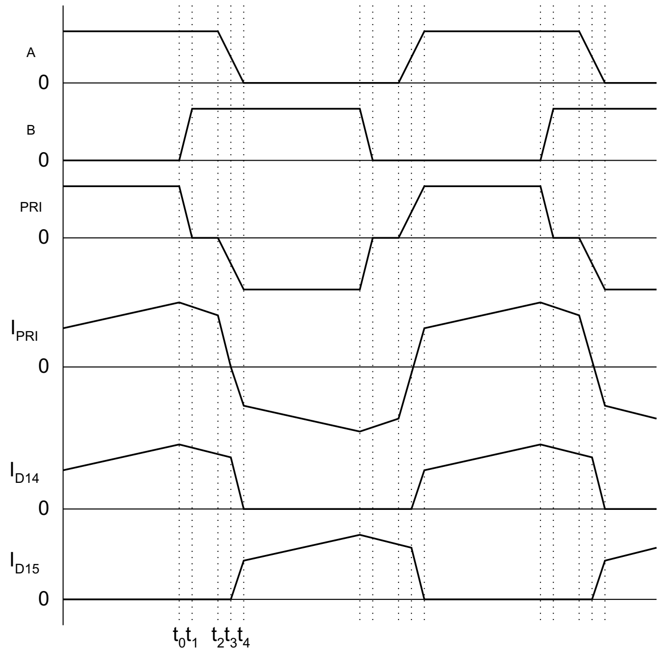


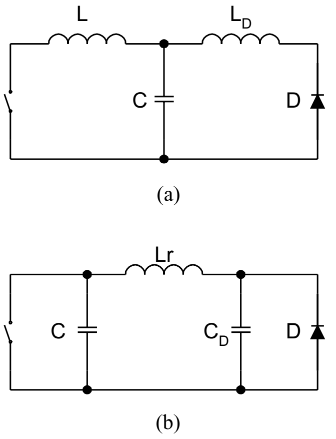
FIGURE 15.13 Circuit waveforms of the phase-shifted, ZVT FB converter.

15.6 Multiresonant Converters MRC

Both ZCS- and ZVS-QRCs optimize the switching condition for either the active switch or the output diode only, but not for both of them simultaneously. The multiresonant switch concept, which is an extension of the concept of the resonant switch, has been developed to overcome such a limitation. The zero-current multiresonant (ZC-MR) and zero-voltage multiresonant (ZV-MR) switches [12], [17] are shown in Fig. 15.14. The multiresonant circuits incorporate all major parasitic components, including switch output capacitance, diode junction capacitance, and transformer leakage inductance into the resonant circuit. In general, ZVS (*half-wave* mode) is more favorable than ZCS in dc-dc converters for high-frequency operation because the parasitic capacitance of the active switch and the diode will form part of the resonant circuit.

An example of a buck ZVS-MRC is shown in Fig. 15.15. Depending on the ratio of the resonant capacitance C_D/C_S, two possible topological modes, namely mode I and mode II, can be operated [20]. The ratio affects the time at which the voltages across the switch S and the output diode D_f become zero. Their waveforms are shown in Fig. 15.16a, b, respectively. If diode voltage V_D falls to zero earlier than switch voltage V_S, the converter will follow mode I. Otherwise, the converter follows mode II.

Instead of having one resonant stage, there are three in this converter. The mode I operation in Fig. 15.16a is described first. Before the switch S is turned on, the output diode D_f is conducting and the resonant inductor current I_{Lr} is negative (flowing through the antiparallel diode of S). Then S is then turned on with ZVS. The resonant inductor current I_{Lr} increases linearly and D_f is still conducting. When I_{Lr} reaches the output current I_o, the first resonant stage starts. The resonant circuit is formed by the resonant inductor L_r and the capacitor C_D across the output diode. This stage ends when S is turned off with ZVS. Then, a second resonant stage starts. The resonant circuit consists of L_r, C_D, and the capacitor across the switch C_s. This stage ends when the output diode becomes forward-biased. A third resonant stage will then start. Here L_r and C_s form the resonant circuit. This stage ends and completes one operation cycle when the diode C_s becomes forward-biased.



(a)

(b)

FIGURE 15.14 Multiresonant switches: (a) ZC-MR switch; and (b) ZV-MR switch.

The only difference between mode I and mode II in Fig. 15.16b is in the third resonant stage, in which the resonant circuit is formed by L_r and C_D. This stage ends when D_f becomes forward-biased. The concept of the multiresonant switch can be applied to conventional converters [19–21]. A family of MRCs is shown in Fig. 15.17.

Although the variation of switching frequency for regulation in MRCs is smaller than that of QRCs, a wide-band frequency modulation is still required. Hence, the optimal design of magnetic components and the EMI filters in MRCs is not easy. It would be desirable to have a constant switching frequency operation. In order to operate the MRCs with constant switching frequency, the diode in Fig. 15.14 can be

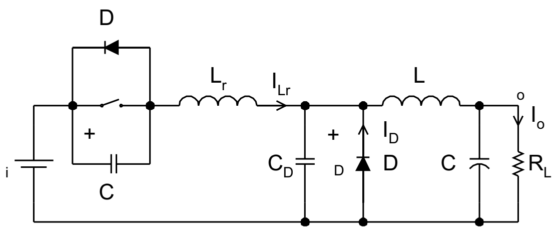
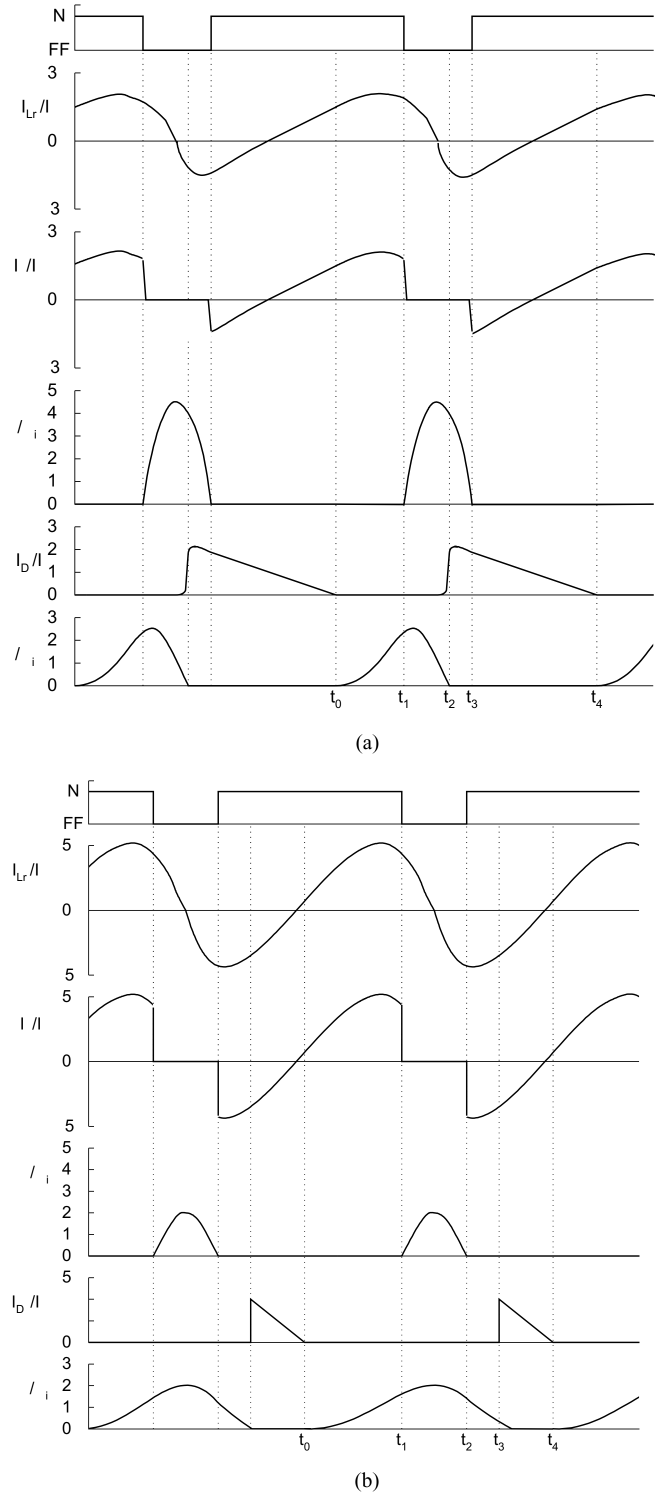


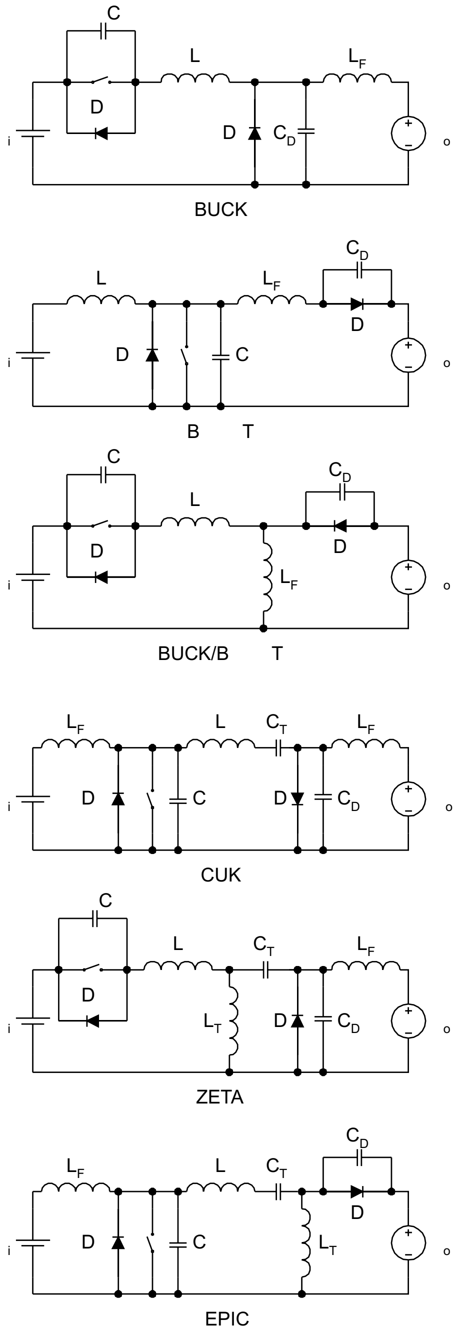
FIGURE 15.15 Buck ZVS-MRC.



(a)

(b)

FIGURE 15.16 Possible modes of the buck ZVS-MRC: (a) mode I; and (b) mode II.


C
L
L_F
D
D
C_D
i
o
BUCK
C_D
L
L_F
D
D
C
B
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C
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L_F
BUCK/B
T
L_F
L
C_T
L_F
D
C
D
C_D
CUK
C
L
C_T
L_F
D
L_T
D
C_D
ZETA
C_D
L_F
L
C_T
D
D
C
L_T
EPIC

FIGURE 15.17 Use of the multiresonant switch in conventional PWM converters.

replaced with an active switch S_2 [22]. A constant-frequency multiresonant (CF-MR) switch is shown in Fig. 15.18. The output voltage is regulated by controlling the on-time of the two switches. This concept can be illustrated with the buck converter as shown in Fig. 15.19, together with the gate drive waveforms and operating stages. Both S_1 and S_2 are turned on during the time when currents flow through the antiparallel diodes of S_1 and S_2. This stage ends when S_2 is turned off with ZVS. The first resonant stage is then started. The resonant circuit is formed by L_r and C_{S2}. A second resonant stage begins. Then L_r resonates with C_{S1} and C_{S2}. The voltage across

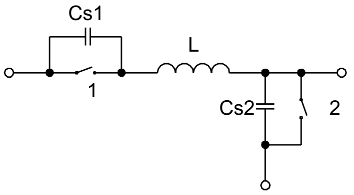
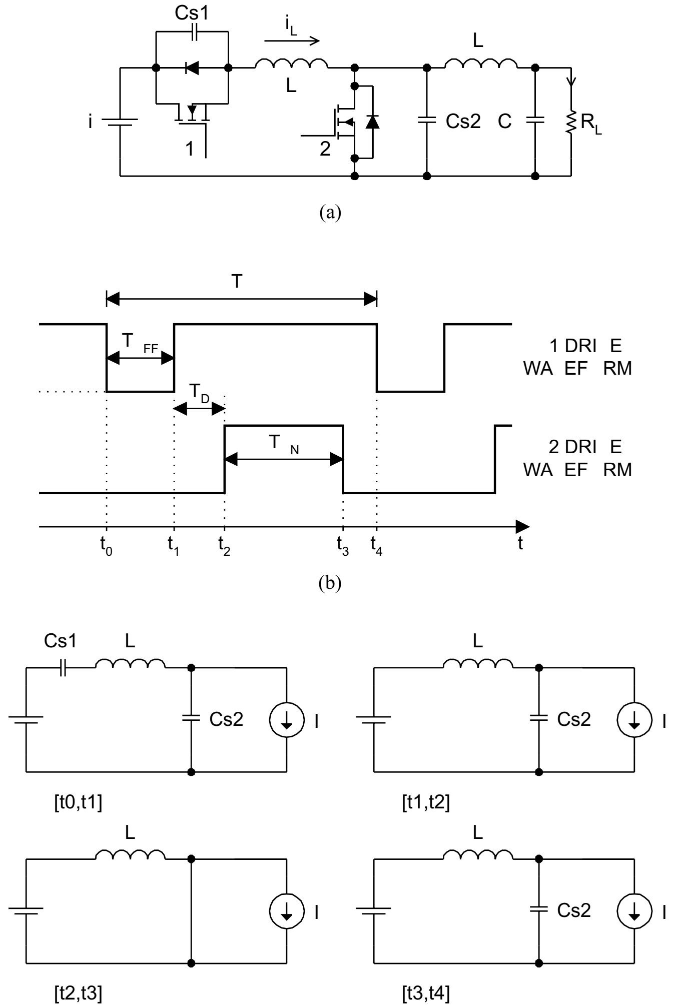


FIGURE 15.18 Constant frequency multiresonant switch.

S_1 oscillates to zero. When I_{Lr} becomes negative, S_1 will be turned on with ZVS. Then L_r resonates with C_{S2}. When current flows through D_{S2} S_2 will be turned on. As the output voltage is the average voltage across S_2, output voltage regulation is achieved by controlling the conduction time of S_2.

All switches in MRCs operate with ZVS, which reduces switching losses and switching noise and eliminates oscillation due to the parasitic effects of the components (such as the junction capacitance of the diodes). However, all switches are under high-current and voltage stresses, resulting in an increase in the conduction loss.


Cs1
i_L
L
L
i
1
2
Cs2 C
R_L
T
T FF
T D
T N
1 DRI E WA EF RM
2 DRI E WA EF RM
t_0 t_1 t_2 t_3 t_4 t
Cs1 L
Cs2
I
[t0,t1]
L
Cs2
I
[t1,t2]
L
I
[t2,t3]
L
Cs2
I
[t3,t4]

(a)

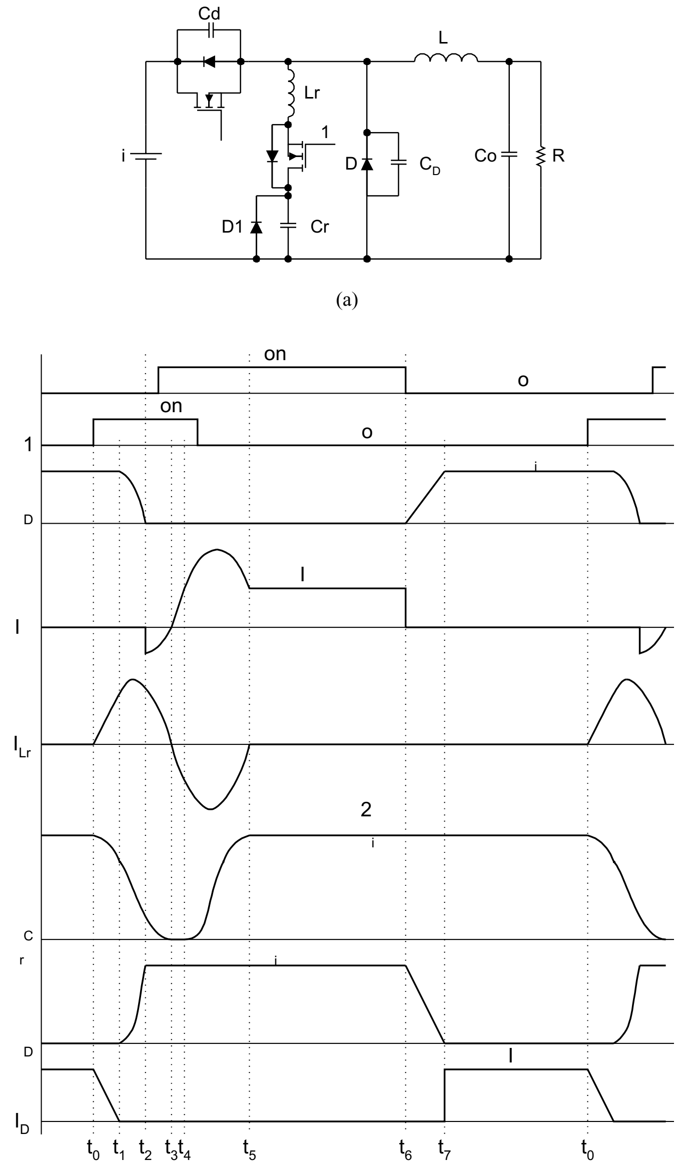
(b)

(c)

FIGURE 15.19 Constant frequency buck MRC: (a) Circuit schematics; (b) gate drive waveforms; and (c) operating stages.

15.7 Zero-Voltage-Transition (ZVT) Converters

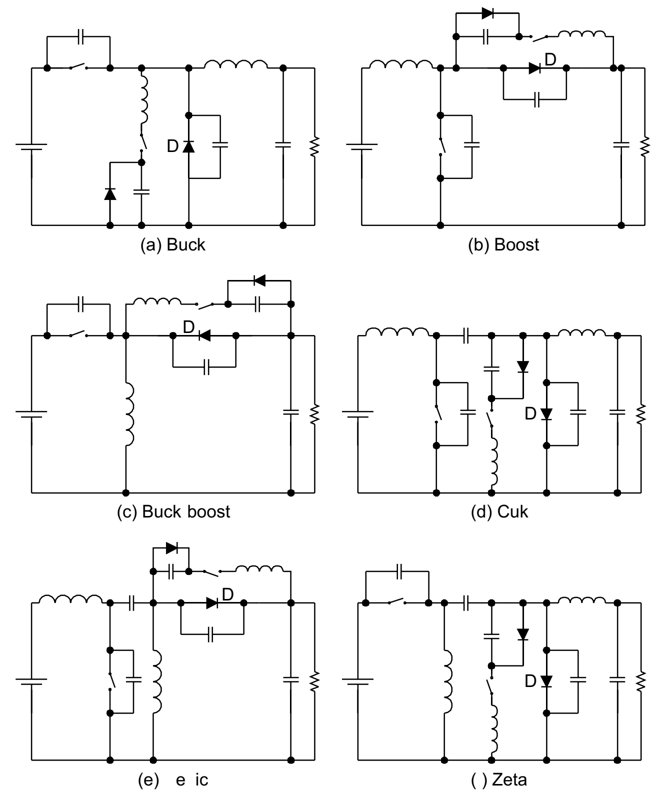
By introducing a resonant circuit in parallel with the switches, the converter can achieve ZVS for both power switch and diode without significantly increasing their voltage and current stresses [23]. Figure 15.20a shows a buck-type ZVT-


Cd
L
Lr
1
i
D
C_D
Co
R
D1
Cr
on
o
on
1
o
D
i
I
I
I_{Lr}
2
i
C
r
i
D
I
I_D
t_0 t_1 t_2 $t_3 t_4$ t_5 t_6 t_7 t_0

(a)

(b)

FIGURE 15.20 Buck ZVT-PWM converter: (a) Circuit schematics; and (b) circuit waveforms.


(a) Buck (b) Boost

(c) Buck boost (d) Cuk

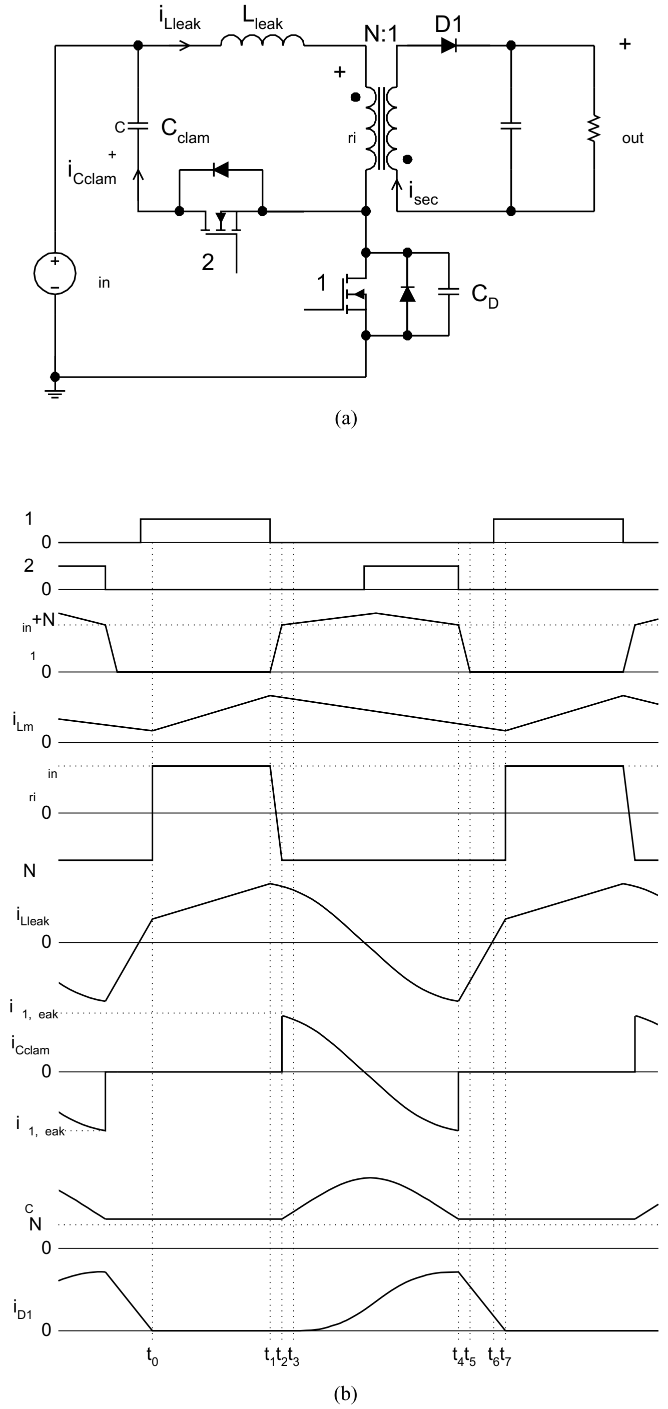
(e) e ic ( ) Zeta

FIGURE 15.21 Conventional ZVT-PWM converters.

PWM converter and Figure 15.20b shows the associated waveforms. The converter consists of a main switch S and an auxiliary switch S_1. It can be seen that the voltage and current waveforms of the switches are like squarewave type except during turn-on and turn-off switching intervals, where ZVT takes place. The main switch and the output diode are under ZVS and are subjected to low voltage and current stresses. The auxiliary switch is under ZCS, resulting in low switching loss.

The concept of ZVT can be extended to other PWM circuits by adding the resonant circuit. Some basic ZVT-PWM converters are shown in Fig. 15.21.

15.8 Nondissipative Active Clamp Network


(a)

(b)

FIGURE 15.22 Active clamp flyback converter: (a) Circuit schematics; and (b) circuit waveforms.

The active-clamp circuit can utilize the transformer leakage inductance energy and can minimize the turn-off voltage stress in the isolated converters. The active clamp circuit provides a means of achieving ZVS for the power switch and reducing the rate of change of the diode's reverse recovery current. An example of a flyback converter with active clamp is shown in Fig. 15.22a and the circuit waveforms are shown in Fig. 15.22b. Clamping action is obtained by using a series combination of an active switch (i.e., S_2) and a large capacitor so that the voltage across the main switch (i.e., S_1) is clamped to a minimum value. Then S_2 is turned on with ZVS. However, S_2 is turned off with finite voltage and current, and has turn-off switching loss. The clamp-mode ZVS-MRCs is discussed in References [24–26].

15. Load Resonant Converters

Load resonant converters (LRCs) have many distinct features over conventional power converters. Due to the soft commutation of the switches, no turn-off loss or stress is present. These LRCs are especially well-suited for high-power applications because they allow high-frequency operation for equipment size/weight reduction, without sacrificing conversion efficiency and imposing extra stress on the switches. Basically, LRCs can be divided into three different configurations, namely series resonant converters, parallel resonant converters, and series-parallel resonant converters.

15. .1 Series Resonant Converters

Series resonant converters (SRCs) have their load connected in series with the resonant tank circuit, which is formed by L_r and C_r [15, 27–29]. The half-bridge configuration is shown in Fig. 15.23. When the resonant inductor current i_{Lr} is positive, it flows through T_1 if T_1 is on; otherwise it flows through diode D_2. When i_{Lr} is negative, it flows through T_2 if T_2 is on; otherwise it flows through diode D_1. In steady-state symmetrical operation, both active switches are operated in a complementary manner. Depending on the ratio between the switching frequency ω_S and the converter resonant frequency ω_r, the converter has several possible operating modes.

15. .1.1 Discontinuous Conduction Mode with $\omega_S < 0.5\omega_r$

Figure 15.24a shows the waveforms of i_{Lr} and the resonant capacitor voltage v_{Cr} in this mode of operation. From 0 to t_1, T_1 conducts. From t_1 to t_2, the current in T_1 reverses its direction. The current flows through D_1 and back to the supply source. From t_2 to t_3, all switches are in the off state. From t_3 to t_4, T_2 conducts. From t_4 to t_5, the current in T_2 reverses its direction. The current flows through D_2 and back to the supply source. Both T_1 and T_2 are switched on under ZCS condition and they are switched off under zero current and zero voltage conditions. However, the switches are under high current stress in this mode of operation and thus have higher conduction loss.

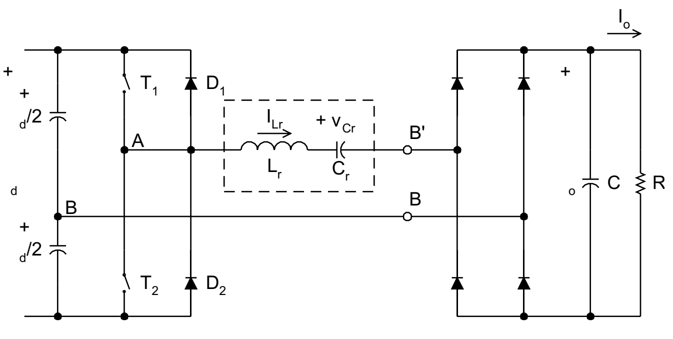


FIGURE 15.23 An SRC half-bridge configuration.

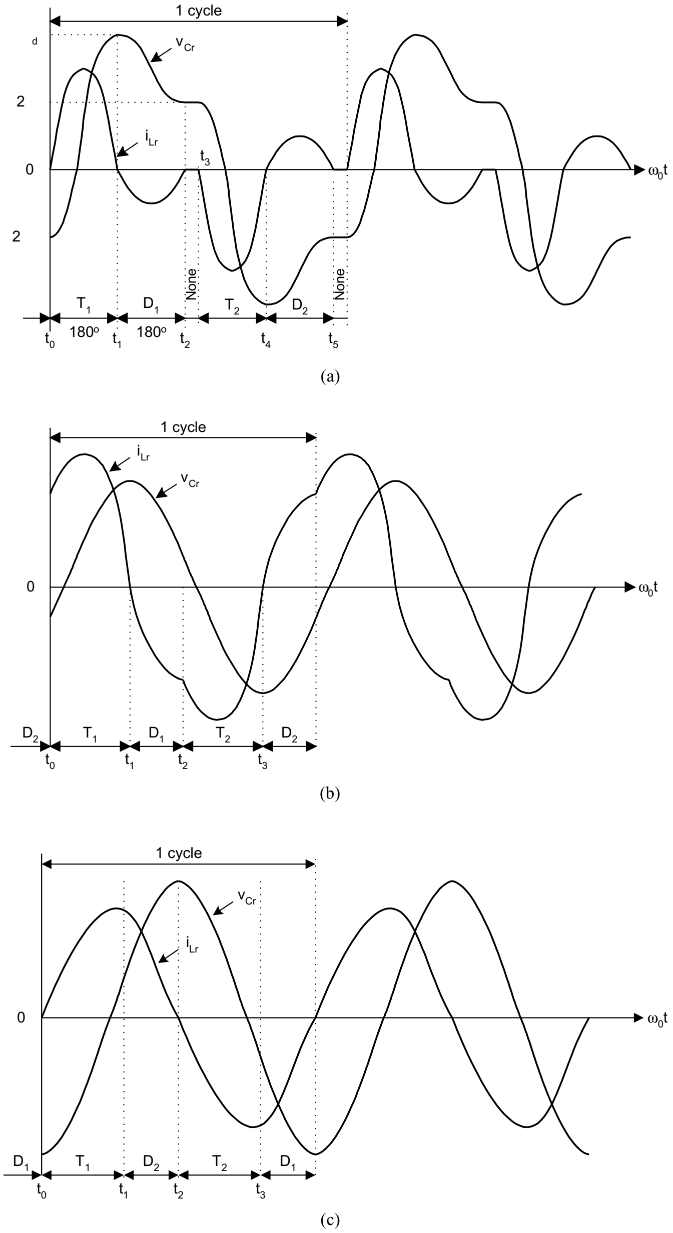


FIGURE 15.24 Circuit waveforms under different operating conditions: (a) $\omega_S < 0.5\omega_r$; (b) $0.5\ \omega_r < \omega_S$; and (c) $\omega_r < \omega_S$.

15. .1.2 Continuous Conduction Mode with $0.5\omega_r < \omega_S < \omega_r$

Figure 15.24b shows the circuit waveforms. From 0 to t_1, i_{Lr} transfers from D_2 to T_1. When T_1 is switched on with finite switch current and voltage, turn-on switching loss will result. Moreover, the diodes must have good reverse recovery characteristics in order to reduce the reverse recovery current. From t_1 to t_2, D_1 conducts and T_1 is turned off softly with zero voltage and zero current. From t_2 to t_3, T_2 is switched on with finite switch current and voltage. At t_3, T_2 is turned off softly and D_2 conducts until t_4.

15. .1.3 Continuous Conduction Mode with $\omega_r < \omega_S$

Figure 15.24e shows the circuit waveforms. From 0 to t_1, i_{Lr} transfers from D_1 to T_1. Thus, T_1 is switched on with zero current and zero voltage. At t_1, T_1 is switched off with finite voltage and current, resulting in turn-off switching loss. From t_1 to t_2, D_2 conducts. From t_2 to t_3, T_2 is switched on with zero current and zero voltage. At t_3, T_2 is switched off and i_{Lr} transfers from T_2 to D_1. As the switches are turned on with ZVS, lossless snubber capacitors can be added across the switches.

The following parameters are defined: voltage conversion ratio M, characteristic impedance Z_r; resonant frequency f_r; normalized load resistance r; and normalized switching frequency γ.

$$M = nV_o/V_{\text{in}} \tag{15.2a}$$

$$Z_r = \sqrt{L_r/C_r} \tag{15.2b}$$

$$f_r = 1/(2\pi\sqrt{L_rC_r}) \tag{15.2c}$$

$$r = n^2R_L/Z_r^T \tag{15.2d}$$

$$\gamma = f_s/f_r \tag{15.2e}$$

$$M = 1/\sqrt{(\gamma - 1/\gamma)^2/r^2 + 1} \tag{15.2f}$$

The relationships between M and γ for different value of r are shown in Fig. 15.25. The boundary between CCM and DCM is at $r = 1.27\gamma$. When the converter is operating in DCM and $0.2 < \gamma < 0.5$, $M = 1.27r\gamma$.

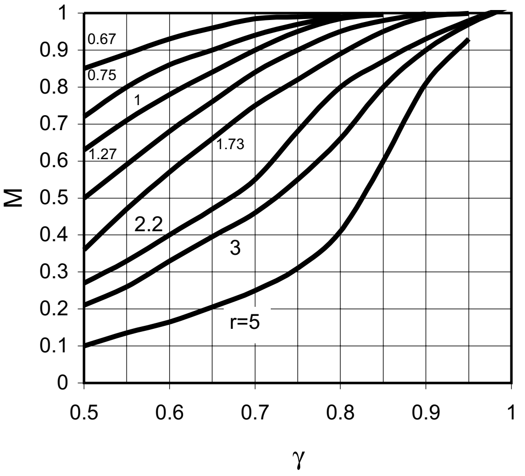


FIGURE 15.25 M vs γ in SRC.

The SRC has the following advantages. Transformer saturation can be avoided because the series capacitor can block the dc component. The light load efficiency is high because both device current and conduction loss are low. However, the major disadvantages are that there is difficulty in regulating the output voltage under light load and no load conditions. Moreover, the output dc filter capacitor has to carry high ripple current, which could be a major problem in low-output voltage and high-output current applications [29].

15. .2 Parallel Resonant Converters

Parallel resonant converters (PRCs) have their load connected in parallel with the resonant tank capacitor C_r [27–30]. The half-bridge configuration is shown in Fig. 15.26. The SRC behaves as a current source, whereas the PRC acts as a voltage source. For voltage regulation, PRC requires a smaller operating frequency range than the SRC to compensate for load variation.

15. .2.1 Discontinuous Conduction Mode

The steady-state waveforms of the resonant inductor current i_{Lr} and the resonant capacitor voltage v_{Cr} are shown in Fig. 15.27a. Initially both i_{Lr} and v_{Cr} are zero. From 0 to t_2, T_1 conducts and is turned on with zero current. When i_{Lr} is less than the output current I_o, i_{Lr} increases linearly from 0 to t_1 and the output current circulates through the diode bridge. From t_1 to t_3, L_r resonates with C_r. Starting from t_2, i_{Lr} reverses its direction and flows through D_1. Then T_1 is turned off with zero current and zero voltage. From t_3 to t_4, v_{Cr} decreases linearly due to the relatively constant value of I_o. At t_4, when v_{Cr} equals zero, the output current circulates through the diode bridge again. Both i_{Lr} and v_{Cr} will stay at zero for an interval. From t_5 to t_9, the preceding operations will be repeated for T_2 and D_2. The output voltage is controlled by adjusting the time interval of $[t_4, t_5]$.

15. .2.3 Continuous Conduction Mode $\omega_S < \omega_r$

This mode is similar to the operation in the DCM, but with a higher switching frequency. Both i_{Lr} and v_{Cr} become continuous. The waveforms are shown in Fig. 15.27b. The switches

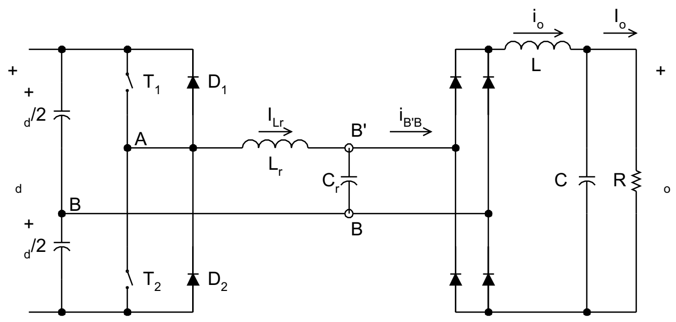


FIGURE 15.26 The PRC half-bridge configuration.

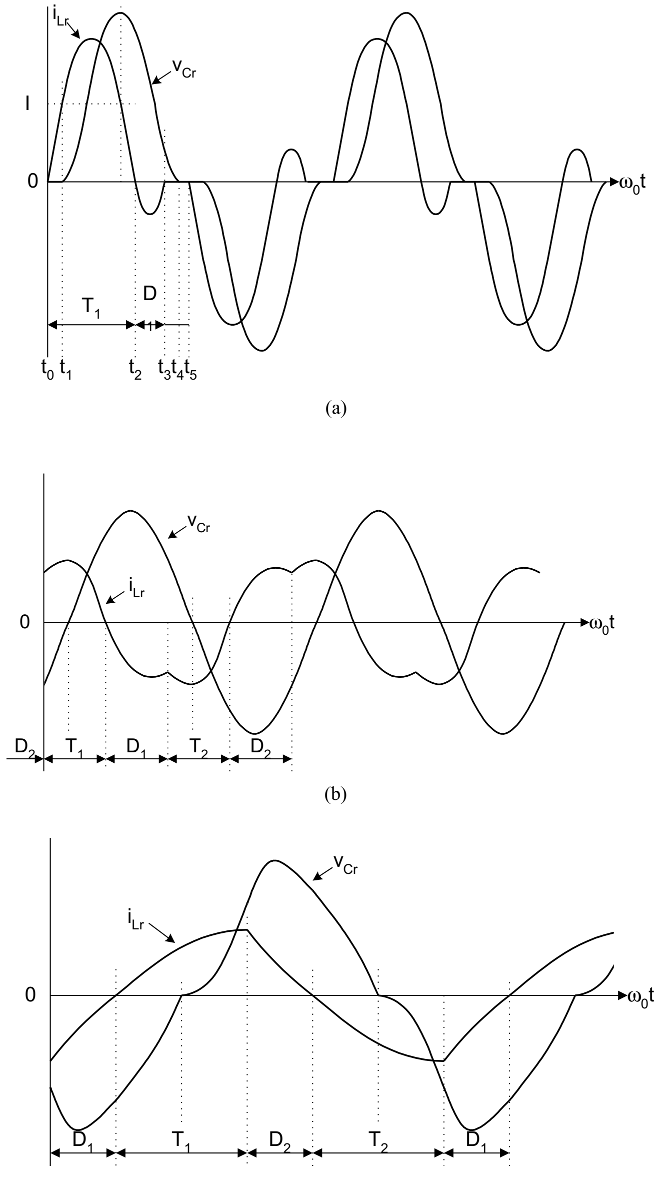


FIGURE 15.27 Circuit waveforms under different operating conditions: (a) Discontinuous conduction mode; (b) continuous conduction mode $\omega_S < \omega_r$; and (c) continuous conduction mode $\omega_S > \omega_r$.

T_1 and T_2 are hard turned on with finite voltage and current and are soft turned off with ZVS.

15. .2.3 Continuous Conduction Mode $\omega_S > \omega_r$

If the switching frequency is higher than ω_r, the antiparallel diode of the switch will be turned on before the switch is triggered. Thus, the switches are turned on with ZVS. However, the switches are hard turned off with finite current and voltage.

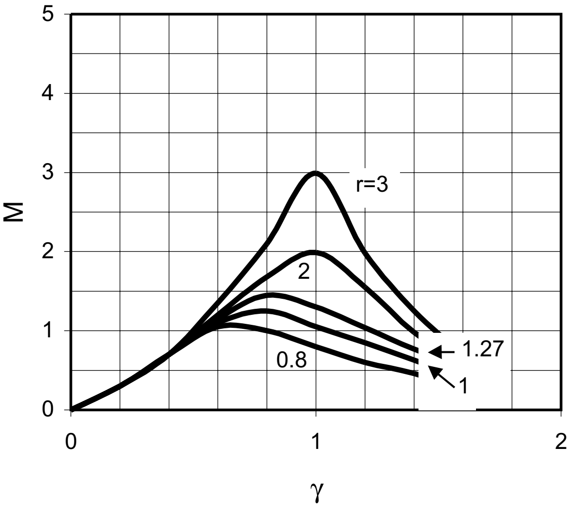


FIGURE 15.28 M vs γ in PRC.

The parameters defined in Eq. (15.2) are applicable. The relationships between M and γ for various values of r are shown in Fig. 15.28. During the DCM (i.e., $\gamma < 0.5$), M is in linear relationship with γ. Output voltage regulation can be achieved easily. The output voltage is independent of the output current. The converter shows good voltage source characteristics. It is also possible to step up and step down the input voltage.

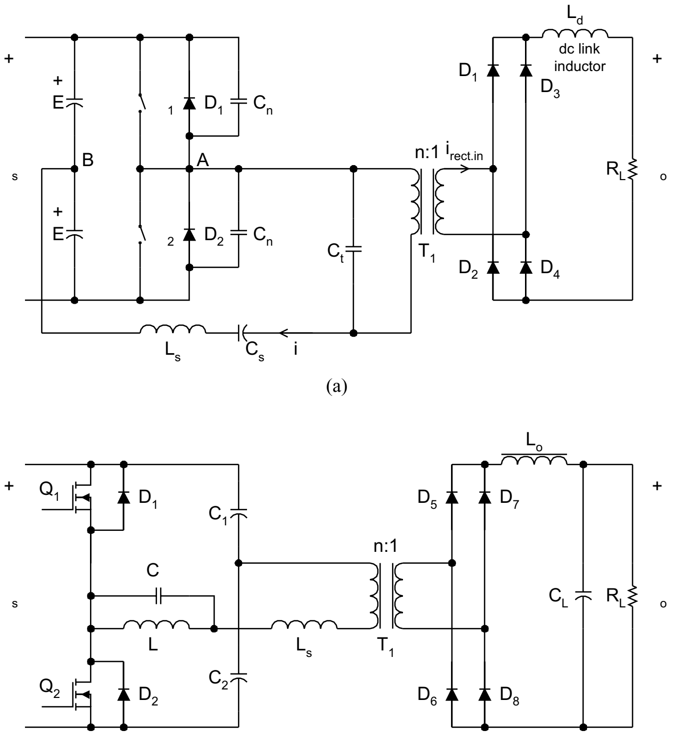


FIGURE 15.29 Different types of SPRC.: (a) LCC-type; and (b) LLC-type.

The PRC has the advantages that the load can be short-circuited and the circuit is suitable for low-output voltage, high-output current applications. However, the major disadvantage of the PRC is the high device current. Moreover, as device current does not decrease with the load, the efficiency drops with a decrease in the load [29].

15. .3 Series-Parallel Resonant Converter

The series-parallel resonant converter (SPRC) combines the advantages of the SRC and the PRC. The SPRC has an additional capacitor or inductor connected in the resonant tank circuit [29–31]. Figure 15.29a shows an LCC-type SPRC, in which an additional capacitor is placed in series with the resonant inductor. Figure 15.29b shows an LLC-type SPRC, in which an additional inductor is connected in parallel with the resonant capacitor in the SRC. However, there are many possible combinations of the resonant tank circuit. Detailed analysis can be found in Reference [31].

15.1 Control Circuits for Resonant Converters

Since 1985s, various control integrated circuits (ICs) for resonant converters have been developed. Some common ICs for different converters are described in this section.

15.1 .1 RCs and MRCs

Output regulations in many resonant-type converters, such as QRCs and MRCs, are achieved by controlling the switching frequency. The ZCS applications require controlled switch-on times while ZVS applications require controlled switch-off times. The fundamental control blocks in the IC include an error amplifier, voltage-controlled-oscillator (VCO), one-shot generator with a zero wave-crossing detection comparator, and an output stage to drive the active switch. Typical ICs include UC1861-UC1864 for ZVS applications and UC 1865-UC 1868 for ZCS applications [32]. Figure 15.30 shows the controller block diagram of UC 1864.

The maximum and minimum switching frequencies (i.e., $f_{\max}$ and $f_{\min}$) are controlled by the resistors R_{ange} and $R_{\min}$ and capacitor C_{vco}; $f_{\max}$ and $f_{\min}$ can be expressed as

$$f_{\max} = \frac{3.6}{(R_{\text{ange}}/R_{\min})C_{\text{VCO}}} \quad \text{and} \quad f_{\min} = \frac{3.6}{R_{\min}C_{\text{VCO}}} \tag{15.3}$$

The frequency range Δf is then equal to

$$\Delta f = f_{\max} - f_{\min} = \frac{3.6}{R_{\text{ange}}C_{\text{VCO}}} \tag{15.4}$$

The frequency range of the ICs is from 10 kHz to 1 MHz. The output frequency of the oscillator is controlled by the error amplifier (E/A) output. An example of a ZVS-MR forward converter is shown in Figure 15.31.

15.1 .2 Phase-Shifted, VT B Circuit

The UCC3895 is a phase-shift PWM controller that can generate a phase shifting pattern of one half-bridge with respect to the other. The application diagram is shown in Fig. 15.32.

The four outputs OUTA, OUTB, OUTC, and OUTD are used to drive the MOSFETs in the full-bridge. The dead time between OUTA and OUTB is controlled by DELAB and the dead time between OUTC and OUTD is controlled by

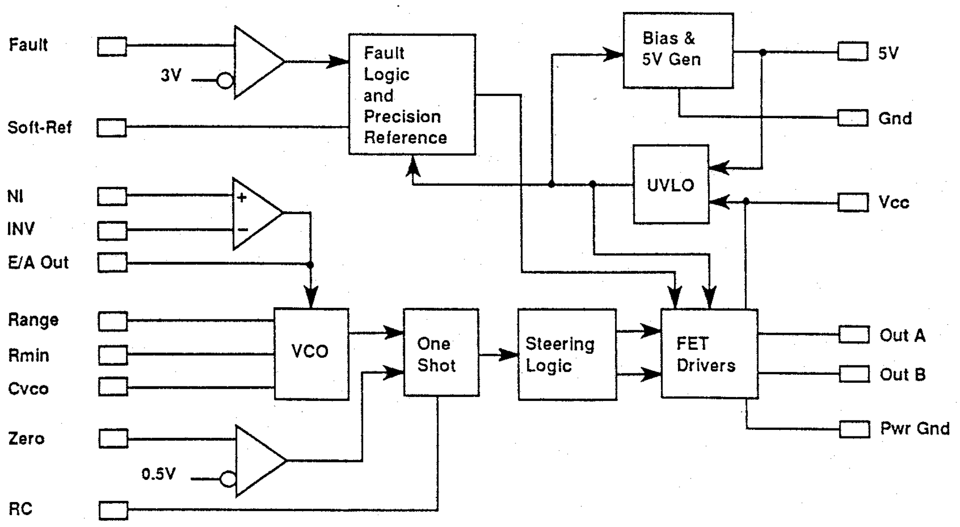


FIGURE 15.30 Controller block diagram of UC1864 (Courtesy of Unitrode Corp. and Texas Instruments, www.ti.com).

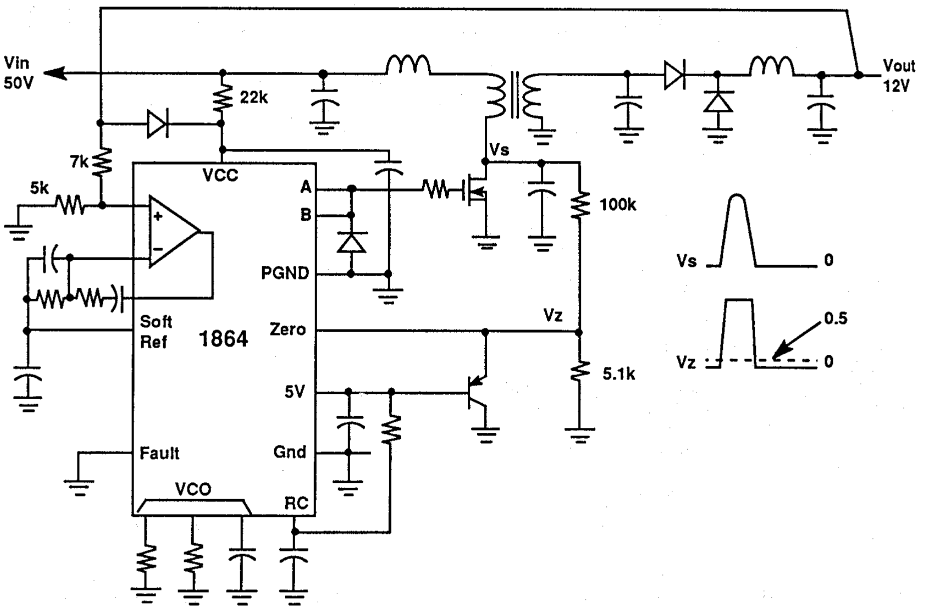

Vin
50V
22k
7k
5k
VCC
A
B
PGND
Soft
Ref
1864
Zero
5V
Fault
Gnd
VCO
RC
Vs
100k
Vz
5.1k
Vout
12V
Vs
0
Vz
0.5
0

FIGURE 15.31 The ZVS-MR forward converter (Courtesy of Unitrode Corp. and Texas Instruments, www.ti.com).

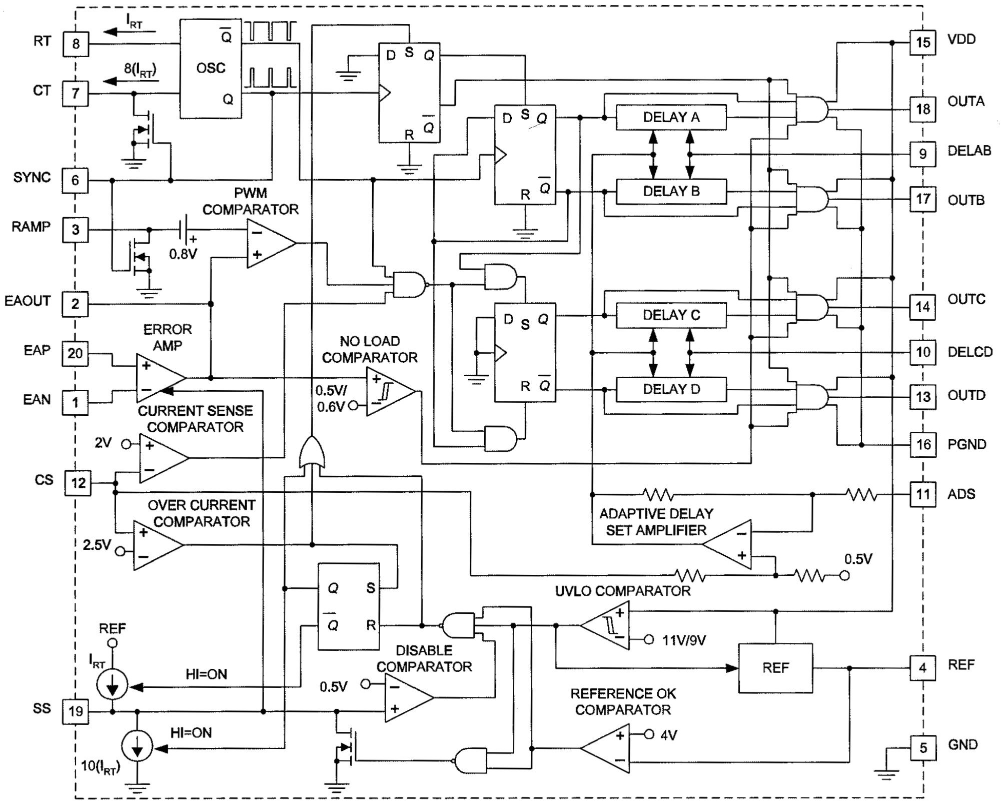

RT
8
I_{RT}
CT
7
$8(I_{RT})$
OSC
Q
Q
SYNC
6
RAMP
3
PWM
COMPARATOR
0.8V
EAOUT
2
EAP
20
ERROR
AMP
EAN
1
CURRENT SENSE
COMPARATOR
2V
CS
12
OVER CURRENT
COMPARATOR
2.5V
REF
I_{RT}
HI=ON
SS
19
HI=ON
$10(I_{RT})$
NO LOAD
COMPARATOR
0.5V/
0.6V
D S Q
R Q
DELAY A
DELAY B
DELAY C
DELAY D
Q S
Q R
DISABLE
COMPARATOR
0.5V
ADAPTIVE DELAY
SET AMPLIFIER
0.5V
UVLO COMPARATOR
11V/9V
REF
REFERENCE OK
COMPARATOR
4V
15
VDD
18
OUTA
9
DELAB
17
OUTB
14
OUTC
10
DELCD
13
OUTD
16
PGND
11
ADS
4
REF
5
GND

FIGURE 15.32 Application diagram of UCC3895 (Courtesy of Unitrode Corp. and Texas Instruments, www.ti.com).

DELCD. Separate delays are provided for the two half-bridges to accommodate differences in resonant capacitor charging currents. The delay in each set is approximated by

$$t_{\mathrm{DELAY}} = \frac{25 \times 10^{-12} R_{\mathrm{DEL}}}{0.75(V_{\mathrm{CS}} - V_{\mathrm{ADS}}) + 0.5} + 25\,\mathrm{ns} \qquad (15.5)$$

where R_{DEL} is the resistor value connected between DELAB or DELCD to ground.

The oscillator period is determined by R_T and C_T. It is defined as

$$t_{\mathrm{OSC}} = \frac{5 R_T C_T}{48} + 120\,\mathrm{ns} \qquad (15.6)$$

The maximum operating frequency is 1 MHz. The phase shift between the two sets of signals is controlled by the ramp voltage and an error amplifier output with a 7 MHz bandwidth.

15.11 Extended-Period Quasi-Resonant EP-QR Converters

Generally, resonant and quasi-resonant converters operate with frequency control. The extended-period quasi-resonant converters proposed by Barbi [33] offer a simple solution to modify existing hard-switched converters into soft-switched ones with constant frequency operation. This makes both output filter design and control simple. Figure 15.33 shows a standard hard-switched boost-type PFC converter. In this hard-switched circuit, the main switch SW1 could be subject to significant switching stress because the reverse recovery current of the diode D_F could be excessive when SW1 is turned on. In practice, a small saturable inductor may be added in series with the power diode D_F in order to reduce the di/dt of the reverse-recovery current. In addition, an optional R-C snubber may be added across SW1 to reduce the dv/dt of SW1. These extra reactance components can, in fact, be used in the EP-QR circuit to achieve soft switching, as shown in Fig. 15.34. The resonant components L_r and C_r have small values and can come from the snubber circuits of a standard hard-switched converter. Thus, the only additional component is the auxiliary switch Q_2. The small resonant inductor is put in series with the main switch SW1 so that SW1 can be switched on under ZC condition and the di/dt problem of the reverse-recovery current be eliminated. The resonant capacitor C_r is used to store energy in order to create the condition for soft switching. The Q_2 is used to control the resonance during the main switch transition. It should be noted that all power devices including SW1, Q_1, and main power diode D_F are turned on and off under ZV and/or ZC conditions. Therefore, the large di/dt problem due to the reverse recovery of the power diode can be eliminated. The soft-switching method is an effective technique for EMI suppression.

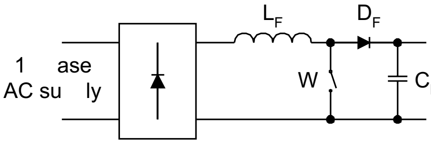


FIGURE 15.33 Boost-type ac-dc power factor correction circuit.

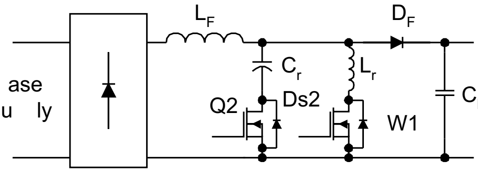


FIGURE 15.34 The EP-QR boost-type ac-dc power factor correction circuit.

Together with the power factor correction technique, soft-switching converters offer a complete solution to meet EMI regulations for both conducted and radiated EMI. The operation of the EP-QR boost PFC circuit [34, 35] can be described in six modes (a-f) as shown in Fig. 15.35. The corresponding idealized waveforms are included in Fig. 15.36.

15.11.1 Circuit Operation

Interval I (t_0 t_1). Due to the resonant inductor L_r, which limits the di/dt of the switch current, switch SW_1 is turned on at zero-current condition with a positive gating signal V_{GS1} to start a switching cycle at $t = t_o$. Current in D_F is diverted to inductor L_r. Because D_F is still conducting during this short

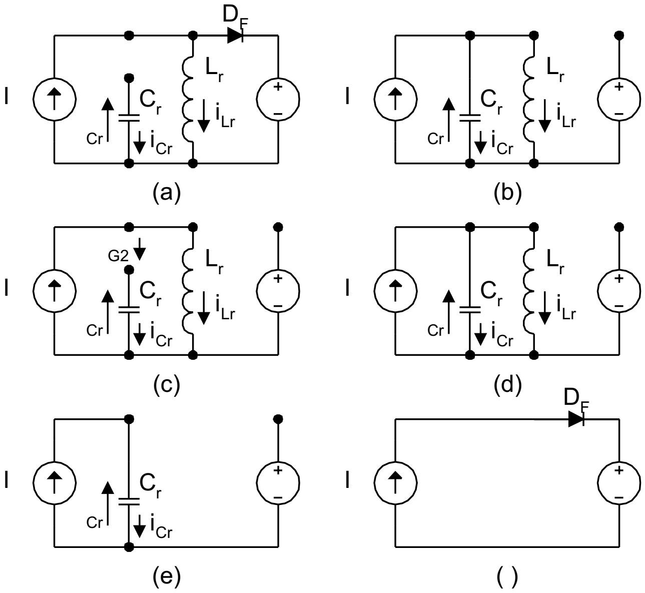


FIGURE 15.35 Operating modes of EP-QR boost-type ac-dc power factor correction circuit.

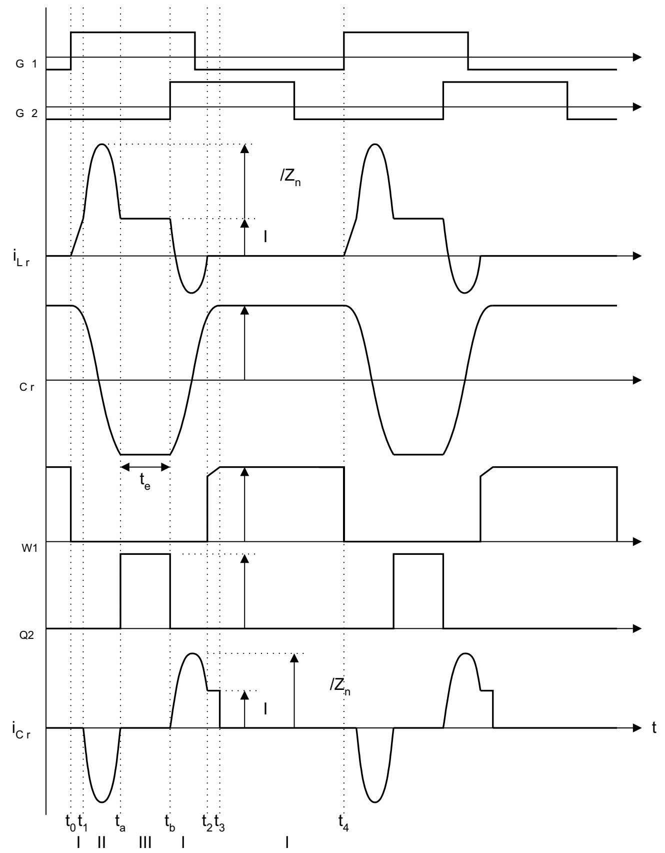


FIGURE 15.36 Idealized waveforms of EP-QR boost-type ac-dc power factor correction circuit.

period, D_{S2} is still reversed biased and is thus not conducting. The equivalent circuit topology for the conducting paths is shown in Fig. 15.35a. Resonant switch Q_2 remains off in this interval.

Interval II (t_1 t_a). When D_F regains its blocking state, D_{S2} becomes forward biased. The first half of the resonance cycle occurs and resonant capacitor C_r starts to discharge and current flows in the loop C_r-Q_2-L_r-SW$_1$. The resonance half-cycle stops at time $t = t_a$ because D_{S2} prevents the loop current i_{Cr} from flowing in the opposition direction. The voltage across C_r is reversed at the end of this interval. The equivalent circuit is shown in Fig. 15.35b.

Interval III (t_a t_b). Between t_a and t_b, current in L_F and L_r continues to build up. This interval is the extended period for the resonance during which energy is pumped into L_r. The corresponding equivalent circuit is showed in Fig. 15.35c.

Interval IV (t_b t_2). Figure 15.35d shows the equivalent circuit for this operating mode. Before SW$_1$ is turned off, the second half of the resonant cycle needs to take place in order that a zero-voltage condition can be created for the turn-off process of SW$_1$. The second half of the resonant cycle starts when auxiliary switch Q_2 is turned on at $t = t_b$. Resonant current then flows through the loop L_r-Q_2-C_r-antiparallel diode of SW$_1$. This current is limited by L_r and thus Q_2 is turned on under a zero-current condition. Because the antiparallel diode of SW$_1$ is conducting, the voltage across SW1 is clamped to the on-state voltage of the antiparallel diode. Therefore SW$_1$ can be turned off at (near) zero-voltage condition before $t = t_2$, at which the second half of the resonant cycle ends.

Interval V (t_2 t_3). During this interval, the voltage across C_r is less than the output voltage V_o. Therefore, D_F is still reverse-biased. Inductor current I_s flows into C_r until V_{Cr} reaches V_o at $t = t_3$. The equivalent circuit is represented in Fig. 15.35e.

Interval VI (t_3 t_4). During this period, the resonant circuit is not in action and the inductor current I_S charges the output capacitor C_F via D_F, as in the case of a classical boost-type PFC circuit. The C_r is charged to V_o and Q_2 can be turned off at zero-voltage and zero-current conditions. Figure 15.35f shows the equivalent topology of this operating mode.

In summary, SW1, Q_2 and D_F are fully soft-switched. Because the two resonance half-cycles take place within a closed loop outside the main inductor, the high resonant pulse will not occur in the inductor current, thus making the well-established averaged current mode control technique applicable for such a QR circuit. For full soft-switching in the turn-off process, the resonant components need to be designed so that the peak resonant current exceeds the maximum value of the inductor current. Typical measured switching waveforms and trajectories of SW1, Q_2 and D_F are shown in Fig. 15.37, Fig. 15.38, and Fig. 15.39, respectively.

15.11.2 Design Procedure

Given:

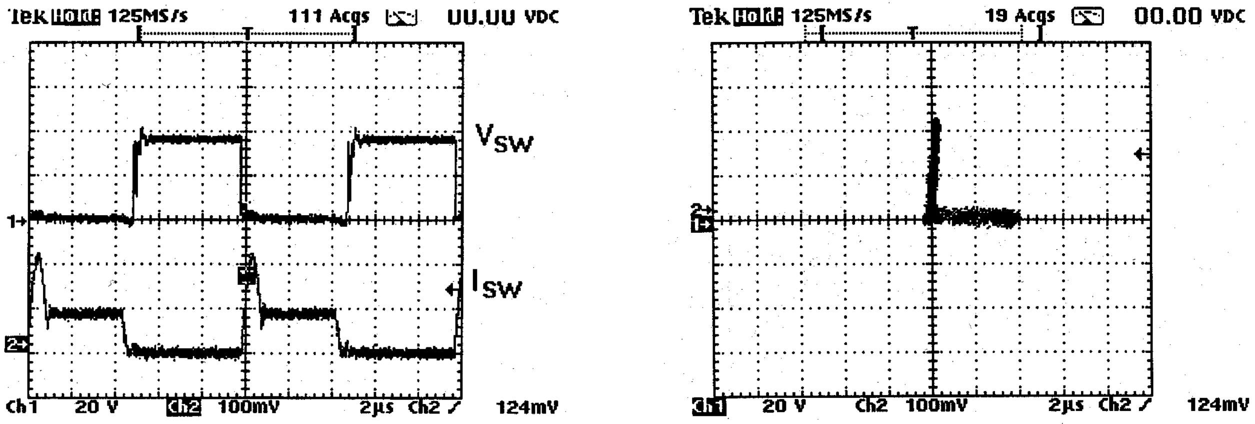
- Input ac voltage = V_s
- Peak AC voltage $V_{s(\max)}(V)$
- Nominal output dc voltage = $V_o(V)$
- Switching frequency = f_{SW} (Hz)
- Output power = $P_o(W)$
- Input current ripple = $\Delta I(A)$
- Output voltage ripple = $\Delta V(V)$

15.11.2.1 Resonant Tank Design

Step 1: Because the peak resonant current must be greater than the peak inductor current (same as peak input line current) in order to achieve soft-turn-off, it is necessary to determine the peak input current $I_{s(\max)}$. Assuming lossless ac-dc power conversion, $I_{s(\max)}$ can be estimated from the following equation:

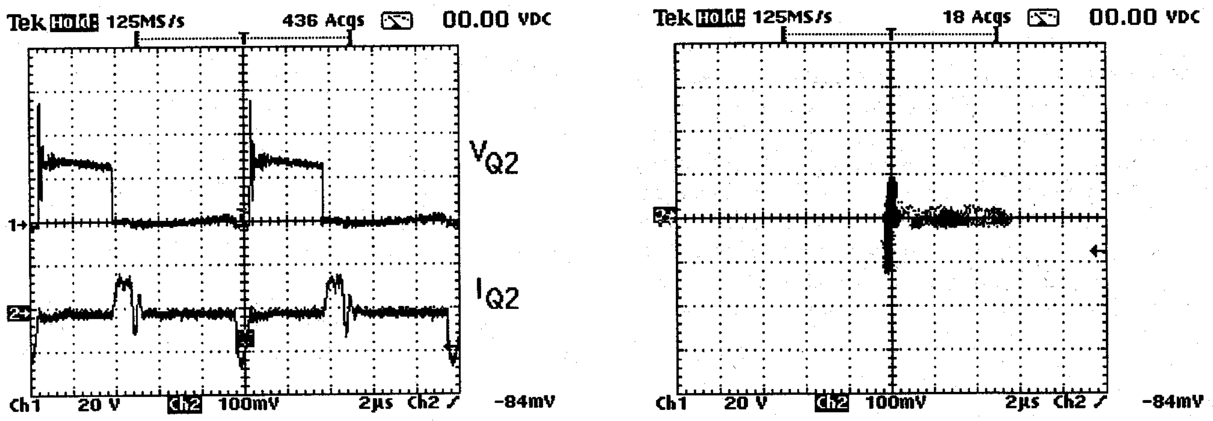
$$I_{s(\max)} \approx \frac{2V_oI_o}{V_{s(\max)}} \tag{15.7}$$

where $I_o = P_o/V_o$ is the maximum output current.



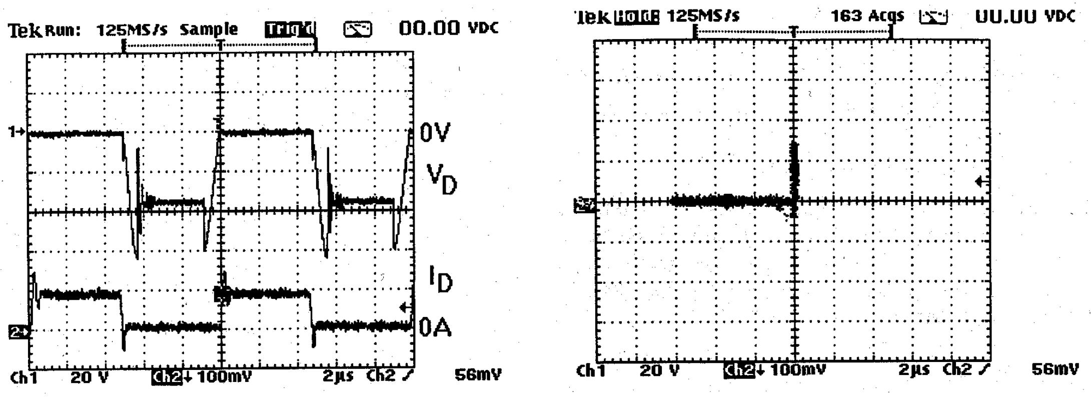
(a) (b)

FIGURE 15.37 (a) Drain-source voltage and current of SW1; and (b) switching locus of SW1.



(a) (b)

FIGURE 15.38 (a) Drain-source voltage and current of Q_2; and (b) switching locus of Q_2.



(a) (b)

FIGURE 15.39 (a) Diode voltage and current; and (b) switching locus of diode.

Step 2: Soft-switching criterion is

$$Z_r \leq \frac{V_o}{I_{s(\max)}} \tag{15.8}$$

where $Z_r = \sqrt{L_r/C_r}$ is the impedance of the resonant tank.

For a chosen resonant frequency f_r, L_r and C_r can be obtained from

$$2\pi f_r = 1/\sqrt{L_r C_r} \tag{15.9}$$

15.11.2.2 Filter Component Design

The minimum conversion ratio is

$$M_{(\min)} = V_o/V_{s(\max)} = \frac{1}{1 - (F_{\mathrm{sw}}/f_r + T_e/T_{\mathrm{sw}})} \tag{15.10}$$

where $T_{\mathrm{sw}} = 1/f_{\mathrm{sw}}$ and t_e is the extended period. From Eq. (5.10), minimum t_e can be estimated.

The turn-on period of the SW1 is

$$T_{\mathrm{on(sw1)}} = t_e + 1/f_r \tag{15.11}$$

Inductor value L is obtained from

$$L \geq \left(\frac{T_{\mathrm{on(sw1)}}}{\Delta I}\right) V_{s(\max)} \tag{15.12}$$

The filter capacitor value C can be determined from

$$C\left(\frac{\Delta V}{T_s/\pi \sin^{-1}(I_o/I_{s(\max)})}\right) = I_o \tag{15.13}$$

where $T_s = 1/f_s$ is the period of the ac voltage supply frequency.

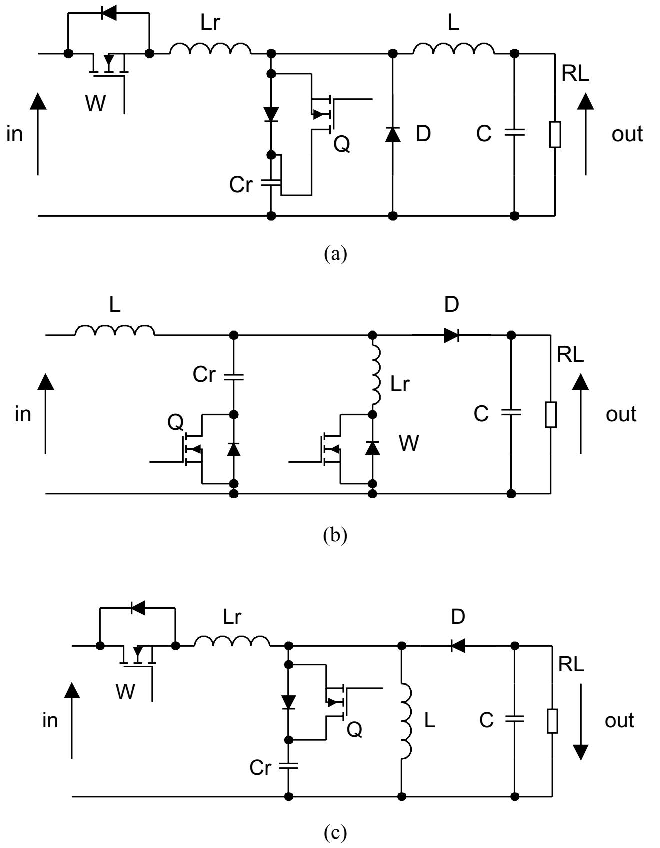


FIGURE 15.40 A family of EP-QR converters: (a) Buck converter; (b) boost converter; and (c) flyback converter.

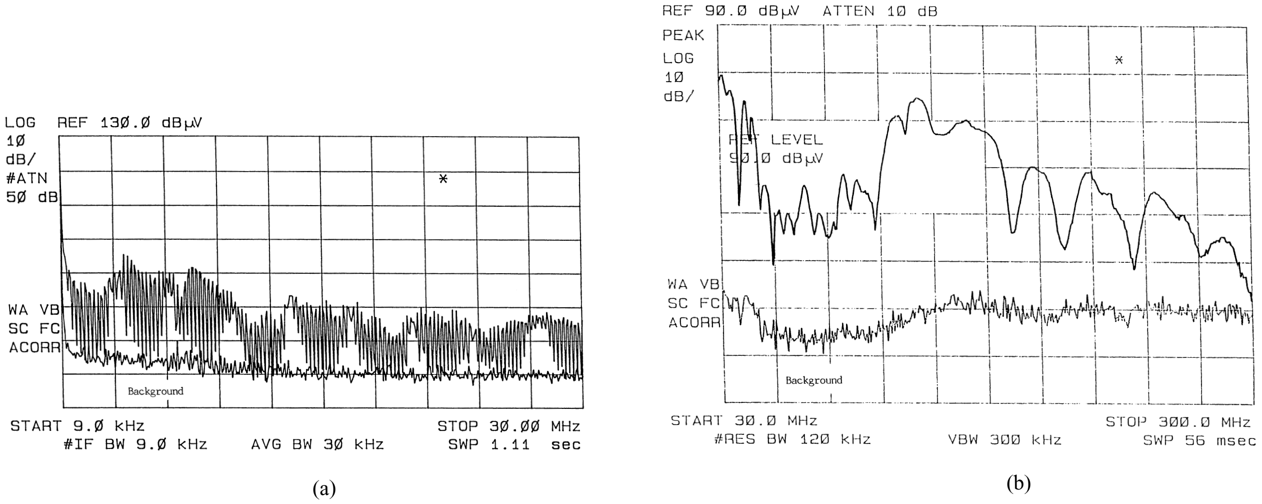
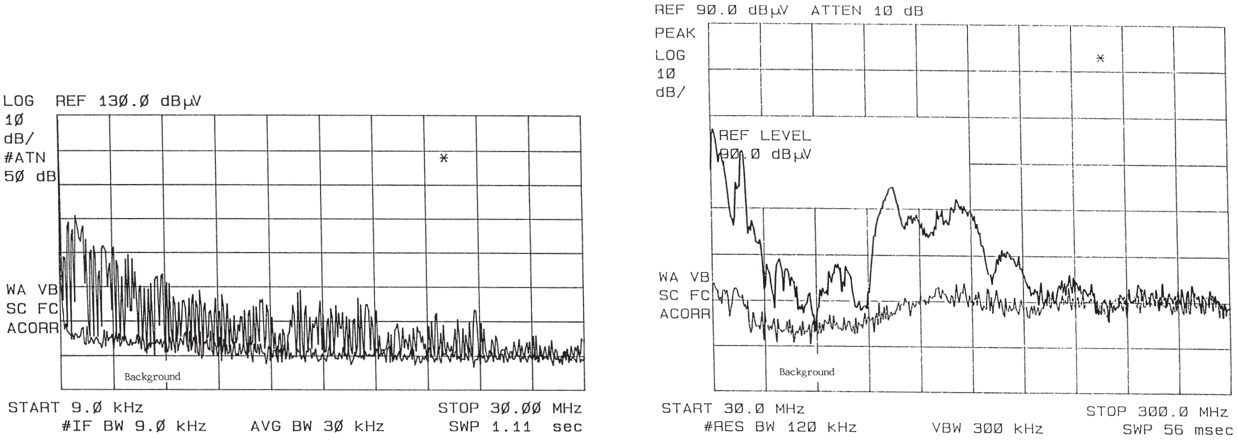


FIGURE 15.41 (a) Conducted EMI from hard-switched flyback converter; and (b) radiated EMI from hard-switched flyback converter.



(a) (b)

FIGURE 15.42 (a) Conducted EMI from soft-switched flyback converter; and (b) radiated EMI from soft-switched flyback converter.

15.12. Soft-Switching and EMI Suppression

A family of EP-QR converters is displayed in Fig. 15.40. Their radiated EMI emission have been compared with that from their hard-switched counterparts [36]. Figure 15.41a, b shows the conducted EMI emission from a hard-switched flyback converter and a soft-switched one, respectively. Their radiated EMI emissions are included in Fig. 15.42. Both converters are tested at an output power of 50W. No special filtering or shielding measures have been taken during the measurement. It is clear from the measurements that soft-switching is an effective means to EMI suppression.

15.13 Snubbers and Soft-Switching for igh Power Devices

Today, most of the medium power (up to 200 kVA) and medium voltage (up to 800 V) inverters are hard-switched. Compared with low-power switched mode power supplies, the high voltage involved in the power inverters makes the dv/dt, di/dt, and switching stress problems more serious. In addition, the reverse recovery of power diodes in the inverter leg may cause a very sharp current spike, leading to severe EMI problems. It should be noted that some high-power devices such as GTO thyristors do not have a square safe operating area (SOA). It is therefore essential that the switching stress they undergo must be within their limits. Commonly used protective measures include the use of snubber circuits to protect high-power devices.

Among various snubbers, two snubber circuits are most well known for applications in power inverters. They are the Undeland snubber [37] (Fig. 15.43) and McMurray snubber circuits [38] (Fig. 15.44). The Undeland snubber is an asymmetric snubber circuit with one turn-on inductor and one turn-off capacitor. The turn-off snubber capacitor C_s is clamped by another capacitor C_c. At the end of each switching cycle, the snubber energy is dumped into C_c and then discharged into the dc bus via a discharge resistor. In order to reduce the snubber loss, the discharge resistor can be replaced by a switched mode circuit. In this way, the Undeland snubber can become a snubber with energy recovery. The McMurray snubber is symmetrical. Both of the turn-off

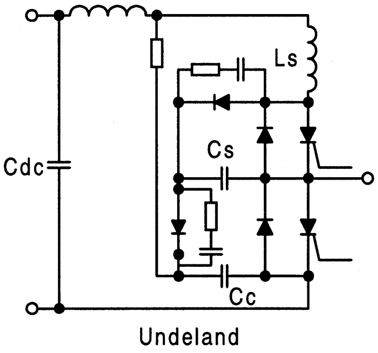


FIGURE 15.43 Undeland snubber.

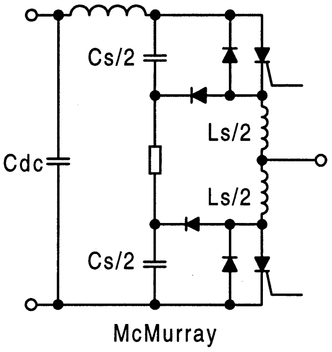


FIGURE 15.44 McMurray snubber.

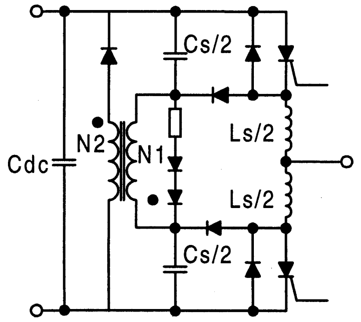


FIGURE 15.45 McMurray snubber with energy recovery.

snubber capacitors share current in parallel during turn off. The voltage transient is limited by the capacitor closest to the turning-off device because the stray inductance to the other capacitor will prevent instantaneous current sharing. The turn-on inductors require midpoint connection. Snubber energy is dissipated into the snubber resistor. Like the Undeland snubber, the McMurray snubber can be modified into an energy recovery snubber. By using an energy recovery transformer as shown in Fig. 15.45. this snubber becomes a regenerative one. Although other regenerative circuits have been proposed, their complexity makes them unattractive in industrial applications. In addition, they do not necessarily solve the power diode reverse recovery problems.

Although the use of snubber circuits can reduce switching stress in power devices, the switching loss is actually damped into the snubber resistors unless regenerative snubbers are used. The switching loss is still a limiting factor to the high frequency operation of power inverters. However, the advent of soft-switching techniques opens up a new way to use high-frequency inverter operation. Because the switching trajectory of a soft-switched switch is close to the voltage and current axis, faster power electronic devices with smaller SOAs can, in principle, be used. In general, both ZVS and ZCS can reduce switching loss in high-power power switches. However, for power switches with tail currents, such as IGBT, ZCS is more effective than ZVS.

15.14 Soft-Switching DC-AC Power Inverters

The soft-switching technique not only offers a reduction in switching loss and thermal requirement, but also allows the possibility of high frequency and snubberless operation. Improved circuit performance and efficiency as well as reduction of EMI emission can be achieved. For zero voltage switching (ZVS) inverter applications, two major approaches that enable inverters to be soft-switched have been proposed. The first approach pulls the dc link voltage to zero momentarily so that the inverter's switches can be turned on and off with ZVS. Resonant dc link and quasi-resonant inverters belong to this category. The second approach uses the resonant pole idea. By incorporating the filter components into the inverter operation, resonance condition and thus zero voltage/current conditions can be created for the inverter switches.

In this section, the following soft-switched inverters are described.

Approach A: Resonant dc link inverters:

1. resonant (pulsating) dc link inverters;
2. actively-clamped resonant dc link inverters;
3. resonant inverters with minimum voltage stress;
4. quasi-resonant soft-switched inverter; and
5. parallel resonant dc link inverter.

Approach B: Resonant pole inverters:

6. resonant pole inverters;
7. auxiliary resonant pole inverters; and
8. auxiliary resonant commutated pole inverters.

Type 1 is the resonant dc link inverter [39–41], which sets the dc link voltage into oscillation so that zero-voltage instants are created periodically for ZVS. Despite the potential advantages that this soft-switching approach can offer, a recent review on existing resonant link topologies for inverters [42] concludes that the resonant dc link system results in an increase in circuit complexity and the frequency spectrum is restricted by the need to use integral pulse density modulation (IPDM) when compared with a standard hard-switched inverter. In addition, the peak pulsating link voltage of resonant link inverters is twice that of the dc link voltage in a standard hard-switched inverter. Although clamp circuits (Type 2) can be used to limit the peak voltage to 1.3–1.5 per unit [41], power devices with higher than normal voltage ratings have to be used.

Circuits of Types 3–5 employ a switched mode front stage circuit, which pulls the dc link voltage to zero momentarily whenever inverter switching is required. This soft-switching approach does not cause extra voltage stress to the inverter and hence the voltage rating of the power devices is only 1 per unit. As ZVS conditions can be created at any time, there is virtually no restriction in the PWM strategies. Therefore, well-established PWM schemes developed in the last two decades can be employed. In some ways, this approach is similar to some dc-side commutation techniques proposed in the past for thyristor inverters [43, 44], although these dc-side commutation techniques were used for turning off thyristors in the inverter bridge and not primarily developed for soft-switching.

Circuits of Types 6–8 retain the use of a constant dc link voltage. They incorporate the use of the resonant components and/or filter components into the inverter circuit operation. This approach is particularly useful for inverter applications in which output filters are required. Examples include uninterruptible power supplies (UPS) and inverters with output filters for motor drives. The LC filter components can form the auxiliary resonant circuits that create the soft-switching conditions. However, these tend to have high-power device count and require complex control strategy.

15.14.1 Resonant Pulsating dc link inverter

A resonant dc link converter for dc-ac power conversion was proposed in 1986 [39]. Instead of using a nominally constant dc link voltage, a resonant circuit is added to cause the dc link voltage to pulsate at a high frequency. This resonant circuit theoretically creates periodic zero-voltage duration at which the inverter switches can be turned on or off. Figure 15.46 shows the schematics of the pulsating link inverter. Typical dc link voltage, inverter's phase voltage, and the line voltages are shown in Fig. 15.47. Because the inverter switching can only occur at zero voltage duration, integral pulse density modulation (IPDM) has to be adopted in the switching strategy.

Analysis of the resonant dc link converter can be simplified by considering that the inverter system is highly inductive. The equivalent circuit is shown in Fig. 15.48.

The link current I_x may vary with the changing load condition, but can be considered constant during the short resonant cycle. If switch S is turned on when the inductor current is I_{Lo}, the resonant dc link voltage can be expressed as

$$V_c(t) = V_s + e^{-\alpha t}[-V_s \cos(\omega t) + \omega L I_M \sin(\omega t)] \quad (15.14)$$

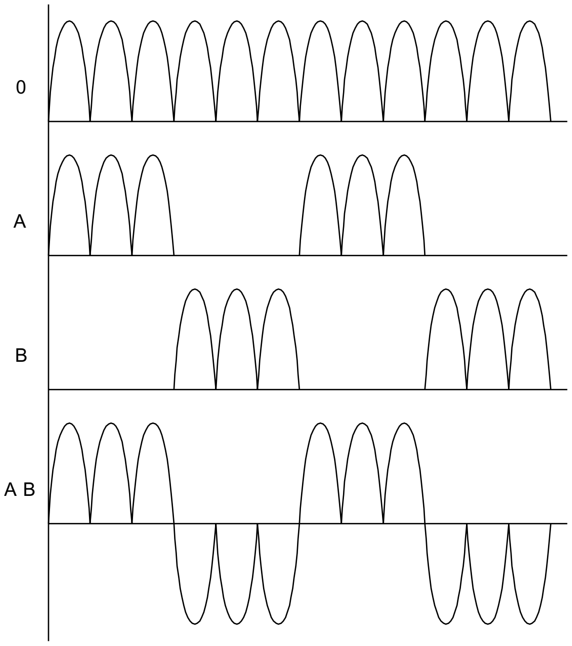


FIGURE 15.47 Typical dc link voltage (V_0), phase voltages (V_A, V_B), and line voltage (V_{AB}) of resonant link inverters.

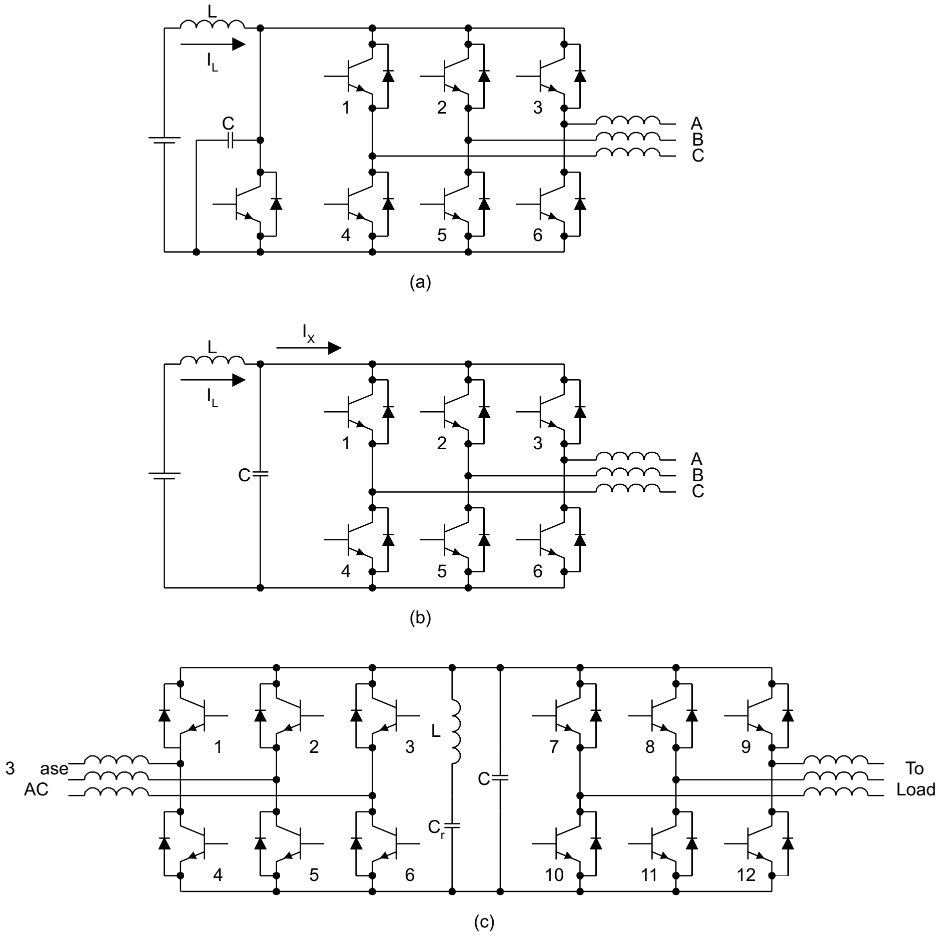


FIGURE 15.46 Resonant-link inverters.

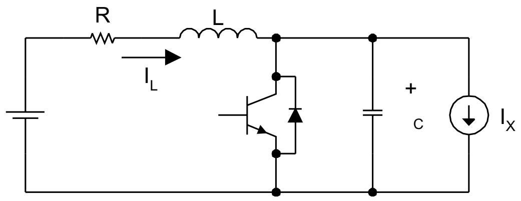


FIGURE 15.48 Equivalent circuit of resonant link inverter.

and inductor current i_L is

$$i_L(t) \approx I_x + e^{-\alpha t}\left[I_M \cos(\omega t) + \frac{V_s}{\omega L}\sin(\omega t)\right] \qquad (15.15)$$

where

$$\alpha = R/2L \qquad (15.16)$$

$$\omega_o = (LC)^{-0.5} \qquad (15.17)$$

$$\omega = (\omega_o^2 - \alpha^2)^{0.5} \qquad (15.18)$$

and

$$I_M = I_{Lo} - I_x \qquad (15.19)$$

The resistance in the inductor could affect resonant behavior because it dissipates some energy. In practice, $(i_L - I_x)$ has to be monitored when S is conducting. In addition, S can be turned on when $(i_L - I_x)$ is equal to a desired value. The objective is to ensure that the dc link voltage can be resonated to zero voltage level in the next cycle.

The pulsating dc link inverter has the following advantages:

- reduction of switching loss;
- snubberless operation;
- high switching frequency (> 18 kHz) operation becomes possible, leading to the reduction of acoustic noise in inverter equipment; and
- reduction of heat sink requirements and thus improvement of power density.

This approach has the following limitations:

- The peak dc pulsating link voltage (2.0 per unit) is higher than the nominal dc voltage value of a conventional inverter. This implies that power devices and circuit components of higher voltage ratings must be used. This could be a serious drawback because power components of higher voltage ratings are not only more expensive, but usually have inferior switching performance than their low-voltage counterparts.
- Although voltage clamp can be used to reduce the peak dc link voltage, the peak voltage value is still higher than normal and the additional clamping circuit makes the control more complicated.
- Integral pulse-density modulation has to be used. Many well-established PWM techniques cannot be employed.

Despite these advantages, this resonant converter concept has paved the way for other soft-switched converters to develop.

15.14.2 Active-Clamped Resonant dc Link Inverter

In order to solve the high-voltage requirement in the basic pulsating dc link inverters, active clamping techniques (Fig. 15.49) have been proposed. The active clamp can reduce the per-unit peak voltage from 2.0 to $\approx 1.3-1.5$ [41]. It has been reported that an operating frequency in the range of 60 to 100 kHz has been achieved [45] with an energy efficiency of 97 for a 50-kVA drive system.

The design equations for an active-clamped resonant link inverter are

$$T_L = \frac{1}{f_L} = 2\sqrt{L_r C_r}\left(\cos^{-1}(1-k) + \frac{\sqrt{k(2-k)}}{k-1}\right) \qquad (15.20)$$

where T_L is the minimum link period, f_L is the maximum link frequency, and k is the clamping ratio. For the active-clamped resonant inverter, k is typically 1.3 to 1.4 p.u.

The rate of rise of the current in the clamping device is

$$\frac{di}{dt} = \frac{(k-1)V_s}{L_r} \qquad (15.21)$$

The peak clamping current required to ensure that the dc bus return to zero voltage is

$$I_{sp} = V_s\sqrt{\frac{k(2-k)C_r}{L_r}} \qquad (15.22)$$

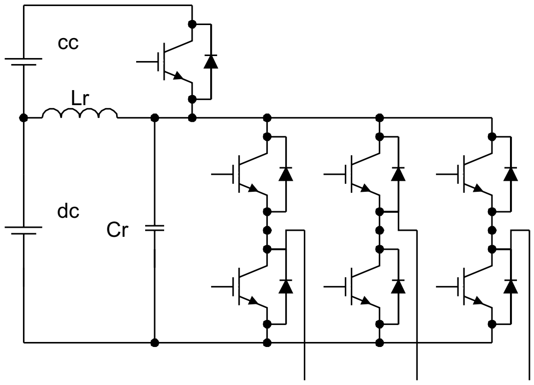


FIGURE 15.49 Active-clamp resonant link inverter.

In summary, resonant (pulsating) dc link inverters offer significant advantages, such as:

- high switching frequency operation;
- low *dv*/*dt* for power devices;
- ZVS with reduced switching loss;
- suitable for 1–250 kW; and
- rugged operation with few failure modes.

15.14.3 Resonant dc Link Inverter with Low Voltage Stress

A resonant dc link inverter with low voltage stress [46] is shown in Fig. 15.50. It consists of a front-end resonant converter that can pull the dc link voltage down just before any inverter switching. This resonant dc circuit serves as an interface between the dc power supply and the inverter. It essentially retains all the advantages of the resonant (pulsating) dc link inverters but it offers extra advantages, including:

- No increase in the dc link voltage when compared with a conventional hard-switched inverter. That is, the dc link voltage is 1.0 per unit.
- The zero voltage condition can be created at any time. The ZVS is not restricted to the periodic zero-voltage instants as in a resonant dc link inverter.
- Well-established PWM techniques can be employed.
- Power devices of standard voltage ratings can be used.

The timing program and the six operating modes (a–f) of this resonant circuit are as shown in Fig. 15.51 and Fig. 15.52, respectively.

(1) Normal mode This is the standard PWM inverter mode. The resonant inductor current $i_{\text{Lr}}(t)$ and the resonant voltage $V_{\text{cr}}(t)$ are given by

$$i_{\text{Lr}}(t) = 0$$

$$v_{\text{Cr}}(t) = V_{\text{s}}$$

where V_s is the nominal dc link voltage.

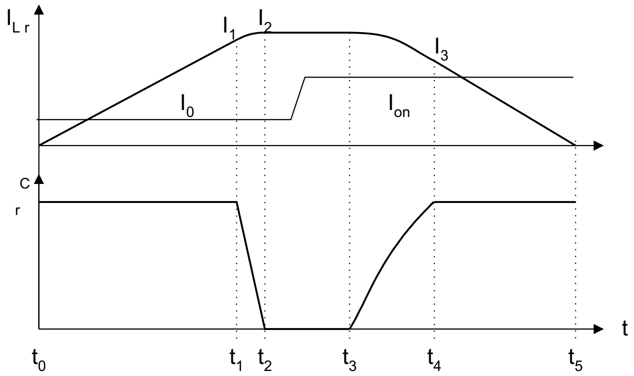


FIGURE 15.51 Timing diagram of a resonant link inverter with minimum voltage stress.

(2) Mode 1 (Initiating mode): $(t_0 - t_1)$ At t_0, mode 1 begins by switching T2 and T3 on with zero current. Then $i_{\text{Lr}}(t)$ increases linearly with a di/dt of V_s/L_r. If $i_{\text{Lr}}(t)$ is equal to the initialized current I_i, T1 is zero-voltage turned off. If $(I_s - I_o) < I_i$, then the initialization is ended when $i_{\text{Lr}}(t)$ is equal to I_i, where I_s is the current flowing into the dc inductor L_{dc}. If $(I_s - I_o) > I_i$, then this mode continues until $i_{\text{Lr}}(t)$ is equal to $(I_s - I_o)$. The equations in this interval are

$$i_{\text{Lr}}(t) = \frac{V_s}{L_2}t$$

$$v_{\text{cr}}(t) = V_s$$

$$i_{\text{Lr}}(t_1) = \frac{V_s}{L_r}t_1 = I_i$$

(3) Mode 2 (Resonant mode): $(t_1 - t_2)$ After T1 is turned off under the ZVS condition, resonance between L_r and C_r occurs. The $V_{\text{cr}}(t)$ decreases from V_s to 0. At t_2, $i_{\text{Lr}}(t)$ reaches the peak value in this interval. The equations are

$$i_{\text{Lr}}(t) = \frac{V_s}{Z_r}\sin(\omega_r t) + [I_1 + (I_o - I_s)]\cos(\omega_r t) - (I_o - I_s)$$

$$V_{\text{cr}}(t) = -V_s\cos(\omega_r t) - [I_1 + (I_o - I_s)]Z_r\sin(\omega_r t)$$

$$I_{\text{L}}(t_2) = I_2 = I_{\text{Lr,peak}}$$

$$V_{\text{cr}}(t_2) = 0$$

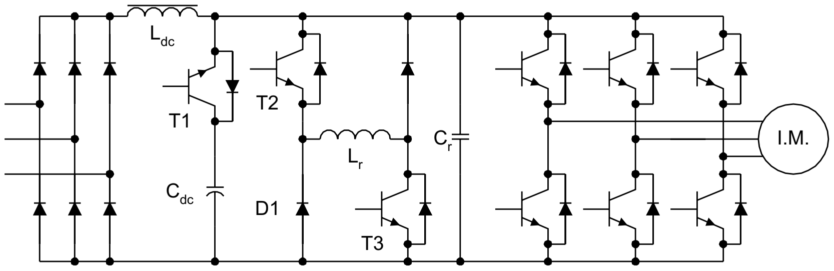
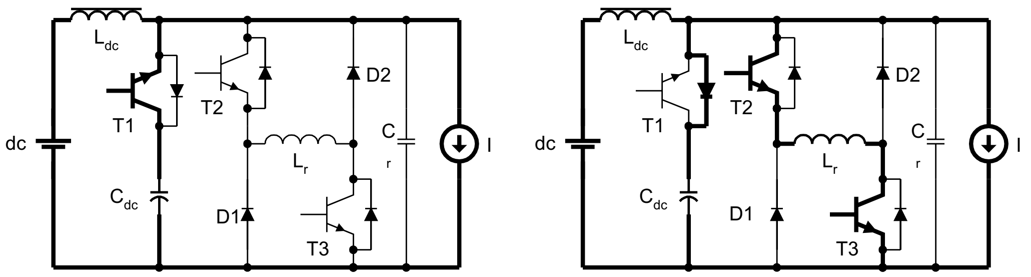
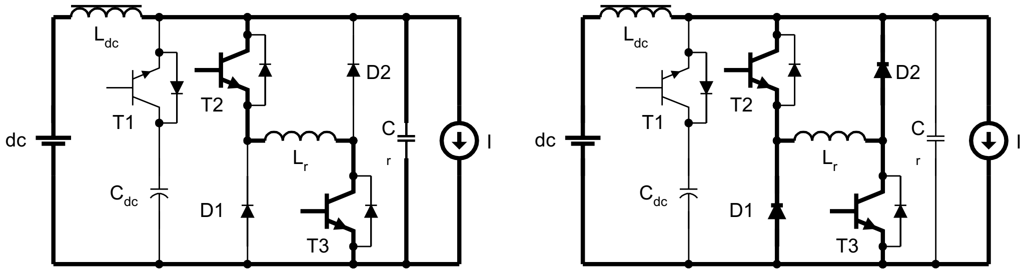


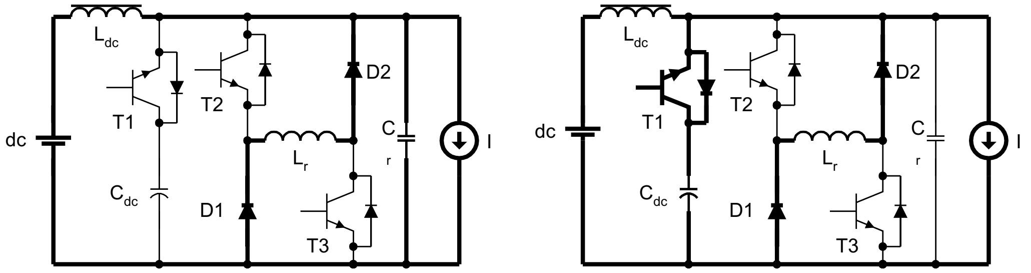
FIGURE 15.50 Resonant dc link inverter with low voltage stress.



(a) normal mode (b) mode 1



(c) mode 2 (d) mode 3



(e) mode 4 ( ) mode 5

FIGURE 15.52 Operating modes of resonant link inverter with minimum voltage stress.

where

$$Z_r = \sqrt{\frac{L_r}{C_r}} \quad \text{and} \quad \omega_r = \frac{1}{\sqrt{L_r C_r}}$$

(4) Mode 3 (Freewheeling mode): ($t_2 - t_3$) The resonant inductor current flows through two freewheeling paths (T2-Lr-D2 and T3-D1-Lr). This duration is the zero voltage period created for ZVS of the inverter, and should be longer than the minimum on and off times of the inverter's power switches:

$$i_{\mathrm{Lr}}(t) = I_2$$

$$v_{\mathrm{cr}}(t) = 0$$

(5) Mode 4 (Resonant mode): ($t_3 - t_4$) This mode begins when T2 and T3 are switched off under ZVS. The second half of the resonance between L_r and C_r starts again. The capacitor voltage $V_{\mathrm{cr}}(t)$ increases back from 0 to V_s and is clamped to V_s. The relevant equations in this mode are

$$i_{\mathrm{Lr}}(t) = [I_2 - (I_{\mathrm{on}} - I_s)]\cos(\omega_r t) - (I_{\mathrm{on}} - I_s)$$

$$V_{\mathrm{cr}}(t) = [I_2 - (I_{\mathrm{on}} - I_s)]Z_r \sin(\omega_r t)$$

$$i_{\mathrm{Lr}}(t_4) = I_3$$

$$V_{\mathrm{cr}}(t_4) = V_s$$

where I_{on} is the load current after the switching state.

(6) Mode 5 (Discharging mode): ($t_4 - t_5$) In this period, T1 is switched on under ZV condition because $V_{\mathrm{cr}}(t) = V_s$. The inductor current decreases linearly. This mode finishes when $i_{Lr}(t)$ becomes zero.

$$i_{\mathrm{Lr}}(t) = -\frac{V_s}{L_r}t + I_3$$

$$v_{\mathrm{cr}}(t) = V_s$$

$$i_{\mathrm{Lr}}(t_5) = 0$$

15.14.4 uasi-Resonant Soft-Switched Inverter 47

15.14.4.1 Circuit Operation

Consider an inverter fed by a dc voltage source V_s. A front-stage interface circuit shown in Fig. 15.53 can be added between the dc voltage source and the inverter. The front stage circuit consists of a quasi-resonant circuit in which the first half of the resonance cycle is set to occur to create the zero-voltage condition whenever inverter switching is needed. After inverter switching has been completed, the second half of the resonance cycle takes place so that the dc link voltage is set back to its normal level. To avoid excessive losses in the resonant circuit, a small capacitor C_{r1} is normally used to provide the dc link voltage while the large smoothing dc link capacitor C_1 is isolated from the resonant circuit just before the zero-voltage duration. This method avoids the requirement for pulling the dc voltage of the bulk capacitor to zero.

The period for this mode is from t_0 to t_1 in Fig. 15.54. In this mode, switch S_b is turned on and switches S_{r1} and S_{r2} are turned off. The inverter in Fig. 15.53 works like a conventional dc link inverter and $V_{cr1} = V_{c1}$ in this mode. The voltage across switch S_b is zero. Before an inverter switching takes place, switch S_{r1} is triggered at t_1 to discharge C_{r1}. This operating mode ends at t_2 when V_{cr1} approaches zero. The equivalent circuit in this mode is shown in Fig. 15.55a. The switch S_b must be turned off at zero voltage when switch S_{r1} is triggered. After S_{r1} is triggered, C_{r1} will be discharged via the loop C_{r1}, C_{r2}, L_r and S_{r1}. Under conditions of $V_{cr2} \leq 0$ and $C_{r1} \leq C_{r2}$, energy stored in C_{r1} will be transferred to C_{r2} and V_{cr1} falls to zero in the first half of the resonant cycle in the equivalent circuit of Fig. 15.55a. V_{cr1} will be clamped to zero by the freewheel diodes in the inverter bridge and will not become negative. Thus, V_{cr1} can be pulled down to zero for zero voltage switching. When the current in inductor L_r becomes zero, switch S_{r1} can be turned off at zero current.

Inverter switching can take place in the period from t_2 to t_3 in which V_{cr1} remains zero. This period must be longer than the turn-on and turn-off times of the switches. When inverter switching has been completed, it is necessary to reset the voltage of capacitor C_{r1}. The equivalent circuit in this mode is shown in Fig. 15.55b. The current in inductor L_r reaches zero at t_3. Due to the voltage in V_{cr2} and the presence of diode D_r, this current then flows in the opposite direction. Then C_{r1} will be recharged via L_r, C_{r2}, C_{r1} and D_r. Diode D_r turns off when the current in L_r becomes zero. Here V_{cr1} will not go beyond 1 per unit because C_{r1} is clamped to supply voltage by diode D_b. Switch S_b can be turned on again at zero voltage condition when V_{cr1} returns to normal dc supply voltage. After Dr turns

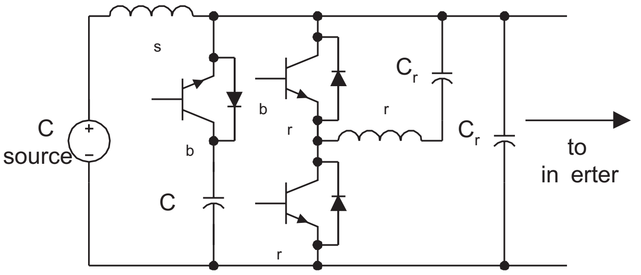


FIGURE 15.53 Quasi-resonant circuit for soft-switched inverter.

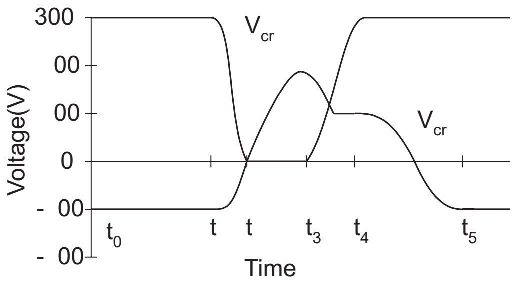
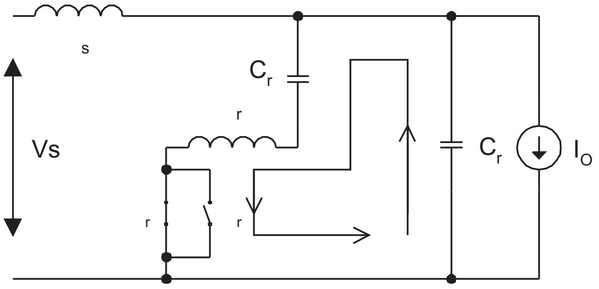
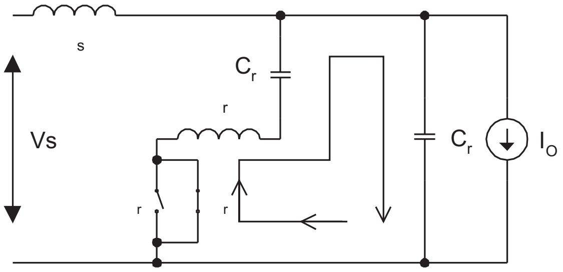


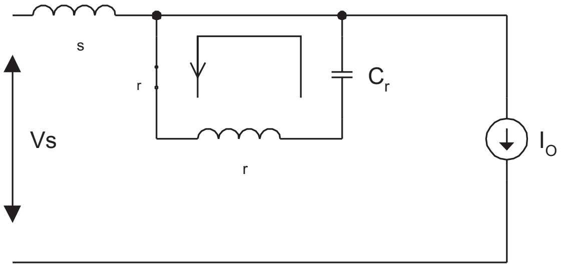
FIGURE 15.54 Typical waveforms for V_{cr1} and V_{cr2}.



(a) Mode



(b) Mode 4



(c) Mode 5

FIGURE 15.55 Equivalent circuits of the quasi-resonant circuit for different modes.

off, V_{cr2} may not be zero. Some positive residual capacitor voltage remains in C_2 at t_4, as shown in Fig. 15.54. In the case V_{cr2} is positive, V_{cr1} cannot be pulled down to zero again in the next switching cycle. Therefore, S_{r2} should be triggered after t_4 to reverse the residual voltage in C_{r2}. At time t_5, S_{r2} turns off at zero current condition and V_{cr2} is now reversed to negative. The equivalent circuit in this mode is shown in Fig. 15.55c. When $V_{\text{cr2}} \leq 0$ and $C_{r1} \leq C_{r2}$, V_{cr1} can be pulled down to zero again before the next inverter switching. The operation can then be repeated in next switching cycle.

15.14.4.2 Design Considerations

(1) C_{r1} and C_{r2} The criterion for getting zero capacitor voltages V_{cr1} is

$$(C_{r1} - C_{r2})V_s + 2C_{r2}V_{o2} - \Delta I\, \pi\sqrt{L_r C_e} \leq 0 \qquad (15.23)$$

where

- V_{o1} is the initial voltage of C_{r1};
- V_{o2} is the initial voltage of C_{r2};
- i_{L0} is the initial current of inductor L_r;
- $\Delta I = I_o - I_s$, which is the difference between load current and supply current. It is assumed to be a constant within a resonant cycle;
- R_r is the equivalent resistance in the resonant circuit; and
- $C_e = \dfrac{C_{r1}C_{r2}}{C_{r1} + C_{r2}}$

When $\Delta I \geq 0$, the preceding criterion is always true under conditions of:

$$C_{r1} \leq C_{r2},\ V_{O2} \leq 0$$

The criterion for recharging voltage V_{cr1} to 1 per unit dc link voltage is:

$$\frac{2C_{r2}}{C_{r1} + C_{r2}} V_{o2} - \frac{\Delta I}{C_{r1} + C_{r2}} \pi\sqrt{L_r C_e} \geq V_s \qquad (15.24)$$

(2) Inductor L_r The L_r should be small so that the dc link voltage can be decreased to zero quickly. However, a small L_r could result in large peak resonant current and therefore requirement of power devices with large current pulse ratings. An increase in the inductance of L_r can limit the peak current in the quasi-resonant circuit. Because the resonant frequency depends on both the inductor and the capacitor, the selection of L_r can be considered together with capacitors C_{r1} and C_{r2} and with other factors such as the current ratings of power devices, the zero-voltage duration, and the switching frequency required in the soft-switching circuit.

(3) Triggering instants of the switches Correct triggering instants for the switches are essential for the successful operation of this soft-switched inverter. For inverter switches, the triggering instants are determined from a PWM modulation. Let T_s be the time at which the inverter switches change states. To get the zero voltage inverter switching, switch S_{r1} should be turned on a half-resonant cycle before the inverter switching instant. The turn-on instant of S_{r1}, which is t_1 in Fig. 15.54, can be written as

$$t_1 = T_s - \frac{\pi}{\omega} \qquad (15.25)$$

where

$$\omega = \sqrt{\omega_0^2 - \alpha^2}, \quad \alpha = \frac{R_r}{2L_r}, \quad \omega_0 = \sqrt{\frac{1}{L_r C_e}}$$

The switch S_b is turned off at t_1.

The S_{r1} may be turned off during its zero current period when diode D_r is conducting. For easy implementation, its turn-off time can be selected as $T_s + \pi/\omega$. Because the dc link voltage can be pulled down to zero in less than half of a resonant cycle, T_s should occur between t_2 and t_3.

At time t_3 (the exact instant depends on the ΔI), the diode D_r turns on in the second half of the resonant cycle to recharge C_{r1}. At t_4, V_{cr1} reaches 1 per unit and diode D_b clamps V_{cr1} to 1 per unit. The switch S_b can be turned on again at t_4, which is a half resonant cycle after the start of t_3:

$$t_4 \approx t_3 + \frac{\pi}{\omega} \qquad (15.26)$$

As t_3 cannot be determined accurately, a voltage sensor can be used, in principle, can be used to provide information for t_4 so that S_b can be turned on to reconnect C_1 to the inverter. In practice, however, S_b can be turned on a few microseconds (longer than $Ts + \pi/\omega$) after t_2 without using a voltage sensor (because it is not critical for S_b to be on exactly at the moment V_{cr} reaches the nominal voltage). As for switch S_{r2}, it can be turned on a few microseconds after t_4. It will be turned off half of resonant cycle $(\pi\sqrt{L_r C_{r2}})$ in the $L_r - C_{r2}$ circuit later. In practice, the timing of S_{r1}, S_{r2} and S_b can be adjusted in a simple tuning procedure for a given set of parameters. Figure

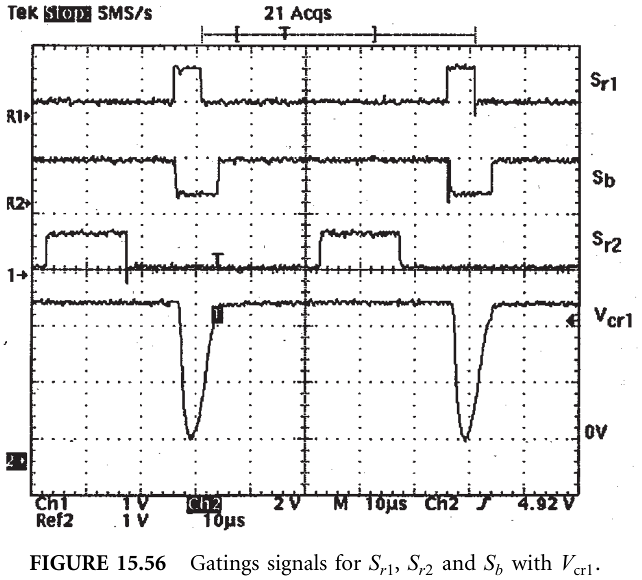


FIGURE 15.56 Gatings signals for S_{r1}, S_{r2} and S_b with V_{cr1}.

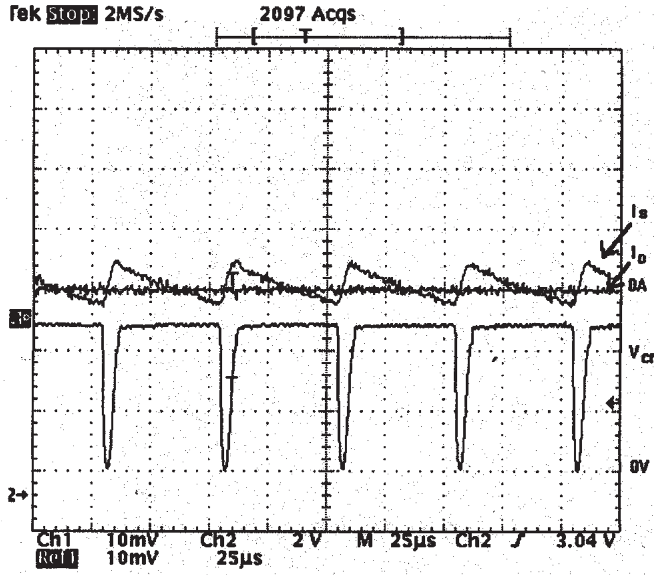


FIGURE 15.57 Typical I_s, I_o and $V_{\rm cr1}$ under no-load condition.

15.56 shows the measured gating signals of S_{r1}, S_{r2} and S_b with the dc link voltage $V_{\rm cr1}$ in a 20-kHz switching inverter. Figures 15.57 and 15.58 show typical I_s I_o, and $I_{\rm cr1}$ under no-load and loaded conditions, respectively.

15.14.4.3 Control of uasi-Resonant Soft-Switched Inverter using Digital Time Control

Based on the zero-average-current error (ZACE) control concept, a digital time control (DTC) method [48] has been developed for a current-controlled quasi-resonant soft-switched inverter. The basic ZACE concept is shown in Fig. 15.59. The current error is obtained from the difference of a reference current and the sensed current. The idea is to have the areas of each transition (*A*1 and *A*2) equal. If the switching

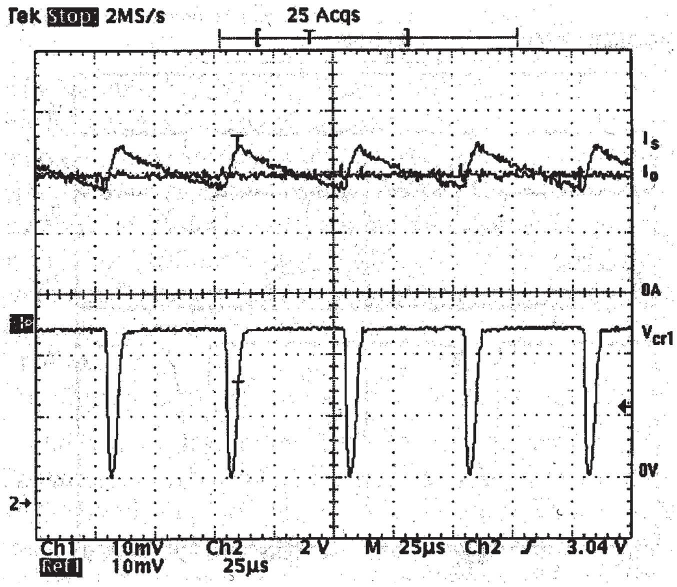


FIGURE 15.58 Typical I_s, I_o and $V_{\rm cr1}$ under loaded condition.

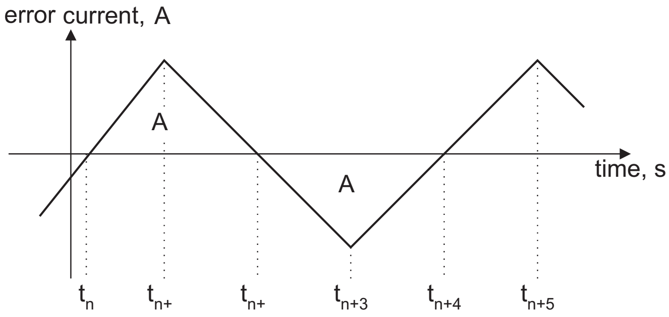

error current, A
A
A
time, s
tn
tn+
tn+
tn+3
tn+4
tn+5

FIGURE 15.59 Zero-average-current error (ZACE) control concept.

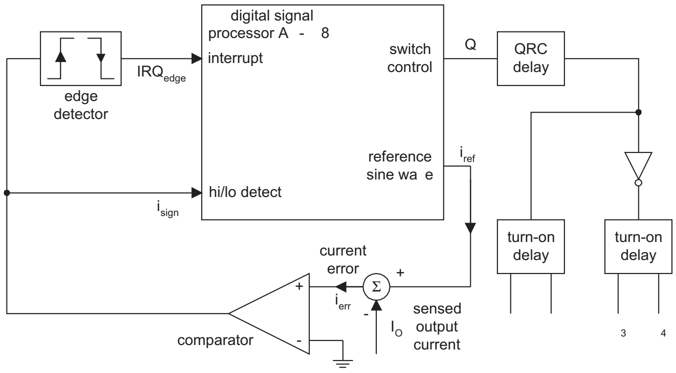

digital signal processor A - 8
interrupt
switch control
Q
QRC delay
edge detector
IRQedge
reference sine wa e
iref
hi/lo detect
isign
turn-on delay
turn-on delay
current error
+
Σ
+
-
ierr
Io
sensed output current
comparator
3
4

FIGURE 15.60 Implementation of DTC.

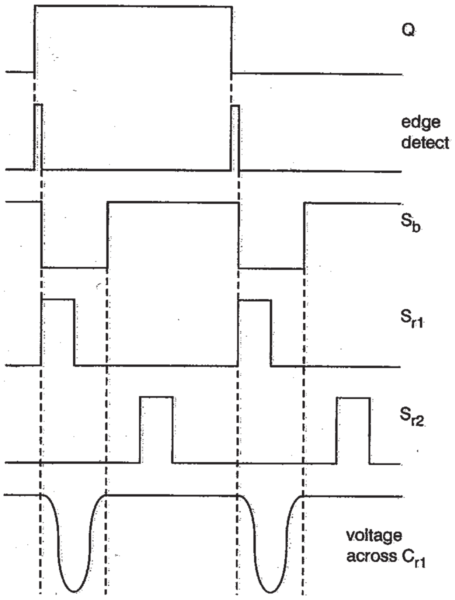

Q
edge detect
Sb
Sr1
Sr2
voltage across Cr1

FIGURE 15.61 Timing diagrams for the gating signals.

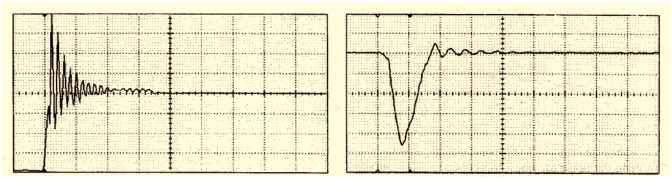


FIGURE 15.62 (a) Typical switch voltage under hard turn-off; and (b) typical switch voltage under soft-turn-off.

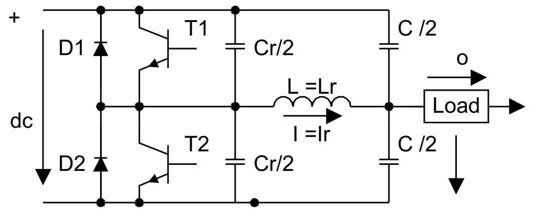

+
dc
D1
D2
T1
T2
Cr/2
Cr/2
L =Lr
I =Ir
C /2
C /2
o
Load

FIGURE 15.63 One leg of a resonant pole inverter.

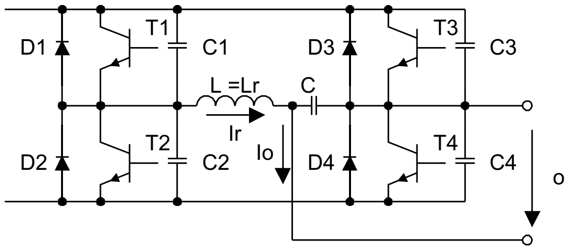

D1
D2
T1
T2
C1
C2
L =Lr
Ir
C
Io
D3
D4
T3
T4
C3
C4
o

FIGURE 15.64 Single-phase resonant pole inverter.

frequency is significantly greater than the fundamental frequency of the reference signal, the rising and falling current segments can be assumed to be linear. The following simplified equation can be established:

$$\Delta t_{n+1} = t_{n+1} - t_n \qquad (15.27)$$

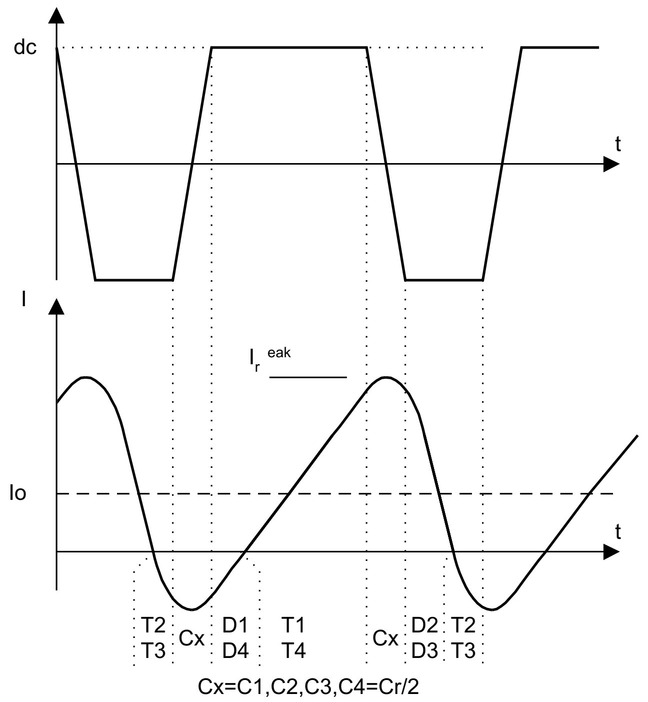


FIGURE 15.65 Timing diagram for a single-phase resonant pole inverter.

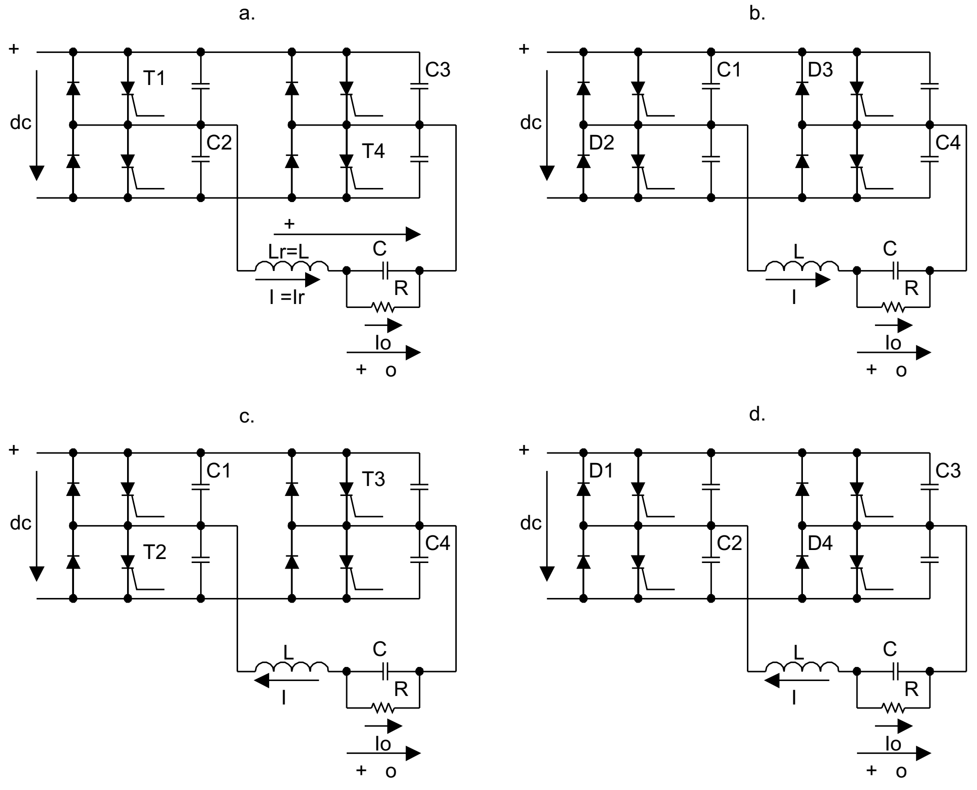

a.
b.
c.
d.
+
dc
T1
C2
C3
T4
+
Lr=L
I =Ir
C
R
Io
+ o
C1
D3
D2
C4
L
I
C1
T3
T2
C4
D1
C3
C2
D4

FIGURE 15.66 Operating mode of a single-phase resonant pole inverter.

The control algorithm for the inverter is

$$\Delta t_{n+3} = \Delta t_{n+2} + D\left[\frac{T_{\text{sw}}}{2} - (t_{n+2} - t_n)\right] \qquad (15.28)$$

where $D = \Delta t_{n+2}/t_{n+2} - t_n$ and $T_{\text{sw}} = t_{n+4} - t_n$.

The schematic of a digital signal processor (DSP)-based controller for the DTC method is shown in Fig. 15.60. The duty cycle can be approximated from the reference sine wave by level shifting and scaling it between 0 and 1. The time $t_{n+2} - t_n$ is the sum of Δt_{n+1} and Δt_{n+2}. These data provide information for the calculation of the next switching time Δt_{n+1}.

The switches are triggered by the changing edge of the switch control *Q*. Approximate delays are added to the individual switching signals for both the inverter switches and the quasi-resonant switches. Typical gating waveforms are shown in Fig. 15.61. The use of the quasi-resonant soft-switched inverter is a very effective way to suppress switching transient and EMI emission. Figure 15.62a,b shows the inverter switch voltage waveforms of a standard hard-switched inverter and a quasi-resonant soft-switched inverter, respectively. It is clear that the soft-switched waveform has much less transient than the hard-switched waveform.

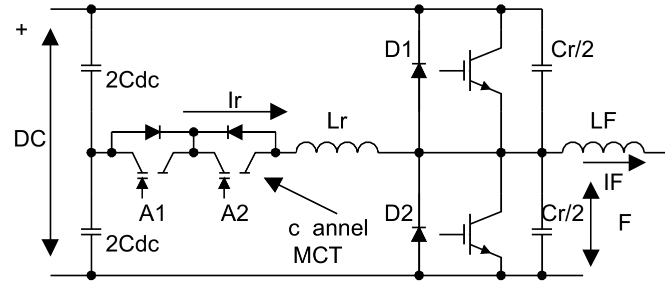


FIGURE 15.67 Improved resonant pole inverter leg.

15.14.5 Resonant Pole Inverter and Auxiliary Resonant Commutated Pole Inverter

The resonant pole inverter (RPI) integrates the resonant components with the output filter components L_f and C_f. The load is connected to the midpoint of the dc bus capacitors as shown in Fig. 15.63. However, it should be noted that the RPI can be described as a resonant inverter. Figure 15.64 shows a single-phase RPI. Its operation can be described with the timing diagram in Fig. 15.65. The operating modes are included in Fig. 15.66. The RPI provides soft-switching for all power switches but it has two disadvantages. First, power devices have to be switched continuously at the resonant frequency determined by the resonant components. Second, the power devices in the RPI circuit require a 2.2 to 2.5 p.u. current turn-off capability.

An improved version of the RPI is the auxiliary resonant commutated pole inverter (ARCPI). The ARCPI for one inverter leg is shown in Fig. 15.67. Unlike the basic RPI, the ARCPI allows the switching frequency to be controlled. Each of the primary switches is closely paralleled with a snubber capacitor to ensure ZV turn-off. Auxiliary switches are connected in series with an inductor, ensuring that they operate under ZC conditions. For each leg, an auxiliary circuit composed of two extra switches A1 and A2, two freewheeling diodes, and a resonant inductor L_r is required. This doubles the number of power switches when compared with hard-switched inverters. Figure 15.68 shows the three-phase ARCPI system. Depending on the load conditions, three commutation modes are generally needed. The commutation methods at low

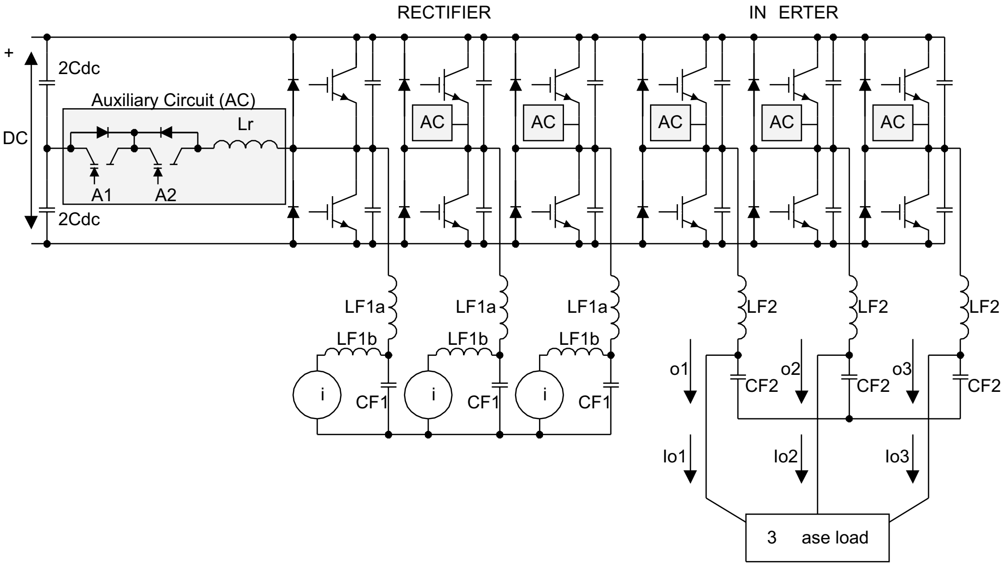


FIGURE 15.68 Three-phase auxiliary resonant commutated pole inverter (ARCPI).

and high current are different. This makes the control of the ARCPI very complex. The increase in control and circuit complexity represents a considerable cost penalty [50].

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16

AC AC Converters

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16.1 Introduction

A power electronic ac/ac converter, in generic form, accepts electric power from one system and converts it for delivery to another ac system with waveforms of different amplitude, frequency, and phase. They may be single-or three-phase types depending on their power ratings. The ac/ac converters employed to vary the rms voltage across the load at constant frequency are known as *ac voltage controllers or ac regulators.* The voltage control is accomplished either by: (i) *phase control* under natural commutation using pairs of silicon-controlled rectifiers (SCRs) or triacs; or (ii) by *on/off control* under forced commutation using fully controlled self-commutated switches such as Gate Turn-off Thyristors (GTOs), power transistors, Insulated Gate Bipolar Transistors (IGBTs), MOS-controlled Thyristors (MCTs), etc. The ac/ac power converters in which ac power at one frequency is directly converted to ac power at another frequency without any intermediate dc conversion link (as in the case of inverters discussed in Chapter 4, Section 14.3) are known as *cycloconverters*, the majority of which use naturally commutated SCRs for their operation when the maximum output frequency is limited to a fraction of the input frequency. With the rapid advancement in fast-acting fully controlled switches, force-commutated cycloconverters (FCC) or recently developed *matrix converters* with bidirectional on/off control switches provide independent control of the magnitude and frequency of the generated output voltage as well as sinusoidal modulation of output voltage and current.

While typical applications of ac voltage controllers include lighting and heating control, on-line transformer tap chaning, soft-starting and speed control of pump and fan drives, the cycloconverters are used mainly for high-power low-speed large ac motor drives for application in cement kilns, rolling mills, and ship propellers. The power circuits, control methods, and the operation of the ac voltage controllers, cycloconverters, and matrix converters are introduced in this chapter. A brief review is also given regarding their applications.

16.2 Single-Phase AC/AC Voltage Controller

The basic power circuit of a single-phase ac-ac voltage controller, as shown in Fig. 16.1a, is composed of a pair of

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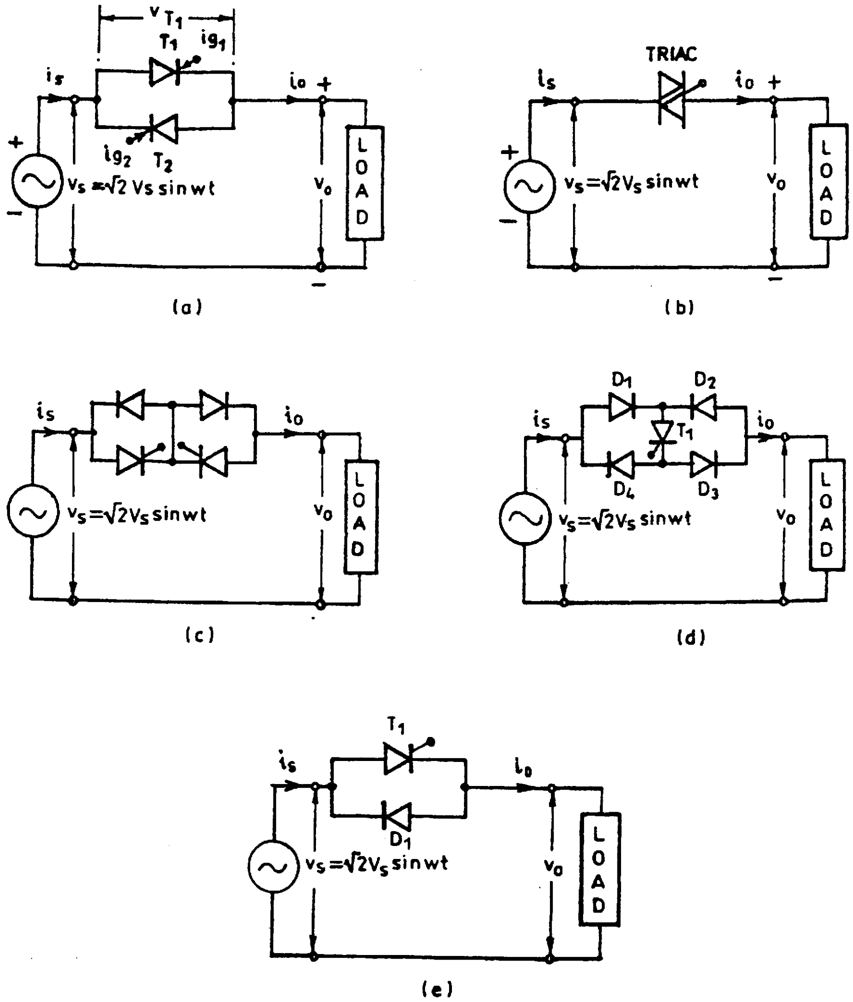

FIGURE 16.1 Single-phase ac voltage controllers: (a) full-wave, two SCRs in inverse parallel; (b) full-wave with Triac; (c) full wave with two SCRs and two diodes; (d) full wave with four diodes and one SCR; and (e) half wave with one SCR and one diode in antiparallel.

SCRs connected back-to-back (also known as inverse-parallel or antiparallel) between the ac supply and the load. This connection provides a *bidirectional full-wave symmetrical* control and the SCR pair can be replaced by a Triac (Fig. 16.1b) for low-power applications. Alternate arrangements are as shown in Fig. 16.1c with two diodes and two SCRs to provide a common cathode connection for simplifying the gating circuit without needing isolation, and in Fig. 16.1d with one SCR and four diodes to reduce the device cost but with increased device conduction loss. An SCR and diode combination, known as a *thyrode controller*, as shown in Fig. 16.1e, provides a *unidirectional half-wave asymmetrical voltage* control with device economy but introduces a dc component and more harmonics and thus is not very practical to use except for a very low power heating load.

With *phase control*, the switches conduct the load current for a chosen period of each input cycle of voltage and with *on/off* control the switches connect the load either for a few cycles of input voltage and disconnect it for the next few cycles (*integral cycle control*) or the switches are turned on and off several times within alternate half-cycles of input voltage (*ac chopper or PWM ac voltage controller*).

16.2.1 Phase-Controlled Single-Phase AC Voltage Controller

For a full-wave, symmetrical phase control, the SCRs T_1 and T_2 in Fig. 16.1a are gated at α and $\pi + \alpha$, respectively, from the zero crossing of the input voltage and by varying α, the power flow to the load is controlled through voltage control in alternate half-cycles. As long as one SCR is carrying current, the other SCR remains reverse-biased by the voltage drop across the conducting SCR. The principle of operation in each half-cycle is similar to that of the controlled half-wave rectifier (Chapter 11, Section 11.2) and one can use the same approach for analysis of the circuit.

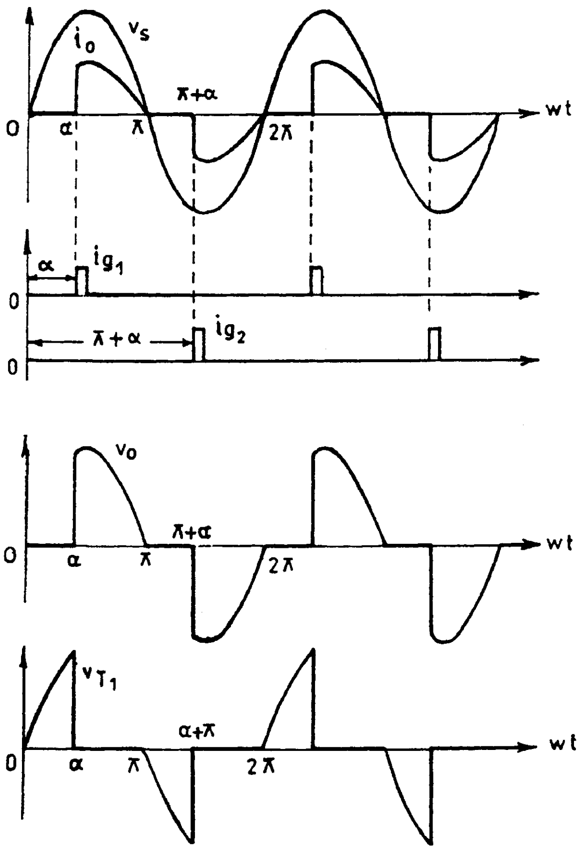

FIGURE 16.2 Waveforms for single-phase ac full-wave voltage controller with R-load.

Operation with R-load. Figure 16.2 shows the typical voltage and current waveforms for the single-phase bidirectional phase-controlled ac voltage controller of Fig. 16.1a with resistive load. The output voltage and current waveforms have half-wave symmetry and thus no dc component.

If $v_s = \sqrt{2}V_s \sin \omega t$ is the source voltage, then the rms output voltage with T_1 triggered at α can be found from the half-wave symmetry as

$$V_o = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} 2V_s^2 \sin^2 \omega t \; d(\omega t)\right]^{1/2} = V_s\left[1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right]^{1/2} \tag{16.1}$$

Note that V_o can be varied from V_s to 0 by varying α from 0 to π. The rms value of load current:

$$I_o = \frac{V_o}{R} \tag{16.2}$$

The input power factor:

$$\frac{P_o}{VA} = \frac{V_o}{V_s} = \left[1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right]^{1/2} \tag{16.3}$$

The average SCR current:

$$I_{A,\text{SCR}} = \frac{1}{2\pi \text{R}}\int_{\alpha}^{\pi} \sqrt{2}V_s \sin \omega t \; d(\omega t) \tag{16.4}$$

As each SCR carries half the line current, the rms current in each SCR is

$$I_{o,\text{SCR}} = I_o/\sqrt{2} \tag{16.5}$$

Operation with RL Load. Figure 16.3 shows the voltage and current waveforms for the controller in Fig. 16.1a with RL load. Due to the inductance, the current carried by the SCR T_1 may not fall to zero at $\omega t = \pi$ when the input voltage goes negative and may continue until $\omega t = \beta$, the extinction angle, as shown. The conduction angle

$$\theta = \beta - \alpha \tag{16.6}$$

of the SCR depends on the firing delay angle α and the load impedance angle ϕ. The expression for the load current $I_o(\omega t)$

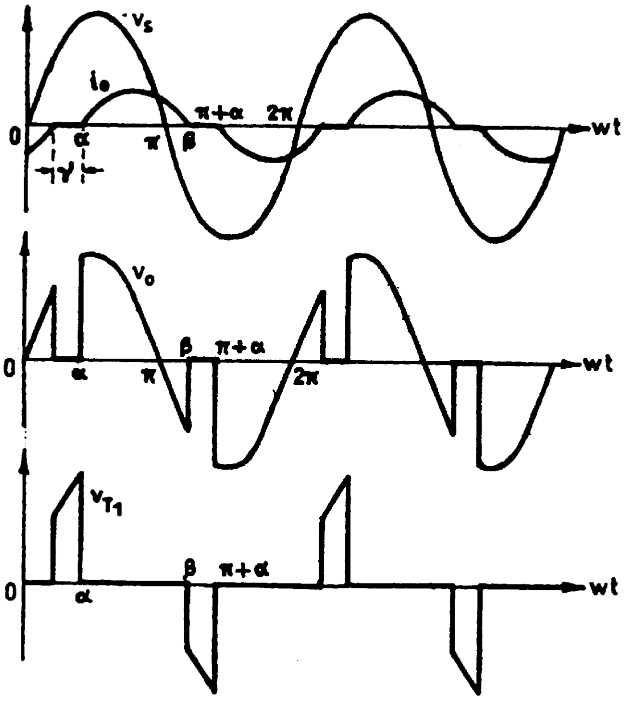

FIGURE 16.3 Typical waveforms of single-phase ac voltage controller with an RL-load.

when conducting from α to β can be derived in the same way as that used for a phase-controlled rectifier in a discontinuous mode (Chaper 11, Section 11.2) by solving the relevant Kirchhoff voltage equation:

$$i_o(\omega t) = \frac{\sqrt{2}V}{Z}[\sin(\omega t - \phi) - \sin(\alpha - \phi)e^{(\alpha - \omega t)/\tan\phi}], \quad \alpha < \omega t < \beta \quad (16.7)$$

where $Z = (R^2 + \omega^2 L^2)^{1/2}$ = load impedance and ϕ = load impedance angle $= \tan^{-1}(\omega L/R)$. The angle β, when the current i_o falls to zero, can be determined from the following transcendental equation obtained by putting $i_o(\omega t = \beta) = 0$ in Eq. (16.7)

$$\sin(\beta - \phi) = \sin(\alpha - \phi) - \sin(\alpha - \phi)e^{(\alpha - \beta)/\tan\phi} \quad (16.8)$$

From Eqs. (16.6) and (16.8) one can obtain a relationship between θ and α for a given value of ϕ as shown in Fig. 16.4, which shows that as α is increased the conduction angle θ decreases and the rms value of the current decreases. The rms output voltage

$$V_o = \left[\frac{1}{\pi}\int_\alpha^\beta 2V_s^2 \sin^2 \omega t \, d(t)\right]^{1/2} = \frac{V_s}{\pi}\left[\beta - \alpha + \frac{\sin 2\alpha}{2} - \frac{\sin 2\beta}{2}\right]^{1/2} \quad (16.9)$$

V_o can be evaluated for two possible extreme values of $\phi = 0$ when $\beta = \pi$ and $\phi = \pi/2$ when $\beta = 2\pi - \alpha$, and the envelope of the voltage-control characteristics for this controller is shown in Fig. 16.5.

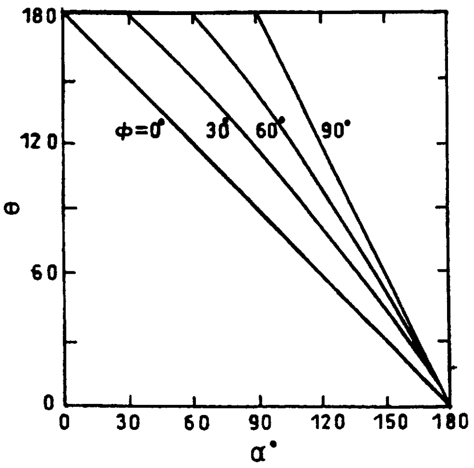

FIGURE 16.4 θ vs α curves for single-phase ac voltage controller with *RL* load.

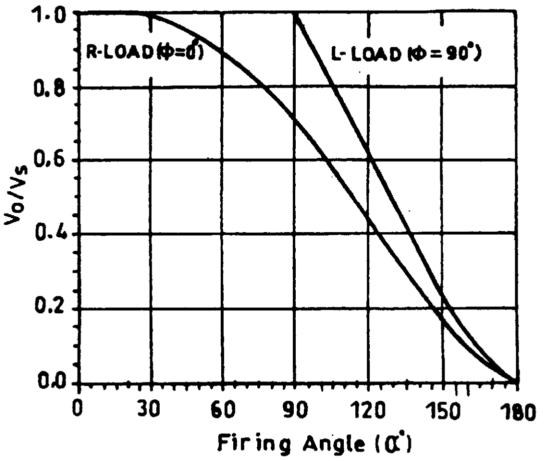

FIGURE 16.5 Envelope of control characteristics of a single-phase ac voltage controller with *RL* load.

The rms SCR current can be obtained from Eq. (16.7) as

$$I_{o,\mathrm{SCR}} = \left[\frac{1}{2\pi}\int_\alpha^\beta i_o^2 \, d(\omega t)\right] \quad (16.10)$$

The rms load current

$$I_o = \sqrt{2}I_{o,\mathrm{SCR}} \quad (16.11)$$

The average value of SCR current

$$I_{A,\mathrm{SCR}} = \frac{1}{2\pi}\int_\alpha^\beta i_o \, d(\omega t) \quad (16.12)$$

Gating Signal Requirements. For the inverse parallel SCRs as shown in Fig. 16.1a, the gating signals of SCRs must be isolated from one another as there is no common cathode. For *R*-load, each SCR stops conducting at the end of each half-cycle and under this condition, single short pulses may be used for gating as shown in Fig. 16.2. With *RL* load, however, this single short pulse gating is not suitable as shown in Fig. 16.6. When SCR T_2 is triggered at $\omega t = \pi + \alpha$, SCR T_1 is still conducting due to the load inductance. By the time the SCR T_1 stops conducting at β, the gate pulse for SCR T_2 has already ceased and T_2 will fail to turn on, causing the converter to operate as a single-phase rectifier with conduction of T_1 only. This necessitates application of a sustained gate pulse either in the form of a continuous signal for the half-cycle period, which increases the dissipation in SCR gate circuit and a large isolating pluse transformer or better a *train of pulses* (*carrier frequency gating*) to overcome these difficulties.

Operation with $\alpha < \phi$. If $\alpha = \phi$, then from Eq. (16.8),

$$\sin(\beta - \phi) = \sin(\beta - \alpha) = 0 \quad (16.13)$$

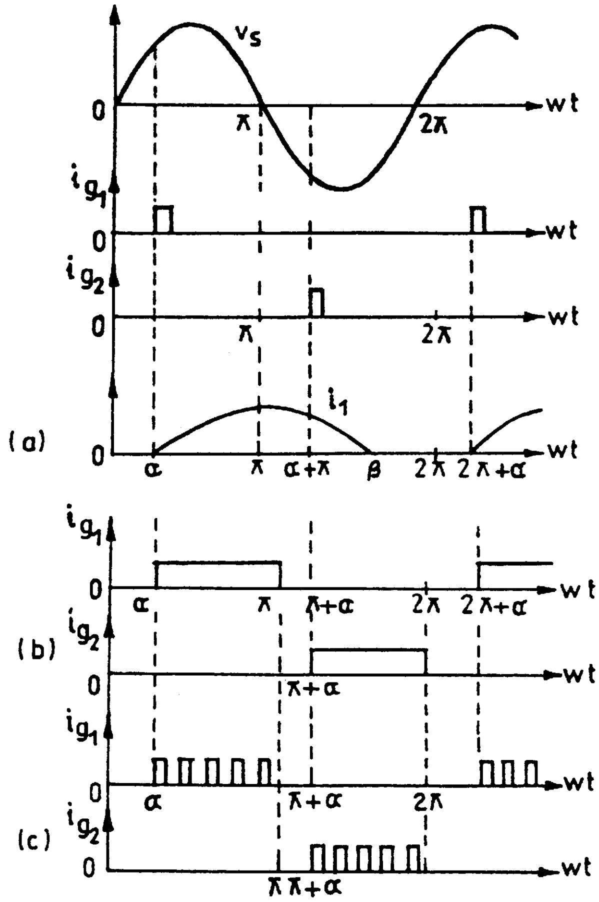

FIGURE 16.6 Single-phase full-wave controller with *RL* load: Gate pulse requirements.

and

$$\beta - \alpha = \theta = \pi \tag{16.14}$$

As the conduction angle θ cannot exceed π and the load current must pass through zero, the control range of the firing angle is $\phi \leq \alpha \leq \pi$. With narrow gating pulses and $\alpha < \phi$, only one SCR will conduct resulting in a rectifier action as shown. Even with a train of pulses, if $\alpha < \phi$, the changes in the firing angle will not change the output voltage and current but both SCRs will conduct for the period π with T_1 becoming on at $\omega t = \pi$ and T_2 at $\omega t + \pi$. This *dead zone* ($\alpha = 0$ to ϕ), whose duration varies with the load impedance angle ϕ, is not a desirable feature in closed-loop control schemes. An alternative approach to the phase control with respect to the input voltage zero crossing has been reported in which the firing angle is defined with respect to the instant when it is the load current (not the input voltage) that reaches zero, this angle being called *the hold-off angle* (γ) *or the control angle* (as marked in Fig. 16.3). This method requires sensing the load current which may otherwise be required anyway in a closed-loop controller for monitoring or control purposes.

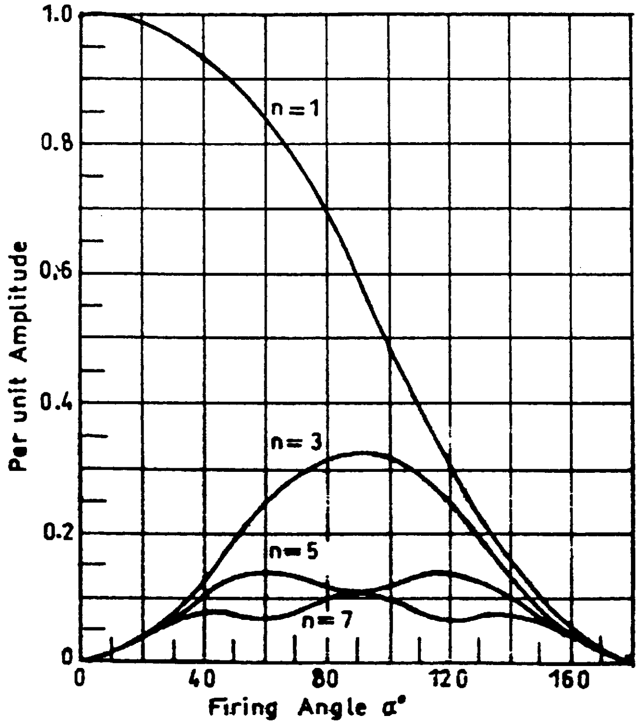

FIGURE 16.7 Harmonic content as a function of the firing angle for a single-phase voltage controller with *RL* load.

Power Factor and Harmonics. As in the case of phase-controlled rectifiers, the important limitations of the phase-controlled ac voltage controllers are the poor power factor and the introduction of harmonics in the source currents. As seen from Eq. (16.3), the input power factor depends on α, and as α increases, the power factor decreases.

The harmonic distortion increases and the quality of the input current decreases with increase of firing angle. The variations of low-order harmonics with the firing angle as computed by Fourier analysis of the voltage waveform of Fig. 16.2 (with *R*-load) are shown in Fig. 16.7. Only odd harmonics exist in the input current because of half-wave symmetry.

16.2.2 Single-Phase AC/AC Voltage Controller with ON/OFF Control

Integral Cycle Control. As an alternative to the phase control, the method of integral cycle control or burst-firing is used for heating loads. Here, the switch is turned on for a time t_n with n integral cycles and turned off for a time t_m with m integral cycles (Fig. 16.8). As the SCRs or Triacs used here are turned on at the zero-crossing of the input voltage and turn-off occurs at zero current, supply harmonics and radio frequency interference are very low.

However, subharmonic frequency components may be generated that are undesirable as they may set up subharmonic resonance in the power supply system, cause lamp flicker, and

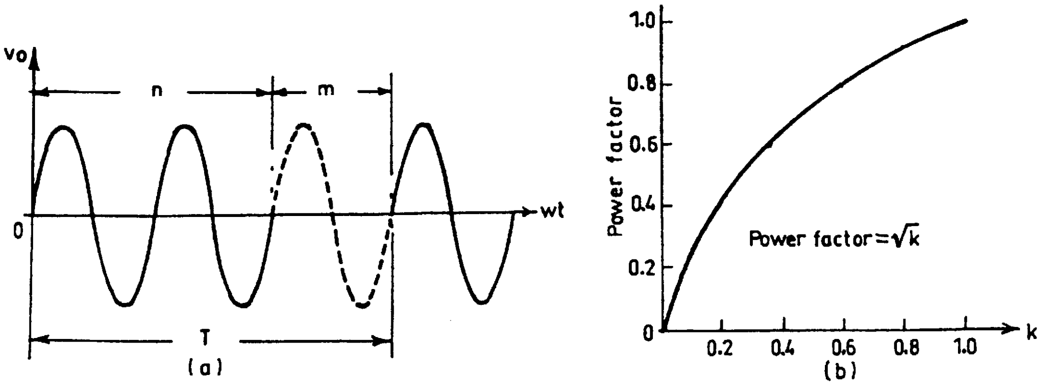

FIGURE 16.8 Integral cycle control: (a) typical load-voltage waveforms; and (b) power factor with the duty cycle *k*.

may interfere with the natural frequencies of motor loads causing shaft oscillations.

For sinusoidal input voltage $v = \sqrt{2}V_s \sin \omega t$, the rms output voltage

$$V_o = V_s\sqrt{k} \tag{16.15}$$

where $k = n/(n+m) =$ *duty cycle* and $V_s =$ rms phase voltage. The power factor is

$$\sqrt{k} \tag{16.16}$$

which is poorer for lower values of the duty cycle *k*.

P M AC Chopper. As in the case of controlled rectifier in Chapter 11, Section 11.6, the performance of ac voltage controllers can be improved in terms of harmonics, quality of output current and input power factor by *pulsewidth modulation* (PWM) control in PWM ac choppers. The circuit configuration of one such single-phase unit is shown in Fig. 16.9. Here, fully controlled switches S_1 and S_2 connected in antiparallel are turned on and off many times during the positive and negative half-cycles of the input voltage, respectively; S_1' and S_2' provide the freewheeling paths for the load current when S_1 and S_2 are off. An input capacitor filter may be provided to attenuate the high switching frequency current drawn from the supply and also to improve the input power factor. Figure 16.10 shows the typical output voltage and load-current waveform for a single-phase PWM ac chopper. It can be shown that the control characteristics of an ac chopper depend on the *modulation index M*, which theoretically varies from zero to unity.

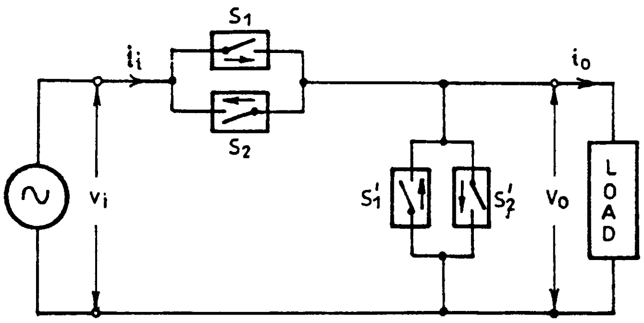

FIGURE 16.9 Single-phase PWM as chopper circuit.

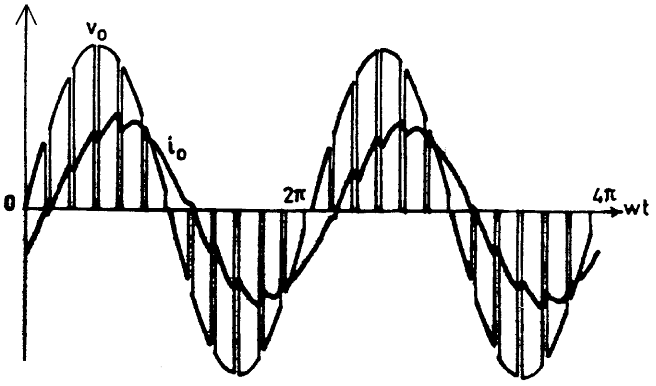

FIGURE 16.10 Typical output voltage and current waveforms of a single-phase PWM ac chopper.

Three-phase PWM choppers consist of three single-phase choppers either delta connected or four-wire star connected.

16.3 Three-Phase AC/AC Voltage Controllers

16.3.1 Phase-Controlled Three-Phase AC Voltage Controllers

Various Configurations. Several possible circuit configurations for three-phase phase-controlled ac regulators with star- or delta-connected loads are shown in Fig. 16.11a–h. The configurations in Fig. 16.11a and b can be realized by three single-phase ac regulators operating independently of each other and they are easy to analyze. In Fig. 16.11a, the SCRs are

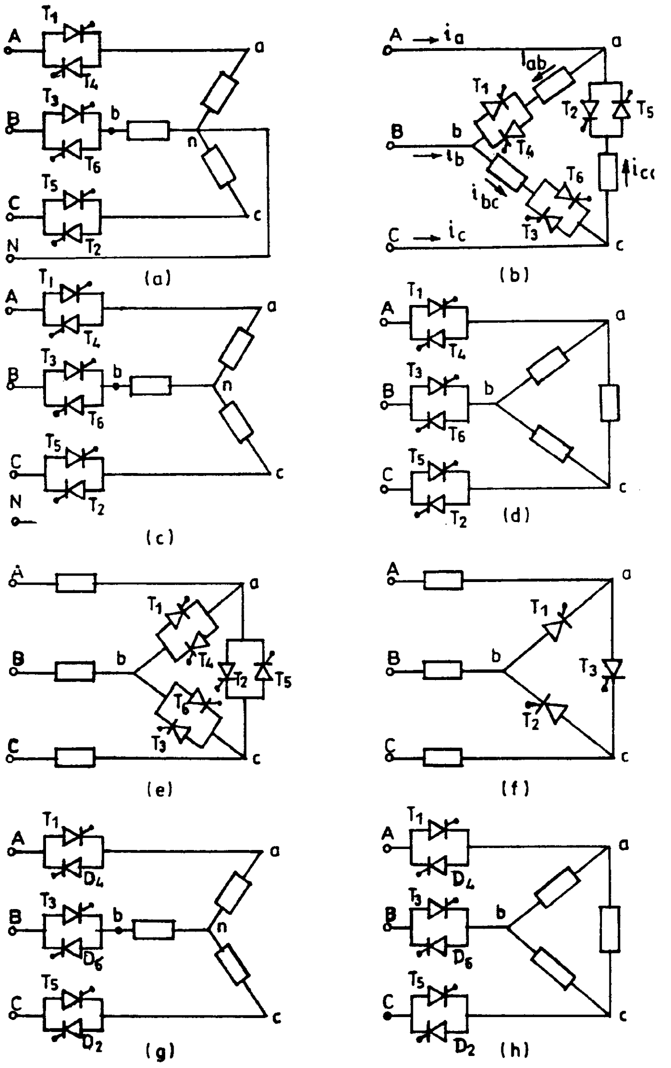

FIGURE 16.11 Three-phase ac voltage-controller circuit configurations.

to be rated to carry line currents and withstand phase voltages, whereas in Fig. 16.11b they should be capable of carrying phase currents and withstand the line voltages. Also, in Fig. 16.11b the line currents are free from triplen harmonics while these are present in the closed delta. The power factor in Fig. 16.11b is slightly higher. The firing angle control range for both these circuits is 0 to 180° for R-load.

The circuits in Fig. 16.11c and d are three-phase three-wire circuits and are difficult to analyze. In both these circuits, at least two SCRs — one in each phase — must be gated simultaneously to get the controller started by establishing a current path between the supply lines. This necessitates two firing pulses spaced at 60° apart per cycle for firing each SCR. The operation modes are defined by the number of SCRs conducting in these modes. The firing control range is 0 to 150°. The triplen harmonics are absent in both these configurations.

Another configuration is shown in Fig. 16.11e when the controllers are delta connected and the load is connected between the supply and the converter. Here, current can flow between two lines even if one SCR is conducting, so each SCR requires one firing pulse per cycle. The voltage and current ratings of SCRs are nearly the same as those of the circuit in Fig. 6.11b. It is also possible to reduce the number of devices to three SCRs in delta as shown in Fig. 16.11f connecting one source terminal directly to one load circuit terminal. Each SCR is provided with gate pulses in each cycle spaced 120° apart. In both Figs. 16.11e and f each end of each phase must be accessible. The number of devices in Fig. 16.11f is fewer but their current ratings must be higher.

As in the case of the single-phase phase-controlled voltage regulator, the total regulator cost can be reduced by replacing six SCRs by three SCRs and three diodes, resulting in three-phase *half-wave controlled* unidirectional ac regulators as shown in Fig. 16.11g and h for star- and delta-connected loads. The main drawback of these circuits is the large harmonic content in the output voltage, particularly the second harmonic because of the asymmetry. However, the dc components are absent in the line. The maximum firing angle in the half-wave controlled regulator is 210°.

16.3.2 Fully Controlled Three-Phase Three-Wire AC Voltage Controller

16.3.2.1 Star-Connected Load with Isolated Neutral

The analysis of operation of the full-wave controller with isolated neutral as shown in Fig. 16.11c is, as mentioned, quite complicated in comparison to that of a single-phase controller, particularly for an RL or motor load. As a simple example, the operation of this controller is considered here with a simple star-connected R-load. The six SCRs are turned on in the sequence 1-2-3-4-5-6 at 60° intervals and the gate signals are sustained throughout the possible conduction angle.

The output phase voltage waveforms for $\alpha = 30$, 75, and 120° for a balanced three-phase R-load are shown in Fig. 16.12. At any interval, either three SCRs or two SCRs, or no SCRs may be on and the instantaneous output voltages to the load are either line-to-neutral voltages (three SCRs on), or one-half of the line-to-line voltage (two SCRs on) or zero (no SCR on).

Depending on the firing angle α, there may be *three* operating modes.

Mode I (also known as Mode 2/3) $0 \leq \alpha \leq 60°$. There are periods when *three* SCRs are conducting, one in each phase for either direction and periods when just *two* SCRs conduct.

For example, with $\alpha = 30°$ in Fig. 16.12a, assume that at $\omega t = 0$, SCRs T_5 and T_6 are conducting, and the current through the R-load in a-phase is zero making $v_{an} = 0$. At $\omega t = 30°$, T_1 receives a gate pulse and starts conducting; T_5

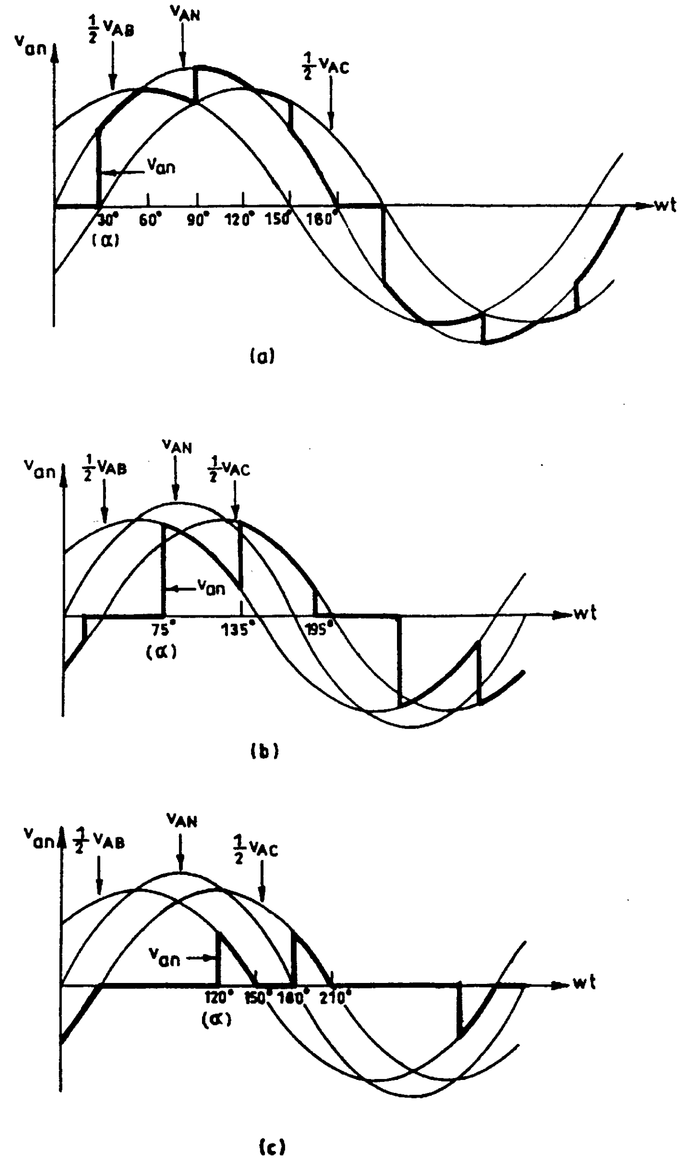

FIGURE 16.12 Output voltage waveforms for a three-phase ac voltage controller with star-connected *R*-load: (a) v_{an} for $\alpha = 30°$; (b) v_{an} for $\alpha = 75°$; and (c) $v_{\text{an}} = 120°$.

and T_6 remain on and $v_{\text{an}} = v_{\text{AN}}$. The current in T_5 reaches zero at 60°, turning T_5 off. With T_1 and T_6 staying on, $v_{an} = 1/2v_{\text{AB}}$. At 90°, T_2 is turned on, the three SCRs T_1, T_2, and T_6 are then conducting and $v_{\text{an}} = v_{\text{AN}}$. At 120°, T_6 turns off, leaving T_1 and T_2 on, so $v_{\text{AN}} = 1/2v_{\text{AC}}$. Thus with the progress of firing in sequence until $\alpha = 60°$, the number of SCRs conducting at a particular instant alternates between two and three.

Mode II (also known as Mode 2 2) $60° \le \alpha \le 90°$. *Two* SCRs, one in each phase, always conduct.

For $\alpha = 75°$ as shown in Fig. 16.12b, just prior to $\alpha = 75°$, SCRs T_5 and T_6 were conducting and $v_{\text{an}} = 0$. At 75°, T_1 is turned on, T_6 continues to conduct while T_5 turns off as v_{CN} is negative; $v_{\text{an}} = 1/2v_{\text{AB}}$. When T_2 is turned on at 135°, T_6 is turned off and $v_{\text{an}} = 1/2v_{\text{AC}}$. The next SCR to turn on is T_3, which turns off T_1 and $v_{\text{an}} = 0$. One SCR is always turned off when another is turned on in this range of α and the output is either one-half line-to-line voltage or zero.

Mode III (also known as Mode 0 2) $90° \le \alpha \le 150°$. When *none* or *two* SCRs conduct.

For $\alpha = 120°$ (Fig. 16.12c), earlier no SCRs were on and $v_{\text{an}} = 0$. At $\alpha = 120°$, SCR T_1 is given a gate signal while T_6 has a gate signal already applied. As v_{AB} is positive, T_1 and T_6 are forward-biased and they begin to conduct and $v_{\text{an}} = 1/2v_{\text{AB}}$. Both T_1 and T_6 turn off when v_{AB} becomes negative. When a gate signal is given to T_2, it turns on and T_1 turns on again.

For $\alpha > 150°$, there is no period when two SCRs are conducting and the output voltage is zero at $\alpha = 150°$. Thus, the range of the firing angle control is $0 \le \alpha \le 150°$.

For *star-connected R-load*, assuming the instantaneous phase voltages as

$$\begin{aligned} v_{\text{AN}} &= \sqrt{2}V_s \sin \omega t \\ v_{\text{BN}} &= \sqrt{2}V_s \sin(\omega t - 120°) \qquad (16.17) \\ v_{\text{CN}} &= \sqrt{2}V_s \sin(\omega t - 240°) \end{aligned}$$

the expressions for the rms output phase voltage V_o can be derived for the three modes as

$$0 \le \alpha \le 60° \qquad V_o = V_s\left[1 - \frac{3\alpha}{2\pi} + \frac{3}{4\pi}\sin 2\alpha\right]^{1/2} \qquad (16.18)$$

$$60° \le \alpha \le 90° \qquad V_o = V_s\left[\frac{1}{2} + \frac{3}{4\pi}\sin 2\alpha + \sin(2\alpha + 60°)\right]^{1/2} \qquad (16.19)$$

$$90° \le \alpha \le 150° \qquad V_o = V_s\left[\frac{5}{4} - \frac{3\alpha}{2\pi} + \frac{3}{4\pi}\sin(2\alpha + 60°)\right]^{1/2} \qquad (16.20)$$

For *star-connected pure L-load*, the effective control starts at $\alpha > 90°$ and the expressions for two ranges of α are:

$$90° \le \alpha \le 120° \qquad V_o = V_s\left[\frac{5}{2} - \frac{3\alpha}{\pi} + \frac{3}{2\pi}\sin 2\alpha\right]^{1/2} \qquad (16.21)$$

$$120° \le \alpha \le 150° \qquad V_o = V_s\left[\frac{5}{2} - \frac{3\alpha}{\pi} + \frac{3}{2\pi}\sin(2\alpha + 60°)\right]^{1/2} \qquad (16.22)$$

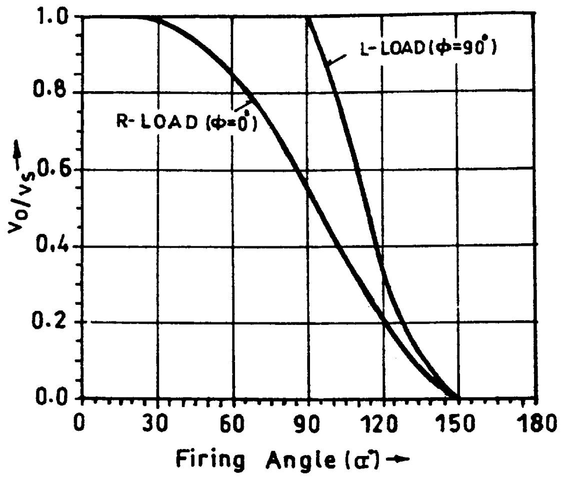

FIGURE 16.13 Envelope of control characteristics for a three-phase full-wave ac voltage controller.

The control characteristics for these two limiting cases ($\phi = 0$ for R-load and $\phi = 90°$ for L-load) are shown in Fig. 16.13. Here, also, as in the single-phase case the dead zone may be avoided by controlling the voltage with respect to the control angle or hold-off angle (γ) from the zero crossing of current in place of the firing angle α.

***RL* Load.** The analysis of the three-phase voltage controller with star-connected RL load with isolated neutral is quite complicated as the SCRs do not cease to conduct at voltage zero and the extinction angle β is to be known by solving the transcendental equation for the case. The Mode-II operation, in this case, disappears [1] and the operation-shift from Mode I to Mode III depends on the so-called critical angle α_{crit} [2, 4], which can be evaluated from a numerical solution of the relevant transcendental equations. Computer simulation either by PSPICE program [3, 7] or a switching-variable approach coupled with an iterative procedure [11] is a practical means of obtaining the output voltage waveform in this case. Figure 16.14 shows typical simulation results, using the later approach [11] for a three-phase voltage-controller-fed RL load for $\alpha = 60$, 90, and 105°, which agree with the corresponding practical oscillograms given in reference [5].

Delta-Connected *R*-load. The configuration is shown in Fig. 16.11b. The voltage across an R-load is the corresponding line-to-line voltage when one SCR in that phase is on. Figure 16.15 shows the line and phase currents for $\alpha = 120°$ and 90° with an R-load. The firing angle α is measured from the zero crossing of the line-to-line voltage and the SCRs are turned on in the sequence as they are numbered. As in the single-phase case, the range of firing angle is $0 \leq \alpha \leq 180°$. The line currents can be obtained from the phase currents as

$$\begin{aligned} i_a &= i_{\text{ab}} - i_{\text{ca}} \\ i_b &= i_{\text{bc}} - i_{\text{ab}} \\ i_c &= i_{\text{ca}} - i_{\text{bc}} \end{aligned} \tag{16.23}$$

The line currents depend on the firing angle and may be discontinuous as shown. Due to the delta connection, the triplen harmonic currents flow around the closed delta and do not appear in the line. The rms value of the line current varies between the range

$$\sqrt{2} I_{\Delta} \leq I_{\text{L,rms}} \leq \sqrt{3} I_{\Delta,\text{rms}} \tag{16.24}$$

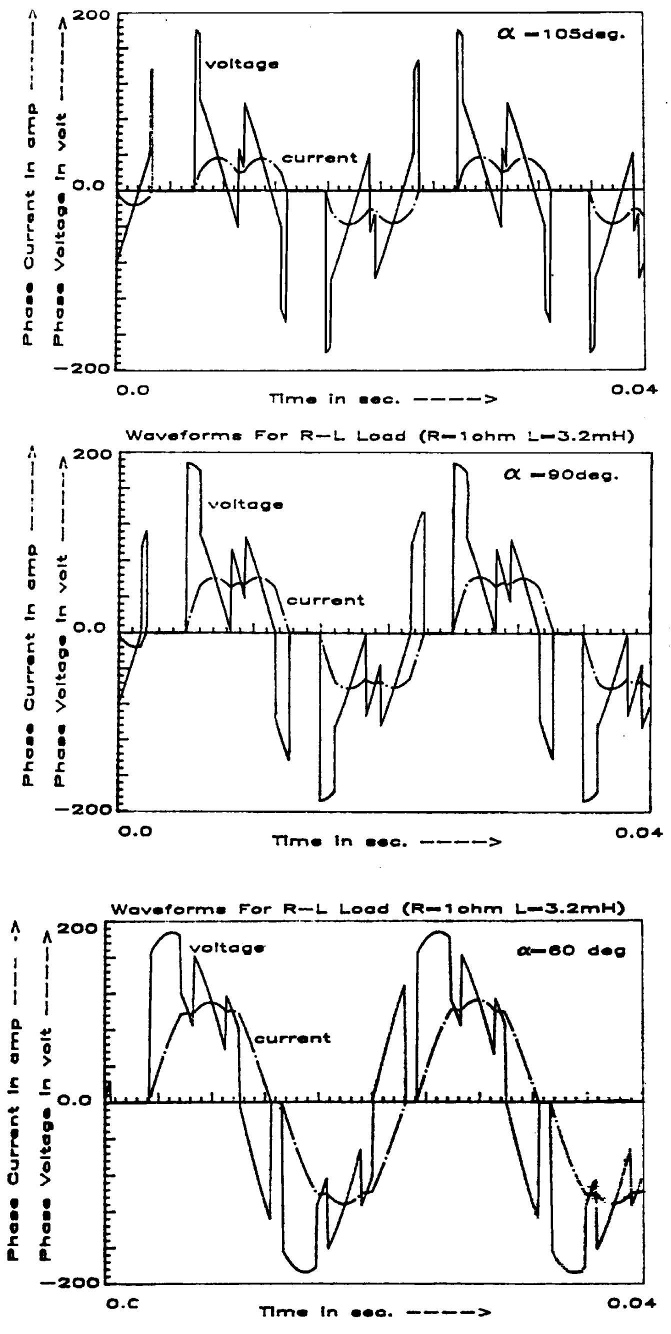

FIGURE 16.14 Typical simulation results for three-phase ac voltage-controller-fed RL load ($R = 1\,\text{ohm}$, $L = 3.2\,\text{mH}$) for $\alpha = 60$, 90, and 105°.

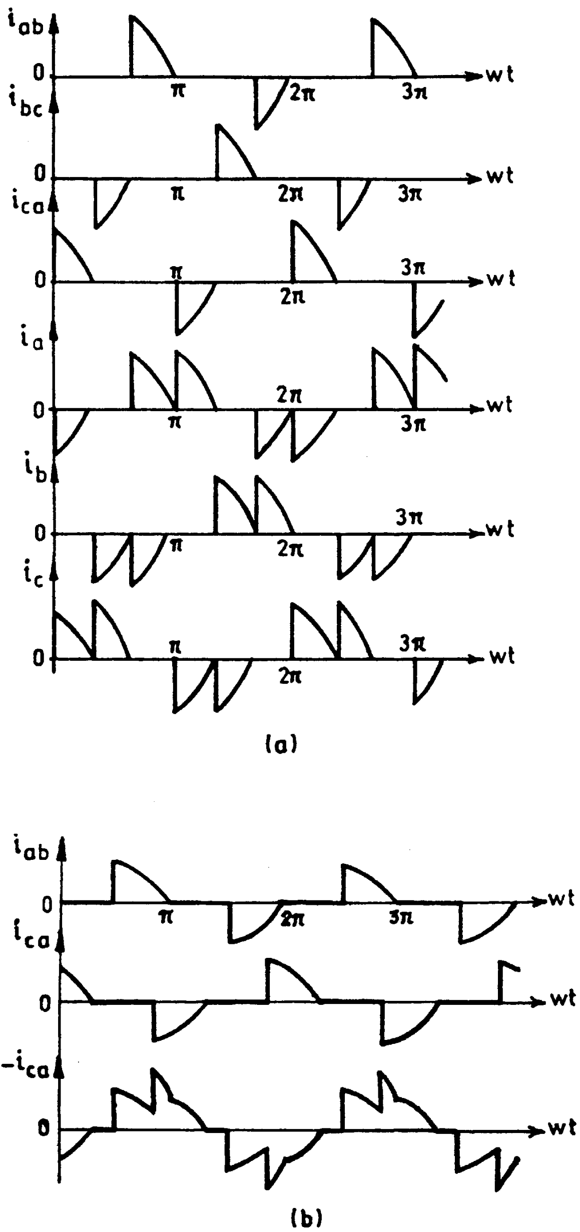

FIGURE 16.15 Waveforms of a three-phase ac voltage controller with a delta-connected R-load: (a) $\alpha = 120°$; (b) $\alpha = 90°$.

as the conduction angle varies from very small (large α) to $180°$ ($\alpha = 0$).

16.4 Cycloconverters

In contrast to the ac voltage controllers operating at constant frequency discussed so far, a cycloconverter operates as a direct ac/ac frequency changer with an inherent voltage control feature. The basic principle of this converter to construct an alternating voltage wave of lower frequency from successive segments of voltage waves of higher frequency ac supply by a switching arrangement was conceived and patented in the 1920s. Grid-controlled mercury-arc rectifiers were used in these converters installed in Germany in the 1930s to obtain $16\frac{2}{3}$-Hz single-phase supply for ac series traction motors from a three-phase 50-Hz system while at the same time a cycloconverter using 18 thyratrons supplying a 400-hp synchronous motor was in operation for some years as a power station auxiliary drive in the United States. However, the practical and commercial utilization of these schemes waited until the SCRs became available in the 1960s. With the development of large power SCRs and microprocessor-based control, the cycloconverter today is a matured practical converter for application in large-power low-speed variable-voltage variable-frequency (VVVF) ac drives in cement and steel rolling mills as well as in variable-speed constant-frequency (VSCF) systems in aircraft and naval ships.

A cycloconverter is a naturally commuted converter with the inherent capability of bidirectional power flow and there is no real limitation on its size unlike an SCR inverter with commutation elements. Here, the switching losses are considerably low, the regenerative operation at full power over complete speed range is inherent, and it delivers a nearly sinusoidal waveform resulting in minimum torque pulsation and harmonic heating effects. It is capable of operating even with the blowing out of an individual SCR fuse (unlike the inverter), and the requirements regarding turn-off time, current rise time and dv/dt sensitivity of SCRs are low. The main limitations of a naturally commutated cycloconverter are: (i) limited frequency range for subharmonic-free and efficient operation; and (ii) poor input displacement/power factor, particularly at low output voltages.

16.4.1 Single-Phase/Single-Phase Cycloconverter

Though rarely used, the operation of a single-phase to single-phase cycloconverter is useful to demonstrate the basic principle involved. Figure 16.16a shows the power circuit of a single-phase bridge-type cycloconverter, which is the same arrangement as that of the dual converter described in Chapter 11, Section 11.4. The firing angles of the individual two-pulse two-quadrant bridge converters are continuously modulated here so that each ideally produces the same fundamental ac voltage at its output terminals as marked in the simplified equivalent circuit in Fig. 16.16b. Because of the unidirectional current-carrying property of the individual converters, it is inherent that the positive half-cycle of the current is carried by the P-converter and the negative half-cycle of the current by the N-converter regardless of the phase of the current with respect to the voltage. This means that for a reactive load, each converter operates in both the rectifying and inverting region

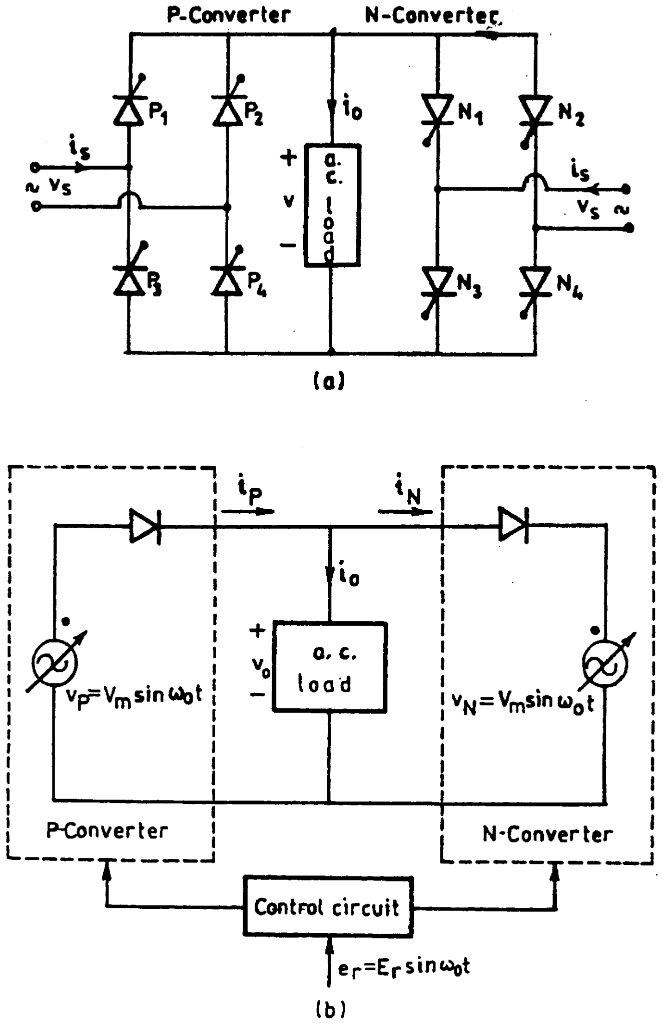

FIGURE 16.16 (a) Power circuit for a single-phase bridge cycloconverter; and (b) simplified equivalent circuit of a cycloconverter.

during the period of the associated half-cycle of the low-frequency output current.

Operation with R-Load. Figure 16.17 shows the input and output voltage waveforms with a pure R-load for a 50 to $16\frac{2}{3}$ Hz cycloconverter. The P- and N-converters operate for all alternate $T_o/2$ periods. The output frequency $(1/T_o)$ can be varied by varying T_o and the voltage magnitude by varying the firing angle α of the SCRs. As shown in the figure, three cycles of the ac input wave are combined to produce one cycle of the output frequency to reduce the supply frequency to one-third across the load.

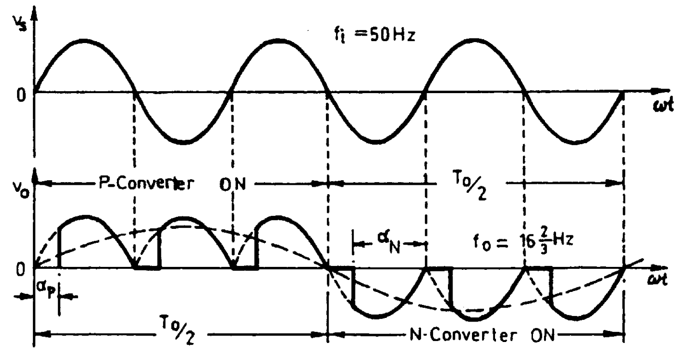

FIGURE 16.17 Input and output waveforms of a 50 to $16\frac{2}{3}$-Hz cycloconverter with RL load.

If α_P is the firing angle of the P-converter, the firing angle of the N-converter α_N is $\pi - \alpha_P$ and the average voltage of the P-converter is equal and opposite to that of the N-converter. The inspection of the waveform with α remaining fixed in each half-cycle generates a square wave having a large low-order harmonic content. A near approximation to sine wave can be synthesized by a phase modulation of the firing angles as shown in Fig. 16.18 for a 50 to 10-Hz cycloconverter. The harmonics in the load-voltage waveform are fewer compared to the earlier waveform. The supply current, however, contains a subharmonic at the output frequency for this case as shown.

Operation with RL Load. The cycloconverter is capable of supplying loads of any power factor. Figure 16.19 shows the idealized output voltage and current waveforms for a lagging power factor load where both the converters are operating as rectifier and inverter at the intervals marked. The load current

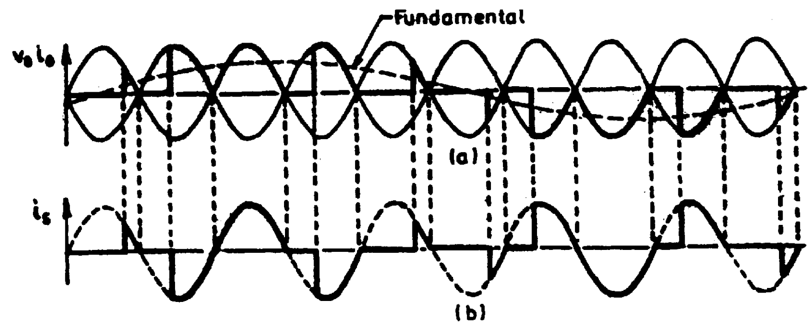

FIGURE 16.18 Waveforms of a single-phase/single-phase cycloconverter (50–10 Hz) with RL load: (a) load voltage and load current; and (b) input supply current.

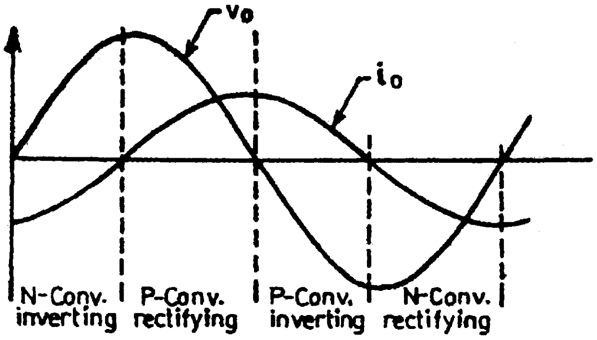

FIGURE 16.19 Load voltage and current waveform for a cycloconverter with *RL* load.

lags the output voltage and the load-current direction determines which converter is conducting. Each converter continues to conduct after its output voltage changes polarity, and during this period the converter acts as an inverter and the power is returned to the ac source. The inverter operation continues until the other converter starts to conduct. By controlling the frequency of oscillation and the *depth of modulation* of the firing angles of the converters (as will be shown later), it is possible to control the frequency and the amplitude of the output voltage.

The load current with *RL* load may be continuous or discontinuous depending on the load phase angle ϕ. At light load inductance or for $\phi \leq \alpha \leq \pi$, there may be discontinuous load current with short zero-voltage periods. The current wave may contain even harmonics as well as subharmonic components. Further, as in the case of a dual converter, though the mean output voltage of the two converters are equal and opposite, the instantaneous values may be unequal and a circulating current can flow within the converters. This circulating current can be limited by having a center-tapped reactor connected between the converters or can be completely eliminated by logical control similar to the dual converter case when the gate pulses to the converter remaining idle are suppressed when the other converter is active. In practice, in addition, a zero current interval of short duration is needed between the operation of the *P*- and *N*-converters to ensure that the supply lines of the two converters are not short-circuited. With circulating current-free operation, the control

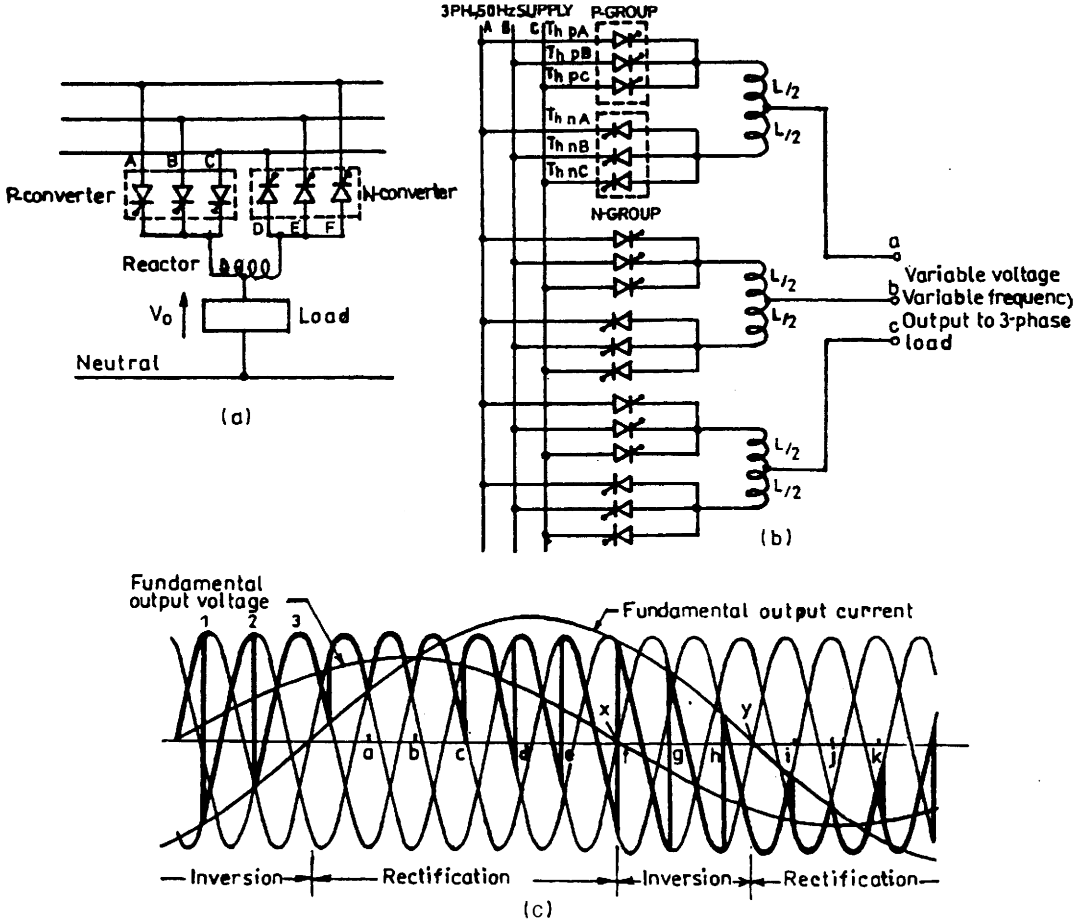
3PH,50HzSUPPLY
P-GROUP
A B C
Th pA
Th pB
Th pC
Th nA
Th nB
Th nC
N-GROUP
L/2
a
b
c
Variable voltage
Variable frequency
Output to 3-phase load
(b)
A B C
P-converter
N-converter
D E F
Reactor
Vo
Load
Neutral
(a)
Fundamental output voltage
1 2 3
Fundamental output current
x
y
a b c d e f g h i j k
Inversion
Rectification
Inversion
Rectification
(c)

FIGURE 16.20 (a) Three-phase half-wave (three-pulse)cycloconverter supplying a single-phase load; (b) three-pulse cycloconverter supplying a three-phase load; (c) output voltage waveform for one phase of a three-pulse cycloconverter operating at 15 Hz from a 50-Hz supply and 0.6 power factor lagging load.

scheme becomes complicated if the load current is discontinuous.

For the circulating current scheme, the converters are kept in virtually continuous conduction over the whole range and the control circuit is simple. To obtain a reasonably good sinusoidal voltage waveform using the line-commutated two-quadrant converters, and to eliminate the possibility of the short circuit of the supply voltages, the output frequency of the cycloconverter is limited to a much lower value of the supply frequency. The output voltage waveform and the output frequency range can be improved further by using converters of higher pulse numbers.

16.4.2 Three-Phase Cycloconverters

16.4.2.1 Three-Phase Three-Pulse Cycloconverter

Figure 16.20a shows a schematic diagram of a three-phase half-wave (three-pulse) cycloconverter feeding a single-phase load, and Fig. 16.20b shows the configuration of a three-phase half-wave (three-pulse) cycloconverter feeding a three-phase load. The basic process of a three-phase cycloconversion is illustrated in Fig. 16.20c at 15 Hz, 0.6 power factor lagging load from a 50-Hz supply. As the firing angle α is cycled from zero at "a" to 180° at "j," half a cycle of output frequency is produced (the gating circuit is to be suitably designed to introduce this oscillation of the firing angle). For this load it can be seen that although the mean output voltage reverses at X, the mean output current (assumed sinusoidal) remains positive until Y. During XY, the SCRs A, B, and C in the P-converter are "inverting." A similar period exists at the end of the negative half-cycle of the output voltage when D, E, and F SCRs in the N-converter are "inverting." Thus the operation of the converter follows in the order of "rectification" and "inversion" in a cyclic manner, with the relative durations being dependent on the load power factor. The output frequency is that of the firing angle oscillation about a quiescent point of 90° (condition when the mean output voltage, given by $V_o = V_{\text{do}} \cos\alpha$, is zero). For obtaining the positive half-cycle of the voltage, firing angle α is varied from 90 to 0° and then to 90°, and for the negative half-cycle, from 90 to 180° and back to 90°. Variation of α within the limits of 180° automatically provides for "natural" line commutation of the SCRs. It is shown that a complete cycle of low-frequency output voltage is fabricated from the segments of the three-phase input voltage by using the phase-controlled converters. The P or N-converter SCRs receive firing pulses that are timed such that each converter delivers the same mean output voltage. This is achieved, as in the case of the single-phase cycloconverter or the dual converter, by maintaining the firing angle constraints of the two groups as $\alpha_P = (180^\circ - \alpha_N)$. However, the instantaneous voltages of two converters are not identical and a large circulating current may result unless limited by an intergroup reactor as shown (*circulating-current cycloconverter*) or completely suppressed by removing the gate pulses from the nonconducting converter by an intergroup blanking logic (*circulating-current-free cycloconverter*).

Circulating-Current Mode Operation. Figure 16.21 shows typical waveforms of a three-pulse cycloconverter operating with circulating current. Each converter conducts continuously with rectifying and inverting modes as shown and the load is supplied with an average voltage of two converters reducing some of the ripple in the process, with the intergroup reactor behaving as a potential divider. The reactor limits the circulating current, with the value of its inductance to the flow of load current being one fourth of its value to the flow of circulating current as the inductance is proportional to the square of the number of turns. The fundamental wave produced by both the converters are the same. The reactor voltage is the instantaneous difference between the converter voltages, and the time integral of this voltage divided by the inductance (assuming negligible circuit resistance) is the circulating current. For a three-pulse cycloconverter, it can be observed that this current reaches its peak when $\alpha_P = 60^\circ$ and $\alpha_N = 120^\circ$.

Output Voltage Equation. A simple expression for the fundamental rms output voltage of the cycloconverter and the required variation of the firing angle α can be derived with the assumptions that: (i) the firing angle α in successive half-cycles is varied slowly resulting in a low-frequency output; (ii) the source impedance and the commutation overlap are neglected; (iii) the SCRs are ideal switches; and (iv) the

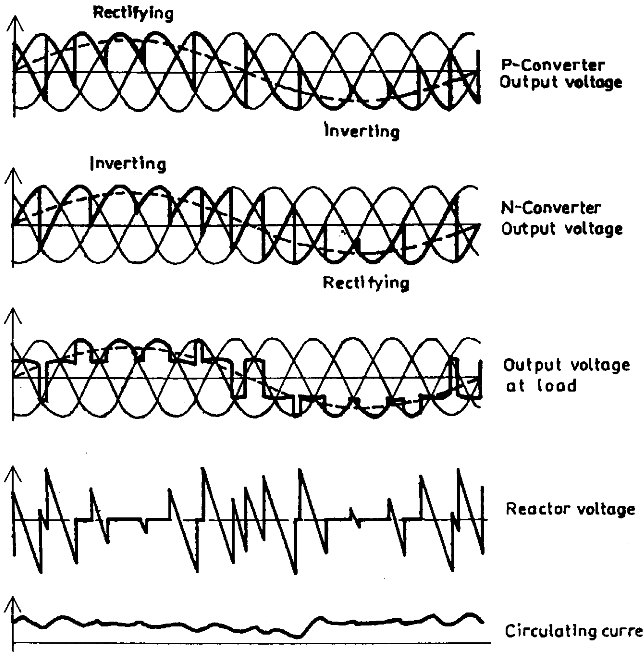

FIGURE 16.21 Waveforms of a three-pulse cycloconverter with circulating current.

current is continuous and ripple-free. The average dc output voltage of a p-pulse dual converter with fixed α is

$$V_{\text{do}} = V_{\text{domax}} \cos\alpha, \text{ where } V_{\text{domax}} = \sqrt{2}V_{\text{ph}}\frac{p}{\pi}\sin\frac{\pi}{p} \qquad (16.25)$$

For the p-pulse dual converter operating as a cycloconverter, the average phase voltage output at any point of the low frequency should vary according to the equation

$$V_{o,\text{av}} = V_{o1,\max}\sin\omega_o t \qquad (16.26)$$

where $V_{o1,\max}$ is the desired maximum value of the fundamental output of the cycloconverter. Comparing Eq. (16.25) with Eq. (16.26), the required variation of α to obtain a sinusoidal output is given by

$$\alpha = \cos^{-1}[(V_{o1,\max}/V_{\text{domax}})\sin\omega_o t] = \cos^{-1}[r\sin\omega_o t] \qquad (16.27)$$

where r is the ratio $(V_{o1,\max}/V_{\text{domax}})$, the *voltage magnitude control ratio.* Equation (16.27) shows α as a nonlinear function with $r(\leq 1)$ as shown in Fig. 16.22.

However, the firing angle α_P of the P-converter cannot be reduced to 0° as this corresponds to $\alpha_N = 180°$ for the N-converter, which, in practice, cannot be achieved because of allowance for commutation overlap and finite turn-off time of the SCRs. Thus the firing angle α_P can be reduced to a certain finite value $\alpha_{\min}$ and the maximum output voltage is reduced by a factor $\cos\alpha_{\min}$.

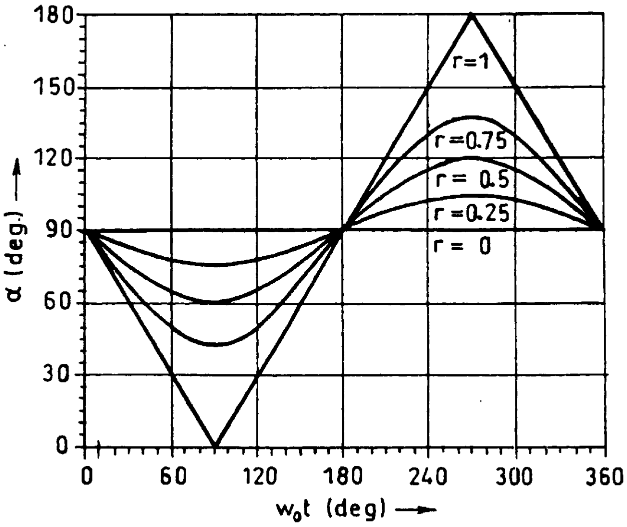

FIGURE 16.22 Variations of the firing angle (α) with r in a cycloconverter.

The fundamental rms voltage per phase of either converter is

$$V_{or} = V_{oN} = V_{oP} = rV_{\text{ph}}\frac{p}{\pi}\sin\frac{\pi}{p} \qquad (16.28)$$

Although the rms value of the low-frequency output voltage of the P-converter and that of the N-converter are equal, the actual waveforms differ and the output voltage at the midpoint of the circulating current limiting reactor (Fig. 16.21), which is the same as the load voltage, is obtained as the mean of the instantaneous output voltages of the two converters.

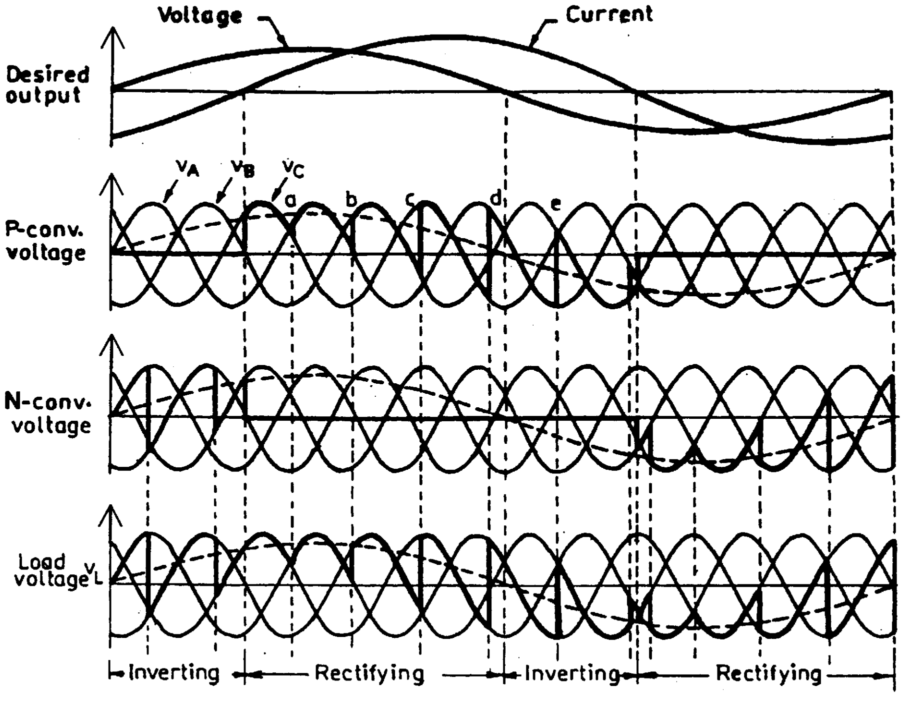

FIGURE 16.23 Waveforms for a three-pulse circulating current-free cycloconverter with RL load.

Circulating-Current-Free Mode Operation. Figure 16.23 shows the typical waveforms for a three-pulse cycloconverter operating in this mode with *RL* load assuming *continuous current* operation. Depending on the load current direction, only one converter operates at a time and the load voltage is the same as the output voltage of the conducting converter. As explained earlier in the case of the single-phase cycloconverter, there is a possibility of a short-circuit of the supply voltages at the crossover points of the converter unless care is taken in the control circuit. The waveforms drawn also neglect the effect of overlap due to the ac supply inductance. A reduction in the output voltage is possible by retarding the firing angle gradually at the points a, b, c, d, e in Fig. 16.23 (this can easily be implemented by reducing the magnitude of the reference voltage in the control circuit). The circulating current is completely suppressed by blocking all the SCRs in the converter that is not delivering the load current. A current sensor is incorporated in each output phase of the cycloconverter that detects the direction of the output current and feeds an appropriate signal to the control circuit to inhibit or blank the gating pulses to the nonconducting converter in the same way as in the case of a dual converter for dc drives. The circulating current-free operation improves the efficiency and the displacement factor of the cycloconverter and also increases the maximum usable output frequency. The load voltage transfers smoothly from one converter to the other.

Three-Phase Six-Pulse and Twelve-Pulse Cycloconverter. A six-pulse cycloconverter circuit configuration is shown in Fig. 16.24. Typical load-voltage waveforms for 6-pulse (with 36 SCRs) and 12-pulse (with 72 SCRs) cycloconverters are shown in Fig. 16.25. The 12-pulse converter is obtained by connecting two 6-pulse configurations in series and appropriate transformer connections for the required phase-shift. It may be seen that the higher pulse numbers will generate waveforms closer to the desired sinusoidal form and thus permit higher frequency output. The phase loads may be isolated from each other as shown or interconnected with suitable secondary winding connections.

16.4.3 Cycloconverter Control Scheme

Various possible control schemes (analog as well as digital) for deriving trigger signals for controlling the basic cycloconverter have been developed over the years.

Out of the several possible signal combinations, it has been shown [12] that a sinusoidal reference signal ($e_r = E_r \sin \omega_o t$) at desired output frequency f_o and a cosine modulating signal ($e_m = E_m \cos \omega_i t$) at input frequency f_i is the best combination possible for comparison to derive the trigger signals for the SCRs (Fig. 16.26 [15]), which produces the output waveform with the lowest total harmonic distortion. The modulating voltages can be obtained as the phase-shifted voltages (B-phase for A-phase SCRs, C-phase voltage for B-phase SCRs, and so on) as explained in Fig. 16.27, where at the intersection point "a"

$$E_m \sin(\omega_i t - 120^\circ) = -E_r \sin(\omega_o t - \phi)$$

or

$$\cos(\omega_i t - 30^\circ) = (E_r/E_m)\sin(\omega_o t - \phi)$$

From Fig. 16.27, the firing delay for A-phase SCR $\alpha = (\omega_i t - 30^\circ)$. Thus,

$$\cos \alpha = (E_r/E_m)\sin(\omega_o t - \phi).$$

The cycloconverter output voltage for continuous current operation

$$V_o = V_{do} \cos \alpha = V_{do}(E_r/E_m)\sin(\omega_o t - \phi) \tag{16.29}$$

which shows that the amplitude, frequency and phase of the output voltage can be controlled by controlling correspondence parameters of the reference voltage, thus making the transfer characteristic of the cycloconverter linear. The derivation of the two complimentary voltage waveforms for the *P*-group or *N*-group converter "blanks" in this way is illustrated in Fig. 16.28. The final cycloconverter output waveshape is composed of alternate half-cycle segments of the complementary *P*-converter and *N*-converter output voltage waveforms that coincide with the positive and negative current half-cycles, respectively.

Control Circuit Block Diagram. Figure 16.29 [16] shows a simplified block diagram of the control circuit for a circulating

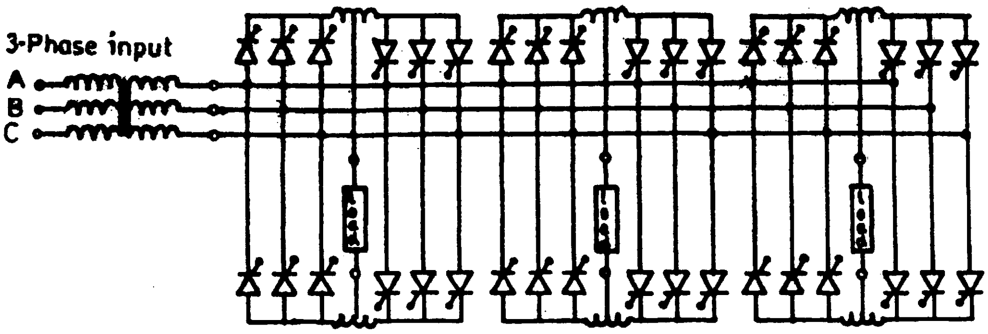

FIGURE 16.24 Three-phase 6-pulse cycloconverter with isolated loads.

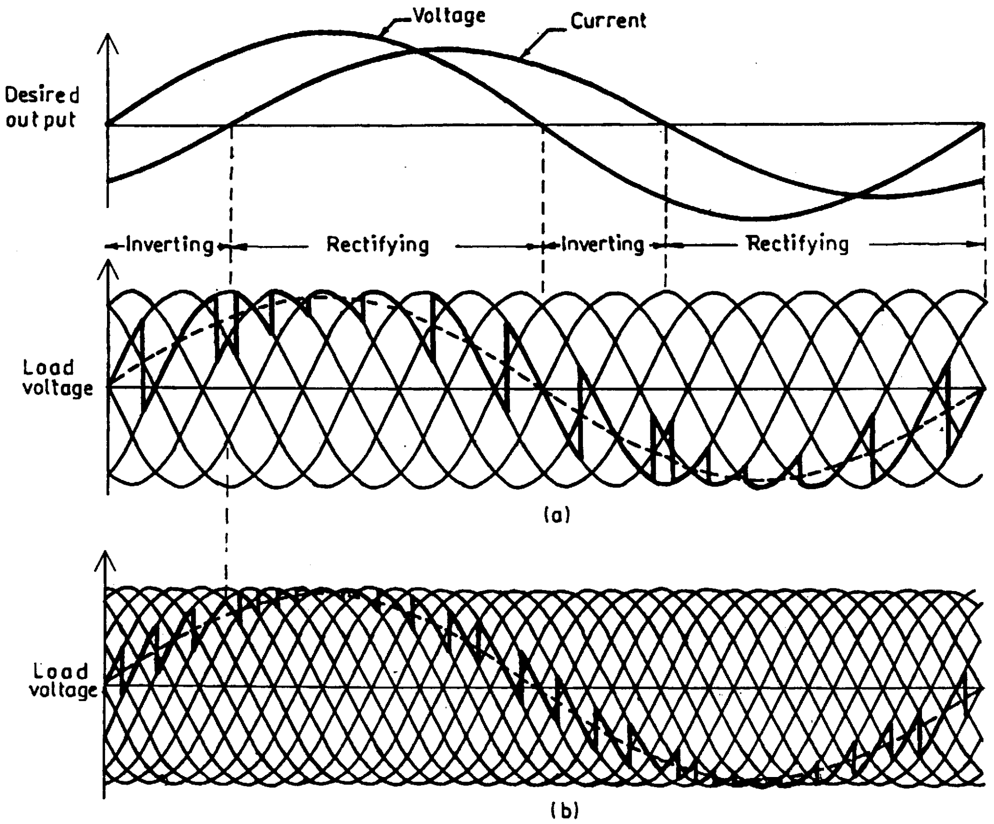

FIGURE 16.25 Cycloconverter load-voltage waveforms with lagging power factor load: (a) 6-pulse connection; and (b) 12-pulse connection.

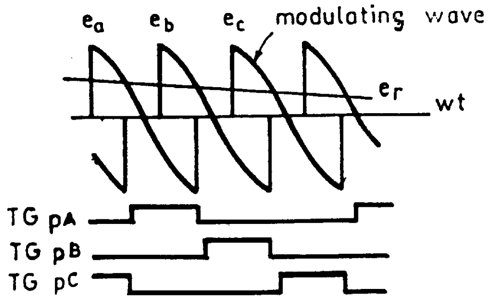
ea
eb
ec
modulating wave
er
wt
TG pA
TG pB
TG pC

FIGURE 16.26 Deriving firing signals for one converter group of a 3-pulse cycloconverter.

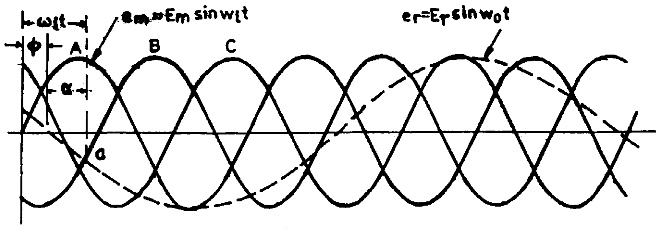

FIGURE 16.27 Derivation of the cosine modulating voltages.

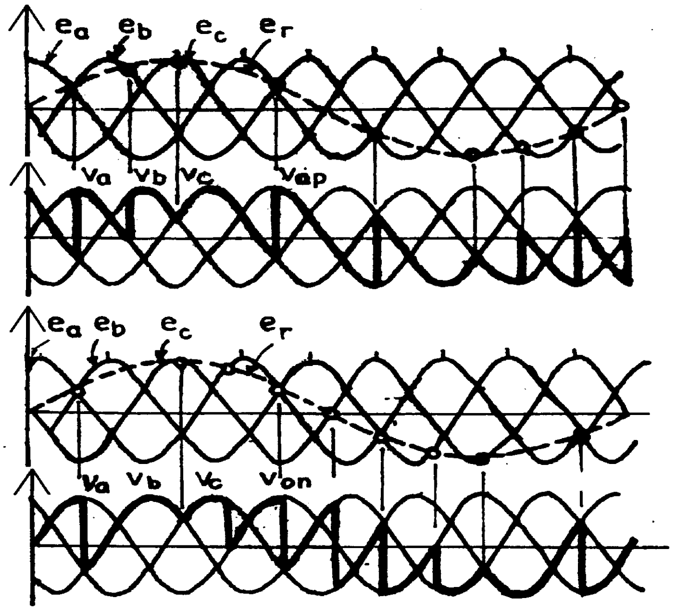

FIGURE 16.28 Derivation of P-converter and N-converter output voltages.

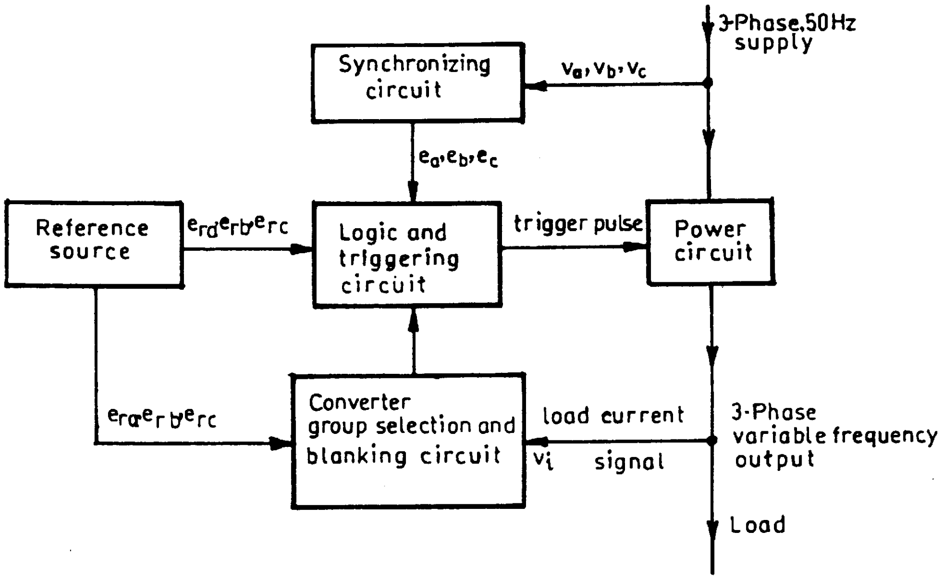
3-Phase,50Hz supply
Synchronizing circuit
va, vb, vc
ea, eb, ec
Reference source
era, erb, erc
Logic and triggering circuit
trigger pulse
Power circuit
era, erb, erc
Converter group selection and blanking circuit
load current signal
vi
3-Phase variable frequency output
Load

FIGURE 16.29 Block diagram for a circulating current-free cycloconverter control circuit.

current-free cycloconverter. The same circuit is also applicable to a circulating current cycloconverter with the omission of the *Converter Group Selection and Blanking Circuit.*

The *Synchronizing circuit* produces the modulating voltages ($e_a = -Kv_b$, $e_b = -Kv_c$, $e_c = -Kv_a$), synchronized with the mains through step-down transformers and proper filter circuits.

The *Reference Source* produces a variable-voltage variable-frequency reference signal (e_{ra}, e_{rb}, e_{rc}) (three-phase for a three-phase cycloconverter) for comparison with the modulation voltages. Various ways (analog or digital) have been developed to implement this reference source as in the case of the PWM inverter. In one of the early analog schemes (Fig. 16.30) [16] for a three-pulse cycloconverter, a variable-frequency unijunction transistor (UJT) relaxation oscillator of frequency $6f_d$ triggers a ring counter to produce a three-phase square-wave output of frequency f_d, which is used to modulate a single-phase fixed frequency (f_c) variable amplitude sinusoidal voltage in a three-phase full-wave transistor chopper. The three-phase output contains $(f_c - f_d)$, $(f_c + f_d)$, $(3f_d + f_c)$, and so forth, frequency components from where the "wanted" frequency component $(f_c - f_d)$ is filtered out for each phase using a lowpass filter. For example, with $f_c = 500$ Hz and frequency of the relaxation oscillator varying between 2820 to 3180 Hz, a three-phase 0–30 Hz reference output can be obtained with the facility for phase-sequence reversal.

The *Logic and Trigger Circuit* for each phase involves comparators for comparison of the reference and modulating voltages and inverters acting as buffer stages. The outputs of the comparators are used to clock the flip-flops or latches whose outputs in turn feed the SCR gates through AND gates and pulse amplifying and isolation circuit. The second input to the AND gates is from the *Converter Group Selection and Blanking Circuit.*

In the *Converter Group Selection and Blanking Circuit*, the zero crossing of the current at the end of each half-cycle is detected and is used to regulate the control signals either to *P*-group or *N*-group converters depending on whether the current goes to zero from negative to positive or positive to

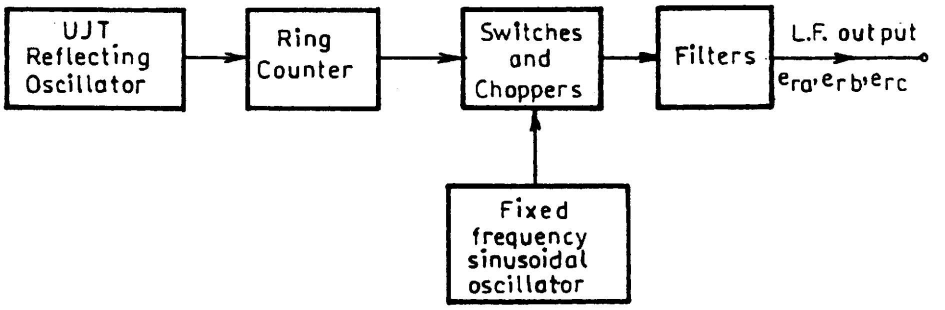
UJT Reflecting Oscillator
Ring Counter
Switches and Choppers
Filters
L.F. output
era, erb, erc
Fixed frequency sinusoidal oscillator

FIGURE 16.30 Block Diagram of a variable-voltage variable-frequency three-phase reference source.

negative, respectively. However, in practice, the current that is discontinuous passes through multiple zero crossings while changing direction, which may lead to undesirable switching of the converters. Therefore in addition to the current signal, the reference voltage signal is also used for the group selection and a *threshold* band is introduced in the current signal detection to avoid inadvertent switching of the converters. Further, a delay circuit provides a blanking period of appropriate duration between the converter group switching to avoid line-to-line short-circuits [16]. In some schemes, the delays are not introduced when a small circulating current is allowed during crossover instants limited by reactors of limited size and this scheme operates in the so-called "dual mode" circulating current as well as circulating current-free mode for minor and major portions of the output cycle, respectively. A different approach to the converter group selection, based on the closed-loop control of the output voltage where a bias voltage is introduced between the voltage transfer characteristics of the converters to reduce circulating current, is discussed in Reference [12].

Improved Control Schemes. With the development of microprocessors and PC-based systems, digital software control has taken over many tasks in modern cycloconverters, particularly in replacing the low-level reference waveform generation and analog signal comparison units. The reference waveforms can easily be generated in the computer, stored in the EPROMs and accessed under the control of a stored program and microprocessor clock oscillator. The analog signal voltages can be converted to digital signals by using analog-to-digital converters (ADCs). The waveform comparison can then be made with the comparison features of the microprocessor system. The addition of time delays and intergroup blanking can also be achieved with digital techniques and computer software. A modification of the cosine firing control, using communication principles such as *regular sampling* in preference to the *natural sampling* (discussed so far) of the reference waveform yielding a stepped sine wave before comparison with the cosine wave [17], has been shown to reduce the presence of *subharmonics* (to be discussed later) in the circulating current cycloconverter, and to facilitate microprocessor-based implementation, as in the case of the PWM inverter.

16.4.4 Cycloconverter Harmonics and Input Current Waveform

The exact waveshape of the output voltage of the cycloconverter depends on: (i) the pulse number of the converter; (ii) the ratio of the output to input frequency (f_o/f_i); (iii) the relative level of the output voltage; (iv) load displacement angle; (v) circulating current or circulating current-free operation; and (vi) the method of control of the firing instants. The harmonic spectrum of a cycloconverter output voltage is different and more complex than that of a phase-controlled converter. It has been revealed [12] that because of the continuous "to-and-fro" phase modulation of the converter firing angles, the harmonic distortion components (known as *necessary distortion terms*) have frequencies that are sums and differences between multiples of output and input supply frequencies.

Circulating Current-Free Operation. A derived general expression for the output voltage of a cycloconverter with circulating current-free operation [12] shows the following spectrum of harmonic frequencies for the 3-pulse, 6-pulse, and 12-pulse cycloconverters employing the cosine modulation technique:

$$\begin{aligned}
\text{3-pulse: } f_{\text{oH}} &= |3(2k-1)f_i \pm 2nf_o| \text{ and } |6kf_i \pm (2n+1)f_o| \\
\text{6-pulse: } f_{\text{oH}} &= |6kf_i \pm (2n+1)f_o| \\
\text{12-pulse: } f_{\text{oH}} &= |6kf_i \pm (2n+1)f_o|
\end{aligned} \tag{16.30}$$

where k is any integer from unity to infinity and n is any integer from zero to infinity. It may be observed that for certain ratios of f_o/f_i, the order of harmonics may be less or equal to the desired output frequency. All such harmonics are known as *subharmonics* as they are not higher multiples of the input frequency. These subharmonics may have considerable amplitudes (e.g., with a 50-Hz input frequency and 35-Hz output frequency, a subharmonic of frequency $3 \times 50 - 4 \times 35 = 10\,\text{Hz}$ is produced whose magnitude is 12.5 of the 35-Hz component [17]) and are difficult to filter and thus are objectionable. Their spectrum increases with the increase of the ratio f_o/f_i and thus limits its value at which a tolerable waveform can be generated.

Circulating-Current Operation. For circulating-current operation with continuous current, the harmonic spectrum in the output voltage is the same as that of the circulating current-free operation except that each harmonic family now terminates at a definite term, rather than having an infinite number of components. They are

$$\begin{aligned}
\text{3-pulse: } f_{\text{oH}} &= |3(2k-1)f_i \pm 2nf_o|,\ n \leq 3(2k-1)+1 \\
&\qquad \text{and } |6kf_i \pm (2n+1)f_o|,\ (2n+1) \leq (6k+1) \\
\text{6-pulse: } f_{\text{oH}} &= |6kf_i \pm (2n+1)f_o|,\ (2n+1) \leq (6k+1) \\
\text{12-pulse: } f_{\text{oH}} &= |6kf_i \pm (2n+1)f_o|,\ (2n+1) \leq (12k+1)
\end{aligned} \tag{16.31}$$

The amplitude of each harmonic component is a function of the output voltage ratio for the circulating current cycloconverter and the output voltage ratio as well as the load displacement angle for the circulating current-free mode.

From the point of view of maximum useful attainable output-to-input frequency ratio (f_i/f_o) with the minimum amplitude of objectionable harmonic components, a guideline is available in Reference [12] for it as 0.33, 0.5, and 0.75 for the 3-, 6-, and 12-pulse cycloconverter, respectively. However, with modification of the cosine wave modulation timings such as *regular sampling* [17] in the case of circulating current cycloconverters only and using a *subharmonic detection and feedback control concept* [18] for both circulating- and circulating-current-free cases, the subharmonics can be suppressed and useful frequency range for the naturally commutated cycloconverters can be increased.

Other Harmonic Distortion Terms. Besides the harmonics as mentioned, other harmonic distortion terms consisting of frequencies of integral multiples of desired output frequency appear if the transfer characteristic between the output and reference voltages is not linear. These are called *unnecessary distortion terms*, which are absent when the output frequencies are much less than the input frequency. Further, some *practical distortion terms* may appear due to some practical nonlinearities and imperfections in the control circuits of the cycloconverter, particularly at relatively lower levels of output voltage.

Input Current Waveform. Although the load current, particularly for higher pulse cycloconverters, can be assumed to be sinusoidal, the input current is more complex as it is made of pulses. Assuming the cycloconverter to be an ideal switching circuit without losses, it can be shown from the instantaneous power balance equation that in a cycloconverter supplying a single-phase load the input current has harmonic components of frequencies ($f_1 \pm 2f_o$), called *characteristic harmonic frequencies* that are independent of pulse number and they result in an oscillatory power transmittal to the ac supply system. In the case of a cycloconverter feeding a balanced three-phase load, the net instantaneous power is the sum of the three oscillating instantaneous powers when the resultant power is constant and the net harmonic component is greatly reduced compared to that of the single-phase load case. In general, the total rms value of the input current waveform consists of three components in-phase, quadrature, and the harmonic. The in-phase component depends on the active power output while the quadrature component depends on the net average of the oscillatory firing angle and is always lagging

16.4.5 Cycloconverter Input Displacement/Power Factor

The input supply performance of a cycloconverter such as displacement factor or fundamental power factor, input power factor and the input current distortion factor are defined similarly to those of the phase-controlled converter. The harmonic factor for the case of a cycloconverter is relatively complex as the harmonic frequencies are not simple multiples of the input frequency but are sums and differences between multiples of output and input frequencies.

Irrespective of the nature of the load, leading, lagging or unity power factor, the cycloconverter requires reactive power decided by the average firing angle. At low output voltage, the average phase displacement between the input current and the voltage is large and the cycloconverter has a low input displacement and power factor. Besides the load displacement factor and output voltage ratio, another component of the reactive current arises due to the modulation of the firing angle in the fabrication process of the output voltage [12]. In a phase-controlled converter supplying dc load, the maximum displacement factor is unity for maximum dc output voltage. However, in the case of the cycloconverter, the maximum input displacement factor is 0.843 with unity power factor load [12, 13]. The displacement factor decreases with reduction in the output voltage ratio. The distortion factor of the input current is given by (I_1/I), which is always less than unity and the resultant power factor (=distortion factor × displaceacement factor) is thus much lower (around 0.76 maximum) than the displacement factor and this is a serious disadvantage of the naturally commutated cycloconverter (NCC).

16.4.6 Effect of Source Impedance

The source inductance introduces commutation overlap and affects the external characteristics of a cycloconverter similar to the case of a phase-controlled converter with dc output. It introduces delay in the transfer of current from one SCR to another, and results in a voltage loss at the output and a modified harmonic distortion. At the input, the source impedance causes "rounding off" of the steep edges of the input current waveforms resulting in reduction in the amplitudes of higher-order harmonic terms as well as a decrease in the input displacement factor.

16.4.7 Simulation Analysis of Cycloconverter Performance

The nonlinearity and discrete time nature of practical cycloconverter systems, particularly for discontinuous current conditions, make an exact analysis quite complex and a valuable design and analytical tool is a digital computer simulation of the system. Two general methods of computer simulation of the cycloconverter waveforms for *RL* and induction motor loads with circulating current and circulating current-free operation have been suggested in Reference [19] where one of the methods, which is very fast and convenient, is the *crossover points method*. This method gives the crossover points (intersections of the modulating and reference waveforms) and the conducting phase numbers for both *P*- and *N*-converters from which the output waveforms for a particular load can be digitally computed at any interval of time for a practical cycloconverter.

16.4.8 orced-Commutated Cycloconverter CC

The naturally commutated cycloconverter (NCC) with SCRs as devices discussed so far, is sometimes referred to as a *restricted frequency changer* as, in view of the allowance on the output voltage quality ratings, the maximum output voltage frequency is restricted ($f_o \ll f_i$) as mentioned earlier. With devices replaced by fully controlled switches such as forced-commutated SCRs, power transistors, IGBTs, GTOs, and so forth, a force-commutated cycloconverter (FCC) can be built where the desired output frequency is given by $f_o = |f_s - f_i|$, when f_s = switching frequency, which may be larger or smaller than the f_i. In the case when $f_o \geq f_i$, the converter is called the *Unrestricted Frequency Changer (UFC)* and when $f_o \leq f_i$, it is called a *Slow Switching Frequency Changer (SSFC)*. The early FCC structures have been treated comprehensively in Reference [13]. It has been shown that in contrast to the NCC, when the input displacement factor (IDF) is always lagging, in UFC it is leading when the load displacement factor is lagging and vice versa, and in SSFC, it is identical to that of the load. Further, with proper control in an FCC, the input displacement factor can be made unity (UDFFC) with concurrent composite voltage waveform or controllable (CDFFC) where P-converter and N-converter voltage segments can be shifted relative to the output current wave for control of IDF continuously from lagging via unity to leading.

In addition to allowing bilateral power flow, UFCs offer an unlimited output frequency range, good input voltage utilization, do not generate input current and output voltage subharmonics, and require only nine bidirectional switches (Fig. 16.31) for a three-phase to three-phase conversion. The main disadvantage of the structures treated in Reference [13] is that they generate large unwanted low-order input current and output voltage harmonics that are difficult to filter out, particularly for low-output voltage conditions. This problem has largely been solved with the introduction of an imaginative PWM voltage-control scheme in Reference [20], which is the basis of newly designated converter called the *Matrix Converter (also known as PWM Cycloconverter)*, which operates as a *Generalized Solid-State Transformer* with significant improvement in voltage and input current waveforms resulting in sine-wave input and sine-wave output as discussed in the next section.

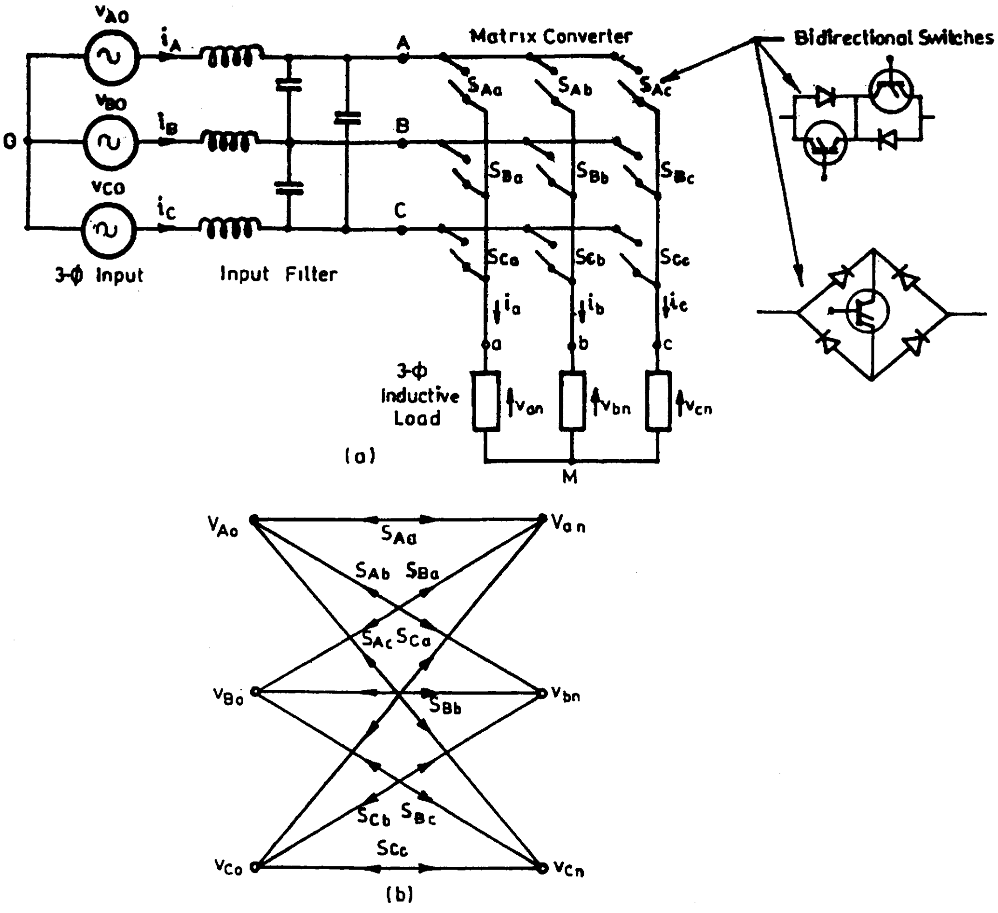

FIGURE 16.31 (a) The 3ϕ-3ϕ matrix converter (force-commutated cycloconverter) circuit with input filter; (b) switching matrix symbol for converter in (a).

16.5 Matrix Converter

The matrix converter (MC) is a development of the force-commutated cycloconverter (FCC) based on bidirectional fully controlled switches, incorporating PWM voltage control, as mentioned earlier. With the initial progress reported in References [20]–[22], it has received considerable attention as it provides a good alternative to the double-sided PWM voltage-source rectifier-inverters having the advantages of being a single-stage converter with only nine switches for three-phase to three-phase conversion and inherent bidirectional power flow, sinusoidal input/output waveforms with moderate switching frequency, the possibility of compact design due to the absence of dc link reactive components and controllable input power factor independent of the output load current. The main disadvantages of the matrix converters developed so far are the inherent restriction of the *voltage transfer ratio* (0.866), a more complex control and protection strategy, and above all the nonavailability of a fully controlled bidirectional high-frequency switch integrated in a silicon chip (Triac, though bilateral, cannot be fully controlled).

The power circuit diagram of the most practical three-phase to three-phase $(3\phi\text{-}3\phi)$ matrix converter is shown in Fig. 16.31a, which uses nine bidirectional switches so arranged that any of three input phases can be connected to any output phase as shown in the switching matrix symbol in Fig. 16.31b. Thus, the voltage at any input terminal may be made to appear at any output terminal or terminals while the current in any phase of the load may be drawn from any phase or phases of the input supply. For the switches, the inverse-parallel combination of reverse-blocking self-controlled devices such as Power MOSFETs or IGBTs or transistor-embedded diode bridge as shown have been used so far. The circuit is called a matrix converter as it provides exactly one switch for each of the possible connections between the input and the output. The switches should be controlled in such a way that, at any time, one and only one of the three switches connected to an output phase must be closed to prevent "short-circuiting" of the supply lines or interrupting the load-current flow in an inductive load. With these constraints, it can be visualized that from the possible 512 $(= 2^9)$ states of the converter, only 27 switch combinations are allowed as given in Table 16.1, which includes the resulting output line voltages and input phase currents. These combinations are divided into three groups. Group I consists of six combinations when each output phase is connected to a different input phase. In Group II, there are three subgroups, each having six combinations with two output phases short-circuited (connected to the same input phase). Group III includes three combinations with all output phases short-circuited.

With a given set of input three-phase voltages, any desired set of three-phase output voltages can be synthesized by

TABLE 16.1 Three-phase/three-phase matrix converter switching combinations

Group	a	b	c	v_{ab}	v_{bc}	v_{ca}	i_A	i_B	i_C	S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}
I	A	B	C	v_{AB}	v_{BC}	v_{CA}	i_a	i_b	i_c	1	0	0	0	1	0	0	0	1
	A	C	B	$-v_{CA}$	$-v_{BC}$	$-v_{AB}$	i_a	i_c	i_b	1	0	0	0	0	1	0	1	0
	B	A	C	$-v_{AB}$	$-v_{CA}$	$-v_{BC}$	i_b	i_a	i_c	0	1	0	1	0	0	0	0	1
	B	C	A	v_{BC}	v_{CA}	v_{AB}	i_c	i_a	i_b	0	1	0	0	0	1	0	1	0
	C	A	B	v_{CA}	v_{AB}	v_{BC}	i_b	i_c	i_a	0	0	1	1	0	0	0	1	0
	C	B	A	$-v_{BC}$	$-v_{AB}$	$-v_{CA}$	i_c	i_b	i_a	0	0	1	0	1	0	1	0	0
II-A	A	C	C	$-v_{CA}$	0	v_{CA}	i_a	0	$-i_a$	1	0	0	0	0	1	0	0	1
	B	C	C	v_{BC}	0	$-v_{BC}$	0	i_a	$-i_a$	0	1	0	0	0	1	0	0	1
	B	A	A	$-v_{AB}$	0	$-v_{AB}$	$-i_a$	i_a	0	0	1	0	1	0	0	1	0	0
	C	A	A	v_{CA}	0	$-v_{CA}$	$-i_a$	0	i_a	0	0	1	1	0	0	1	0	0
	C	B	B	$-v_{BC}$	0	v_{BC}	0	$-i_a$	i_a	0	0	1	0	1	0	0	1	0
	A	B	B	v_{AB}	0	$-v_{AB}$	i_a	$-i_a$	0	1	0	0	0	1	0	0	1	0
II-B	C	A	C	$-v_{CA}$	$-v_{CA}$	0	i_b	0	$-i_b$	0	0	1	1	0	0	0	0	1
	C	B	C	$-v_{BC}$	v_{BC}	0	0	i_b	$-i_b$	0	0	1	0	1	0	0	0	1
	A	B	A	v_{AB}	$-v_{AB}$	0	$-i_b$	i_b	0	1	0	0	0	1	0	1	0	0
	A	C	A	$-v_{CA}$	v_{CA}	0	$-i_b$	0	i_b	1	0	0	0	0	1	1	0	0
	B	C	B	v_{BC}	$-v_{BC}$	0	0	$-i_b$	i_b	0	1	0	0	0	1	0	1	0
	B	A	B	$-v_{AB}$	V_{AB}	0	i_b	$-i_b$	0	0	0	1	0	1	0	0	1	0
II-C	C	C	A	0	v_{CA}	$-v_{CA}$	i_c	0	$-i_c$	0	0	1	0	0	1	1	0	0
	C	C	B	0	$-v_{BC}$	v_{BC}	0	i_c	$-i_c$	0	0	1	0	0	1	0	1	0
	A	A	B	0	v_{AB}	$-v_{AB}$	$-i_c$	i_c	0	1	0	0	1	0	0	0	1	0
	A	A	C	0	$-v_{CA}$	v_{CA}	$-i_c$	0	i_c	1	0	0	1	0	0	0	0	1
	B	B	C	0	v_{BC}	$-v_{BC}$	0	$-i_c$	i_c	0	1	0	0	1	0	0	0	1
	B	B	A	0	$-v_{AB}$	v_{AB}	i_c	$-i_c$	0	0	1	0	0	1	0	1	0	0
III	A	A	A	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0
	B	B	B	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
	C	C	C	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

adopting a suitable switching strategy. However, it has been shown [22, 31] that regardless of the switching strategy there are physical limits on the achievable output voltage with these converters as the maximum peak-to-peak output voltage cannot be greater than the minimum voltage difference between two phases of the input. To have complete control of the synthesized output voltage, the envelope of the three-phase reference or target voltages must be fully contained within the continuous envelope of the three-phase input voltages. Initial strategy with the output frequency voltages as references reported the limit as 0.5 of the input as shown in Fig.16 32a. This can be increased to 0.866 by adding a third harmonic voltage of input frequency $(V_i/4) \cdot \cos 3\omega_i t$ to all target output voltages and subtracting from them a third harmonic voltage of output frequency $(V_o/6) \cdot \cos 3\omega_o t$ as shown in Fig. 16.32b [22, 31]. However, this process involves a considerable amount of additional computations in synthesizing the output voltages. The other alternative is to use the space vector modulation (SVM) strategy as used in PWM inverters without adding third harmonic components but it also yields the maximum voltage transfer ratio as 0.866.

An ac input LC filter is used to eliminate the switching ripples generated in the converter and the load is assumed to be sufficiently inductive to maintain continuity of the output currents.

16.5.1 Operation and Control Methods of the Matrix Converter

The converter in Fig. 16.31 connects any input phase (A, B, and C) to any output phase (a, b, and c) at any instant. When connected, the voltages v_{an}, v_{bn}, v_{cn} at the output terminals are related to the input voltages V_{Ao}, V_{Bo}, V_{Co}, as

$$\begin{bmatrix} v_{\mathrm{an}} \\ v_{\mathrm{bn}} \\ v_{\mathrm{cn}} \end{bmatrix} = \begin{bmatrix} S_{\mathrm{Aa}} & S_{\mathrm{Ba}} & S_{\mathrm{Ca}} \\ S_{\mathrm{Ab}} & S_{\mathrm{Bb}} & S_{\mathrm{cb}} \\ S_{\mathrm{Ac}} & S_{\mathrm{Bc}} & S_{\mathrm{Cc}} \end{bmatrix} \begin{bmatrix} v_{\mathrm{Ao}} \\ v_{\mathrm{Bo}} \\ v_{\mathrm{Co}} \end{bmatrix} \tag{16.32}$$

where S_{Aa} through S_{Cc} are the switching variables of the corresponding switches shown in Fig. 16.31. For a balanced linear star-connected load at the output terminals, the input phase currents are related to the output phase currents by

$$\begin{bmatrix} i_{\mathrm{A}} \\ i_{\mathrm{B}} \\ i_{\mathrm{C}} \end{bmatrix} = \begin{bmatrix} S_{\mathrm{Aa}} & S_{\mathrm{Ab}} & S_{\mathrm{Ac}} \\ S_{\mathrm{Ba}} & S_{\mathrm{Bb}} & S_{\mathrm{Bc}} \\ S_{\mathrm{Ca}} & S_{\mathrm{Cb}} & S_{\mathrm{Cc}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{16.33}$$

Note that the matrix of the switching variables in Eq. (16.33) is a transpose of the respective matrix in Eq. (l6.32). The matrix converter should be controlled using a specific and appropriately timed sequence of the values of the switching variables, which will result in balanced output voltages having the desired frequency and amplitude, while the input currents are balanced and in phase (for unity IDF) or at an arbitrary angle (for controllable IDF) with respect to the input voltages. As the matrix converter, in theory, can operate at any frequency, at the output or input, including zero, it can be employed as a three-phase ac/dc converter, dc/three-phase ac converter, or even a buck/boost dc chopper and thus as a *universal power converter.*

The control methods adopted so far for the matrix converter are quite complex and are subjects of continuing research [22–31]. Of the methods proposed for independent control of the output voltages and input currents, two methods are of wide use and will be reviewed briefly here: (i) the *Venturini* method based on a mathematical approach of transfer function analysis; and (ii) the *Space Vector Modulation* (SVM) approach (as has been standardized now in the case of PWM control of the dc link inverter).

Venturini method. Given a set of three-phase input voltages with constant amplitude V_i and frequency $f_i = \omega_i/2\pi$, this method calculates a switching function involving the duty cycles of each of the nine bidirectional switches and generates the three-phase output voltages by sequential piecewise-sampling of the input waveforms. These output voltages follow a predetermined set of reference or target voltage waveforms and with a three-phase load connected, a set of input currents I_i, and angular frequency ω_i should be in phase for unity IDF or at a specific angle for controlled IDF.

A transfer function approach is employed in Reference [29] to achieve the previously mentioned features by relating the

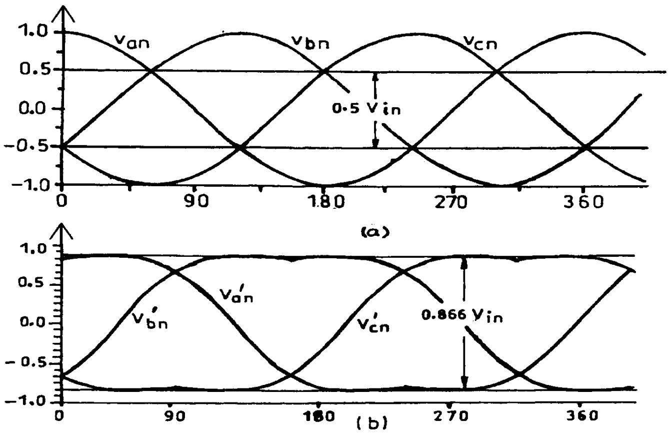

FIGURE 16.32 Output voltage limits for three-phase ac-ac matrix converter: (a) basic converter input voltages; (b) maximum attainable with inclusion of third harmonic voltages of input and output frequency to the target voltages.

input and output voltages and the output and input currents as

$$\begin{bmatrix} V_{o1}(t) \\ V_{o2}(t) \\ V_{o3}(t) \end{bmatrix} = \begin{bmatrix} m_{11}(t) & m_{12}(t) & m_{13}(t) \\ m_{21}(t) & m_{22}(t) & m_{23}(t) \\ m_{31}(t) & m_{32}(t) & m_{33}(t) \end{bmatrix} \begin{bmatrix} V_{i1}(t) \\ V_{i2}(t) \\ V_{i3}(t) \end{bmatrix} \quad (16.34)$$

$$\begin{bmatrix} I_{i1}(t) \\ I_{i2}(t) \\ I_{i3}(t) \end{bmatrix} = \begin{bmatrix} m_{11}(t) & m_{21}(t) & m_{31}(t) \\ m_{12}(t) & m_{22}(t) & m_{32}(t) \\ m_{13}(t) & m_{23}(t) & m_{33}(t) \end{bmatrix} \begin{bmatrix} I_{o1}(t) \\ I_{o2}(t) \\ I_{o3}(t) \end{bmatrix} \quad (16.35)$$

where the elements of the modulation matrix $m_{ij}(t)$ $(i, j = 1, 2, 3)$ represent the duty cycles of a switch connecting output phase i to input phase j within a sample switching interval. The elements of $m_{ij}(t)$ are limited by the constraints

$$0 \leq m_{ij}(t) \leq 1 \qquad \text{and} \qquad \sum_{j=1}^{3} m_{ij}(t) = 1 \quad (i = 1, 2, 3)$$

The set of three-phase target or reference voltages to achieve the maximum voltage transfer ratio for unity IDF is

$$\begin{bmatrix} V_{o1}(t) \\ V_{o2}(t) \\ V_{o3}(t) \end{bmatrix} = V_{om} \begin{bmatrix} \cos \omega_o t \\ \cos(\omega_o t - 120^\circ) \\ \cos(\omega_o t - 240^\circ \end{bmatrix} + \frac{V_{im}}{4} \begin{bmatrix} \cos(3\omega_i t) \\ \cos(3\omega_i t) \\ \cos(3\omega_i t) \end{bmatrix} - \frac{V_{\text{om}}}{6} \begin{bmatrix} \cos(3\omega_o t) \\ \cos(3\omega_o t) \\ \cos(3\omega_o t) \end{bmatrix} \quad (16.36)$$

where V_{om} and V_{im} are the magnitudes of output and input fundamental voltages of angular frequencies ω_0 and ω_i, respectively. With $V_{om} \leq 0.866\ V_{im}$, a general formula for the duty cycles $m_{ij}(t)$ is derived in Reference [29]. For unity IDF condition, a simplified formula is

$$\begin{aligned} m_{ij} = \frac{1}{3} \Bigg\{ & 1 + 2q \cos(\omega_i t - 2(j-1)60^\circ) \Bigg[\cos(\omega_o t - 2(i-1)60^\circ) \\ & + \frac{1}{2\sqrt{3}} \cos(3\omega_i t) - \frac{1}{6} \cos(3\omega_o t) \Bigg] \\ & - \frac{2q}{3\sqrt{3}} [\cos(4\omega_i t - 2(j-1)60^\circ) \\ & - \cos(2\omega_i t - 2(1-j)60^\circ] \Bigg\} \end{aligned} \quad (16.37)$$

where $i, j = 1, 2, 3$ and $q = V_{om}/V_{im}$.

The method developed as in the preceding is based on a *Direct Transfer Function (DTF)* approach using a single modulation matrix for the matrix converter, employing the switching combinations of all three groups in Table 16.1. Another approach called *Indirect Transfer Function (ITF)* approach [23, 24] considers the matrix converter as a combination of PWM voltage source rectifier-PWM voltage source inverter (VSR-VSI) and employs the already well-established VSR and VSI PWM techniques for MC control utilizing the switching combinations of Group II and Group III only of Table 16.1. The drawback of this approach is that the IDF is limited to unity and the method also generates higher and fractional harmonic components in the input and the output waveforms.

SVM Method. The space vector modulation is now a well-documented inverter PWM control technique that yields high voltage gain and less harmonic distortion compared to the other modulation techniques as discussed in Chapter 14, Section 14.6. Here, the three-phase input currents and output voltages are represented as space vectors and SVM is applied simultaneously to the output voltage and input current space vectors. Applications of the SVM algorithm to control of matrix converters have appeared in the literature [27–30] and shown to have inherent capability to achieve full control of the instantaneous output voltage vector and the instantaneous current displacement angle even under supply voltage disturbances. The algorithm is based on the concept that the MC output line voltages for each switching combination can be represented as a voltage space vector defined by

$$V_o = \frac{2}{3} [v_{\text{ab}} + v_{\text{bc}} \exp(j120^\circ) + v_{\text{ca}} \exp(-j120^\circ)] \quad (16.38)$$

Of the three groups in Table 16.1, only the switching combinations of Group II and Group III are employed for the SVM method. Group II consists of switching state voltage vectors having constant angular positions and are called *active* or *stationary* vectors. Each subgroup of Group II determines the position of the resulting output voltage space vector, and the six state space voltage vectors form a six-sextant hexagon used to synthesize the desired output voltage vector. Group III comprises the *zero* vectors positioned at the center of the output voltage hexagon and these are suitably combined with the active vectors for the output voltage synthesis.

The modulation method involves selection of the vectors and their on-time computation. At each sampling period T_s, the algorithm selects four active vectors related to any possible combinations of output voltage and input current sectors in addition to the zero vector to construct a desired reference voltage. The amplitude and the phase angle of the reference voltage vector are calculated and the desired phase angle of the input current vector are determined in advance. For computation of the on-time periods of the chosen vectors, these are combined into two sets leading to two new vectors adjacent to the reference voltage vector in the sextant and having the same direction as the reference voltage vector. Applying the standard SVM theory, the general formulas derived for the vector on-times, which satisfy, at the same time, the reference output voltage and input current displacement angle in Reference [29], are

$$
\begin{aligned}
t_1 &= \frac{2qT_s}{\sqrt{3}\cos\phi_i}\sin(60^\circ - \theta_o)\sin(60^\circ - \theta_i)\\
t_2 &= \frac{2qT_s}{\sqrt{3}\cos\phi_i}\sin(60^\circ - \theta_o)\sin\theta_i\\
t_3 &= \frac{2qT_s}{\sqrt{3}\cos\phi_i}\sin\theta_o\sin(60^\circ - \theta_i)\\
t_4 &= \frac{2qT_s}{\sqrt{3}\cos\phi_i}\sin\theta_o\sin\theta_i
\end{aligned}
\qquad (16.39)
$$

where $q =$ voltage transfer ratio, ϕ_i is the input displacement angle chosen to achieve the desired input power factor (with $\phi_i = 0$, a maximum value of $q = 0.866$ is obtained), θ_o and θ_i are the phase displacement angles of the output voltage and input current vectors, respectively, whose values are limited within the 0–60° range. The on-time of the zero vector is

$$t_o = T_s - \sum_{i=1}^{4} t_i \qquad (16.40)$$

The integral value of the reference vector is calculated over one sample time interval as the sum of the products of the two adjacent vectors and their on-time ratios. The process is repeated at every sample instant.

Control Implementation and Comparison of the Two Methods. Both methods need a Digital Signal Processor (DSP)-based system for their implementation. In one scheme [29] for the Venturini method, the programmable timers, as available, are used to time out the PWM gating signals. The processor calculates the six switch duty cycles in each sampling interval, converts them to integer counts, and stores them in the memory for the next sampling period. In the SVM method, an EPROM is used to store the selected sets of active and zero vectors and the DSP calculates the on-times of the vectors. Then with an identical procedure as in the other method, the timers are loaded with the vector on-times to generate PWM waveforms through suitable output ports. The total computation time of the DSP for the SVM method has been found to be much less than that of the Venturini method. Comparison of the two schemes shows that while in the SVM method the switching losses are lower, the Venturini method shows better performance in terms of input current and output voltage harmonics

16.5.2 Commutation and Protection Issues in a Matrix Converter

As the matrix converter has no dc link energy storage, any disturbance in the input supply voltage will affect the output voltage immediately and a proper protection mechanism has to be incorporated, particularly against overvoltage from the supply and overcurrent in the load side. As mentioned, two types of bidirectional switch configurations have hitherto been used—one, the transistor (now IGBT) embedded in a diode bridge, and the other, the two IGBTs in antiparallel with reverse voltage blocking diodes (shown in Fig 16.31). In the latter configuration, each diode and IGBT combination operates in two quadrants only, which eliminates the circulating currents otherwise built up in the diodo-bridge configuration that can be limited by only bulky commutation inductors in the lines.

The MC does not contain freewheeling diodes that usually achieve safe commutation in the case of other converters. To maintain the continuity of the output current as each switch turns off, the next switch in sequence must be immediately turned on. In practice, with bidirectional switches, a momentary short-circuit may develop between the input phases when the switches cross over and one solution is to use a *semisoft current commutation* using a multistepped switching procedure to ensure safe commutation [28, 34]. This method requires independent control of each two-quadrant switches, sensing the direction of the load current and introducing a delay during the change of switching states.

A clamp capacitor connected through two three-phase full-bridge diode rectifiers involving an additional 12 diodes (a new configuration with the number of additional diodes reduced to six using the antiparallel switch diodes has been reported [34]) at the input and output lines of the MC serves as a voltage clamp for possible voltage spikes under normal and fault conditions.

A three-phase single-stage LC filter consisting of three capacitors in star and three inductors in the line is used to adequately attenuate the higher-order harmonics and render sinusoidal input current. Typical values of L and C based on a 415-V converter with a maximum line current of 6.5 A and a

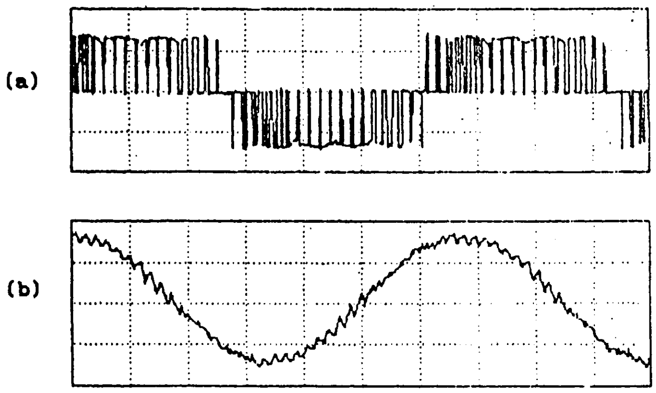

FIGURE 16.33 Experimental waveforms for a matrix converter at 30-Hz frequency from a 50-Hz input: (a) output line voltage; and (b) output line current.

switching frequency of 20 kHz are 3 mH and 1.5 μF only [32]. The filter may cause a minor phase shift in the input displacement angle that needs correction. Figure 16.33 shows typical experimental waveforms of output line voltage and line current of an MC. The output line current is mostly sinusoidal except for a small ripple, when the switching frequency is around 1 kHz only.

16.6 Applications of AC/AC Converters

16.6.1 Applications of AC Voltage Controllers

AC voltage controllers are used either for control of the rms value of voltage or current in lighting control, domestic and industrial heating, speed control of fan, pump or hoist drives, soft starting of induction motors, so forth, or as *static ac switches (on/off control)* in transformer tap changing, temperature control, speed stabilization of high inertia induction motor drives such as centrifuge, capacitor switching in static reactive power compensation, and so forth.

In *fan or pump drives* with induction motors, the torque varies as the square of the speed. Thus the speed control is required in a narrow range and an ac voltage controller is suitable for an induction motor with a full load slip of 0.1 to 0.2 in such applications. For these drives, braking or reverse operations are not needed, but for the crane hoist drive, both motoring and braking are needed and a four-quadrant ac voltage controller can be obtained by a modification of the ac voltage controller circuit as shown in Fig. 16.34. The SCR pairs A, B, and C provide operation in quadrants I and IV and A' B, and C' in quadrants II and III. While changing from one set of SCR pairs to another, care should be taken to ensure that the incoming pair is activated only after the outgoing pair is fully turned off.

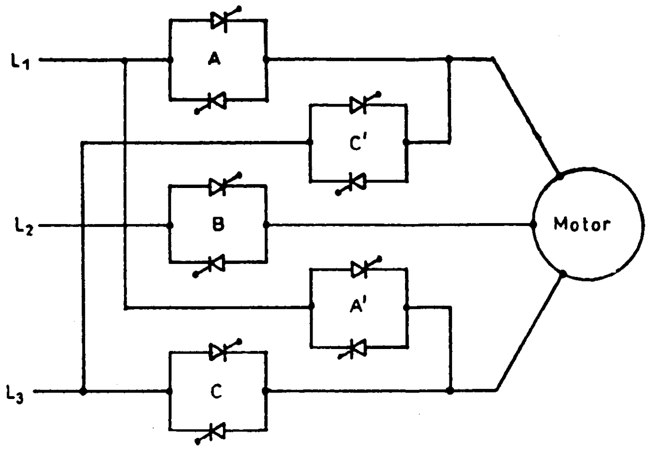

FIGURE 16.34 Four-quadrant ac voltage controller.

The ac voltage controllers are being used increasingly for *soft-starting* of induction motors, as they have a number of advantages over the conventional starters, such as smooth acceleration and deceleration, ease in implementation of current control, simple protection against single-phasing or unbalanced operation, reduced maintenance and losses, absence of current inrush, and so forth. Even for the fixed-speed industrial applications, the voltage controllers can be used to provide a reduced stator voltage to an induction motor to improve its efficiency at light load and result in energy saving. Operation at an optimum voltage reduces the motor flux, which, in turn, reduces the core loss and the magnetizing component of the stator copper loss. Considerable savings in energy can be obtained in applications where a motor operates at no load for a significant time, such as in drills, machine tools, woodworking machines, reciprocating air-compressors, and so forth. A popular approach to find an optimum operating voltage is to maximize the motor power factor by maintaining a minimum phase shift between the voltage and current after sensing them.

The ac switch with on/off control used in driving a high-inertia centrifuge involves switching on of the motor when the speed of the centrifuge drops below the minimum allowable level and switching off motor when the speed reaches the maximum allowable level thus maintaining a constant average speed. An identical scheme of control is used with an ac switch for temperature control of an electric heater or air-conditioner.

Integral-cycle control is well suited to heating control while it may cause flicker in normal incandescent lighting control and speed fluctuations in motor control. However, with this control less voltage distortion is produced in the ac supply system and less radio frequency interference is propagated when compared with the phase-controlled system.

16.6.2 Applications of Cycloconverters

Cycloconverters as frequency changers essentially find well-established applications in: (i) high-power low-speed reversible ac motor drives with constant frequency input; and (ii) constant frequency power supplies with a variable frequency input as in the VSCF (variable-speed constant frequency) system. They also find potential applications in: (iii) controllable VAR generators for power factor correction; and (iv) ac system interties linking two independent power systems as demonstrated in Reference [13].

Variable Speed AC Drives. In this category, the applications of cycloconverter-controlled induction motor and synchronous motor drives have been adequately reviewed in Reference [15]. Cycloconverter-fed synchronous motors are well suited for low-speed drives with high torque at standstill, and high-capacity gearless cement mills (tube or ball-mill above 5 MW) have been the first applications of these drives.

Since the 1960s, as developed by Siemens and Brown Boveri, one of the early installations has employed a motor rating of 6.4 MW having a rotor diameter of 5 m and 16.5 m in length while the stator construction is similar to that of a hydroelectric generator with 44 poles requiring 5.5 Hz for a maximum speed of 15 rpm. The motor is flanged with the mill cylinder without additional bearings or "wrapped" directly around it. This is known as *ring motor* [35]. With the evolution of *field orientation* or *vector control*, cycloconverter-fed synchronous motors have replaced or are replacing the dc drives in the reversing rolling mills (2/4 MW) with extreme high dynamic requirements for torque and speed control [36, 48, 49] in mine winders and haulage [37, 49] of similar high ratings, and in icebreakers and ships equipped with diesel generators with power ratings of about 20 MW per unit [38]. In these applications, the cycloconverter-fed synchronous motor is in the *self-controlled* mode and is known as an *ac commutatorless motor* when the cycloconverter firing signals are derived from a rotor shaft position sensor so that the frequency is slaved to the rotor speed and not *vice versa*. As a result the hunting and stability problems are eliminated and the torque is not limited to pull-out value. Further, with field control the motor can be operated at leading power factor when the cycloconverter can operate with *load commutation* from the motor side at high speed in addition to the line commutation from the supply at low speed, thus providing speed control over a wide range. A cycloconverter-fed ac commutatorless motor was reported in Reference [39] where the cycloconverter is operated both in the sinusoidal and trapezoidal mode the latter is attractive for a better system power factor and higher voltage output at the cost of increased harmonic content [1]. A stator-flux oriented vector control scheme for 6-pulse circulating current-free cycloconverter-fed synchronous motor with a flux observer suitable for a rolling mill drive (300-0-300 rpm) is reported in Reference [40]. A 12-pulse, 9.64 MVA, 120/33.1-Hz cycloconverter-linear synchronous motor combination for the Maglev Vehicle ML-500, a high-speed train (517 km/hr) has been in the process of development in Japan since the early 1980s [41].

Regarding cycloconverter-fed induction motors, early applications were for control of multiple ran-out table motors of a hot strip mill, high-performance servodrives, and controlled slip-frequency drive for diesel electric locomotives. Slip power-controlled drives in the form of static Scherbius drives with very high ratings using a cycloconverter in the rotor of a doubly fed slip-ring induction motor have been in operation for high-capacity pumps, compressors [42], and even in a proton-synchrotron accelerator drive in CERN, Geneva [43]. Although synchronous motors have been preferred for very high-capacity low-speed drives because of their high rating, the ability to control power factor and precisely set speed independent of supply voltage and load variations., induction motors because of their absence of excitation control loop, simple structure, easy maintainability and quick response have been installed for cycloconverter-fed drives in Japan. For example, a seamless tube piercing mill [44] where a squirrel-cage 6-pole 3-MW, 188/300-rpm, 9.6/15.38-Hz, 2700-V motor is controlled by a cycloconverter bank of capacity 3750 kVA and output voltage 3190 V.

Constant Frequency Power Supplies. Some applications such as aircraft and naval ships need a well-regulated constant frequency power output from a variable frequency ac power source. For example, in aircraft power conversion, the alternator connected to the engine operating at a variable speed of 10,000 to 20,000 rpm provides a variable frequency output power over a 1200–2400-Hz range, which can be converted to an accurately regulated fixed-frequency output power at 400 Hz through a cycloconverter with a suitable filter placed within a closed loop. The output voltages of the cycloconverter are proportional to the fixed-frequency (400 Hz) sine wave reference voltage generator in the loop.

Both synchronous and induction motors can be used for VSCF generation. The static Scherbius system can be modified (known as Kramer drive) by feeding slip power through a cycloconverter to a shaft-mounted synchronous machine with a separate exciter for VSCF generation. A new application in very high-power ratings of constant frequency variable-speed motor generators with a cycloconverter is in pumped storage schemes using reversible pump turbines for adaptation of the generated power to varying loads or keeping the ac system frequency constant. In 1993, a 400-MW variable-speed pumped storage system was commissioned by Hitachi at Qkhawachi Hydropower plant [45] in Japan where the field windings of a 20-pole generator/motor are excited with three-phase low-frequency ac current via slip-rings by a 72-MVA, three-phase 12-pulse line-commuted cycloconverter. The armature terminals rated at 18 kV are connected to a 500-kV utility grid through a step-up transformer. The output frequency of the circulating current-free cycloconverter is controlled within ±5 Hz and the line frequency is 60 Hz. The variable-speed system has a synchronous speed of 360 rpm with a speed range −330 to 390 rpm. The operational system efficiency in the pump mode is improved by 3 when compared to the earlier constant speed system.

Static VAR Generation. Cycloconverters with a high-frequency (HF) base, either a HF generator or an oscillating LC tank can be used for reactive power generation and control, replacing synchronous condensers or switched capacitors as demonstrated in Reference [13]. If the cycloconverter is controlled to generate output voltage waves whose wanted components are in phase with the corresponding system voltages, reactive power can be supplied in either direction to the ac system by amplitude control of the cycloconverter output voltages. The cycloconverter will draw leading current from (that is, it will supply lagging current to) the ac system when its output voltage is greater than that of the system voltage and *vice versa*.

Interties Between AC Power Systems. The naturally commutated cycloconverter (NCC) was originally developed for this application to link a three-phase 50-Hz ac system with a single-phase $16\frac{2}{3}$ Hz railway supply system in Germany in the 1930s. Applications involve slip-power-controlled motors with sub- and super-synchronous speeds. The stator of the motor is connected to 50-Hz supply, which is connected to the rotor as well through a cvcloconverter and the motor drives a single-phase synchronous generator feeding to $16\frac{2}{3}$ Hz system [46, 47]. A static asynchronous intertie between two different systems of different frequency can be obtained by using two NCCs in tandem, each with its input terminals connected to a common HF base. As long as the base frequency is appropriately higher than that of either system, two system frequencies can either be the same or different. The power factor at either side can be maintained at any desired level [13].

16.6.3 Applications of Matrix Converters

The practical applications of the matrix converters, as of now, is very limited. The main reasons are: (i) nonavailability of the bilateral fully controlled monolithic switches capable of high-frequency operation; (ii) complex control law implementation; (iii) an intrinsic limitation of the output/input voltage ratio; and (iv) commutation [50] and protection of the switches. To date, the switches are assembled from existing discrete devices resulting in increased cost and complexity and only experimental circuits of capacity well below 100 kVA have been built . However, with the advances in device technology, it is hoped that the problems will be solved eventually and the MC will not only replace the NCCs in all the applications mentioned under Section 16.6.2 but will also take over from the PWM rectifier inverters as well. In Reference [51], it has been shown that with space vector PWM control using overmodulation, the voltage transfer ratio may be increased to 1.05 at the expense of more harmonics and large filter capacitors.

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DC/DC Conversion Technique and Nine Series L Converters

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17.1 Introduction

The dc/dc converters are widely used in industrial applications and computer hardware circuits, and the dc/dc conversion technique has been developed very quickly. Since the 1950s there have been five generations of dc/dc converters developed. They are the first-generation (classical) converters, second-generation (multiquadrant) converters, third-generation (switched-component) converters, fourth-generation (soft-switching) converters, and fifth-generation (synchronous rectifier) converters.

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The first-generation converters perform in a single-quadrant mode and in a low-power range (up to 100 W). These converters include the buck converter, the boost converter, and the buck-boost converter. However, because of the effects of parasitic elements, the output voltage and power transfer efficiency of all these converters are restricted.

The voltage-lift technique is a popular method that is widely applied in electronic circuit design because it effectively overcomes the effects of parasitic elements and greatly increases the output voltage. Therefore, these dc/dc converters can convert the source voltage into a higher output voltage with high-power efficiency, high-power density and a simple structure.

The second-generation converters perform in two- or four-quadrant operation with medium output power range (say, hundreds of watts or higher). Because of high-power conversion, these converters are usually applied in industrial applications with high-power transmission, for example, dc motor drives with multiquadrant operation. Most of second-generation converters are still made of capacitors and inductors, as a result they are large.

The third-generation converters are called switched-component dc/dc converters, and are made of either inductors or capacitors, which are called switched inductors and switched capacitors. They usually perform in two- or four-quadrant operation with a high-output power range (say, thousands of watts). As they are made only of inductors or capacitors, they are small.

Switched-capacitor dc/dc converters are made only of switched-capacitors. Because switched capacitors can be integrated into power semiconductor integrated circuit (IC) chips, they have limited size and work at high switching frequency. They have been successfully employed in the inductorless dc/dc converters and have opened the way to constructing converters with high power density. Therefore, they have drawn much attention from research workers and manufacturers. However, while most of these converters reported in the literature perform single-quadrant operation, some of them work in the push-pull state. In addition, their control circuit and topologies are very complex, especially for the large difference between input and output voltages.

Switched-inductor dc/dc converters are made of only inductor, and have been derived from four-quadrant choppers. They usually perform multiquadrant operation with very simple structure. The significant advantage of these converters is their simplicity and high power density. No matter how large the difference between the input and output voltages, only one inductor is required for each switched inductor dc/dc converter. Therefore, they are in great demand for industrial applications.

The fourth-generation converters are called soft-switching converters. The soft-switching technique involves many methods implementing resonance characteristics, and one popular method is the resonant-switching method. The two main groups are zero-current-switching (ZCS) and zero-voltage-switching (ZVS), and as reported in the literature, they usually perform in single-quadrant operation. We have developed this technique in the two- and four-quadrant operation for the high-output power range (say, thousands of watts).

Multiquadrant ZCS/ZVS quasi-resonant converters (QRC) implement the ZCS/ZVS technique in four-quadrant operation. As switches turn-on and turn-off the moment the current/voltage is equal to zero, the power losses during switching on and off become zero. Consequently, these converters have high power density and transfer efficiency. Usually, the repeating frequency is not very high and the converters work in a monoresonance frequency, and the components of higher-order harmonics are very low. Using fast Fourier transform (FFT) analysis, we determine that the total harmonic distortion (THD) is very small. Therefore, the electromagnetic interference (EMI) is weak, and electromagnetic sensitivity (EMS) and electromagnetic compatibility (EMC) are reasonable.

Fifth-generation converters are called synchronous rectifier (SR) dc/dc converters. Corresponding to the development of microelectronics and computer science, the power supplies with low output voltage (5, 3.3, and 1.8 ~ 1.5 V) and strong output current (30, 50, 100 up to 200 A) are required in industrial applications and computer peripheral equipment; traditional diode bridge rectifiers are not available for this requirement. Many prototypes of synchronous rectifier dc/dc converters using the soft-switching technique have been developed. Synchronous rectifier dc/dc converters possess the technical features of very low voltage, strong current and high-power transfer efficiency η (90, 92 up to 95) and high power density (22–25 W/in^3).

Luo has been studying the dc/dc conversion technique for a long time and obtained outstanding results. He has created nine series converters, namely Luo-converters, and they are as follows:

positive output Luo-converters;
negative output Luo-converters;
double output Luo-converters;
multiple-quadrant Luo-converters;
switched capacitor multiquadrant Luo-converters;
switched inductor multiquadrant Luo-converters;
multiquadrant ZCS quasi-resonant Luo-converters;
multiquadrant ZVS quasi-resonant Luo-converters; and
synchronous rectifier dc/dc Luo-converters.

All of his research results have been published in major international journals and at major international conferences. Many experts, including Rashid, of West Florida University, Kassakian, of MIT, and Rahman, of Memorial University of Newfoundland are very interested in his work, and acknowledge his outstanding achievements.

In this handbook, we present only the circuit diagram and list a few parameters of each converter, such as the output voltage and current, voltage-transfer gain and output voltage variation ratio, and the discontinuous condition and output voltage.

In this chapter, the input voltage is V_I or V_1 and load voltage is V_O or V_2. The pulsewidth modulated (PWM) pulse train has repeating frequency f, and the repeating period is $T = 1/f$. The conduction duty is k, the switching-on period is kT and the switching-off period is $(1 - k)T$. All average values are in capital letters, and instantaneous values are in small letters, for example, V_1 and $v_1(t)$ or v_1. The variation ratio of the freewheeling diode current is ζ. The voltage-transfer gain is M and power transfer efficiency is η.

17.2 Positive Output Luo-Converters

The first-generation converters are called classical converters that perform in a single-quadrant mode and in the low power range. The development of the first-generation converters has a very long history, and there have been many prototypes. We can sort them in three categories:

- Fundamental topologies: buck converter, boost converter and buck-boost converter;
- developed topologies: positive output Luo-converters, negative output Luo-converters, double output Luo-converters, and the Cuk-converter; and
- transformer-type topologies: flyback converter, half-bridge converter, and forward converter.

17.2.1 Fundamental Topologies

The **buck converter** is a step-down converter and is shown in Fig. 17.1a. The typical output voltage and current waveforms are shown in Fig. 17.1b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.1c and d. Its output voltage and output current are:

$$V_O = kV_I \quad \text{and} \quad I_O = \frac{1}{k} I_I$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small and the load current is high.

The **boost converter** is a step-up converter and is shown in Fig. 17.2a. The typical output voltage and current waveforms are shown in Fig. 17.2b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.2c,d. Its output voltage and current are:

$$V_O = \frac{1}{1 - k} V_I \quad \text{and} \quad I_O = (1 - k) I_I$$

The output voltage is higher than the input voltage. This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high.

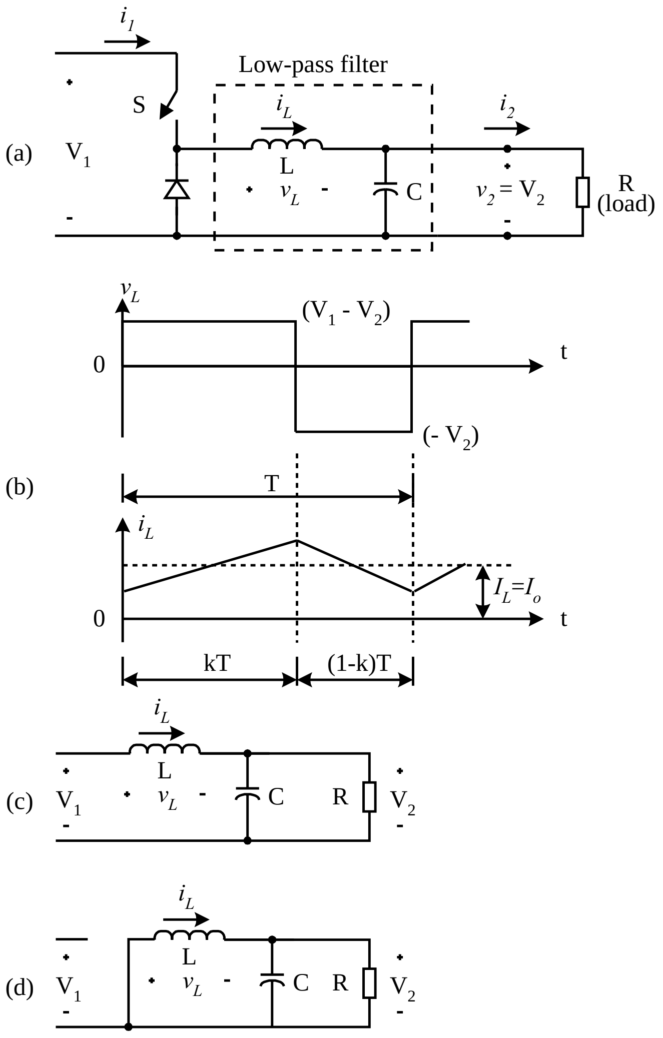


FIGURE 17.1 Buck Converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit. Rashid, M.H. *Power Electronics: Circuits, Devices and Applications, 2/e*, © 1993, pp. 318, 321, 324, 327, 479. Adapted by permission of Pearson Education, Inc., Upper Saddle River, New Jersey.

The **buck-boost converter** is a step-down/step-up converter, which is shown in Fig. 17.3a. The typical output voltage and current waveforms are shown in Fig. 17.3b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.3c,d. Its output voltage and current are:

$$V_O = \frac{k}{1 - k} V_I \quad \text{and} \quad I_O = \frac{1 - k}{k} I_I$$

When k is greater than 0.5, the output voltage can be higher than the input voltage. This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high.

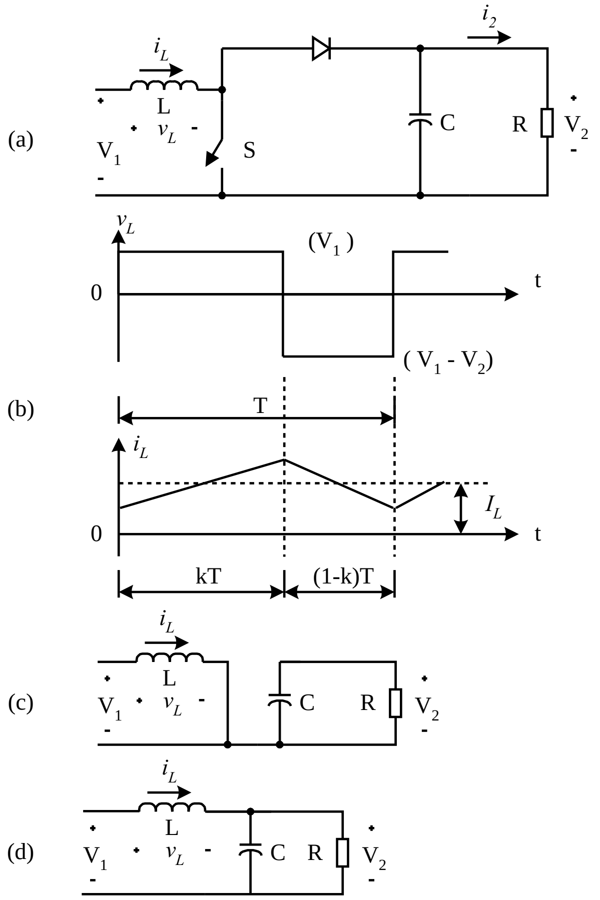


FIGURE 17.2 Boost converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit. Rashid, M.H. *Power Electronics: Circuits, Devices and Applications, 2/e*, © 1993, pp. 318, 321, 324, 327, 479. Adapted by permission of Pearson Education, Inc., Upper Saddle River, New Jersey.

17.2.2 Developed Topologies

The **positive output Luo-converter** is a step-down/step-up converter, which is derived from the buck-boost converter. It has one more inductor and capacitor, and is shown in Fig. 17.4a. The typical output voltage and current waveforms are shown in Fig. 17.4b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.4c,d. Its output voltage and current are:

$$V_O = \frac{k}{1-k} V_I \quad \text{and} \quad I_O = \frac{1-k}{k} I_I$$

When k is greater than 0.5, the output voltage can be higher than the input voltage. This converter may work in the discontinuous mode if the frequency f is small, k is small, inductance L is small, and the load current is high.

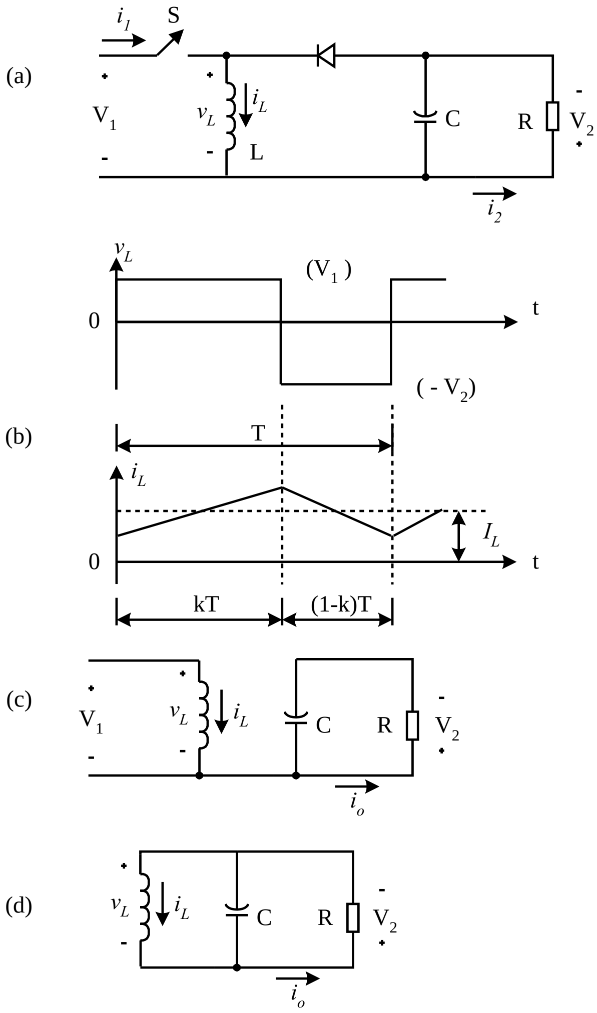


FIGURE 17.3 Buck-boost converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit. Rashid, M.H. *Power Electronics: Circuits, Devices and Applications, 2/e*, © 1993, pp. 318, 321, 324, 327, 479. Adapted by permission of Pearson Education, Inc., Upper Saddle River, New Jersey.

A **negative output Luo-converter** is a negative output step-down/step-up converter, which is derived from the buck-boost converter. It has one more inductor and capacitor, and is shown in Fig. 17.5a. The typical output voltage and current waveforms are shown in Fig. 17.5b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.5c,d. Its output voltage and current (absolute value) are:

$$V_O = \frac{k}{1-k} V_I \quad \text{and} \quad I_O = \frac{1-k}{k} I_I$$

When k is greater than 0.5, the output voltage can be higher than the input voltage. This converter may work in the

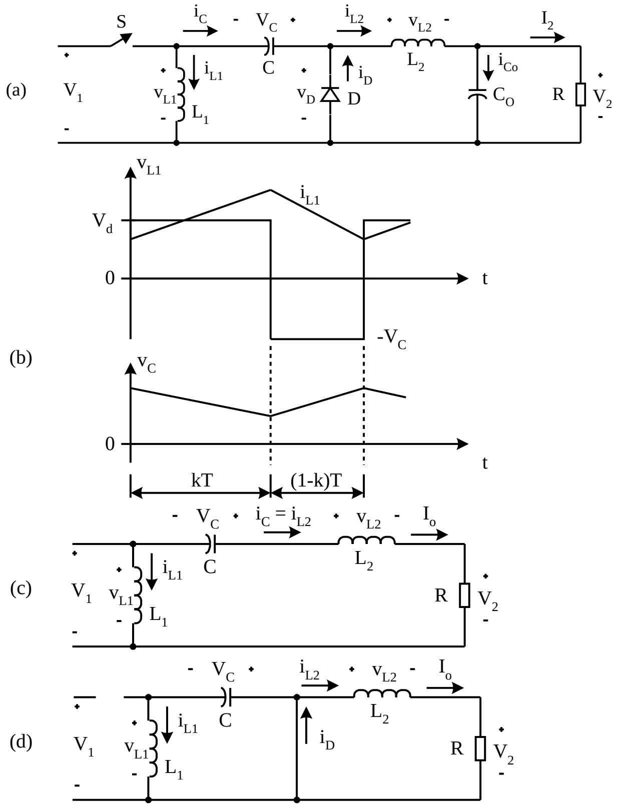

(a)
S
i_C
- V_C +
i_{L2}
+ v_{L2} -
I_2
V_1
v_{L1}
i_{L1}
L_1
C
v_D
i_D
D
L_2
i_{Co}
C_O
R
V_2
(b)
v_{L1}
i_{L1}
V_d
0
t
$-V_C$
v_C
0
t
kT
(1-k)T
(c)
- V_C + $i_C = i_{L2}$ + v_{L2} - I_o
C
L_2
V_1 v_{L1} i_{L1} L_1
R V_2
(d)
- V_C + i_{L2} + v_{L2} - I_o
C
L_2
V_1 v_{L1} i_{L1} L_1
i_D
R V_2

FIGURE 17.4 Positive output Luo-converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; (d) switch-off equivalent circuit.

discontinuous mode if the frequency f is small, k is small, inductance L is small, and the load current is high.

The **double output Luo-converter** is a double output step-down/step-up converter, which is derived from a **P/O Luo**-converter and an **N/O Luo**-converter. It has two conversion paths and two output voltages V_{O+} and V_{O-}. It is shown in Fig. 17.6a. The typical output voltage and current waveforms are shown in Fig. 17.6b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.6c,d. By carefully selecting the components we can obtain the output voltages and currents (absolute value)

$$V_{O+} = |V_{O-}| = \frac{k}{1-k} V_I \quad I_{O+} = \frac{1-k}{k} I_{I+}$$

and

$$I_{O-} = \frac{1-k}{k} I_{I-}$$

When k is greater than 0.5, the output voltage can be higher than the input voltage. This converter may work in the discontinuous mode if the frequency f is small, k is small, inductance L is small, and the load current is high.

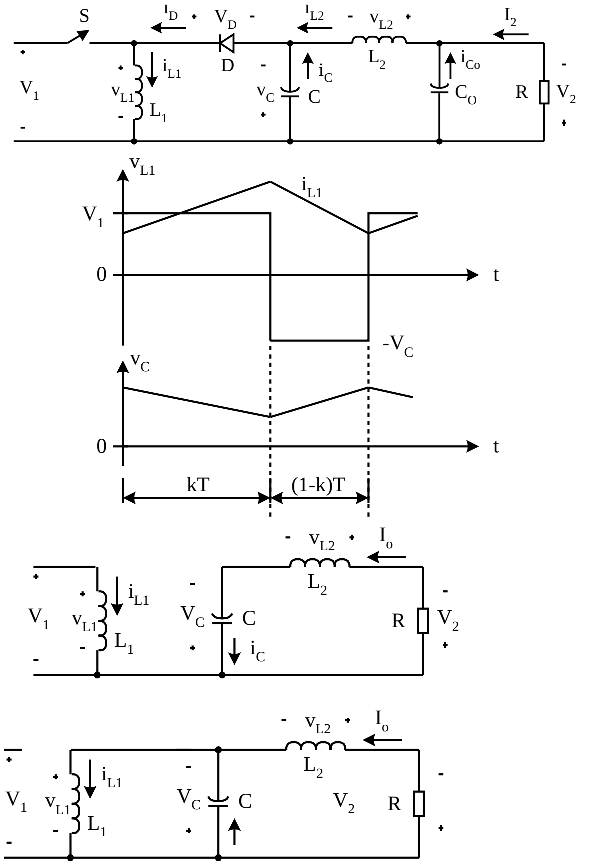

S
I_D
+ V_D -
i_{L2}
- v_{L2} +
I_2
V_1
v_{L1}
i_{L1}
L_1
D
v_C
i_C
C
L_2
i_{Co}
C_O
R
V_2
v_{L1}
i_{L1}
V_1
0
t
$-V_C$
v_C
0
t
kT
(1-k)T
- v_{L2} + I_o
L_2
V_1 v_{L1} i_{L1} L_1
V_C C i_C
R V_2
- v_{L2} + I_o
L_2
V_1 v_{L1} i_{L1} L_1
V_C C
V_2 R

FIGURE 17.5 Negative ouput Luo-converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

The **Cuk-converter** is a negative output step-down/step-up converter, which is derived from the boost converter. It has one more inductor and capacitor, and is shown in Fig. 17.7a. The typical output voltage and current waveforms are shown in Fig. 17.7b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.7c,d. Its output voltage and current (absolute value) are:

$$V_O = \frac{k}{1-k} V_I \quad \text{and} \quad I_O = \frac{1-k}{k} I_I$$

When k is greater than 0.5, the output voltage can be higher than the input voltage. This converter may work in the discontinuous mode if the frequency f is small, k is small, inductance L is small, and the load current is high.

17.2.3 Transformer-Type Topologies

The **Fly-back converter** is a negative output step-up converter, which is shown in Fig. 17.8. The transformer turns ratio is N. If the transformer has never been saturated during operation,

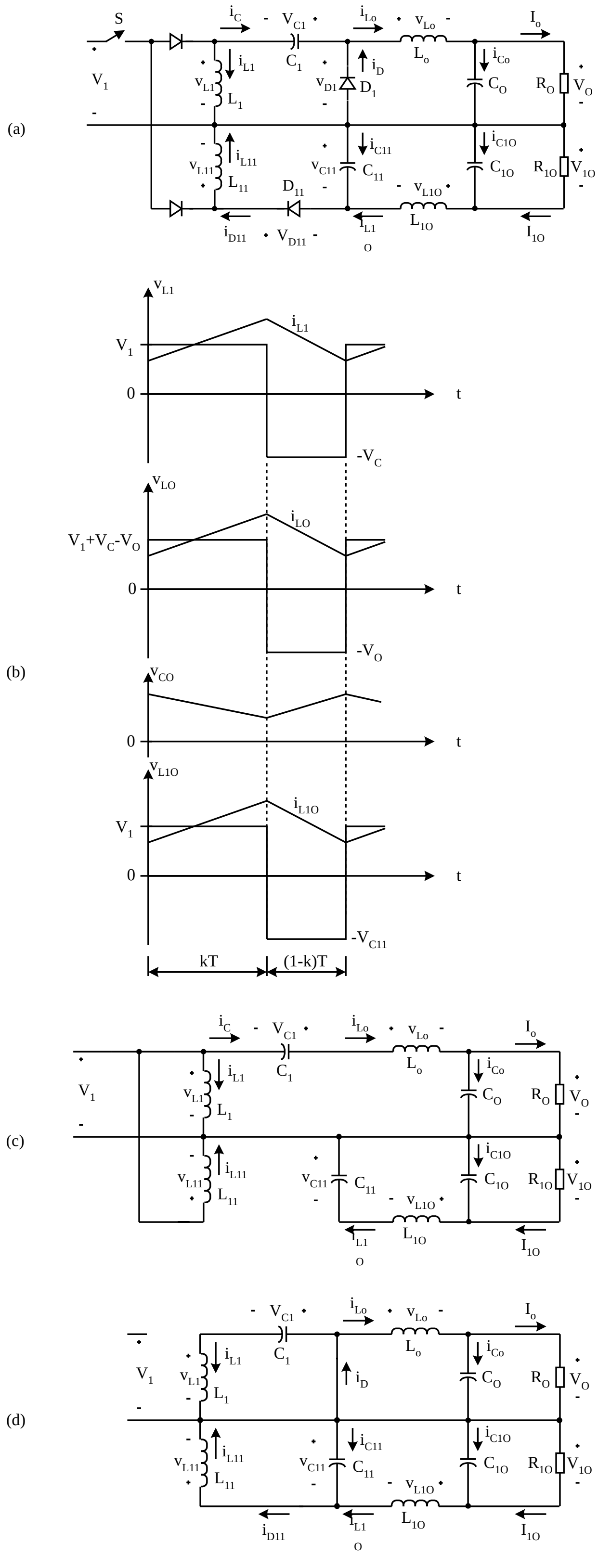

(a)
S
V1
iC
VC1
C1
iLo
vLo
Lo
Io
iL1
vL1
L1
iD
vD1
D1
iCo
CO
RO
VO
iL11
vL11
L11
D11
vC11
iC11
C11
iC1O
C1O
R1O
V1O
vL1O
L1O
iD11
VD11
iL1O
I1O
(b)
vL1
iL1
V1
0
t
-VC
vLO
iLO
V1+VC-VO
-VO
vCO
vL1O
iL1O
-VC11
kT
(1-k)T
(c)
(d)

FIGURE 17.6 Double output Luo-converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

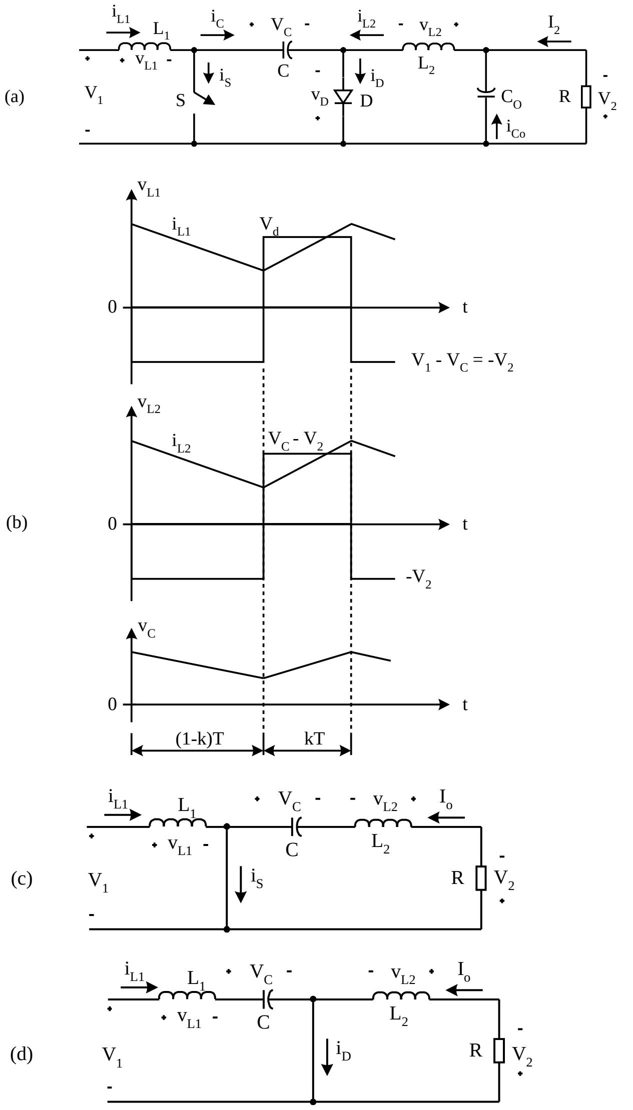

(a)
iL1
L1
vL1
iC
VC
C
iL2
vL2
L2
I2
V1
iS
S
vD
iD
D
CO
iCo
R
V2
(b)
vL1
iL1
Vd
0
t
V1 - VC = -V2
vL2
iL2
VC - V2
-V2
vC
(1-k)T
kT
(c)
Io
(d)

FIGURE 17.7 The Cuk converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit. Rashid, M.H. *Power Electronics: Circuits, Devices and Applications, 2/e*, © 1993, pp. 318, 321, 324, 327, 479. Adapted by permission of Pearson Education, Inc., Upper Saddle River, New Jersey.

it works as a boost converter. Its output voltage and current (absolute value) are:

$$V_O = N\frac{k}{1-k}V_I \quad \text{and} \quad I_O = \frac{1-k}{kN}I_I$$

This converter may work in the discontinuous mode if the frequency *f* is small, conduction duty *k* is small, inductance *L* is small, and the load current is high.

The **half-bridge converter** is a step-up converter, which is shown in Fig. 17.9. There are two switches and one double secondary coils transformer required. The transformer turns

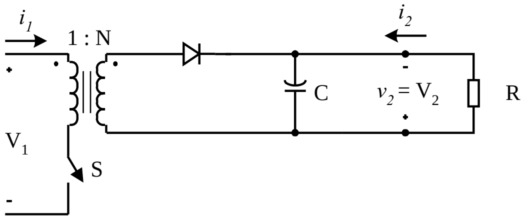


FIGURE 17.8 Flyback converter. Rashid, M.H. *Power Electronics: Circuits, Devices and Applications, 2/e,* © 1993, pp. 318, 321, 324, 327, 479. Adapted by permission of Pearson Education, Inc., Upper Saddle River, New Jersey.

ratio is N. If the transformer has never been saturated during operation, it works as a half-bridge rectifier plus a buck converter. Its output voltage and current are:

$$V_O = kNV_I \quad \text{and} \quad I_O = \frac{1}{kN} I_I$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high.

The **forward converter** is a step-up converter, which is shown in Fig. 17.10. The transformer turns ratio is N (usually $N > 1$). If the transformer has never been saturated during operation, it works as a buck converter. The output voltage and current are:

$$V_O = kNV_I \quad \text{and} \quad I_O = \frac{1}{kN} I_I$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high.

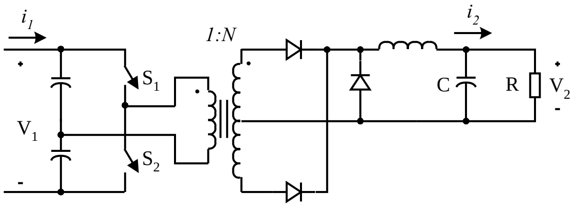


FIGURE 17.9 Half-bridge converter. Rashid, M.H. *Power Electronics: Circuits, Devices and Applications, 2/e,* © 1993, pp. 318, 321, 324, 327, 479. Adapted by permission of Pearson Education, Inc., Upper Saddle River, New Jersey.

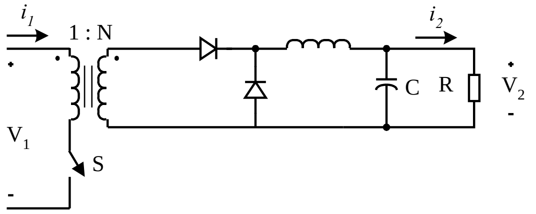


FIGURE 17.10 Forward converter. Rashid, M.H. *Power Electronics: Circuits, Devices and Applications, 2/e,* © 1993, pp. 318, 321, 324, 327, 479. Adapted by permission of Pearson Education, Inc., Upper Saddle River, New Jersey.

17.2.4 Seven 7 Self-Lift DC/DC Converters

Because of the effect of the parasitic elements, the voltage-conversion gain is limited. Especially, when the conduction duty k is towards unity, the output voltage is sharply reduced. The voltage-lift technique is a popular method used in electronic circuit design. The application of this technique can effectively overcome the effect of the parasitic elements, and largely increase the voltage-transfer gain. In this section we introduce seven self-lift converters that are working in the continuous mode.

- P/O Luo self-lift converter;
- reverse P/O Luo self-lift converter;
- simplified P/O Luo self-lift converter;
- N/O Luo self-lift converter;
- Cuk self-lift converter;
- reverse Cuk self-lift converter; and
- enhanced self-lift circuit.

The **P/O Luo self-lift converter** is shown in Fig. 17.11a. The typical output voltage and current waveforms are shown in Fig. 17.11b. The equivalent circuits during switch-on and

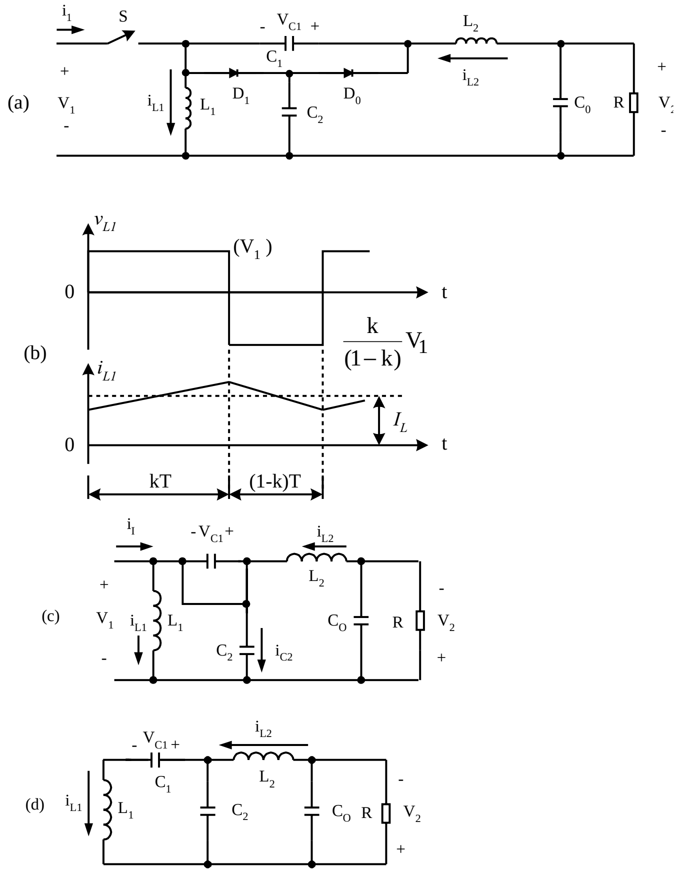


FIGURE 17.11 Positive output Luo self-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

switch-off periods are shown in Fig. 17.11c,d. Its output voltage and current are:

$$V_O = \frac{1}{1-k} V_I \quad \text{and} \quad I_O = (1-k) I_I$$

The voltage transfer gain in the continuous mode is

$$M_S = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{8M_S} \frac{1}{f^2 C_O L_2}$$

The **reverse P/O Luo self-lift converter** is shown in Fig. 17.12a. Typical output voltage and current waveforms are shown in Fig. 17.12b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.12c,d. Its output voltage and current (absolute value) are:

$$V_O = \frac{1}{1-k} V_I \quad \text{and} \quad I_O = (1-k) I_I$$

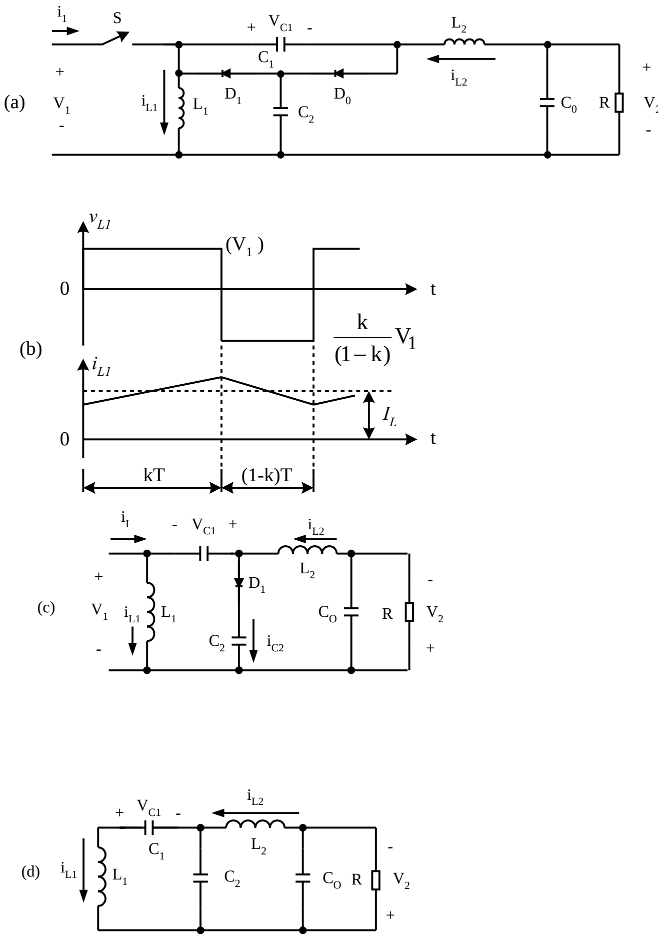
The voltage-transfer gain in the continuous mode is

$$M_S = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

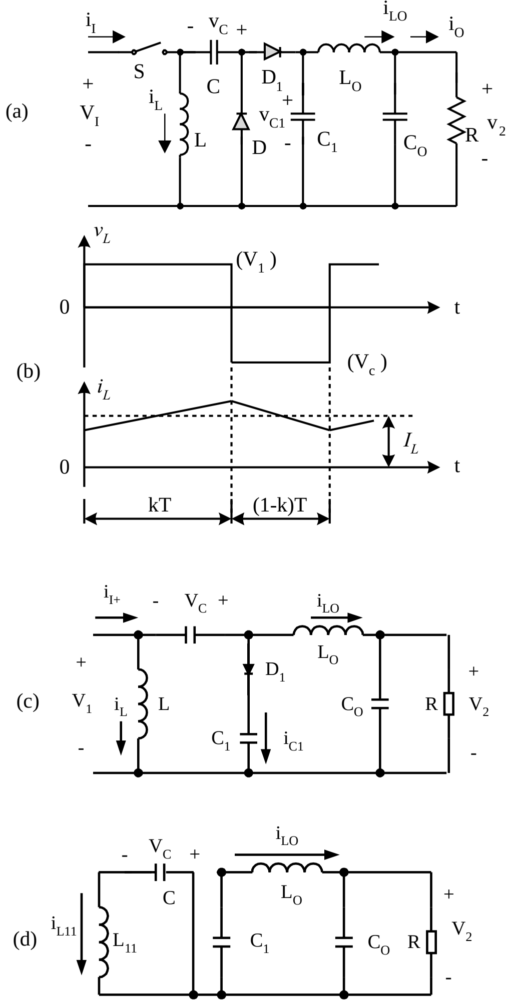
$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{16M_S} \frac{1}{f^2 C_O L_2}$$

The **simplified P/O Luo self-lift converter** is shown in Fig. 17.13a. Typical output voltage and current waveforms are



(a)
(b)
(c)
(d)
i1
S
V1
VC1
C1
D1
D0
L1
iL1
C2
L2
iL2
C0
R
V2
vL1
(V1)
k/(1−k) V1
iL1
IL
0
t
kT
(1-k)T
iC2
CO

FIGURE 17.12 Negative output Luo self-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.



(a)
(b)
(c)
(d)
iI
S
VI
VC
C
D1
D
VC1
C1
L
iL
LO
iLO
iO
CO
R
V2
vL
(V1)
(Vc)
IL
0
t
kT
(1-k)T
V1
iC1
iL11
L11

FIGURE 17.13 Simplified positive output Luo self-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

shown in Fig. 17.13b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.13c,d. Its output voltage and current are:

$$V_O = \frac{1}{1-k} V_I \quad \text{and} \quad I_O = (1-k) I_I$$

The voltage-transfer gain in the continuous mode is

$$M_S = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128} \frac{1}{f^3 L_O C_1 C_0 R}$$

The **N/O Luo self-lift converter** is shown in Fig. 17.14a. Typical output voltage and current waveforms are shown in Fig. 17.14b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.14c,d. Its output voltage and current (absolute value) are:

$$V_O = \frac{1}{1-k} V_I \quad \text{and} \quad I_O = (1-k) I_I$$

The voltage-transfer gain in the continuous mode is

$$M_S = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128} \frac{1}{f^3 L_O C_1 C_0 R}$$

The **Cuk self-lift converter** is shown in Fig. 17.15a. Typical output voltage and current waveforms are shown in Fig. 17.15b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.15c,d. Its output voltage and current (absolute value) are

$$V_O = \frac{1}{1-k} V_I \quad \text{and} \quad I_O = (1-k) I_I$$

The voltage-transfer gain in the continuous mode is

$$M_S = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1-k}$$

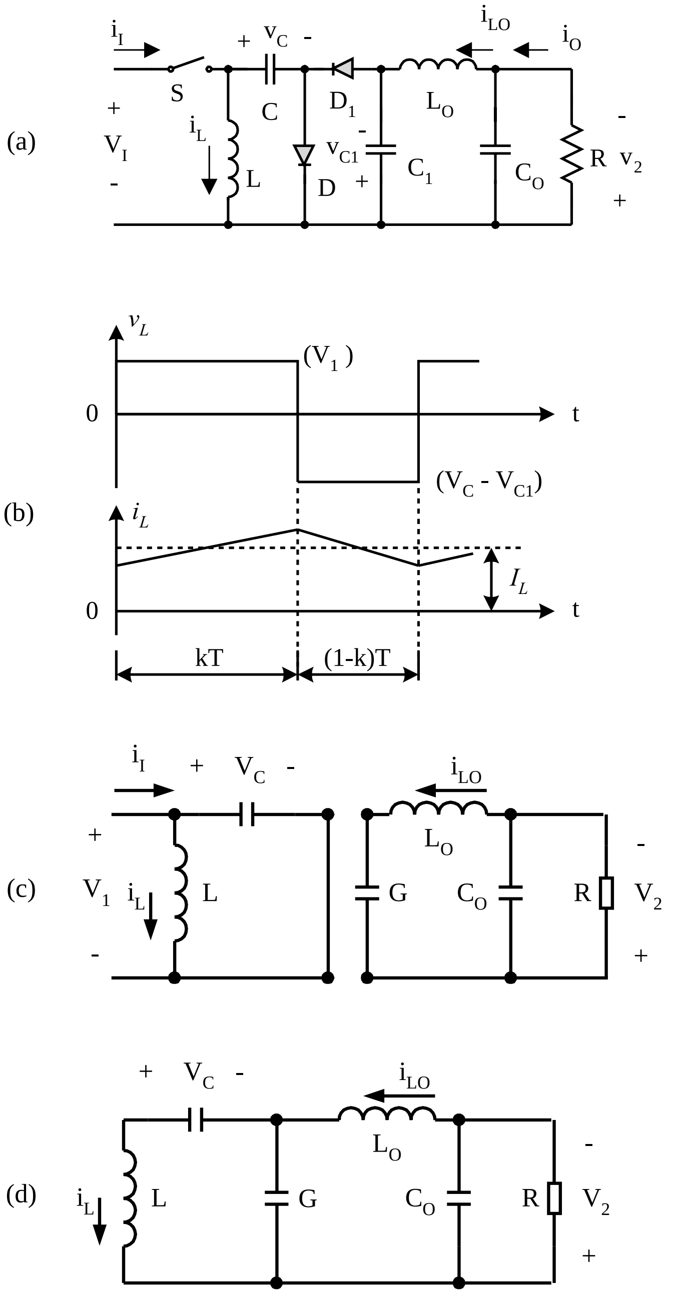


FIGURE 17.14 Negative output Luo self-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128} \frac{1}{f^3 L_O C_1 C_0 R}$$

The **reverse Cuk self-lift converter** is shown in Fig. 17.16a. Typical output voltage and current waveforms are shown in Fig. 17.16b. The equivalent circuits during switch-on and

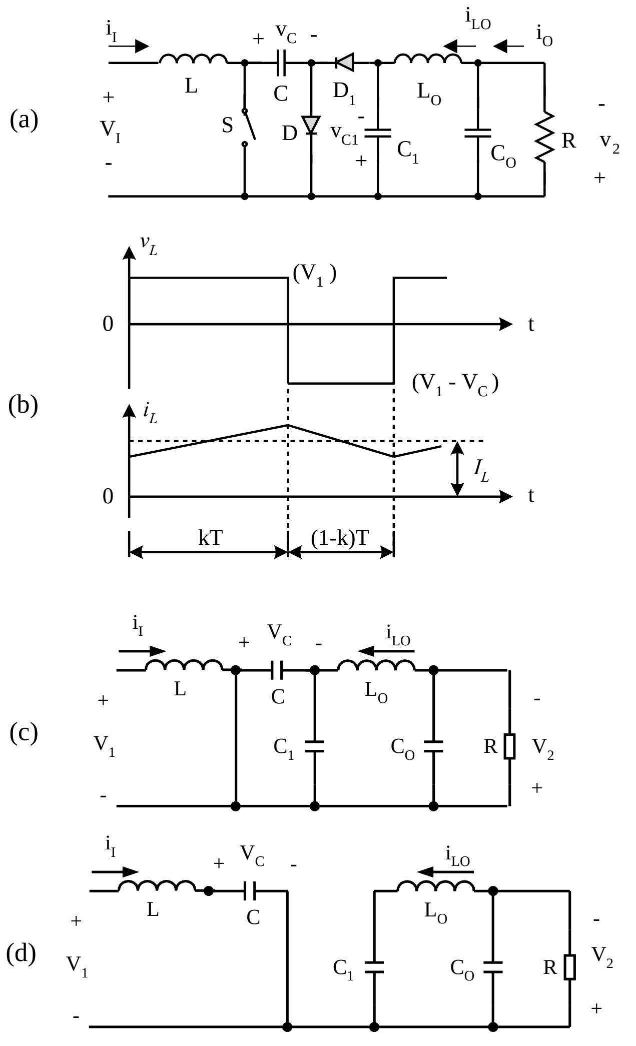

(a)
i_I
$+ v_C -$
i_{LO}
i_O
L
C
D_1
L_O
S
D
v_{C1}
C_1
C_O
R
v_2
V_I
(b)
v_L
(V_1)
$(V_1 - V_C)$
i_L
I_L
0
t
kT
(1-k)T
(c)
V_C
V_1
V_2
(d)

FIGURE 17.15 Cuk self-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

switch-off periods are shown in Fig. 17.16c,d. Its output voltage and current are:

$$V_O = \frac{1}{1-k} V_I \quad \text{and} \quad I_O = (1-k) I_I$$

The voltage-transfer gain in the continuous mode is

$$M_S = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v/2}{V_O} = \frac{k}{128} \frac{1}{f^3 L_O C_1 C_0 R}$$

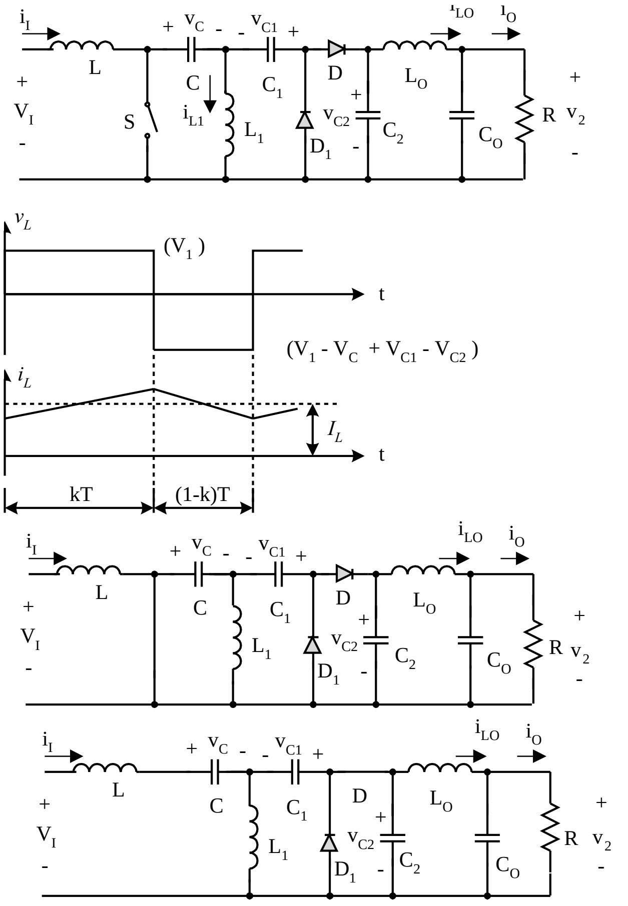

i_I
$+ v_C -$
$- v_{C1} +$
i_{LO}
i_O
L
C
C_1
D
L_O
S
i_{L1}
L_1
v_{C2}
D_1
C_2
C_O
R
v_2
V_I
v_L
(V_1)
$(V_1 - V_C + V_{C1} - V_{C2})$
i_L
I_L
t
kT
(1-k)T

FIGURE 17.16 The reverse Cuk self-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

The **enhanced self-lift converter** is shown in Fig. 17.17a. Typical output voltage and current waveforms are shown in Fig. 17.17b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.17c,d. Its output voltage and current are:

$$V_O = \frac{2-k}{1-k} V_I \quad \text{and} \quad I_O = \frac{1-k}{2-k} I_I$$

The voltage-transfer gain in the continuous mode is

$$M_S = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{2-k}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128} \frac{1}{f^3 L_O C_1 C_0 R}$$

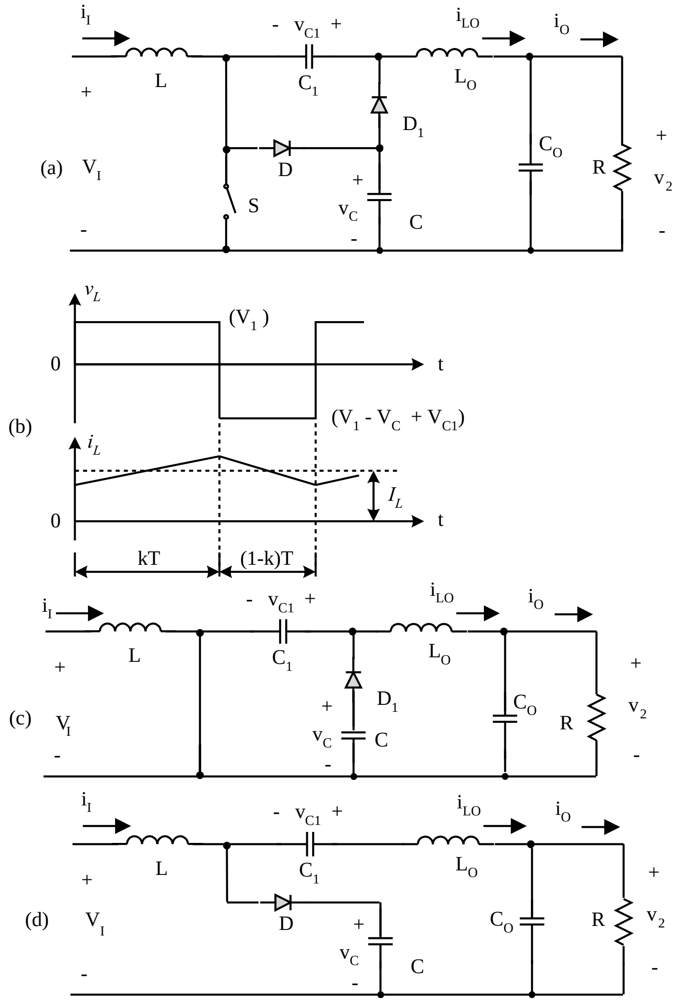


FIGURE 17.17 Enhanced self-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

17.2.5 Positive Output Luo-Converters

The **P/O Luo-converters** perform the voltage conversion from one positive source to another positive load voltage using the voltage-lift technique. They work in the first quadrant with large voltage amplification, and their voltage-transfer gain is high. Five circuits are introduced in the literature. They are:

- elementary circuit;
- self-lift circuit;
- re-lift circuit;
- triple-lift circuit; and
- quadruple-lift circuit.

An additional lift circuit can be derived from the formentioned circuits. In all P/O Luo-converters, we define normalized inductance

$$L = \frac{L_1 L_2}{L_1 + L_2}$$

and normalized impedance

$$z_N = \frac{R}{fL}$$

The **P/O Luo elementary circuit** is shown in Fig. 17.4a. Typical output voltage and current waveforms are shown in Fig. 17.4b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.4c,d. Its output voltage and current are:

$$V_O = \frac{k}{1-k} V_I \quad \text{and} \quad I_O = \frac{1-k}{k} I_I$$

When k is greater than 0.5, the output voltage can be higher than the input voltage.

The voltage-transfer gain in the continuous mode is

$$M_E = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{k}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{8M_E} \frac{1}{f^2 C_O L_2}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_E \leq k\sqrt{\frac{z_N}{2}}$$

The output voltage in the discontinuous mode is

$$V_O = k(1-k)\frac{R}{2fL} V_I \quad \text{with} \quad \sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k}$$

The **P/O Luo self-lift circuit** is shown in Fig. 17.11a. Typical output voltage and current waveforms are shown in Fig. 17.11b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.11c,d. Its output voltage and current are:

$$V_O = \frac{1}{1-k} V_I \quad \text{and} \quad I_O = (1-k) I_I$$

The voltage-transfer gain in the continuous mode is

$$M_S = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{8M_S}\frac{1}{f^2 C_O L_2}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_S \le \sqrt{k}\sqrt{\frac{z_N}{2}}$$

The output voltage in the discontinuous mode is

$$V_O = \left[1 + k^2(1-k)\frac{R}{2fL}\right]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{R}{2fL}} \ge \frac{1}{1-k}$$

The **P/O Luo re-lift circuit** is shown in Fig. 17.18a. The typical output voltage and current waveforms are shown in Fig. 17.18b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.18c,d. Its output voltage and current are:

$$V_O = \frac{2}{1-k}V_I \quad \text{and} \quad I_O = \frac{1-k}{2}I_I$$

The voltage-transfer gain in the continuous mode is

$$M_R = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{2}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{8M_R}\frac{1}{f^2 C_O L_2}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_R \le \sqrt{kz_N}$$

The output voltage in the discontinuous mode is

$$V_O = \left[2 + k^2(1-k)\frac{R}{2fL}\right]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{R}{fL}} \ge \frac{2}{1-k}$$

The **P/O** Luo triple-lift circuit is shown in Fig. 17.19a. The typical output voltage and current waveforms are shown in Fig. 17.19b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.19c,d. Its output voltage and current are:

$$V_O = \frac{3}{1-k}V_I \quad \text{and} \quad I_O = \frac{1-k}{3}I_I$$

The voltage-transfer gain in the continuous mode is

$$M_T = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{3}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{8M_T}\frac{1}{f^2 C_O L_2}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_T \le \sqrt{\frac{3kz_N}{2}}$$

The output voltage in the discontinuous mode is

$$V_O = \left[3 + k^2(1-k)\frac{R}{2fL}\right]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{3R}{2fL}} \ge \frac{3}{1-k}$$

The **P/O Luo quadruple-lift circuit** is shown in Fig. 17.20a. The typical output voltage and current waveforms are shown in Fig. 17.20b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.20c,d. Its output voltage and current are:

$$V_O = \frac{4}{1-k}V_I \quad \text{and} \quad I_O = \frac{1-k}{4}I_I$$

The voltage-transfer gain in the continuous mode is

$$M_Q = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{4}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{8M_Q}\frac{1}{f^2 C_O L_2}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L

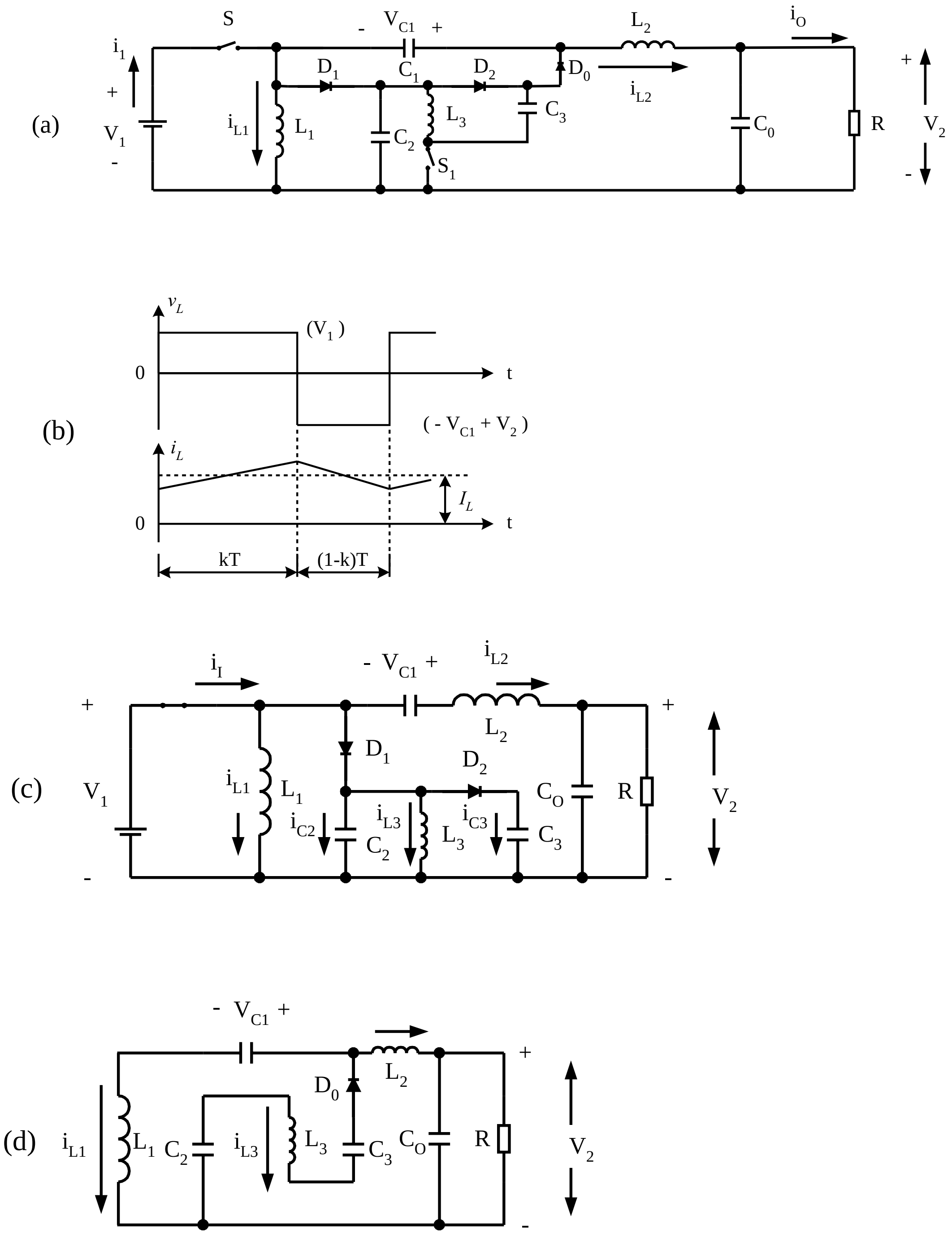

(a)
S
- V_{C1} +
L_2
i_O
i_1
+
V_1
-
D_1
C_1
D_2
D_0
i_{L2}
i_{L1}
L_1
C_2
L_3
C_3
S_1
C_0
R
+
V_2
-
(b)
v_L
(V_1)
0
t
$(-V_{C1}+V_2)$
i_L
I_L
0
t
kT
(1-k)T
(c)
i_I
- V_{C1} +
i_{L2}
+
V_1
-
L_2
D_1
D_2
i_{L1}
L_1
i_{C2}
C_2
i_{L3}
L_3
i_{C3}
C_3
C_O
R
+
V_2
-
(d)
- V_{C1} +
D_0
L_2
i_{L1}
L_1
C_2
i_{L3}
L_3
C_3
C_O
R
+
V_2
-

FIGURE 17.18 Positive output Luo re-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

is small, and the load current is high. The condition for the discontinuous mode is

$$M_Q \le \sqrt{2kz_N}$$

The output voltage in the discontinuous mode is

$$V_O = \left[4 + k^2(1-k)\frac{R}{2fL}\right]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{2r}{fL}} \ge \frac{4}{1-k}$$

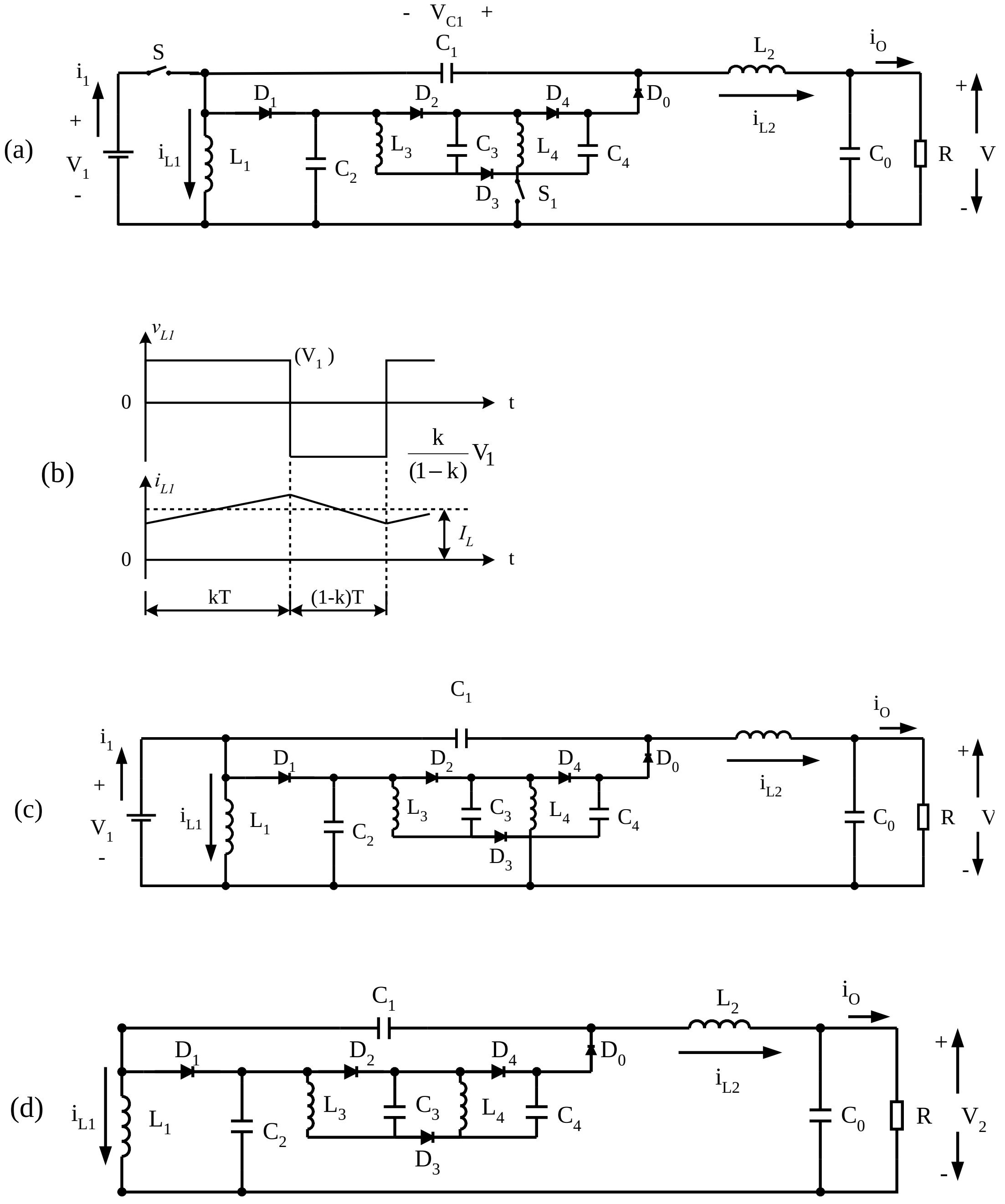

(a)
- V_C1 +
C1
S
i1
+
V1
-
iL1
L1
D1
C2
D2
L3
C3
D3
L4
S1
D4
C4
D0
L2
iL2
iO
C0
R
+
V
-
(b)
v_L1
(V1)
0
t
k/(1−k) V1
i_L1
I_L
kT
(1-k)T
(c)
(d)
V2

FIGURE 17.19 Positive output Luo triple-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

Summary for all **P/O Luo**-converters:

$$M = \frac{V_O}{V_I} = \frac{I_I}{I_O} \quad L = \frac{L_1 L_2}{L_1 + L_2} \quad z_N = \frac{R}{fL} \quad R = \frac{V_O}{I_O}$$

To write common formulas for all circuits parameters, we define that subscript $j = 0$ for the elementary circuit, $j = 1$ for the self-lift circuit, $j = 2$ for the re-lift circuit, $j = 3$ for the triple-lift circuit, $j = 4$ for the quadruple-lift circuit, and so on. The voltage-transfer gain is

$$M_j = \frac{k^{h(j)}[j + h(j)]}{1 - k}$$

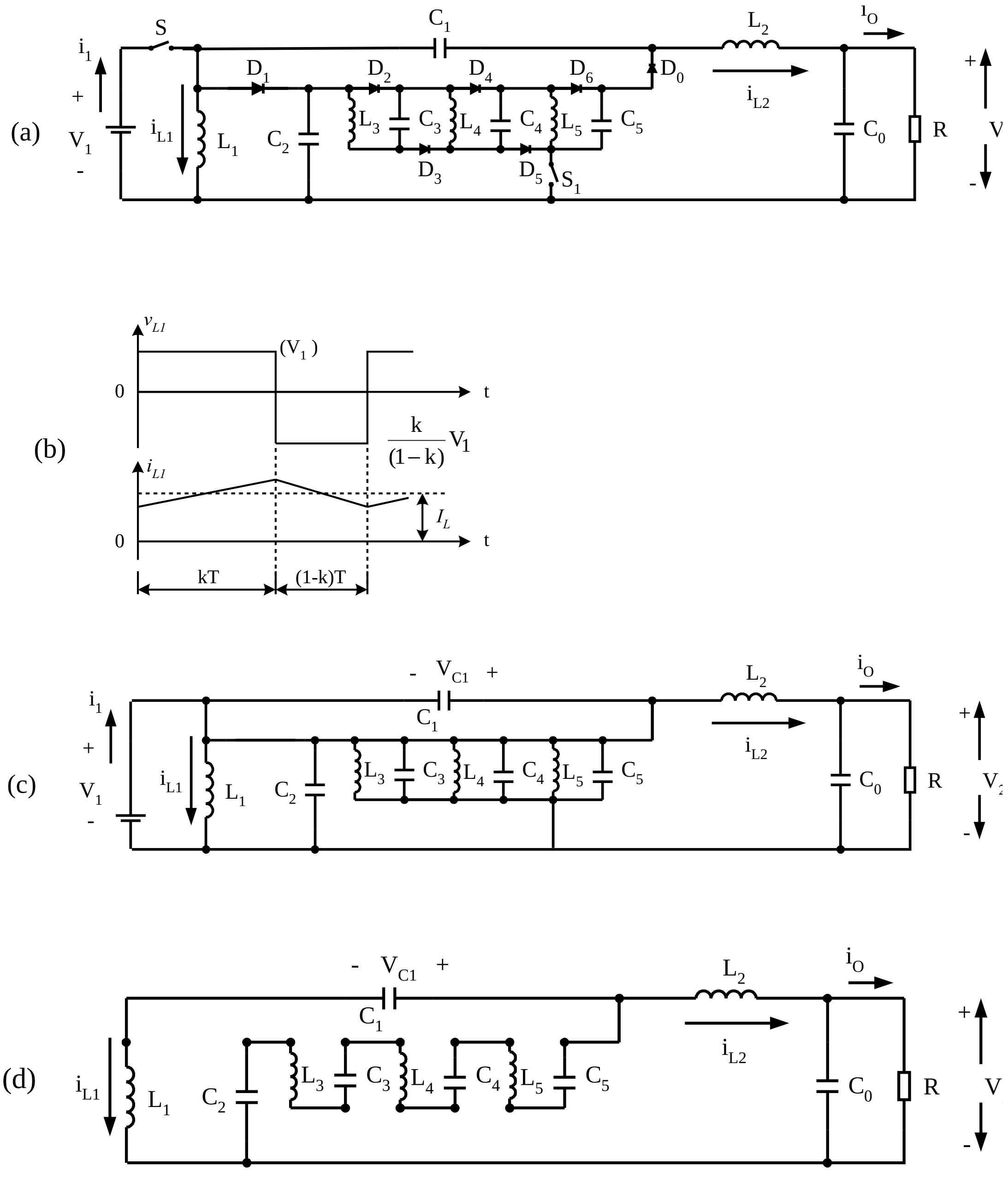

(a)
S
i_1
+
V_1
-
i_{L1}
L_1
C_2
D_1
D_2
L_3
C_3
D_3
D_4
L_4
C_4
D_5
S_1
D_6
L_5
C_5
C_1
D_0
L_2
i_{L2}
i_O
C_0
R
+
V
-
(b)
v_{L1}
(V_1)
0
t
$\frac{k}{(1-k)}V_1$
i_{L1}
I_L
0
t
kT
(1-k)T
(c)
i_1
+
V_1
-
i_{L1}
L_1
C_2
- V_{C1} +
C_1
L_3
C_3
L_4
C_4
L_5
C_5
L_2
i_{L2}
i_O
C_0
R
+
V
-
(d)
i_{L1}
L_1
C_2
- V_{C1} +
C_1
L_3
C_3
L_4
C_4
L_5
C_5
L_2
i_{L2}
i_O
C_0
R
+
V
-

FIGURE 17.20 Positive output Luo quadruple-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

The variation ratio of the output voltage is

$$\varepsilon_j = \frac{\Delta v_O/2}{V_O} = \frac{k}{8M_j}\frac{1}{f^2 C_O L_2}$$

The condition for the discontinuous mode is

$$\frac{k^{[1+h(j)]}}{M_j^2}\frac{j+h(j)}{2}z_N \geq 1$$

The output voltage in the discontinuous mode is

$$V_{O-j} = \left\{ j + k^{[2-h(j)]}\frac{1-k}{2}z_N \right\} V_I$$

where

$$h(j) = \begin{cases} 0 & if \quad j \geq 1 \\ 1 & if \quad j = 0 \end{cases}$$

is the **Hong** function.

17.2.6 Simplified Positive Output Luo-Converters

By carefully checking the P/O Luo-converters we can see that there are two switches required from the re-lift circuit. In order to use only one switch in all P/O Luo-converters, we modify the circuits. In this section we introduce the following four circuits:

- simplified self-lift circuit;
- simplified re-lift circuit;
- simplified triple-lift circuit; and the
- simplified quadruple-lift circuit.

An additional lift circuit can be derived from the forementioned circuits. In all S P/O Luo-Converters, we define

$$z_N = \frac{R}{fL}$$

normalized impedance.

The **S P/O Luo self-lift circuit** is shown in Fig. 17.13a. The typical output voltage and current waveforms are shown in Fig. 17.13b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.13c,d. Its output voltage and current are

$$V_O = \frac{1}{1-k} V_I \quad \text{and} \quad I_O = (1-k) I_I$$

The voltage-transfer gain in the continuous mode is

$$M_S = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128} \frac{1}{f^3 L_O C_1 C_O R}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_S \leq \sqrt{k} \sqrt{\frac{z_N}{2}}$$

The output voltage in the discontinuous mode is

$$V_O = \left[1 + k^2 (1-k) \frac{R}{2fL}\right] V_I \quad \text{with} \quad \sqrt{k} \sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k}$$

The **S P/O Luo re-lift circuit** is shown in Fig. 17.21a. The typical output voltage and current waveforms are shown in Fig. 17.21b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.21c,d. Its output voltage and current are

$$V_O = \frac{2}{1-k} V_I \quad \text{and} \quad I_O = \frac{1-k}{2} I_I$$

The voltage-transfer gain in the continuous mode is

$$M_R = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{2}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128} \frac{1}{f^3 L_O C_1 C_O R}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_R \leq \sqrt{k z_N}$$

The output voltage in the discontinuous mode is

$$V_O = \left[2 + k^2 (1-k) \frac{R}{2fL}\right] V_I \quad \text{with} \quad \sqrt{k} \sqrt{\frac{R}{fL}} \geq \frac{2}{1-k}$$

The **S P/O Luo triple-lift circuit** is shown in Fig. 17.22a. The typical output voltage and current waveforms are shown in Fig. 17.22b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.22c,d. Its output voltage and current are

$$V_O = \frac{3}{1-k} V_I \quad \text{and} \quad I_O = \frac{1-k}{3} I_I$$

The voltage-transfer gain in the continuous mode is

$$M_T = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{3}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128} \frac{1}{f^3 L_O C_1 C_O R}$$

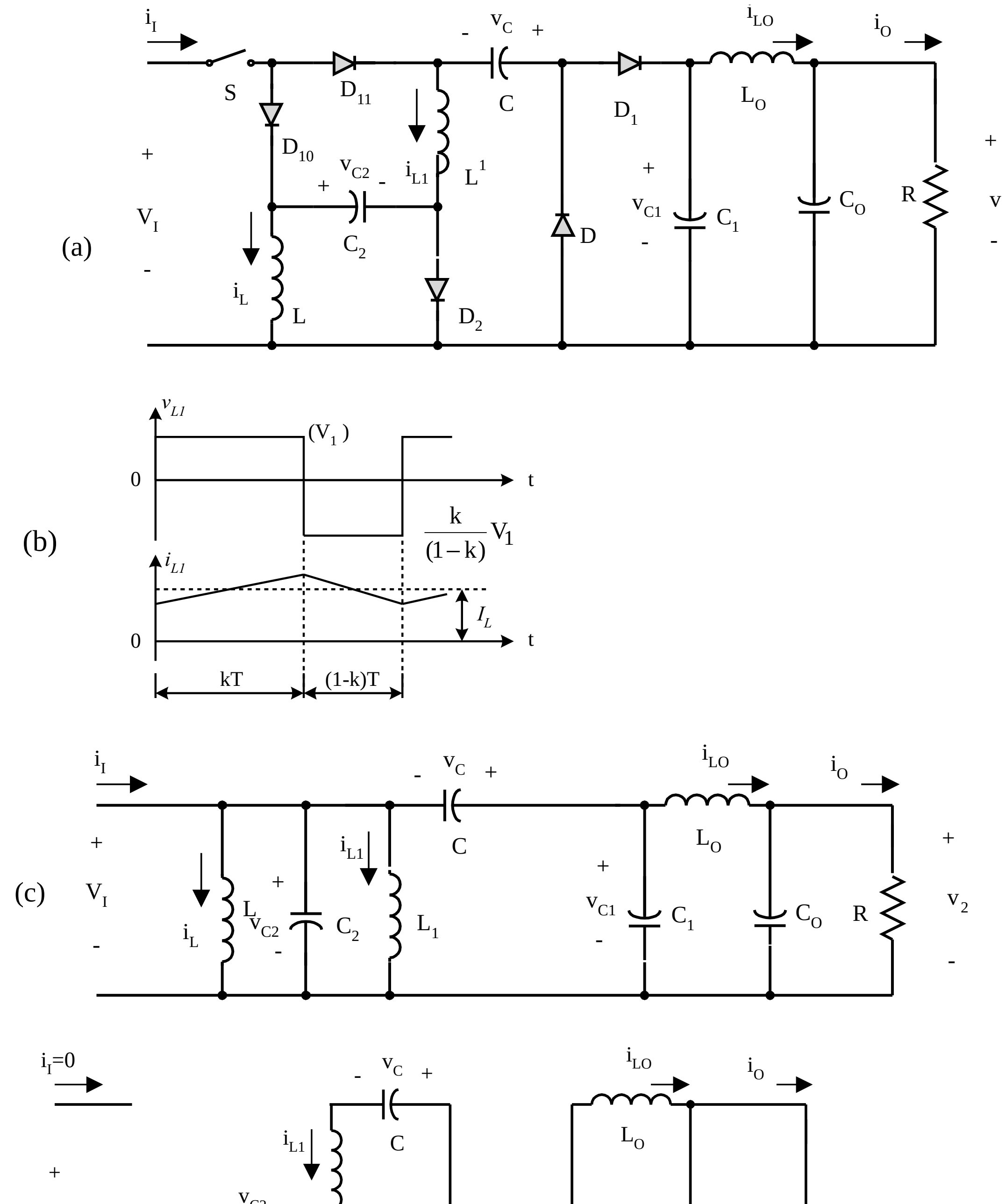

(a)
i_I
S
D_{11}
v_C
C
i_{LO}
i_O
D_{10}
v_{C2}
i_{L1}
L^1
C_2
V_I
i_L
L
D_2
D
D_1
L_O
v_{C1}
C_1
C_O
R
v
(b)
v_{L1}
(V_1)
0
t
$\frac{k}{(1-k)}V_1$
i_{L1}
I_L
kT
(1-k)T
(c)
i_I
V_I
i_L
L
v_{C2}
C_2
i_{L1}
L_1
v_C
C
i_{LO}
L_O
i_O
v_{C1}
C_1
C_O
R
v_2
(d)
i_I=0
V_I
i_L
L
v_{C2}
C_2
i_{L1}
L_1
v_C
C
i_{LO}
L_O
i_O
v_{C1}
C_1
C_O
R
v_2

FIGURE 17.21 Simplified positive output Luo re-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

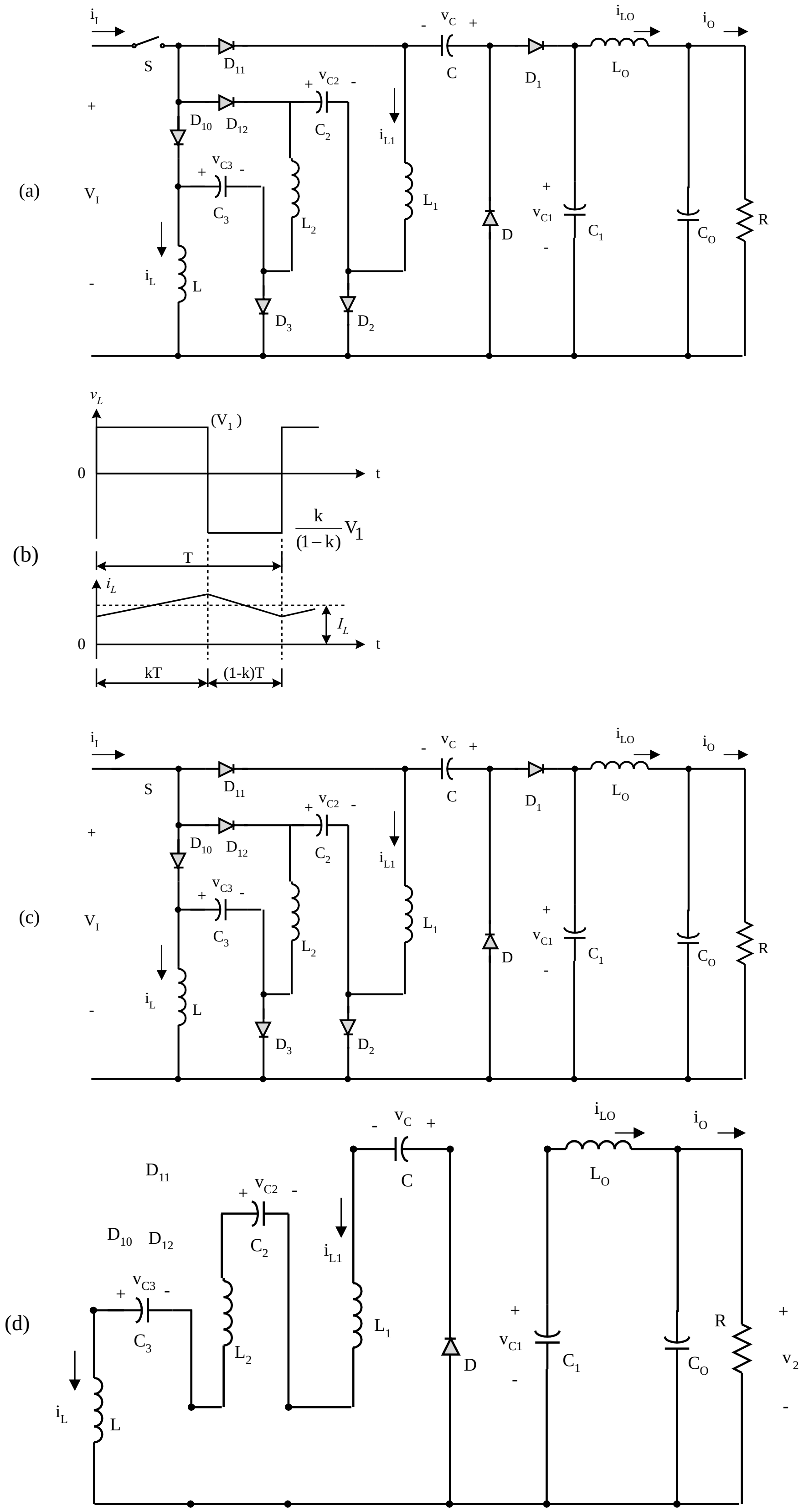

(a)
i_I
S
+
V_I
-
D_{11}
D_{10}
D_{12}
v_{C2}
C_2
v_{C3}
C_3
i_L
L
L_2
D_3
D_2
i_{L1}
L_1
v_C
C
D
D_1
v_{C1}
C_1
i_{LO}
L_O
i_O
C_O
R
(b)
v_L
(V_1)
0
t
$\frac{k}{(1-k)}V_1$
T
i_L
I_L
kT
(1-k)T
(c)
(d)
v_2

FIGURE 17.22 Simplified positive output Luo triple-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_T \leq \sqrt{\frac{3kz_N}{2}}$$

The output voltage in the discontinuous mode is

$$V_O = \left[3 + k^2(1-k)\frac{R}{2fL}\right]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{3R}{2fL}} \geq \frac{3}{1-k}$$

The **S P/O Luo quadruple-lift circuit** is shown in Fig. 17.23a. The typical output voltage and current waveforms are shown in Fig. 17.23b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.23c,d. Its output voltage and current are

$$V_O = \frac{4}{1-k}V_I \quad \text{and} \quad I_O = \frac{1-k}{4}I_I$$

The voltage-transfer gain in the continuous mode is

$$M_Q = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{4}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128}\frac{1}{f^3 L_O C_1 C_O R}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_Q \leq \sqrt{2kz_N}$$

The output voltage in the discontinuous mode is

$$V_O = \left[4 + k^2(1-k)\frac{R}{2fL}\right]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{2R}{fL}} \geq \frac{4}{1-k}$$

Summary for all **S P/O Luo**-converters:

$$M = \frac{V_O}{V_I} = \frac{I_I}{I_O} \qquad z_N = \frac{R}{fL} \qquad R = \frac{V_O}{I_O}$$

To write common formulas for all circuit parameters, we define that subscript $j = 1$ for the self-lift circuit, $j = 2$ for the re-lift circuit, $j = 3$ for the triple-lift circuit, $j = 4$ for the quadruple-lift circuit, and so on. The voltage-transfer gain is

$$M_j = \frac{j}{1-k}$$

The variation ratio of the output voltage is

$$\varepsilon_j = \frac{\Delta v_O/2}{V_O} = \frac{k}{128}\frac{1}{f^3 L_O C_1 C_O R}$$

The condition for the discontinuous mode is

$$M_j \leq \sqrt{\frac{jkz_N}{2}}$$

The output voltage in the discontinuous mode is

$$V_{O-j} = \left[j + k^2(1-k)\frac{z_N}{2}\right]V_I$$

Using these circuits is easy to convert a 24-V input source voltage into a 1000-V output load-voltage. Some applications in insulation testing have been reported.

17.3 Negative Output Luo-Converters

The **N/O Luo-converters** perform voltage conversion from positive to negative voltages using the voltage-lift technique. They work in the third quadrant with large voltage amplification, and their voltage-transfer gain is high. Five circuits are introduced in the literature. They are:

- elementary circuit;
- self-lift circuit;
- re-lift circuit;
- triple-lift circuit; and
- quadruple-lift circuit.

An additional lift circuit can be derived from the forementioned circuits. In all N/O Luo-Converters, we define normalized impedance

$$z_N = \frac{R}{fL}$$

The **N/O Luo elementary circuit** is shown in Fig. 17.5a. The typical output voltage and current waveforms are shown in Fig. 17.5b. The equivalent circuits during switch-on and

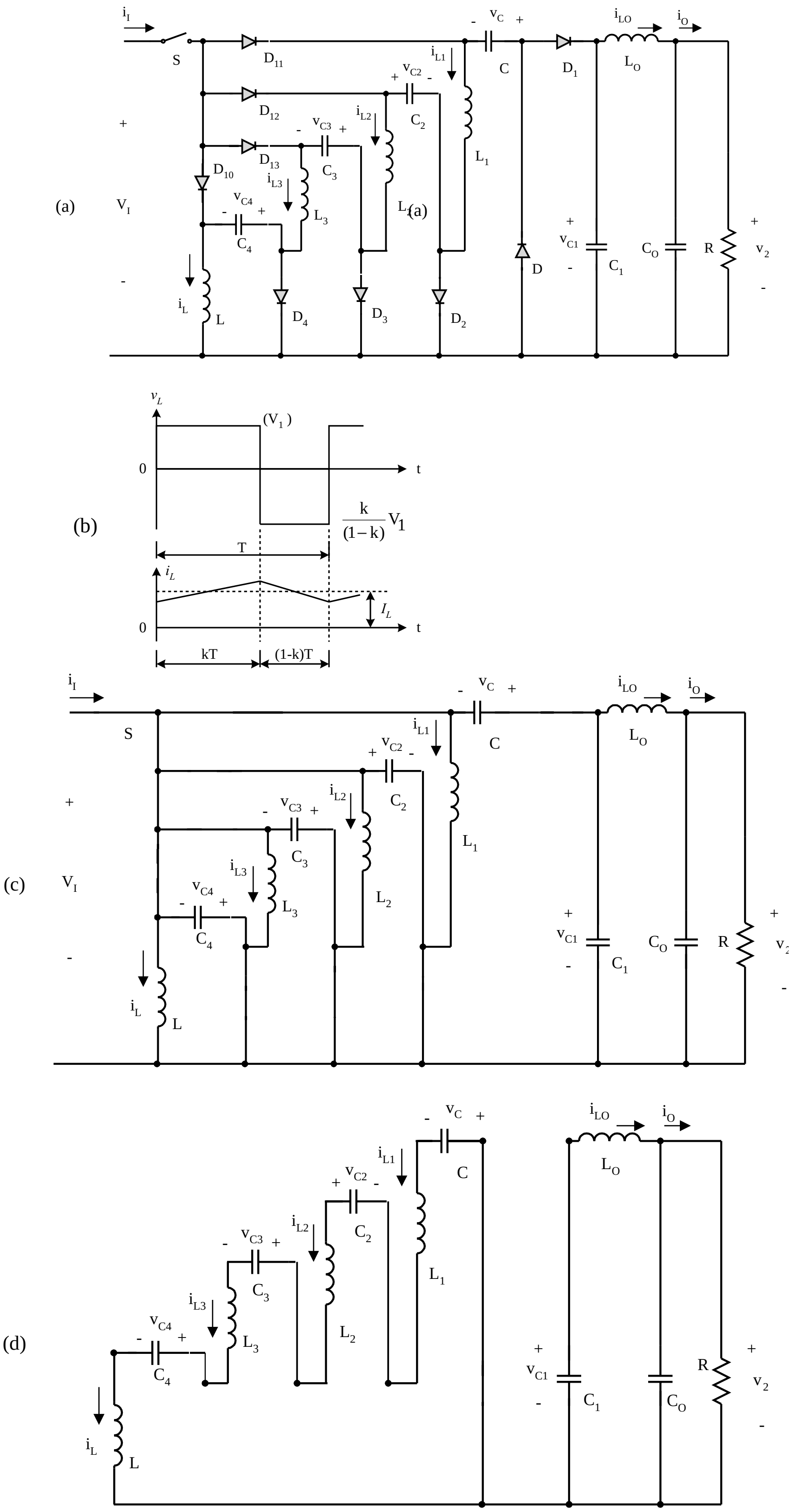

(a)
i_I
S
D_{11}
D_{12}
D_{13}
D_{10}
+
V_I
-
v_C
C
i_{L1}
v_{C2}
C_2
L_1
v_{C3}
i_{L2}
C_3
L_2
i_{L3}
v_{C4}
C_4
L_3
i_L
L
D_4
D_3
D_2
D
D_1
i_{LO}
L_O
i_O
v_{C1}
C_1
C_O
R
v_2
(b)
v_L
(V_1)
0
t
$\frac{k}{(1-k)}V_1$
T
i_L
I_L
kT
(1-k)T
(c)
(d)

FIGURE 17.23 Simplified positive output Luo quadruple-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

switch-off periods are shown in Fig. 17.5c,d. Its output voltage and current (the absolute value) are

$$V_O = \frac{k}{1-k} V_I \quad \text{and} \quad I_O = \frac{1-k}{k} I_I$$

When k is greater than 0.5, the output voltage can be higher than the input voltage.

The voltage-transfer gain in the continuous mode is

$$M_E = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{k}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128} \frac{1}{f^3 C C_O L_O R}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_E \leq k \sqrt{\frac{z_N}{2}}$$

The output voltage in the discontinuous mode is

$$V_O = k(1-k) \frac{R}{2fL} V_I \quad \text{with} \quad \sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k}$$

The **N/O Luo self-lift circuit** is shown in Fig. 17.14a. The typical output voltage and current waveforms are shown in Fig. 17.14b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.14c,d. Its output voltage and current (the absolute value) are

$$V_O = \frac{1}{1-k} V_I \quad \text{and} \quad I_O = (1-k) I_I$$

The voltage-transfer gain in the continuous mode is

$$M_S = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{1}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128} \frac{1}{f^3 C C_O L_O R}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_S \leq \sqrt{k} \sqrt{\frac{z_N}{2}}$$

The output voltage in the discontinuous mode is

$$V_O = \left[1 + k^2(1-k) \frac{R}{2fL} \right] V_I \quad \text{with} \quad \sqrt{k} \sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k}$$

The **N/O Luo re-lift circuit** is shown in Fig. 17.24a. The typical output voltage and current waveforms are shown in Fig. 17.24b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.24c,d. Its output voltage and current (the absolute value) are

$$V_O = \frac{2}{1-k} V_I \quad \text{and} \quad I_O = \frac{1-k}{2} I_I$$

The voltage-transfer gain in the continuous mode is

$$M_R = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{2}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128} \frac{1}{f^3 C C_O L_O R}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_R \leq \sqrt{k z_N}$$

The output voltage in the discontinuous mode is

$$V_O = \left[2 + k^2(1-k) \frac{R}{2fL} \right] V_I \quad \text{with} \quad \sqrt{k} \sqrt{\frac{R}{fL}} \geq \frac{2}{1-k}$$

The **N/O Luo triple-lift circuit** is shown in Fig. 17.25a. The typical output voltage and current waveforms are shown in Fig. 17.25b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.25c,d. Its output voltage and current (the absolute value) are

$$V_O = \frac{3}{1-k} V_I \quad \text{and} \quad I_O = \frac{I-k}{3} I_I$$

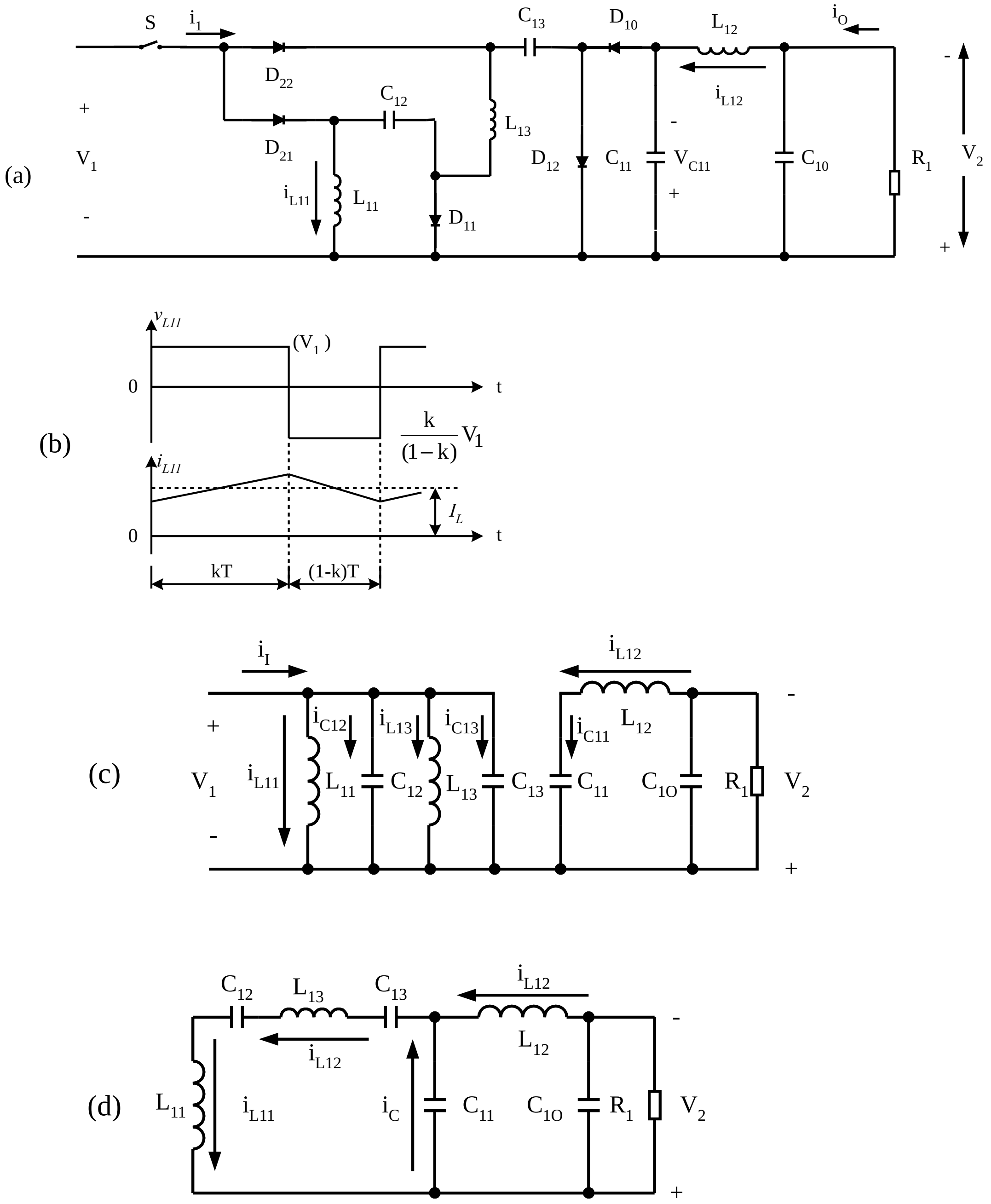

(a)
S
i_1
D_{22}
D_{21}
C_{12}
C_{13}
L_{13}
D_{10}
L_{12}
i_O
i_{L12}
D_{12}
C_{11}
V_{C11}
C_{10}
R_1
V_2
V_1
i_{L11}
L_{11}
D_{11}
+
-
(b)
v_{L11}
(V_1)
0
t
$\frac{k}{(1-k)}V_1$
i_{L11}
I_L
kT
(1-k)T
(c)
i_I
i_{L12}
V_1
i_{L11}
i_{C12}
L_{11}
C_{12}
i_{L13}
L_{13}
i_{C13}
C_{13}
i_{C11}
C_{11}
L_{12}
C_{1O}
R_1
V_2
(d)
C_{12}
L_{13}
C_{13}
i_{L12}
L_{12}
L_{11}
i_{L11}
i_C
C_{11}
C_{1O}
R_1
V_2

FIGURE 17.24 Negative output Luo re-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

The voltage-transfer gain in the continuous mode is

$$M_T = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{3}{1-k}$$

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128}\frac{1}{f^3 C C_O L_O R}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_T \leq \sqrt{\frac{3kz_N}{2}}$$

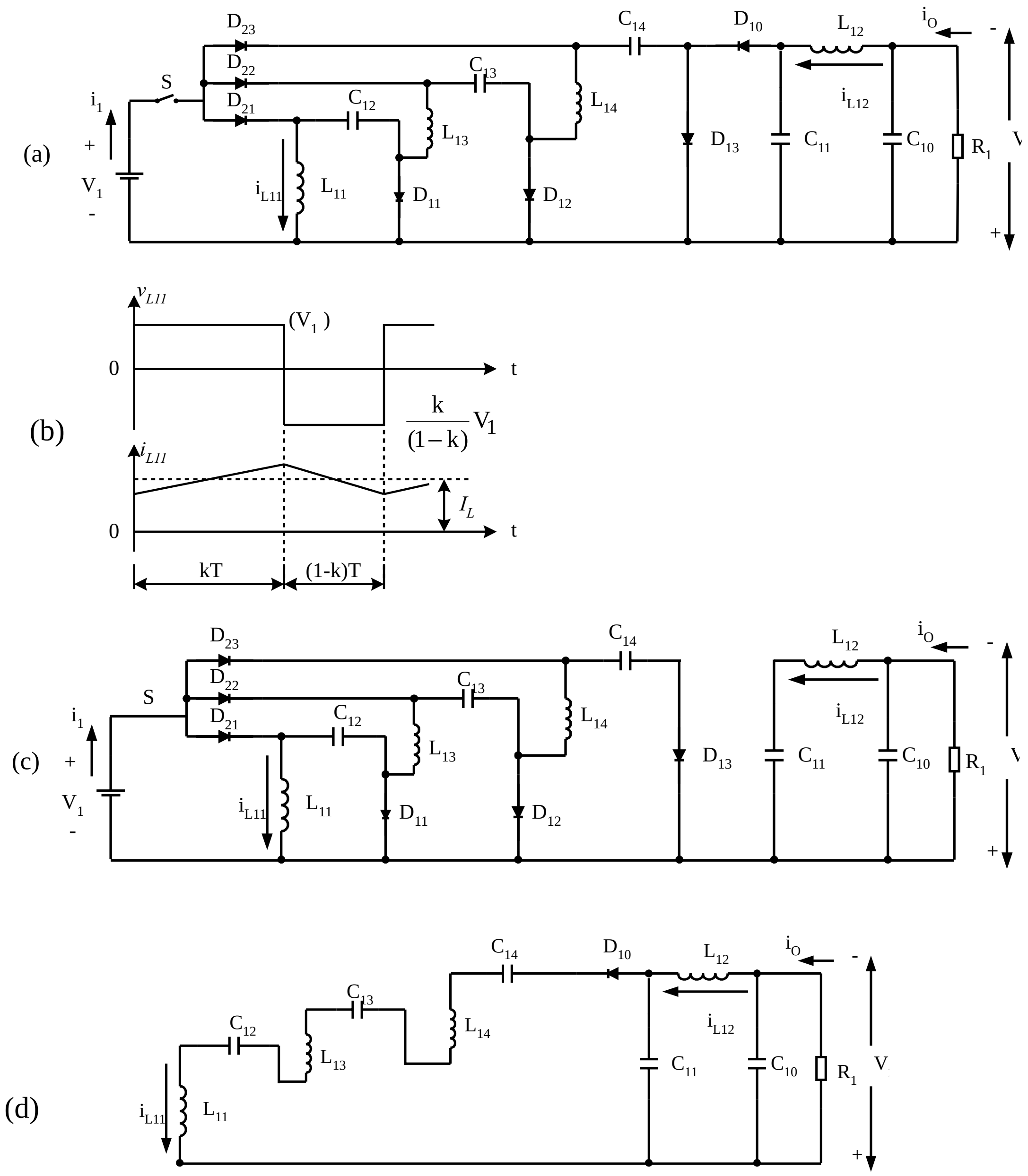

(a)
i1
+
V1
-
S
D23
D22
D21
C12
C13
C14
D10
L12
iO
iL12
L11
iL11
L13
L14
D11
D12
D13
C11
C10
R1
-
+
(b)
vL1I
(V1)
0
t
k/(1−k) V1
iL1I
IL
0
t
kT
(1-k)T
(c)
(d)

FIGURE 17.25 Negative output Luo triple-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

The output voltage in the discontinuous mode is

$$V_O = \left[3 + k^2(1-k)\frac{R}{2fL}\right]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{3R}{2fL}} \geq \frac{3}{1-k}$$

The **N/O Luo quadruple-lift circuit** is shown in Fig. 17.26a. The typical output voltage and current waveforms are shown in Fig. 17.26b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.26c,d. Its output voltage and current (the absolute value) are

$$V_O = \frac{4}{1-k}V_I \quad \text{and} \quad I_O = \frac{1-k}{4}I_I$$

The voltage-transfer gain in the continuous mode is

$$M_Q = \frac{V_O}{V_I} = \frac{I_I}{I_O} = \frac{4}{1-k}$$

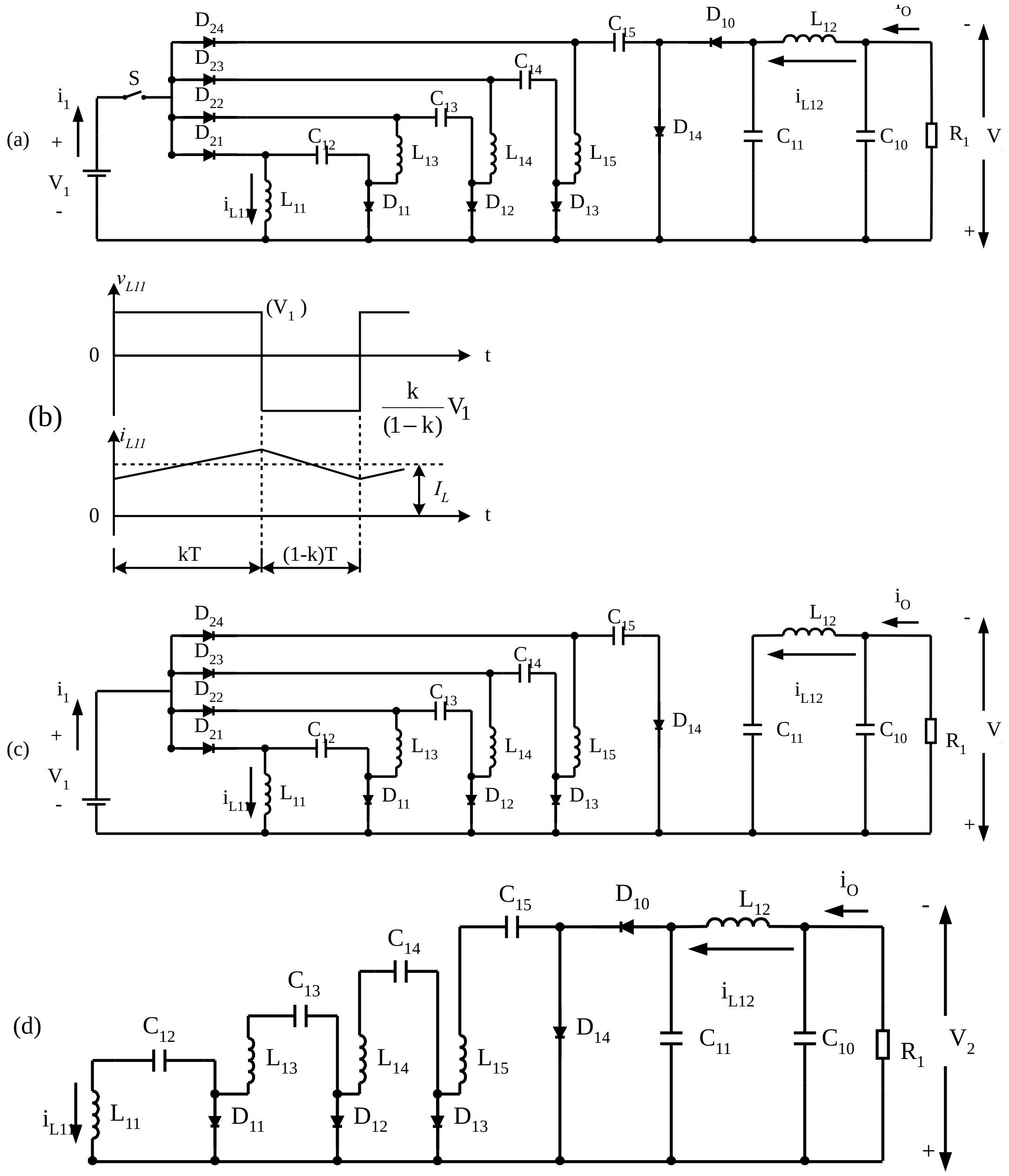

(a)
S
i_1
+
V_1
-
D_{24}
D_{23}
D_{22}
D_{21}
C_{12}
C_{13}
C_{14}
C_{15}
L_{11}
i_{L11}
L_{13}
L_{14}
L_{15}
D_{11}
D_{12}
D_{13}
D_{14}
D_{10}
L_{12}
i_{L12}
i_O
C_{11}
C_{10}
R_1
V
(b)
v_{L11}
(V_1)
0
t
$\frac{k}{(1-k)}V_1$
i_{L11}
I_L
kT
(1-k)T
(c)
(d)
V_2

FIGURE 17.26 Negative output Luo quadruple-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

The variation ratio of the output voltage v_O in the continuous mode is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128}\frac{1}{f^3 C C_O L_O R}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_Q \le \sqrt{2kz_N}$$

The output voltage in the discontinuous mode is

$$V_O = \left[4 + k^2(1-k)\frac{R}{2fL}\right]V_I \quad \text{with} \quad \sqrt{k}\sqrt{\frac{2R}{fL}} \ge \frac{4}{1-k}$$

Summary for all **N/O Luo-converters**:

$$M = \frac{V_O}{V_I} = \frac{I_I}{I_O} \quad z_N = \frac{R}{fL} \quad R = \frac{V_O}{I_O}$$

To write common formulas for all circuits parameters, we define that subscript $j = 0$ for the elementary circuit, $j = 1$ for the self-lift circuit, $j = 2$ for the re-lift circuit, $j = 3$ for the triple-lift circuit, $j = 4$ for the quadruple-lift circuit, and so on. The voltage-transfer gain is

$$M_j = \frac{k^{h(j)}[j + h(j)]}{1 - k}$$

The variation ratio of the output voltage is

$$\varepsilon = \frac{\Delta v_O/2}{V_O} = \frac{k}{128} \frac{1}{f^3 C C_O L_O R}$$

The condition for the discontinuous mode is

$$\frac{k^{[1+h(j)]}}{M_j^2} \frac{j + h(j)}{2} z_N \geq 1$$

The output voltage in the discontinuous mode is

$$V_{O-j} = \left\{ j + k^{[2-h(j)]} \frac{1-k}{2} z_N \right\} V_I$$

where

$$h(j) = \begin{cases} 0 & if \quad j \geq 1 \\ 1 & if \quad j = 0 \end{cases}$$

is the **Hong** function.

Using these circuits it is easy to convert a 24-V input source-voltage into a −1000-V output load-voltage. Some applications in insulation testing have been reported.

17.4 Double Output Luo-Converters

Double output Luo-converters perform the voltage conversion from positive to positive and negative voltages simultaneously using the voltage-lift technique. They work in the first and third quadrants with large voltage amplification, and their voltage-transfer gain is high.

There are two groups of these converters: double output Luo-converters (**D/O Luo**-converters); and simplified double output Luo-converters (**S D/O Luo**-Converters). We will introduce them one by one.

17.4.1 Double Output Luo-Converters

Five circuits are introduced in the literature:

- elementary circuit;
- self-lift circuit;
- re-lift circuit;
- triple-lift circuit; and
- quadruple-lift circuit.

An additional lift circuit can be derived from the forementioned circuits. In all D/O Luo-converters, each circuit has two conversion paths a positive conversion path and a negative conversion path. The positive path prefers P/O Luo-converters, and the negative path prefers N/O Luo-converters. We define normalized inductance $L = L_1 L_2 / L_1 + L_2$ and normalized impedance $z_{N+} = R/fL$ for the positive path, and normalized impedance $z_{N-} = R_1/fL_{11}$ the negative path. We usually purposely select $R = R_1$ and $L = L_{11}$, so that we have $z_N = z_{N+} = z_{N-}$.

The **D/O Luo elementary circuit**, shown in Fig. 17.6a was introduced in Section 17.2.2. The typical output voltage and current waveforms are shown in Fig. 17.6b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.6c,d. Its output voltages and currents (absolute values) are:

$$V_{O+} = |V_{O-}| = \frac{k}{1-k} V_I \quad I_{O+} = \frac{1-k}{k} I_{I+}$$

and

$$I_{O-} = \frac{1-k}{k} I_{I-}$$

When k is greater than 0.5, the output voltage can be higher than the input voltage.

The voltage-transfer gain in the continuous mode is

$$M_E = \frac{V_{O+}}{V_I} = \frac{|V_{O-}|}{V_I} = \frac{k}{1-k}$$

The variation ratio of the output voltage v_{O+} in the continuous mode is

$$\varepsilon_+ = \frac{\Delta v_{O+}/2}{V_{O+}} = \frac{k}{8 M_E} \frac{1}{f^2 C_O L_2}$$

The variation ratio of the output voltage v_{O-} in the continuous mode is

$$\varepsilon_- = \frac{\Delta v_{O-}/2}{V_{O-}} = \frac{k}{128} \frac{1}{f^3 C_{11} C_{10} L_{12} R_1}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L

is small, and the load current is high. The condition for the discontinuous mode is

$$M_E \le k\sqrt{\frac{z_N}{2}}$$

The output voltages in the discontinuous mode are

$$V_O = V_{O+} = |V_{O-}| = k(1-k)\frac{z_N}{2}V_I \quad \text{with} \quad \sqrt{\frac{z_N}{2}} \ge \frac{1}{1-k}$$

A **D/O Luo self-lift circuit** is shown in Fig. 17.27a. The typical output voltage and current waveforms are shown in Fig. 17.27b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.27c,d. Its output voltages and currents (absolute values) are:

$$V_{O+} = |V_{O-}| = \frac{1}{1-k}V_I \quad I_{O+} = (1-k)I_{I+}$$

and

$$I_{O-} = (1-k)K_{I-}$$

The voltage-transfer gain in the continuous mode is

$$M_S = \frac{V_{O+}}{V_I} = \frac{|V_{O-}|}{V_I} = \frac{1}{1-k}$$

The variation ratio of the output voltage v_{O+} in the continuous mode is

$$\varepsilon_+ = \frac{\Delta v_{O+}/2}{V_{O+}} = \frac{k}{8M_S}\frac{1}{f^2 C_O L_2}$$

The variation ratio of the output voltage v_{O-} in the continuous mode is

$$\varepsilon_- = \frac{\Delta v_{O-}/2}{V_{O-}} = \frac{k}{128}\frac{1}{f^3 C_{11} C_{10} L_{12} R_1}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_S \le \sqrt{k}\sqrt{\frac{z_N}{2}}$$

The output voltages in the discontinuous mode are

$$V_O = V_{O+} = |V_{O-}| = \left[1 + k^2(1-k)\frac{z_N}{2}\right]V_I$$

with

$$\sqrt{\frac{kz_N}{2}} \ge \frac{1}{1-k}$$

A **D/O Luo re-lift circuit** is shown in Fig. 17.28a. The typical output voltage and current waveforms are shown in Fig. 17.28b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.28c,d. Its output voltages and currents (absolute values) are:

$$V_{O+} = |V_{O-}| = \frac{2}{1-k}V_I \quad I_{O+} = \frac{1-k}{2}I_{I+}$$

and

$$I_{O-} = \frac{1-k}{2}I_{I-}$$

The voltage-transfer gain in the continuous mode is

$$M_R = \frac{V_{O+}}{V_I} = \frac{|V_{O-}|}{V_I} = \frac{2}{1-k}$$

The variation ratio of the output voltage v_{O+} in the continuous mode is

$$\varepsilon_+ = \frac{\Delta v_{O+}/2}{V_{O+}} = \frac{k}{8M_R}\frac{1}{f^2 C_O L_2}$$

The variation ratio of the output voltage v_{O-} in the continuous mode is

$$\varepsilon_- = \frac{\Delta v_{O-}/2}{V_{O-}} = \frac{k}{128}\frac{1}{f^3 C_{11} C_{10} L_{12} R_1}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_R \le \sqrt{kz_N}$$

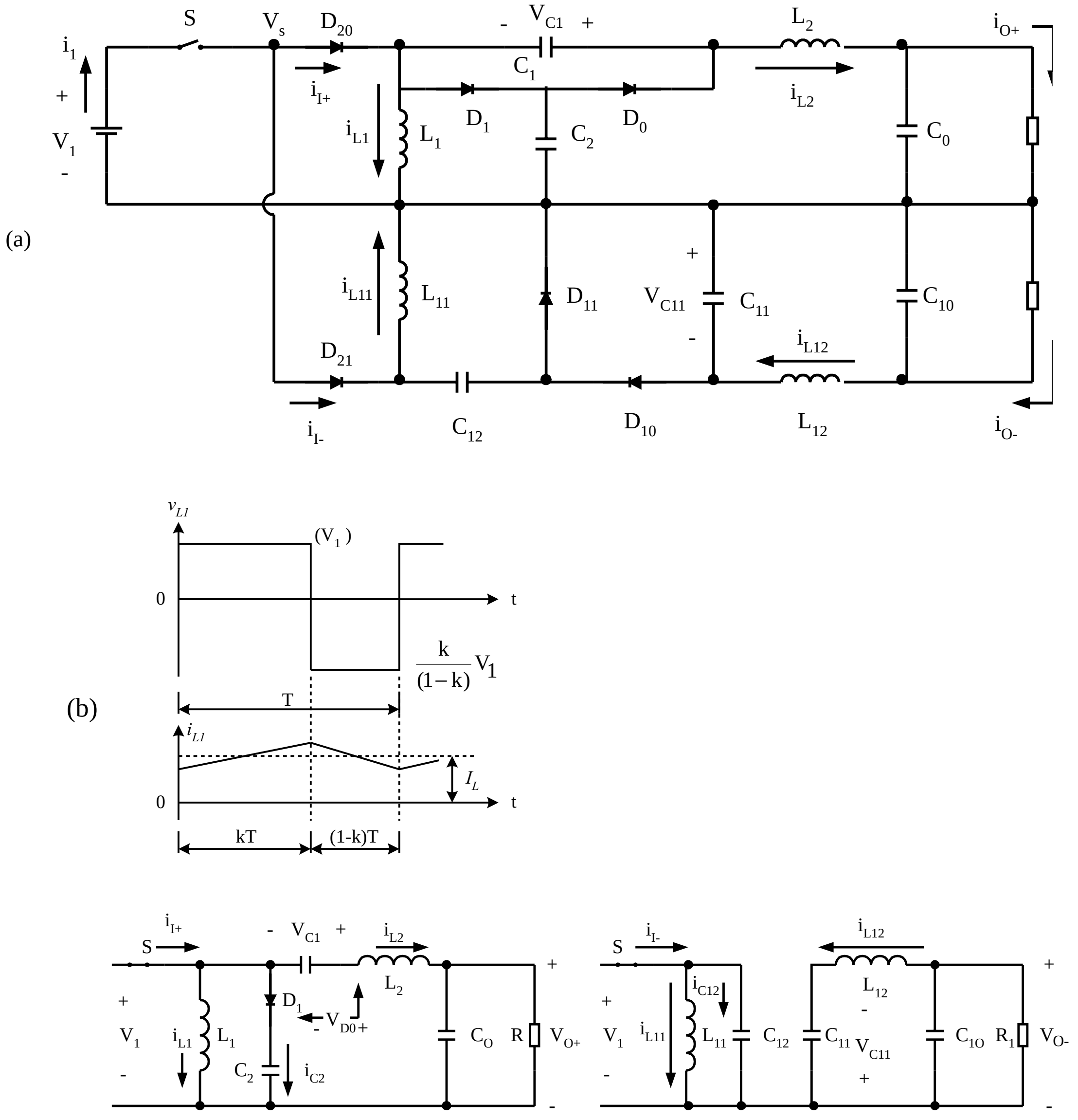
The output voltages in the discontinuous mode are

$$V_O = V_{O+} = |V_{O-}| = \left[2 + k^2(1-k)\frac{z_N}{2}[V_I]\right]$$

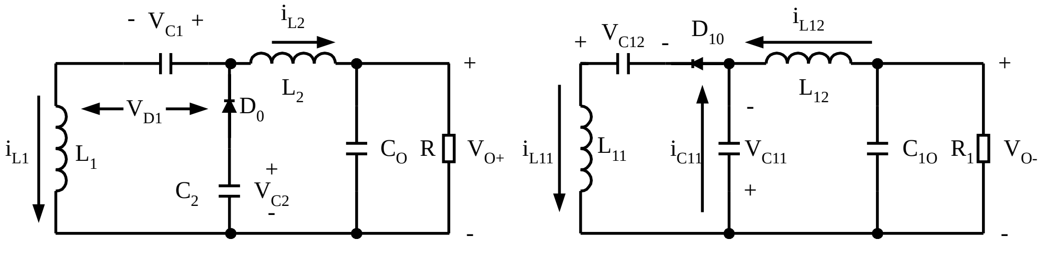
with

$$\sqrt{kz_N} \ge \frac{2}{1-k}$$

A **D/O Luo triple-lift circuit** is shown in Fig. 17.29a. The typical output voltage and current waveforms are shown in


(a)
S
V_s
D_{20}
i_1
+
V_1
-
i_{I+}
i_{L1}
L_1
D_1
- V_{C1} +
C_1
C_2
D_0
L_2
i_{L2}
i_{O+}
C_0
i_{L11}
L_{11}
D_{11}
+
V_{C11}
-
C_{11}
C_{10}
i_{L12}
D_{21}
i_{I-}
C_{12}
D_{10}
L_{12}
i_{O-}
(b)
v_{L1}
(V_1)
0
t
$\frac{k}{(1-k)}V_1$
T
i_{L1}
I_L
0
t
kT
(1-k)T
i_{I+}
S
+
V_1
-
i_{L1}
L_1
- V_{C1} +
D_1
- V_{D0} +
C_2
i_{C2}
i_{L2}
L_2
C_O
R
+
V_{O+}
-
i_{I-}
S
+
V_1
-
i_{L11}
L_{11}
i_{C12}
C_{12}
C_{11}
i_{L12}
L_{12}
-
V_{C11}
+
C_{1O}
R_1
+
V_{O-}
-

(c) S: ON; D_0, D_{10}: OFF


- V_{C1} +
i_{L2}
L_2
V_{D1}
D_0
i_{L1}
L_1
C_2
+
V_{C2}
-
C_O
R
+
V_{O+}
-
+ V_{C12} -
D_{10}
i_{L12}
L_{12}
i_{L11}
L_{11}
i_{C11}
-
V_{C11}
+
C_{1O}
R_1
+
V_{O-}
-

(d) S: OFF; D_0, D_{10}: ON

FIGURE 17.27 Double output Luo self-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

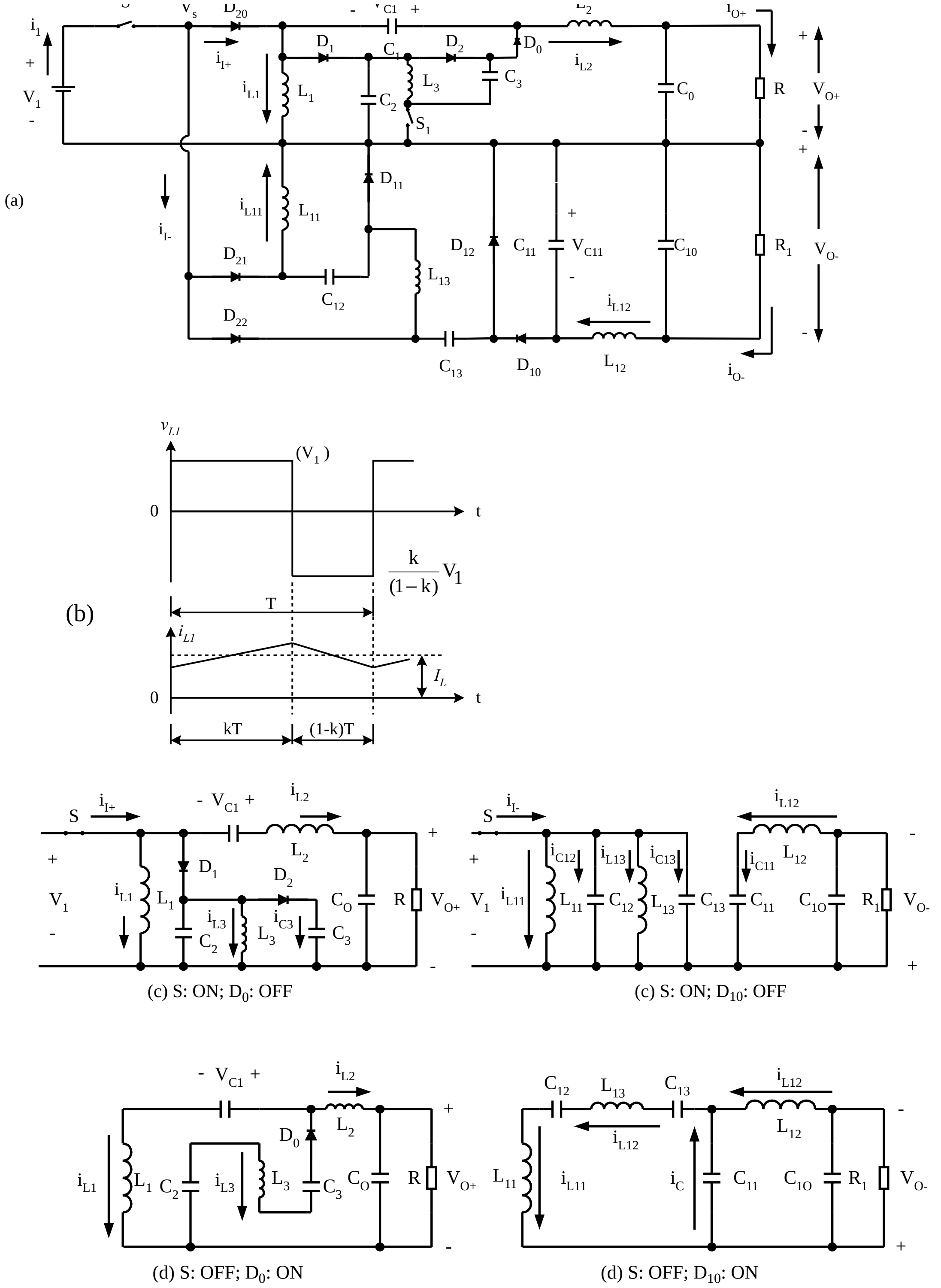

(a)
i1
+
V1
-
Vs
D20
iI+
iL1
L1
D1
- VC1 +
C1
D2
L3
C3
C2
S1
D0
L2
iL2
C0
iO+
R
+
VO+
-
+
iI-
iL11
L11
D11
D21
C12
L13
D22
C13
D12
C11
+
VC11
-
D10
iL12
L12
C10
R1
VO-
-
iO-
(b)
vL1
(V1)
0
t
k/(1−k) V1
T
iL1
IL
0
t
kT
(1-k)T
S
iI+
- VC1 +
iL2
L2
+
V1
-
iL1
L1
D1
D2
iL3
L3
iC3
C2
C3
CO
R
VO+
+
-
(c) S: ON; D0: OFF
S
iI-
iL12
L12
+
V1
-
iL11
L11
iC12
C12
iL13
L13
iC13
C13
iC11
C11
C1O
R1
VO-
-
+
(c) S: ON; D10: OFF
- VC1 +
iL2
L2
D0
iL1
L1
C2
iL3
L3
C3
CO
R
VO+
+
-
(d) S: OFF; D0: ON
C12
L13
C13
iL12
iL12
L12
L11
iL11
iC
C11
C1O
R1
VO-
-
+
(d) S: OFF; D10: ON

FIGURE 17.28 Double output Luo re-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

Fig. 17.29b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.29c,d. Its output voltages and currents (absolute values) are:

$$V_O = |V_{O-}| = \frac{3}{1-k}V_I \quad I_{O+} = \frac{1-k}{3}I_{I+}$$

and

$$I_{O-} = \frac{1-k}{3}I_{I-}$$

The voltage-transfer gain in the continuous mode is

$$M_T = \frac{V_{O+}}{V_I} = \frac{|V_{O-}|}{V_I} = \frac{3}{1-k}$$

The variation ratio of the output voltage v_{O+} in the continuous mode is

$$\varepsilon_+ = \frac{\Delta v_{O+}/2}{V_{O+}} = \frac{k}{8M_T}\frac{1}{f^2C_OL_2}$$

The variation ratio of the output voltage v_{O-} in the continuous mode is

$$\varepsilon_- = \frac{\Delta v_{O-}/2}{V_{O-}} = \frac{k}{128}\frac{1}{f^3C_{11}C_{10}L_{12}R_1}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_T \le \sqrt{\frac{3kz_N}{2}}$$

The output voltages in the discontinuous mode are

$$V_O = V_{O+} = |V_{O-}| = \left[3 + k^2(1-k)\frac{z_N}{2}\right]V_I$$

with

$$\sqrt{\frac{3kz_N}{2}} \ge \frac{3}{1-k}$$

A **D/O Luo quadruple-lift circuit** is shown in Fig. 17.30a. The typical output voltage and current waveforms are shown in Fig. 17.30b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.30c,d. Its output voltages (absolute values) are:

$$V_{O+} = |V_{O-}| = \frac{4}{1-k}V_I \quad I_{O+} = \frac{1-k}{4}I_{I+}$$

and

$$I_{O-} = \frac{1-k}{4}I_{I-}$$

The voltage-transfer gain in the continuous mode is

$$M_Q = \frac{V_{O+}}{V_I} = \frac{|V_{O-}|}{V_I} = \frac{4}{1-k}$$

The variation ratio of the output voltage v_{O+} in the continuous mode is

$$\varepsilon_+ = \frac{\Delta v_{O+}/2}{V_{O+}} = \frac{k}{8M_Q}\frac{1}{f^2C_OL_2}$$

The variation ratio of the output voltage v_{O-} in the continuous mode is

$$\varepsilon_- = \frac{\Delta v_{O-}/2}{V_{O-}} = \frac{k}{128}\frac{1}{f^3C_{11}C_{10}L_{12}R_1}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_Q \le \sqrt{2kz_N}$$

The output voltages in the discontinuous mode are

$$V_O = V_{O+} = |V_{O-}| = \left[4 + k^2(1-k)\frac{z_N}{2}\right]V_I$$

with

$$\sqrt{2kz_N} \ge \frac{4}{1-k}$$

Summary for all **D/O Luo-converters**:

$$M = \frac{V_{O+}}{V_I} = \frac{|V_{O-}|}{V_I} \quad L = \frac{L_1L_2}{L_1+L_2} \quad L = L_{11}$$

$$R = R_1 \quad z_{N+} = \frac{R}{fL} \quad z_{N-} = \frac{R_1}{fL_{11}}$$

so that

$$z_N = z_{N+} = z_{N-}.$$

To write common formulas for all circuit parameters, we define that subscript $j = 0$ for the elementary circuit, $j = 1$ for the self-lift circuit, $j = 2$ for the re-lift circuit, $j = 3$ for the

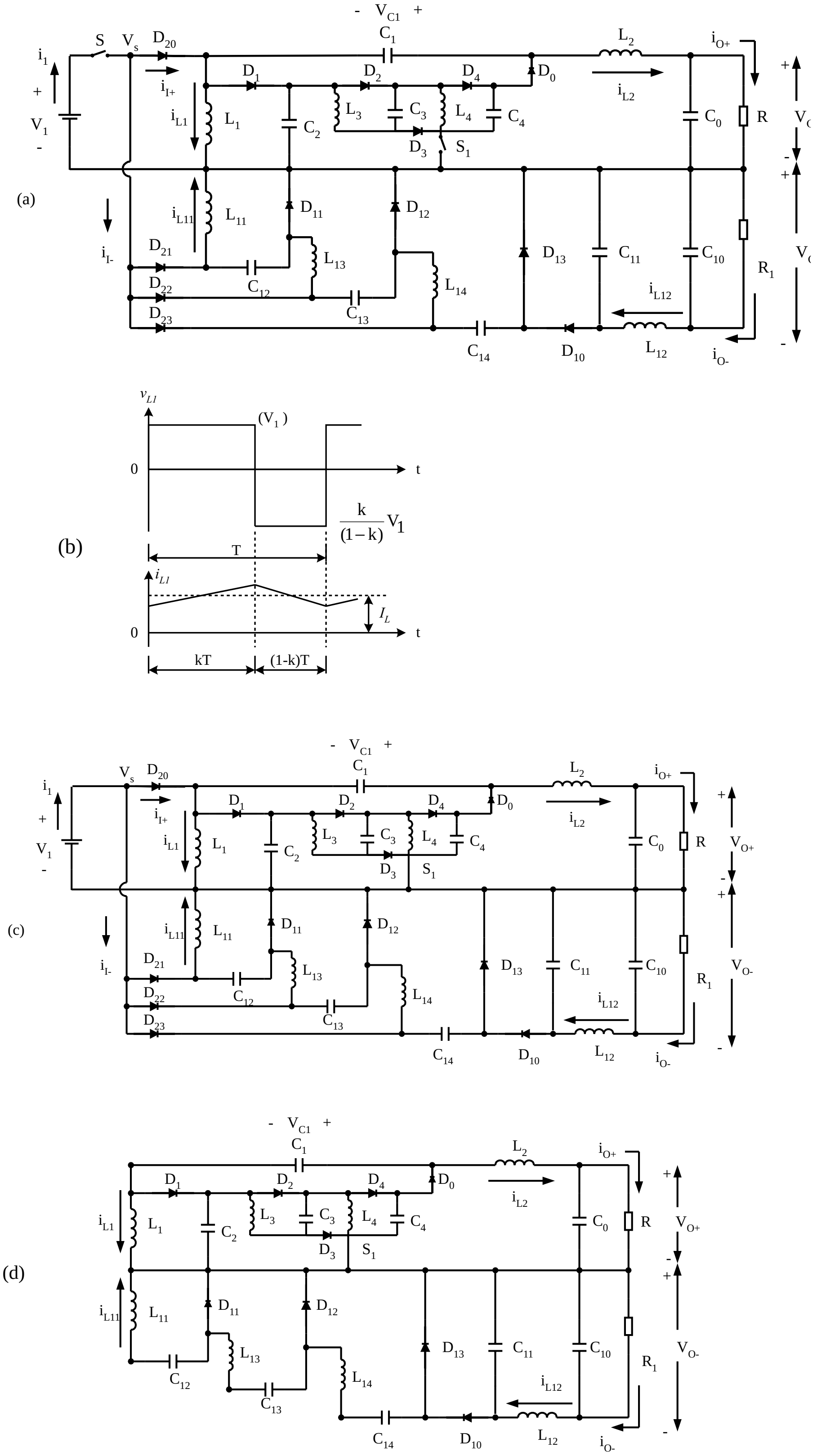

(a)
S
V_s
D_20
D_1
D_2
D_3
D_4
D_0
- V_C1 +
C_1
C_2
C_3
C_4
L_1
L_2
L_3
L_4
S_1
i_1
+
V_1
-
i_I+
i_L1
i_L2
i_O+
C_0
R
V_O
L_11
i_L11
D_11
D_12
L_13
L_14
D_21
D_22
D_23
i_I-
C_12
C_13
C_14
D_13
D_10
C_11
C_10
i_L12
L_12
R_1
i_O-
(b)
v_L1
(V_1)
0
t
k/(1-k) V_1
T
i_L1
I_L
kT
(1-k)T
(c)
V_O+
V_O-
(d)

FIGURE 17.29 Double output Luo triple-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

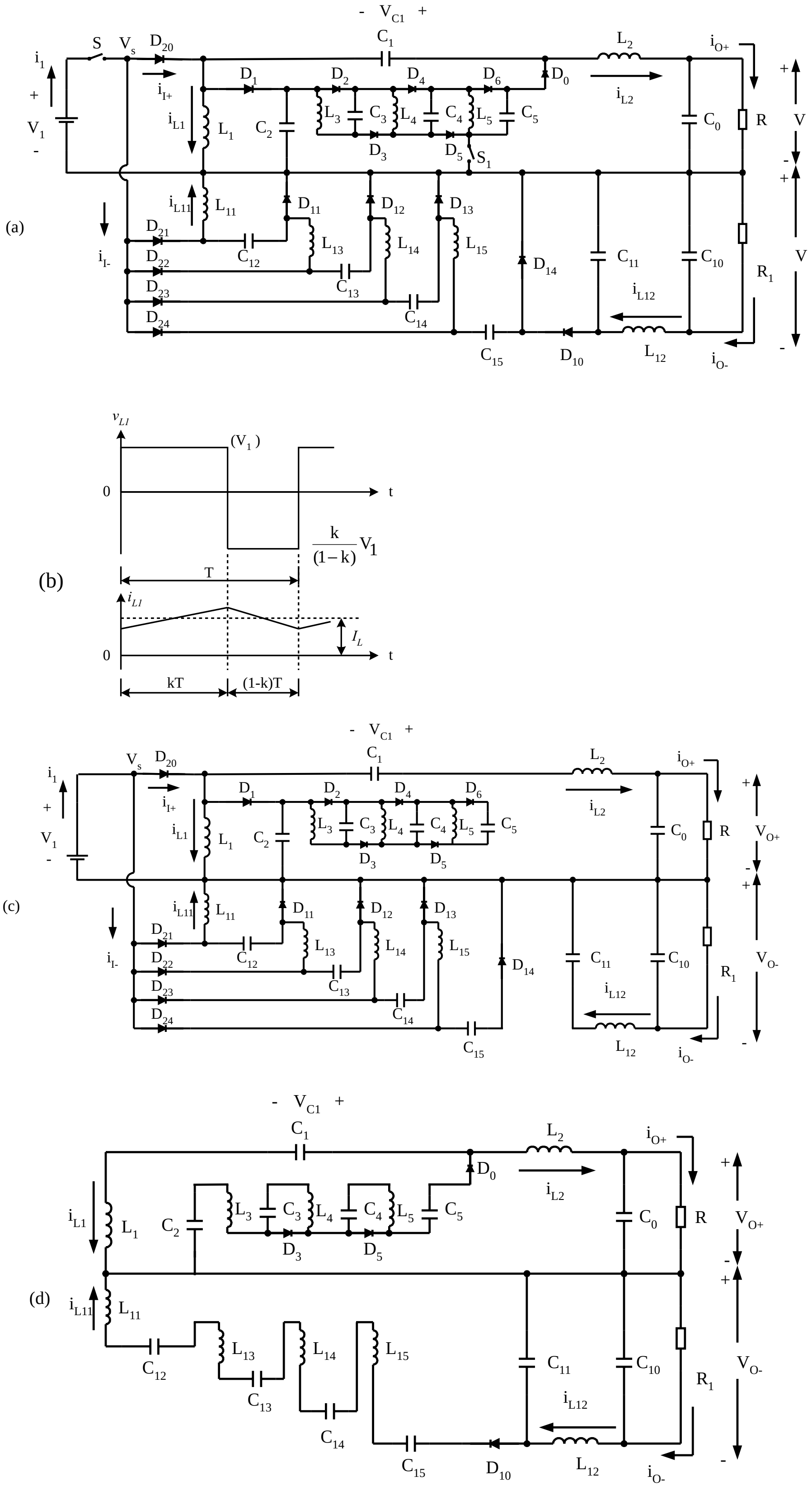

(a)
(b)
(c)
(d)
S
V_s
D_{20}
V_1
i_1
i_{I+}
i_{I-}
i_{L1}
i_{L11}
L_1
L_2
L_3
L_4
L_5
L_{11}
L_{12}
L_{13}
L_{14}
L_{15}
C_0
C_1
C_2
C_3
C_4
C_5
C_{10}
C_{11}
C_{12}
C_{13}
C_{14}
C_{15}
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_{10}
D_{11}
D_{12}
D_{13}
D_{14}
D_{21}
D_{22}
D_{23}
D_{24}
S_1
- V_{C1} +
i_{L2}
i_{L12}
i_{O+}
i_{O-}
R
R_1
V
V_{O+}
V_{O-}
v_{L1}
(V_1)
0
t
$\frac{k}{(1-k)}V_1$
T
i_{L1}
I_L
kT
(1-k)T

FIGURE 17.30 Double output Luo quadruple-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

triple-lift circuit, $j = 4$ for the quadruple-lift circuit, and so on. The voltage-transfer gain is

$$M_j = \frac{k^{h(j)}[j + h(j)]}{1 - k}$$

The variation ratio of the output voltage v_{O+} in the continuous mode is

$$\varepsilon_{+j} = \frac{\Delta v_{O+}/2}{V_{O+}} = \frac{k}{8M_j} \frac{1}{f^2 C_O L_2}$$

The variation ratio of the output voltage v_{O-} in the continuous mode is

$$\varepsilon_{-j} = \frac{\Delta v_{O-}/2}{V_{O-}} = \frac{k}{128} \frac{1}{f^3 C_{11} C_{10} L_{12} R_1}$$

The condition for the discontinuous mode is

$$\frac{k^{[1+h(j)]}}{M_j^2} \frac{j + h(j)}{2} z_N \geq 1$$

The output voltage in the discontinuous mode is

$$V_{O-j} = \left\{ j + k^{[2-h(j)]} \frac{1-k}{2} z_N \right\} V_I$$

where

$$h(j) = \begin{cases} 0 & if \quad j \geq 1 \\ 1 & if \quad j = 0 \end{cases}$$

is the **Hong** function.

Using these circuits is easy to convert a 24-V input source-voltage into a ±1000-V output load-voltage. Some applications in insulation testing have been reported.

17.4.2 Simplified Double Output Luo-Converters

By carefully checking P/O Luo-converters we can see that there are two switches required from the re-lift circuit. In order to use only one switch in all P/O Luo-converters, we modify the circuits. In this section we introduce the following four circuits:

- simplified self-lift circuit;
- simplified re-lift circuit;
- simplified triple-lift circuit; and
- simplified quadruple-lift circuit.

An additional lift circuit can be derived from the forementioned circuits. In all S P/O Luo-converters, we define normalized impedance as $z_{N+} = r/fL_1$ for the positive path and normalized impedance as $z_{N-} = R_1/fL_{11}$ for the negative path. We usually select $R = R_1$ and $L_1 = L_{11}$, so that we have $z_N = z_{N+} = z_{N-}$.

The **S D/O Luo self-lift circuit** is shown in Fig. 17.31a. The typical output voltage and current waveforms are shown in Fig. 17.31b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.31c,d. Its output voltages and currents (absolute values) are:

$$V_{O+} = |V_{O-}| = \frac{1}{1-k} V_I \quad I_{O+} = (1-k) I_{I+}$$

and

$$I_{O-} = (1-k) I_{I-}$$

The voltage-transfer gain in the continuous mode is

$$M_S = \frac{V_{O+}}{V_I} = \frac{|V_{O-}|}{V_I} = \frac{1}{1-k}$$

The variation ratio of the output voltage v_{O+} in the continuous mode is

$$\varepsilon_+ = \frac{\Delta v_{O+}/2}{V_{O+}} = \frac{k}{128} \frac{1}{f^3 C_2 C_O L_2 R}$$

The variation ratio of the output voltage v_{O-} in the continuous mode is

$$\varepsilon_- = \frac{\Delta v_{O-}/2}{V_{O-}} = \frac{k}{128} \frac{1}{f^3 C_{11} C_{10} L_{12} R_1}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_S \leq \sqrt{k} \sqrt{\frac{z_N}{2}}$$

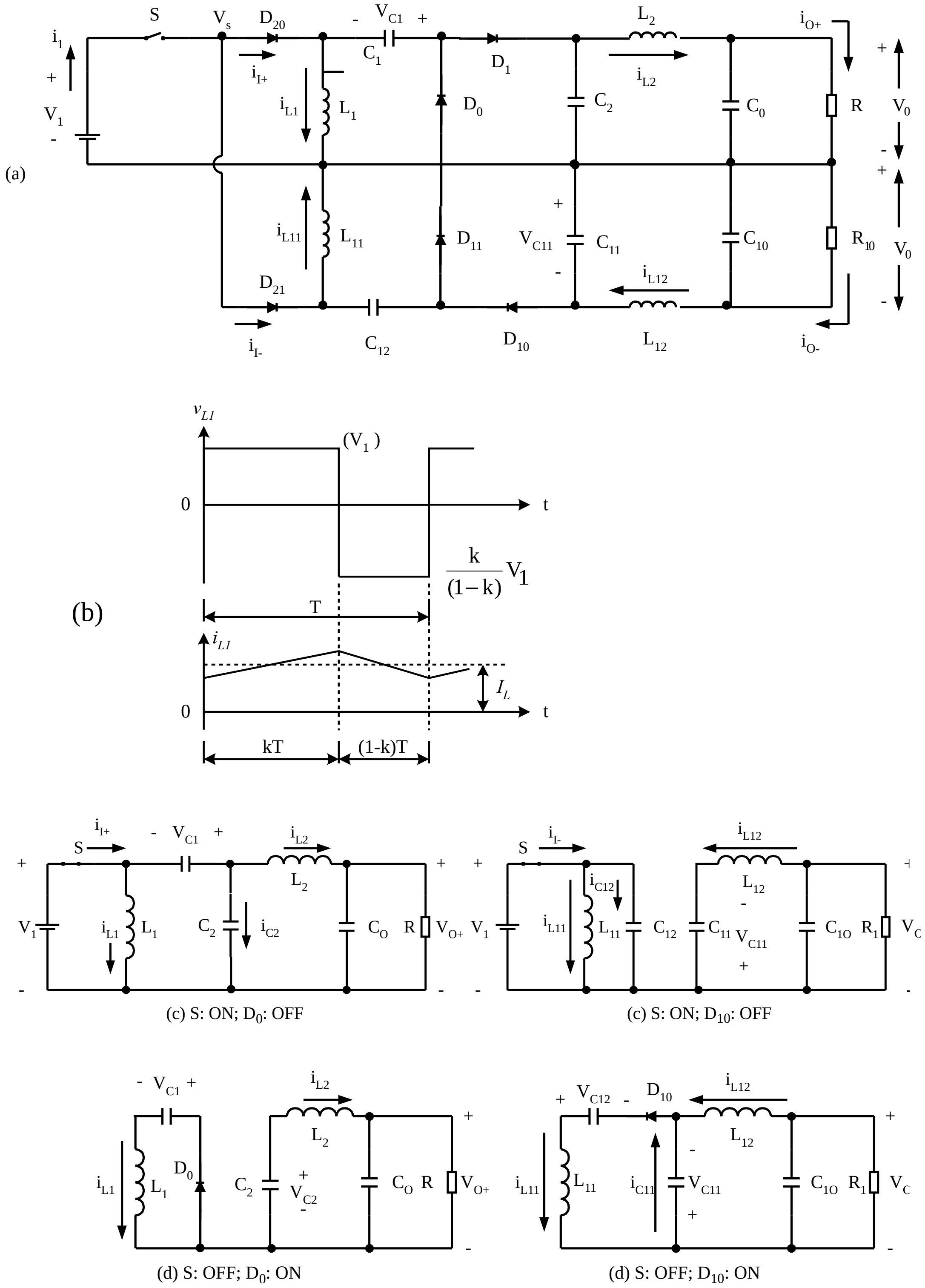
Output voltages in the discontinuous mode are

$$V_O = V_{O+} = |V_{O-}| = \left[1 + k^2 (1-k) \frac{z_N}{2} \right] V_I$$

with

$$\sqrt{\frac{k z_N}{2}} \geq \frac{1}{1-k}$$

An **S D/O Luo re-lift circuit** is shown in Fig. 17.32a. The typical output voltage and current waveforms are shown in Fig. 17.32b. The equivalent circuits during switch-on and


(a)
S
V_s
D_{20}
V_{C1}
C_1
D_1
L_2
i_{O+}
i_1
V_1
i_{I+}
i_{L1}
L_1
D_0
i_{L2}
C_2
C_0
R
V_0
i_{L11}
L_{11}
D_{11}
V_{C11}
C_{11}
C_{10}
R_{10}
D_{21}
i_{L12}
i_{I-}
C_{12}
D_{10}
L_{12}
i_{O-}
(b)
v_{L1}
(V_1)
0
t
$\frac{k}{(1-k)}V_1$
T
i_{L1}
I_L
kT
(1-k)T
i_{C2}
C_O
V_{O+}
i_{I-}
i_{C12}
C_{1O}
R_1
V_{C2}
V_{C12}
i_{C11}

(c) S: ON; D_0: OFF

(c) S: ON; D_{10}: OFF

(d) S: OFF; D_0: ON

(d) S: OFF; D_{10}: ON

FIGURE 17.31 Simplified double output Luo self-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

switch-off periods are shown in Fig. 17.32c,d. Its output voltages and currents (absolute values) are:

$$V_{O+} = |V_{O-}| = \frac{2}{1-k}V_I \quad I_{O+} = \frac{1-k}{2}I_{I+}$$

and

$$I_{O-} = \frac{1-k}{2}I_{I-}$$

The voltage-transfer gain in the continuous mode is

$$M_R = \frac{V_{O+}}{V_I} = \frac{|V_{O-}|}{V_I} = \frac{2}{1-k}$$

The variation ratio of the output voltage v_{O+} in the continuous mode is

$$\varepsilon_+ = \frac{\Delta v_{O+}/2}{V_{O+}} = \frac{k}{128}\frac{1}{f^3 C_2 C_O L_2 R}$$

The variation ratio of the output voltage v_{O-} in the continuous mode is

$$\varepsilon_- = \frac{\Delta v_{O-}/2}{V_{O-}} = \frac{k}{128}\frac{1}{f^3 C_{11} C_{10} L_{12} R_1}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is $M_R \leq \sqrt{kz_N}$.

Output voltages in the discontinuous mode are

$$V_O = V_{O+} = |V_{O-}| = \left[2 + k^2(1-k)\frac{z_N}{2}\right]V_I$$

with

$$\sqrt{kz_N} \geq \frac{2}{1-k}$$

An **S D/O Luo triple-lift circuit** is shown in Fig. 17.33a. The typical output voltage and current waveforms are shown in Fig. 17.33b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.33c,d. Its output voltages and currents (absolute values) are:

$$V_{O+} = |V_{O-}| = \frac{3}{1-k}V_I \quad I_{O+} = \frac{1-k}{3}I_{I+}$$

and

$$I_{O-} = \frac{1-k}{3}I_{I-}$$

The voltage-transfer gain in the continuous mode is

$$M_T = \frac{V_{O+}}{V_I} = \frac{|V_{O-}|}{V_I} = \frac{3}{1-k}$$

The variation ratio of the output voltage v_{O+} in the continuous mode is

$$\varepsilon_+ = \frac{\Delta v_{O+}/2}{V_{O+}} = \frac{k}{128}\frac{1}{f^3 C_2 C_O L_2 R}$$

The variation ratio of the output voltage v_{O-} in the continuous mode is

$$\varepsilon_- = \frac{\Delta v_{O-}/2}{V_{O-}} = \frac{k}{128}\frac{1}{f^3 C_{11} C_{10} L_{12} R_1}$$

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_T \leq \sqrt{\frac{3kz_N}{2}}$$

Output voltages in the discontinuous mode are

$$V_O = V_{O+} = |V_{O-}| = \left[3 + k^2(1-k)\frac{z_N}{2}\right]V_I$$

with

$$\sqrt{\frac{3kz_N}{2}} \geq \frac{3}{1-k}$$

An **S D/O Luo quadruple-lift circuit** is shown in Fig. 17.34a. The typical output voltage and current waveforms are shown in Fig. 17.34b. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.34c,d. Its output voltages and currents (absolute values) are:

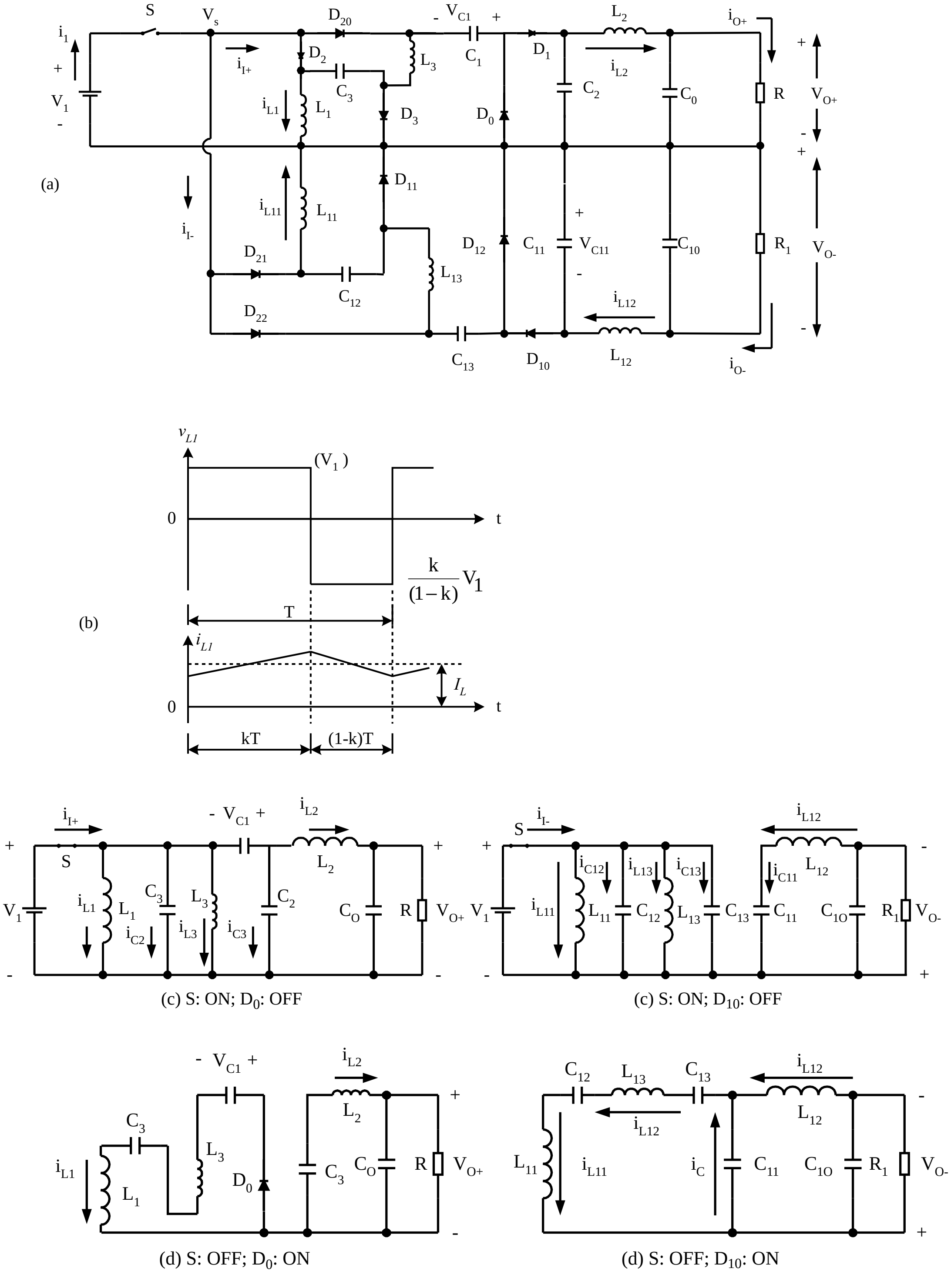
$$V_{O+} = |V_{O-}| = \frac{4}{1-k}V_I \quad I_{O+} = \frac{1-k}{4}I_{I+}$$

and

$$I_{O-} = \frac{1-k}{4}I_{I-}$$

The voltage-transfer gain in the continuous mode is

$$M_Q = \frac{V_{O+}}{V_I} = \frac{|V_{O-}|}{V_I} = \frac{4}{1-k}$$


(a)
S
V_s
i_1
V_1
D_{20}
D_2
C_3
L_3
D_3
L_1
i_{L1}
i_{I+}
$- V_{C1} +$
C_1
D_1
D_0
L_2
i_{L2}
C_2
C_0
R
i_{O+}
V_{O+}
i_{I-}
D_{11}
L_{11}
i_{L11}
D_{21}
C_{12}
L_{13}
D_{22}
C_{13}
D_{12}
C_{11}
V_{C11}
D_{10}
i_{L12}
L_{12}
C_{10}
R_1
V_{O-}
i_{O-}
(b)
v_{L1}
(V_1)
0
t
$\frac{k}{(1-k)}V_1$
T
i_{L1}
I_L
kT
(1-k)T
i_{C2}
i_{L3}
i_{C3}
i_{C12}
i_{L13}
i_{C13}
i_{C11}
C_O
C_{1O}
i_C

(c) S: ON; D_0: OFF

(c) S: ON; D_{10}: OFF

(d) S: OFF; D_0: ON

(d) S: OFF; D_{10}: ON

FIGURE 17.32 Simplified double output Luo re-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; (d) switch-off equivalent circuit.

The variation ratio of the output voltage v_{O+} in the continuous mode is

$$\varepsilon_+ = \frac{\Delta v_{O+}/2}{V_{O+}} = \frac{k}{128}\frac{1}{f^3 C_2 C_O L_2 R}$$

The variation ratio of the output voltage v_{O-} in the continuous mode is

$$\varepsilon_- = \frac{\Delta v_{O-}/2}{V_{O-}} = \frac{k}{128}\frac{1}{f^3 C_{11} C_{10} L_{12} R_1}$$

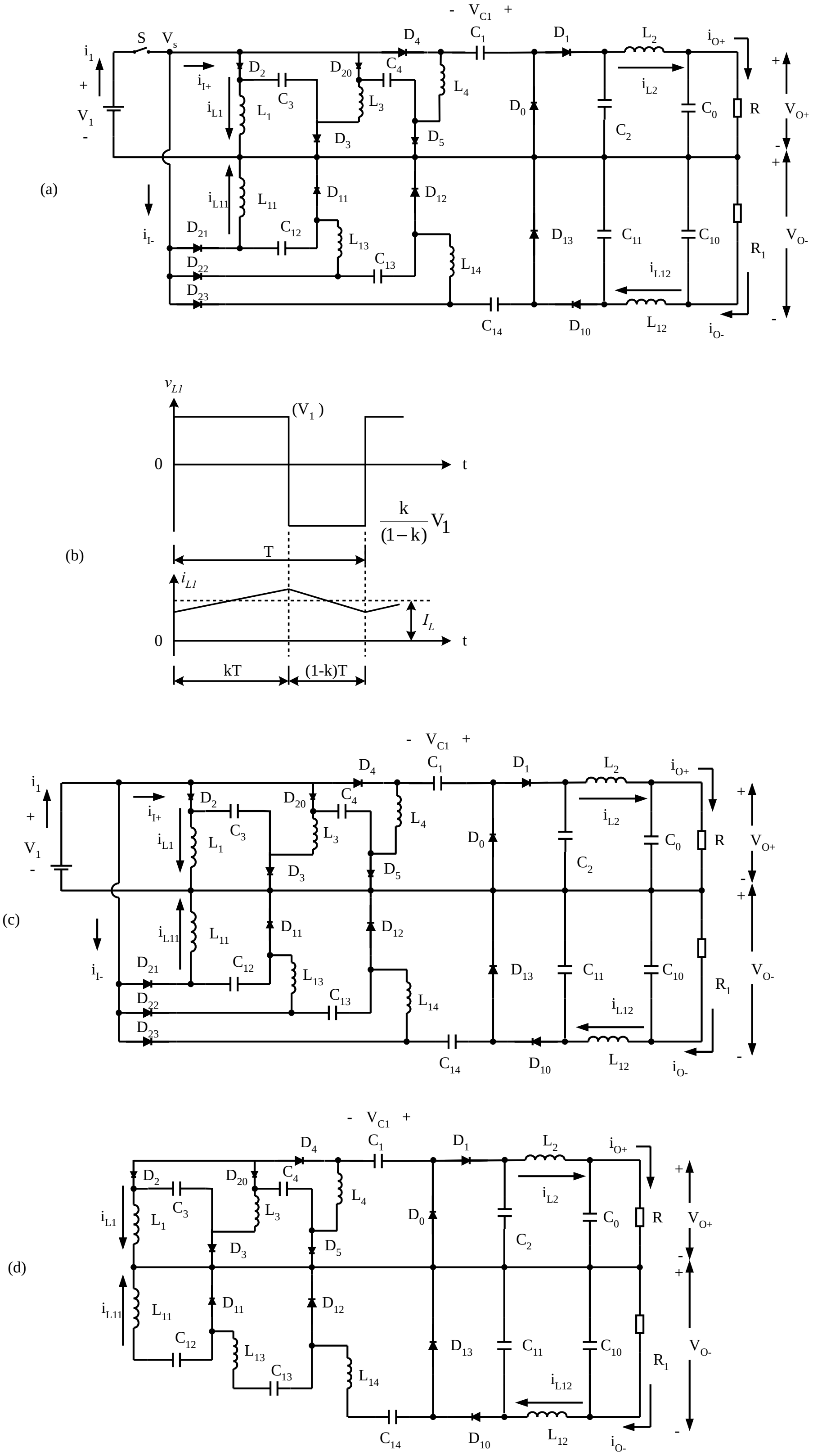

(a)
S
V_s
i_1
V_1
i_{I+}
i_{I-}
i_{L1}
i_{L11}
$-\ V_{C1}\ +$
D_1
D_2
D_3
D_4
D_5
D_0
D_{10}
D_{11}
D_{12}
D_{13}
D_{20}
D_{21}
D_{22}
D_{23}
C_0
C_1
C_2
C_3
C_4
C_{10}
C_{11}
C_{12}
C_{13}
C_{14}
L_1
L_2
L_3
L_4
L_{11}
L_{12}
L_{13}
L_{14}
i_{L2}
i_{L12}
i_{O+}
i_{O-}
R
R_1
V_{O+}
V_{O-}
(b)
v_{L1}
(V_1)
0
t
$\frac{k}{(1-k)}V_1$
T
i_{L1}
I_L
kT
(1-k)T
(c)
(d)

FIGURE 17.33 Simplified double output Luo triple-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

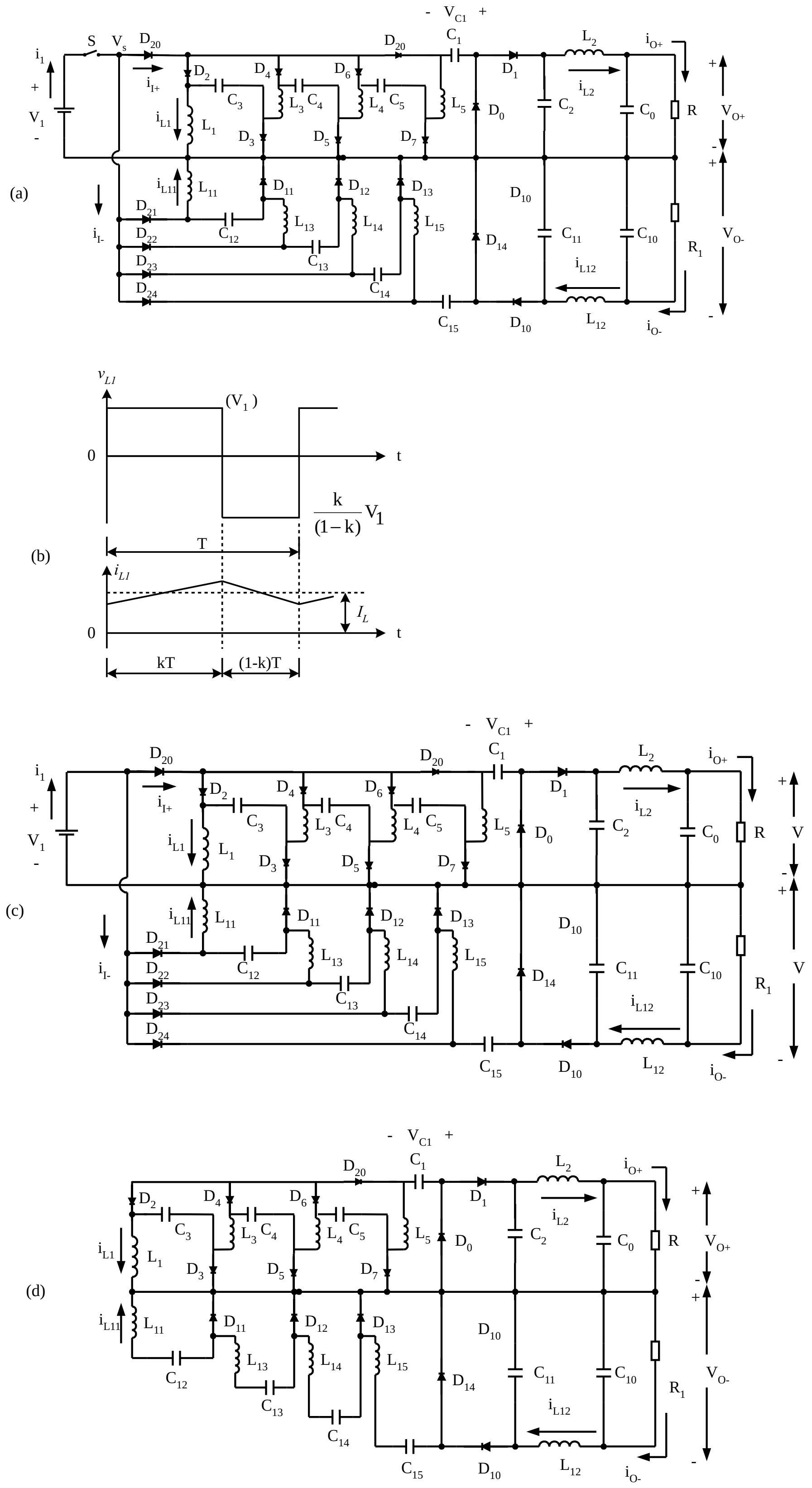

(a)
S
V_s
D_{20}
i_1
V_1
i_{I+}
i_{L1}
L_1
D_2
C_3
D_3
D_4
L_3
C_4
D_5
D_6
L_4
C_5
D_7
L_5
$-\ V_{C1}\ +$
C_1
D_1
D_0
L_2
i_{L2}
C_2
C_0
i_{O+}
R
V_{O+}
i_{L11}
L_{11}
D_{11}
D_{12}
D_{13}
L_{13}
L_{14}
L_{15}
i_{I-}
D_{21}
D_{22}
D_{23}
D_{24}
C_{12}
C_{13}
C_{14}
C_{15}
D_{14}
D_{10}
C_{11}
C_{10}
i_{L12}
L_{12}
R_1
V_{O-}
i_{O-}
(b)
v_{L1}
(V_1)
0
t
$\frac{k}{(1-k)}V_1$
T
i_{L1}
I_L
kT
(1-k)T
(c)
V
(d)

FIGURE 17.34 Simplified double output Luo quadruple-lift converter: (a) circuit diagram; (b) waveforms of inductor voltage and current; (c) switch-on equivalent circuit; and (d) switch-off equivalent circuit.

This converter may work in the discontinuous mode if the frequency f is small, conduction duty k is small, inductance L is small, and the load current is high. The condition for the discontinuous mode is

$$M_Q \le \sqrt{2kz_N}$$

Output voltages in the discontinuous mode are

$$V_O = V_{O+} = |V_{O-}| = \left[4 + k^2(1-k)\frac{z_N}{2}\right]V_I$$

with

$$\sqrt{2kz_N} \ge \frac{4}{1-k}$$

Summary for all **S D/O Luo**-converters:

$$M = \frac{V_{O+}}{V_I} = \frac{|V_{O-}|}{V_I} \quad L_1 = L_{11} \quad R = R_1 \quad z_{N+} = \frac{R}{fL_1}$$

$$z_{N-} = \frac{R_1}{fL_{11}} \quad \text{so that} \quad z_N = z_{N+} = z_{N-}$$

To write common formulas for all circuits parameters, subscript $j = 1$ for the self-lift circuit, $j = 2$ for the re-lift circuit, $j = 3$ for the triple-lift circuit, $j = 4$ for the quadruple-lift circuit, and so on. The voltage-transfer gain is

$$M_j = \frac{j}{1-k}$$

The variation ratio of the output voltage v_{O+} in the continuous mode is

$$\varepsilon_{+j} = \frac{\Delta v_{O+}/2}{V_{O+}} = \frac{k}{128}\frac{1}{f^3 C_2 C_O L_2 R}$$

The variation ratio of the output voltage v_{O-} in the continuous mode is

$$\varepsilon_{-j} = \frac{\Delta v_{O-}/2}{V_{O-}} = \frac{k}{128}\frac{1}{f^3 C_{11} C_{10} L_{12} R_1}$$

The condition for the discontinuous mode is

$$M_j \le \sqrt{\frac{jkz_N}{2}}$$

The output voltage in the discontinuous mode is

$$V_{O-j} = \left(j + k^2\frac{1-k}{2}z_N\right)V_I$$

Using these circuits is easy to convert a 24-V input source-voltage into a ±1000-V output load-voltage. Some applications in insulation testing have already been published.

17.5 Multiple-Quadrant Operating Luo-Converters

Multiple-quadrant operating converters are second-generation converters. These converters usually perform between two voltage sources V_1 and V_2. Voltage source V_1 is the positive voltage and voltage V_2 is the load voltage. In the investigation both voltages are constant voltage, as V_1 and V_2 are constant values, the voltage-transfer gain is constant. Our research will concentrate on the working current, minimum conduction duty $k_{\min}$, and the power transfer efficiency η.

Multiple-quadrant operating Luo-converters are second-generation converters and they have three modes:

- two-quadrant dc/dc Luo-converter in forward operation;
- two-quadrant dc/dc Luo-converter in reverse operation; and
- four-quadrant dc/dc Luo-converter.

The two-quadrant dc/dc Luo-converter in forward operation has been derived from the positive output Luo-converter. It performs in the first quadrant Q_{I} and the second quadrant Q_{II} corresponding to the dc motor forward operation in motoring and regenerative braking states.

The two-quadrant dc/dc Luo-converter in reverse operation has been derived from the negative output Luo-converter. It performs in the third quadrant Q_{III} and the fourth quadrant Q_{IV} corresponding to the dc motor reverse operation in motoring and regenerative braking states.

The four-quadrant dc/dc Luo-converter has been derived from the double output Luo-converter. It performs four-quadrant operation corresponding to the dc motor forward and reverse operation in motoring and regenerative braking states.

In the following analysis the input source and output load are usually constant voltages as shown by V_1 and V_2. Switches S_1 and S_2 in this diagram are power MOSFET devices, and they are driven by a pulsewidth-modulated (PWM) switching signal with repeating frequency **f** and conduction duty **k.** In this paper the switch-repeating period is $T = 1/f$, so that the switch-on period is kT and switch-off period is $(1-k)T$. The equivalent resistance is R for each inductor. During switch-on the voltage drop across the switches and diodes is V_S and V_D, respectively.

17.5.1 Two-Quadrant DC/DC Luo-Converter in forward Operation

An **F 2Q Luo-converter** shown in Fig. 17.35, has two switches with two passive diodes, two inductors and one capacitor. The

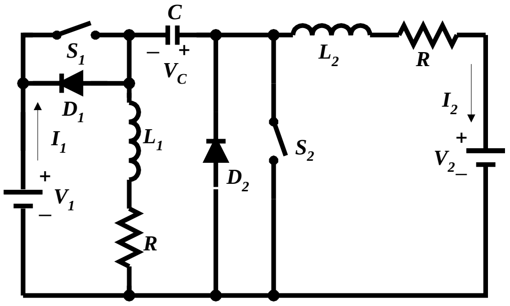


FIGURE 17.35 Forward two-quadrant operating Luo-converter.

source voltage (V_1) and load voltage (V_2) are usually considered as constant voltages. The load can be a battery or motor back-electromotive force (EMF). For example, the source voltage is 42 V and load voltage is +14 V. There are two modes of operation: (1) Mode A (Quadrant I) electrical energy is transferred from source side V_1 to load side V_2; and (2) Mode B (Quadrant II) electrical energy is transferred from load side V_2 to source side V_1.

Mode A. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.36a,b. The typical output voltage and current waveforms are shown in Fig. 17.36c.

Output current I_2 is $I_2 = \frac{1-k}{k} I_1$ and

$$I_2 = \frac{V_1 - V_S - V_D - V_2 \frac{1-k}{k}}{R\left(\frac{k}{1-k} + \frac{1-k}{k}\right)}$$

The minimum conduction duty k corresponding to $I_2 = 0$ is

$$k_{\min} = \frac{V_2}{V_1 + V_2 - V_S - V_D}$$

The power transfer efficiency

$$\eta_A = \frac{P_O}{P_I} = \frac{V_2 I_2}{V_1 I_1} = \frac{1}{1 + \frac{V_S + V_D}{V_2}\frac{k}{1-k} + \frac{RI_2}{V_2}\left[1 + \left(\frac{1-k}{k}\right)^2\right]}$$

The variation ratio of capacitor voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{(1-k)I_2}{2fC\left(V_1 - RI_2\frac{1}{1-k}\right)}$$

The variation ratio of inductor current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1}/2}{I_{L1}} = k\frac{V_1 - V_S - RI_1}{2fL_1 I_1}$$

The variation ratio of inductor current i_{L2} is

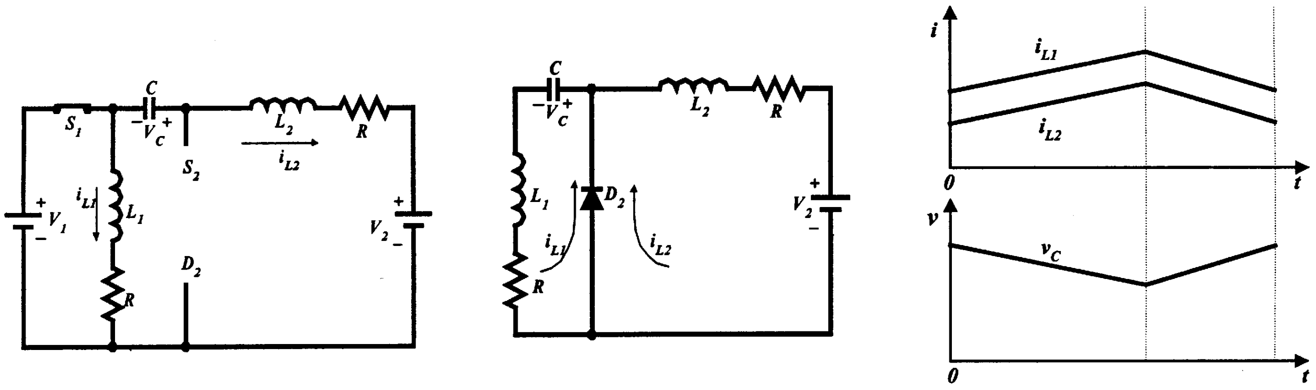
$$\xi_2 = \frac{\Delta i_{L2}/2}{I_{L2}} = k\frac{V_1 - V_S - RI_1}{2fL_2 I_2}$$

The variation ratio of the diode current i_{D2} is

$$\zeta_{D2} = \frac{\Delta i_{D2}/2}{I_{L1} + I_{L2}} = k\frac{V_1 - V_S - RI_1}{2fL(I_1 + I_2)} = k^2\frac{V_1 - V_S - RI_1}{2fLI_1}$$

If the diode current becomes zero before S_1 switches on again, the converter works in a discontinuous region. The condition is $\zeta_{D2} = 1$, that is,

$$k^2 = \frac{2fLI_1}{V_1 - V_S - RI_1}$$



(a) (b) (c)

FIGURE 17.36 Mode A: (a) switch on; (b) switch off; and (c) waveforms with enlarged variations.

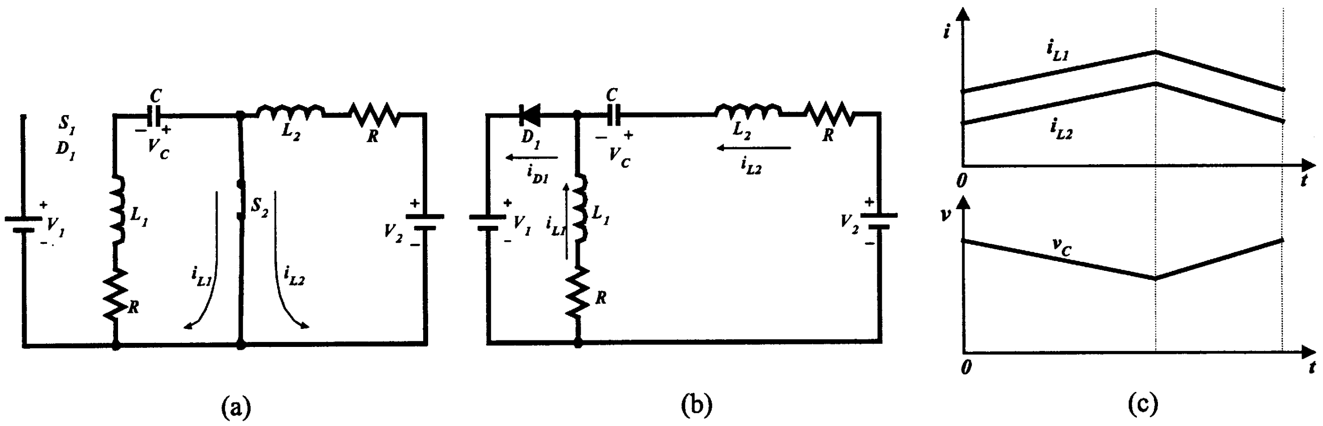


FIGURE 17.37 Mode B: (a) switch on; (b) switch off; and (c) waveforms with enlarged variations.

Mode B. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.37a,b. The typical output voltage and current waveforms are shown in Fig. 17.37c.

Output current I_1 is $I_1 = \frac{1-k}{k} I_2$ and

$$I_1 = \frac{V_2 - (V_1 + V_S + V_D)\frac{1-k}{k}}{R\left(\frac{k}{1-k} + \frac{1-k}{k}\right)}$$

The minimum conduction duty k corresponding to $I_1 = 0$ is

$$k_{\min} = \frac{V_1 + V_S + V_D}{V_1 + V_2 + V_S + V_D}$$

The power transfer efficiency

$$\eta_B = \frac{P_O}{P_I} = \frac{V_1 I_1}{V_2 I_2} = \frac{1}{1 + \frac{V_s + V_D}{V_1} + \frac{RI_1}{V_1}\left[1 + \left(\frac{1-k}{k}\right)^2\right]}$$

The variation ratio of capacitor voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{kI_1}{2fC\left[\frac{V_2}{1-k} - V_1 - RI_1\frac{k}{(1-k)^2}\right]}$$

The variation ratio of inductor current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1}/2}{I_{L1}} = k\frac{V_2 - V_S - RI_2}{2fL_1 I_1}$$

The variation ratio of inductor current i_{L2} is

$$\xi_2 = \frac{\Delta i_{L2}/2}{I_{L2}} = k\frac{V_2 - V_S - RI_2}{2fL_2 I_2}$$

The variation ratio of the diode current i_{D1} is

$$\zeta_{D1} = \frac{\Delta i_{D2}/2}{I_{L1} + I_{L2}} = k\frac{V_2 - V_S - RI_2}{2fL(I_1 + I_2)} = k^2\frac{V_2 - V_S - RI_2}{2fLI_2}$$

If the diode current becomes zero before S_2 switches on again, the converter works in a discontinuous region. The condition is $\zeta_{D1} = 1$, that is,

$$k^2 = \frac{2fLI_2}{V_2 - V_S - RI_2}$$

17.5.2 Two-Quadrant DC/DC Luo-Converter in Reverse Operation

The **R 2Q Luo-converter** shown in Fig. 17.38 has two switches with two passive diodes, two inductors and one capacitor. The source voltage (V_1) and load voltage (V_2) are usually considered as constant voltages. The load can be a battery or motor back-electromotive force (EMF). For example, the source voltage is 42 V and load voltage is −14 V. There are two modes of operation: (1) Mode C (Quadrant III) electrical energy is transferred from source side V_1 to load side $-V_2$; and (2) Mode D (Quadrant IV) electrical energy is transferred from load side $-V_2$ to source side V_1.

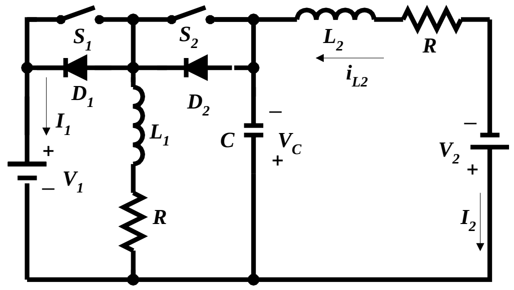


FIGURE 17.38 Reverse two-quadrant operating Luo-converter.

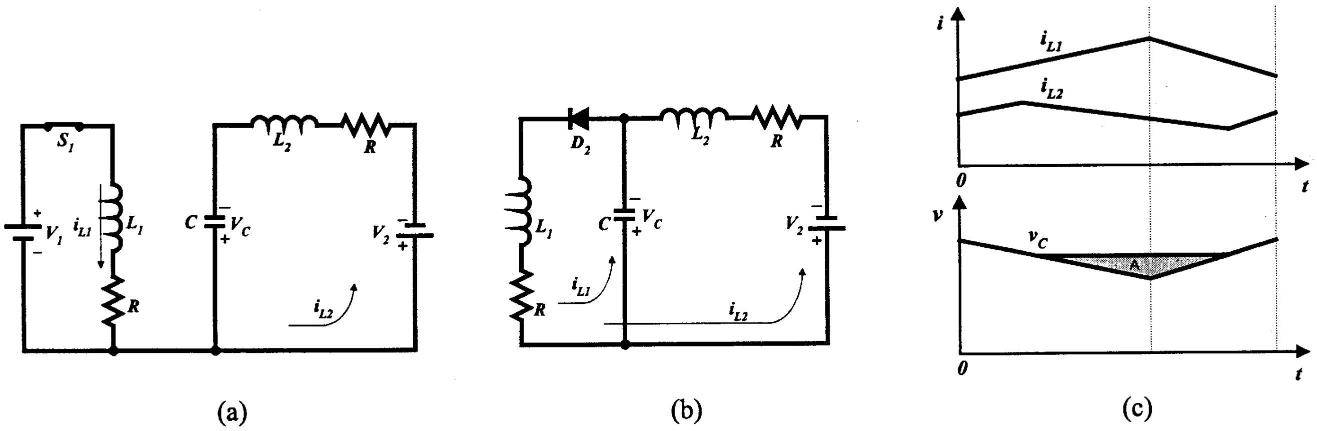


FIGURE 17.39 Mode C: (a) switch on; (b) switch off; and (c) waveforms with enlarged variations.

Mode C. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.39a,b. The typical output voltage and current waveforms are shown in Fig. 17.39c.

Output current I_2 is

$$I_2 = \frac{1-k}{k} I_1$$

and

$$I_2 = \frac{V_1 - V_S - V_D - V_2 \frac{1-k}{k}}{R\left[\frac{1}{k(1-k)} + \frac{1-k}{k}\right]}$$

The minimum conduction duty k corresponding to $I_2 = 0$ is

$$k_{\min} = \frac{V_2}{V_1 + V_2 - V_S - V_D}$$

The power transfer efficiency

$$\eta_C = \frac{P_O}{P_I} = \frac{V_2 I_2}{V_1 I_1} = \frac{1}{1 + \frac{V_S + V_D}{V_2}\frac{k}{1-k} + \frac{RI_2}{V_2}\left[1 + \left(\frac{1}{1-k}\right)^2\right]}$$

The variation ratio of capacitor voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{kI_2}{2fC\left[\frac{k}{1-k}V_1 - \frac{RI_2}{(1-k)^2}\right]}$$

The variation ratio of inductor current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1}/2}{I_{L1}} = k\frac{V_1 - V_S - RI_1}{2fL_1 I_1}$$

and the variation ratio of inductor current i_{D2} is

$$\zeta_{D2} = \xi_1 = \frac{\Delta i_{D2}/2}{I_{L1}} = k\frac{V_1 - V_S - RI_1}{2fL_1 I_1}$$

The variation ratio of inductor current i_{L2} is

$$\xi_2 = \frac{\Delta i_{L2}/2}{I_2} = \frac{k}{16f^2 CL_2}$$

If the diode current becomes zero before S_1 switches on again, the converter works in a discontinuous region. The condition is $\zeta_{D2} = 1$, that is,

$$k = \frac{2fL_1 I_1}{V_1 - V_S - RI_1}$$

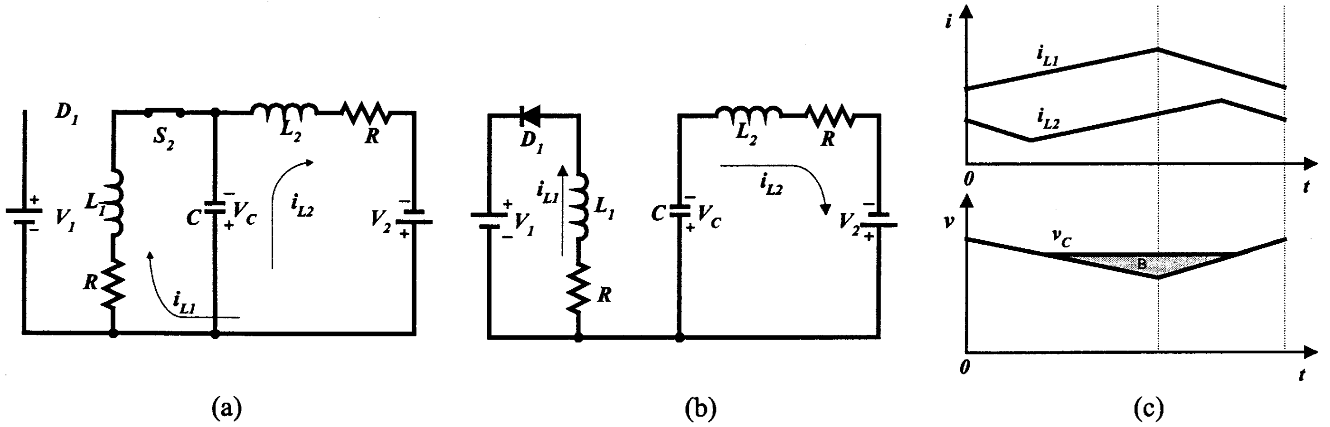
Mode D. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.40a,b. The typical output voltage and current waveforms are shown in Fig. 17.40c.

Output current I_1 is $I_1 = \frac{1-k}{k} I_2$ and

$$I_1 = \frac{V_2 - (V_1 + V_S + V_D)\frac{1-k}{k}}{R\left[\frac{1}{k(1-k)} + \frac{k}{1-k}\right]}$$

The minimum conduction duty k corresponding to $I_1 = 0$ is

$$k_{\min} = \frac{V_1 + V_S + V_D}{V_1 + V_2 + V_S + B_D}$$



(a) (b) (c)

FIGURE 17.40 Mode D: (a) switch on; (b) switch off; (c) waveforms with enlarged variations.

The power transfer efficiency

$$\eta_D = \frac{P_O}{P_I} = \frac{V_1 I_1}{V_2 I_2} = \frac{1}{1 + \frac{V_S + V_D}{V_1} + \frac{RI_1}{V_1}\left[\frac{1}{(1-k)^2} + \left(\frac{k}{1-k}\right)^2\right]}$$

The variation ratio of capacitor voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{kI_1}{2fC\left[\frac{1-k}{k}V_1 + \frac{RI_1}{k(1-k)}\right]}$$

The variation ratio of inductor current i_{L1} is

$$\xi_1 = \frac{\Delta i_{L1}/2}{I_{L1}} = (1-k)\frac{V_2 - V_S - RI_2}{2fL_1 I_1}$$

and the variation ratio of inductor current i_{D1} is

$$\zeta_{D1} = \xi_1 = \frac{\delta i_{D1}/2}{I_{L1}} = k\frac{V_2 - V_S - RI_2}{2fL_1 I_2}$$

The variation ratio of inductor current i_{L2} is

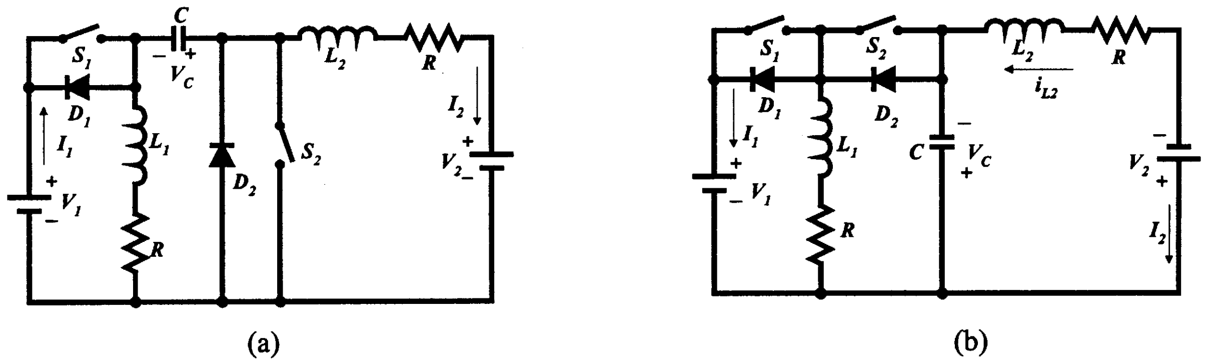
$$\xi_2 = \frac{\Delta i_{L2}/2}{I_2} = \frac{1-k}{16f^2 CL_2}$$

If the diode current becomes zero before S_2 switches on again, the converter works in the discontinuous region. The condition is $\zeta_{D1} = 1$, that is,

$$k = \frac{2fL_1 I_2}{V_2 - V_S - RI_2}$$

17.5.3 our- uadrant DC/DC Luo-Converter

The **4Q Luo-converter** shown in Fig. 17.41 has two switches with two passive diodes, two inductors and one capacitor. The source voltage (V_1) and load voltage (V_2) are usually considered as constant voltages. The load can be a battery or motor back-electromotive force (EMF). For example, the source voltage is 42 V and load voltage is ±14 V. There are four modes of operation:



(a) (b)

FIGURE 17.41 Four-quadrant operating Luo-converter. (a) Circuit 1; and (b) circuit 2.

1. Mode A (Quadrant I): Electrical energy is transferred from source side V_1 to load side V_2;
2. Mode B (Quadrant II): Electrical energy is transferred from load side V_2 to source side V_1;
3. Mode C (Quadrant III): Electrical energy is transferred from source side V_1 to load side $-V_2$; and
4. Mode D (Quadrant IV): Electrical energy is transferred from load side $-V_2$ to source side V_1.

Each mode has two states: "on" and "off." Usually, each state is operating in a different conduction duty k. The switches are the power MOSFET devices. Circuit 1 in Fig. 17.41 implements Modes A and B, and circuit 2 in Fig. 17.41 implements Modes C and D. Circuits 1 and 2 can be changed over by auxiliary switches (not shown in the figure).

Mode A. During the **on** state switch S_1 is closed, and switch S_2 and diodes D_1 and D_2 are not conducting. In this case inductor currents i_{L1} and i_{L2} increase, and $i_1 = i_{L1} + i_{L2}$. During the **off** state switches S_1, S_2, and diode D_1 are off and diode D_2 is conducted. In this case current i_{L1} flows via diode D_2 to charge capacitor C. In the meantime, current i_{L2} continues to flow through load battery V_2. The freewheeling diode current $i_{D2} = i_{L1} + i_{L2}$.

Mode A implements the characteristics of the buck-boost conversion.

Mode B. During the **on** state switch S_2 is closed, and switch S_1 and diodes D_1 and D_2 are not conducting. In this case inductor current i_{L2} increases by biased V_2, and inductor current i_{L1} increases by biased V_C. Therefore, capacitor voltage V_C reduces. During the **off** state switches S_1, S_2 and diode D_2 are not on, and only diode D_1 is on. In this case source current $i_1 = i_{L1} + i_{L2}$, which is a negative value to perform the regenerative operation. Inductor current i_{L2} flows through capacitor C, and it is charged by current i_{L2}. After capacitor C, i_{L2} then flows through the source V_1. Inductor current i_{L1} flows through the source V_1 as well via diode D_1.

Mode B implements the characteristics of the boost conversion.

Mode C. During the **on** state switch S_1 is closed, and switch S_2 and diodes D_1 and D_2 are not conducting. In this case inductor currents i_{L1} and i_{L2} increase and $i_1 = i_{L1}$. During the **off** state switches S_1, S_2 and diode D_1 are off and diode D_2 is conducting. In this case current i_{L1} flows via diode D_2 to charge capacitor C and the load battery V_2 via inductor L_2. The freewheeling diode current $i_{D2} = i_{L1} = i_C + i_2$.

Mode C implements the characteristics of the buck-boost conversion.

Mode D. During the **on** state switch S_2 is closed, and switch S_1 and diodes D_1 and D_2 are not conducting. In this case inductor current i_{L1} increases by biased V_2, and inductor current i_{L2} decreases by biased $(V_2 - V_C)$. Therefore, capacitor voltage V_C reduces. Current $i_{L1} = i_{C-\text{on}} + i_2$. During the **off** state switches S_1, S_2 and diode D_2 are not on, and only diode D_1 is on. In this case source current $i_1 = i_{L1}$, which is a negative value to perform the regenerative operation. Inductor current i_2 flows through capacitor C that is charged by current i_2, that is, $i_{C-\text{off}} = i_2$.

TABLE 17.1 Switch status (blank space means OFF)

Switch or Diode	Mode A (QI)		Mode B (QII)		Mode C (QIII)		Mode D (QIV)	
	State-on	State-off	State-on	State-off	State-on	State-off	State-on	State-off
Circuit	Circuit 1				Circuit 2			
S_1	ON				ON			
D_1				ON				ON
S_2			ON				ON	
D_2		ON				ON		

Mode D implements the characteristics of the boost conversion.

Summary. The switch status is shown in Table 17.1.

Operation of modes A, B, C, and D is the same as in the description in Sections 17.5.1 and 17.5.2.

17.6 Switched-Capacitor Multiquadrant Luo-Converters

Switched-component converters are third-generation converters, and they are made only of inductors or capacitors. They usually perform in the systems between two voltage sources: V_1 and V_2. Voltage source V_1 is positive voltage and voltage V_2 is the load voltage that can be positive or negative. In the investigation both voltages are constant voltage. As V_1 and V_2 are constant values, the voltage-transfer gain is constant. Our research will concentrate on the working current and the power transfer efficiency η. The resistance R of the capacitors and inductors has to be considered for the power transfer efficiency η calculation.

From a review of the literature, we found that almost all of the papers investigated switched-component converters working in single-quadrant operation. Luo and his colleagues have developed this technique into multiquadrant operation, which we will describe here in the next sections.

Switched capacitor multiquadrant Luo-converters are third-generation converters, and they are made only of capacitors. Because these converters implement voltage-lift and current-amplification techniques, they have the advantages of high power density, high-power transfer efficiency and low EMI. They have two modes:

- two-quadrant switched-capacitor dc/dc Luo-converter; and
- four-quadrant switched-capacitor dc/dc Luo-converter.

The two-quadrant switched-capacitor dc/dc Luo-converter in forward operation has been derived for the energy transmission of a dual-voltage system in two-quadrant operation. Both source and load voltages are positive polarity. It performs in the first-quadrant Q_I and the second quadrant Q_{II} corresponding to the dc motor forward operation in motoring and regenerative braking states.

The four-quadrant switched-capacitor dc/dc Luo-converter has been derived for the energy transmission of a dual-voltage system in four-quadrant operation. The source voltage is positive and load voltage can be positive or negative polarity. It performs four-quadrant operation corresponding to the dc motor forward and reverse operation in motoring and regenerative braking states.

From the analysis and calculation, the conduction duty k does not affect the power transfer efficiency, but it does affect the input and output power in a small region. The maximum output power corresponds to $k = 0.5$.

17.6.1 Two-Quadrant Switched-Capacitor DC/DC Luo-Converter

This converter is shown in Fig. 17.42. It consists of nine switches, seven diodes and three capacitors. The high source voltage V_H and low load voltage V_L are usually considered as constant voltages, for example, the source voltage is 48 V and the load voltage is 14 V. There are two modes of operation:

- Mode A (Quadrant I): electrical energy is transferred from the V_H side to the V_L side; and
- Mode B (Quadrant II): electrical energy is transferred from the V_L side to the V_H side.

Each mode has two states: "on" and "off." Usually, each state is operating in different conduction duty k. The switching period is T, where $T = 1/f$, where f is the switching frequency. The switches are the power MOSFET devices. The parasitic resistance of all switches is r_S. The equivalent resistance of all capacitors is r_C and the equivalent voltage drop of all diodes is V_D. Usually, we select the three capacitors to have same capacitance $C = C_1 = C_2 = C_3$. Some reference data are useful: $r_S = 0.03\ \Omega$, $r_C = 0.02\ \Omega$ and $V_D = 0.5$ V, $f = 5$ kHz, and $C = 5000\ \mu$F. The switch status is shown in Table 17.2.

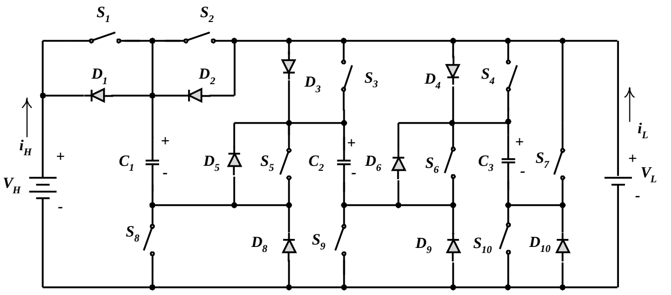


FIGURE 17.42 Two-quadrant switched-capacitor dc/dc Luo-converter.

TABLE 17.2 Switch status (blank space means OFF)

Switch or Diode	Mode A		Mode B	
	State-on	State-off	State-on	State-off
S_1	ON			
D_1				ON
S_2, S_3, S_4		ON		
D_2, D_3, D_4			ON	
S_5, S_6, S_7				ON
D_5, D_6	ON			
S_8, S_9			ON	
S_{10}	ON	ON		
D_8, D_9, D_{10}		ON		

For Mode A, the **on** state is shown in Fig. 17.43a: switches S_1 and S_{10} are closed and diodes D_5 and D_5 are conducting. Other switches and diodes are open. In this case capacitors C_1, C_2 and C_3 are charged via the circuit V_H–S_1–C_1–D_5–C_2–D_6–C_3–S_{10}, and the voltage across capacitors C_1, C_2 and C_3 is increasing. The equivalent circuit resistance is $R_{AN} = (2r_S + 3r_C) = 0.12\ \Omega$, and the voltage deduction is $2V_D = 1$ V. The **off** state is shown in Fig. 17.43b: switches S_2, S_3 and S_4 are closed and diodes D_8, D_9 and D_{10} are conducting. Other switches and diodes are open. In this case capacitor C_1 (C_2 and C_3) is discharged via the circuit S_2(S_3 and S_4)–V_L–D_8(D_9 and D_{10})–C_1(C_2 and C_3), and the voltage across capacitor C_1 (C_2 and C_3) is decreasing. Mode A implements the **current-amplification technique**. The voltage and current waveforms are shown in Fig. 17.43c. All three capacitors are charged in series during the on state. The input current flows through three capacitors and the charges accumulated on the three capacitors should be the same. These three capacitors are discharged in parallel the off state. Therefore, the output current is amplified by three times.

The variation of the voltage across capacitor C_1 is:

$$\Delta v_{C1} = \frac{k(V_H - 3V_{C1} = 2V_D)}{fCR_{AN}} = \frac{2.4k(1-k)(V_H - 3V_L - 5V_D)}{(2.4 + 0.6k)fCR_{AN}}$$

After calculation,

$$V_{C1} = \frac{k(V_H - 2V_D) + 2.4(1-k)(V_L + V_D)}{2.4 + 0.6k}$$

The average output current is

$$I_L = \frac{3}{T}\int_{kT}^{T} i_{C1}(t)dt \approx 3(1-k)\frac{V_{C1} - V_L - V_D}{R_{AF}}$$

The average input current is

$$I_H = \frac{1}{T}\int_{0}^{kT} i_{C1}(t)dt \approx k\frac{V_H - 3V_{C1} - 2V_D}{R_{AN}}$$

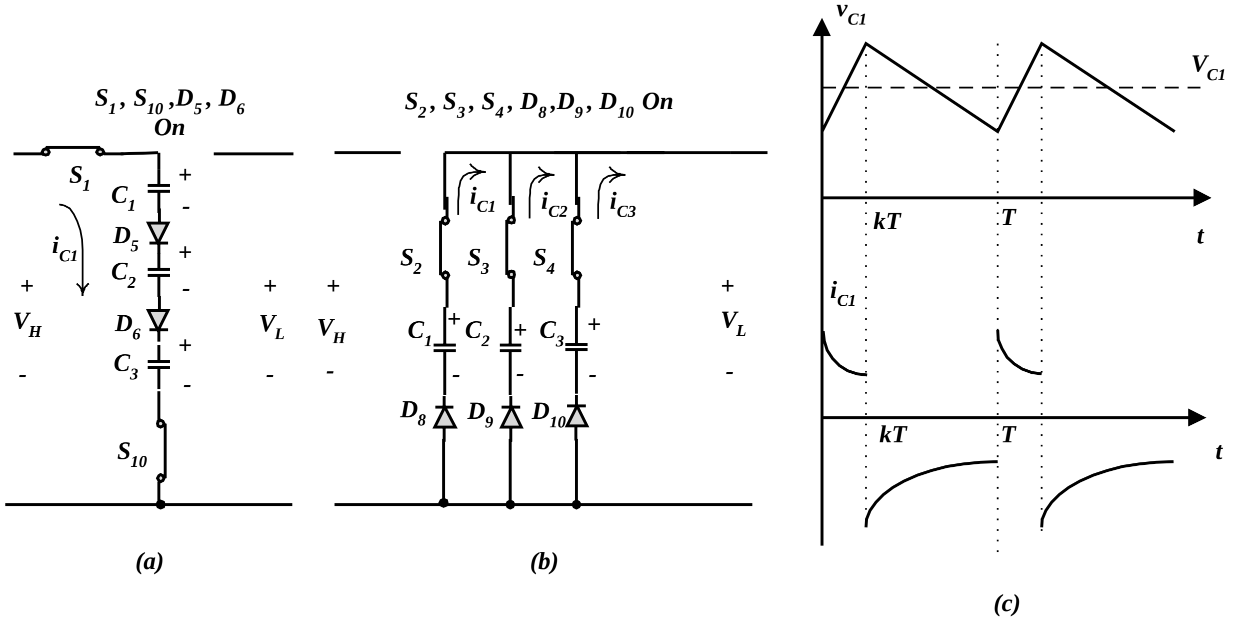


FIGURE 17.43 Mode A operation: (a) on state; (b) off state; and (c) voltage and current waveforms.

Therefore, we have $3I_H = I_L$.

The output power is

$$P_O = V_L I_L = 3(1-k)V_L \frac{V_{C1} - V_L - V_D}{R_{AF}}$$

The input power is

$$P_I = V_H I_H = kV_H \frac{V_H - 3V_{C1} - V_D}{R_{AN}}$$

The transfer efficiency is

$$\eta_A = \frac{P_O}{P_I} = \frac{1-k}{k}\frac{3V_L}{V_H}\frac{V_{C1} - V_L - V_D}{V_H - 3V_{C1} - V_D}\frac{R_{AN}}{R_{AF}} = \frac{3V_L}{V_H}$$

For Mode B, the **on** state is shown in Fig. 17.44a: switches S_8, S_9 and S_{10} are closed and diodes D_2, D_3 and D_4 are conducting. Other switches and diodes are off. In this case all three capacitors are charged via each circuit V_L–D_2(and D_3, D_4)–C_1(and C_2, C_3)–S_8(and S_9, S_{10}), and the voltage across three capacitors are increasing. The equivalent circuit resistance is $R_{BN} = r_S + r_C$ and the voltage deduction is V_D in each circuit. The **off** state is shown in Fig. 17.44b; switches S_5, S_6 and S_7 are closed and diode D_1 is on. Other switches and diodes are open. In this case all capacitors are discharged via the circuit V_L–S_7–C_3–S_6–C_2–S_5–C_1–D_1–V_H, and the voltage across all capacitors is decreasing. Mode B implements the **voltage-lift technique**. The voltage and current waveforms are shown in Fig. 17.44c. All three capacitors are charged in parallel during the on state. The input voltage is applied to the three capacitors symmetrically, so that the voltages across these three capacitors should be the same. They are discharged in series during the off state. Therefore, the output voltage is lifted by three times.

The variation of the voltage across capacitor C is:

$$\Delta v_{C1} = \frac{k(1-k)[4(V_L - V_D) - V_H]}{fCR_{BN}}$$

After calculation,

$$V_{C1} = k(V_L - V_D) + \frac{1-k}{3}(V_H - V_L + V_D)$$

The average input current

$$I_L = \frac{1}{T}\left[3\int_0^{kT} i_{C1}(t)dt + \int_{kT}^{T} i_{C1}(t)dt \approx 3k\frac{V_L - V_{C1} - V_D}{R_{BN}} + (1-k)\frac{3V_{C1} + V_L - V_H - V_D}{R_{BF}}\right]$$

The average output current

$$I_H = \frac{1}{T}\int_{kT}^{T} i_{C1}(t)dt \approx (1-k)\frac{3V_{C1} + V_L - V_H - V_D}{R_{BF}}$$

From this formula, we have $4I_H = I_L$.

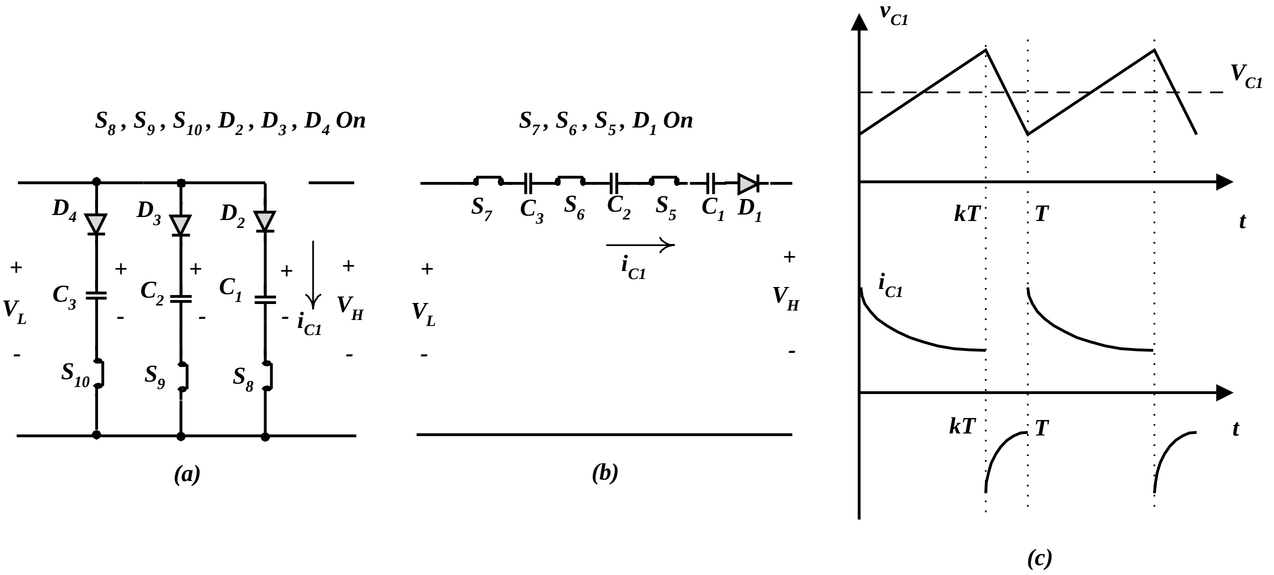


FIGURE 17.44 Mode B operation: (a) on state; (b) off state; and (c) voltage and current waveforms.

The input power

$$P_I = V_L I_L$$

$$= V_L\left[3k\frac{V_L - V_C - V_D}{R_{BN}} + (1-k)\frac{3V_C + V_L - V_H - V_D}{R_{BF}}\right]$$

The output power

$$P_O = V_H I_H = V_H(1-k)\frac{3V_C + V_L - V_H - V_D}{R_{BF}}$$

The transfer efficiency is

$$\eta_B = \frac{P_O}{P_I} = \frac{V_H}{4V_L}$$

17.6.2 Four-Quadrant Switched-Capacitor DC/DC Luo-Converter

The **four-quadrant switched-capacitor dc/dc Luo-converter** is shown in Fig. 17.45. Because it performs the *voltage-lift technique*, it has a simple structure with four-quadrant operation. This converter consists of eight switches and two capacitors. The source voltage V_1 and load voltage V_2 (e.g., a battery or DC motor back-EMF) are usually constant voltages. Here, they are assumed to be ±21 and ±14 V. Capacitors C_1 and C_2 are the same, and $C_1 = C_2 = 2000\,\mu\text{F}$. The circuit equivalent resistance $R = 50\,\text{m}\Omega$. Therefore, there are four modes of operation for this converter:

1. Mode A the energy is transferred from source to positive voltage load; the first quadrant-operation Q_{I};
2. Mode B the energy is transferred from positive voltage load to source; the second quadrant-operation Q_{II};
3. Mode C the energy is transferred from source to negative voltage load; the third quadrant-operation Q_{III}; and
4. Mode D the energy is transferred from negative voltage load to source; the fourth quadrant-operation Q_{IV}.

The first quadrant (Mode A) is the so-called forward motoring (Forw. Mot.) operation; V_1 and V_2 are positive, and I_1 and I_2 are positive as well. The second quadrant (Mode B) is the so-called forward regenerative (Forw. Reg.) braking operation; V_1 and V_2 are positive, and I_1 and I_2 are negative. The third quadrant (Mode C) is the so-called reverse motoring (Rev. Mot.) operation; V_1 and I_1 are positive, and V_2 and I_2 are negative. The fourth quadrant (Mode D) is the so-called reverse regenerative (Rev. Reg.) braking operation; V_1 and I_2 are positive, and I_1 and V_2 are negative.

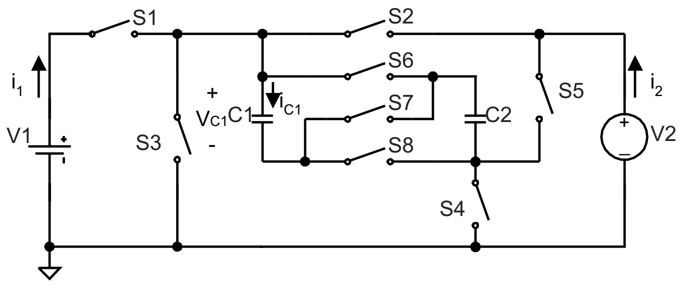


FIGURE 17.45 Four quadrant switched capacitor dc/dc Luo-converter.

TABLE 17.3 Switch status (none of the mentioned switches are open)

Quadrant No. and Mode	Condition	State		Source Side	Load Side
		ON	OFF		
Q_{I} Mode A	$V_1 > V_2$	$S_{1,4,6,8}$	$S_{2,4,6,8+}$	V_1+	V_2+
Forw. Mot.	$V_1 < V_2$	$S_{1,4,6,8}$	$S_{2,4,7}$	I_1+	I_2+
Q_{II} Mode B	$V_1 > V_2$	$S_{2,4,6,8}$	$S_{1,4,7}$	V_1+	V_2+
Forw. Reg.	$V_1 < V_2$	$S_{2,4,6,8}$	$S_{1,4,6,8}$	I_1-	I_2-
Q_{III} Mode C	$V_1 > \lvert V_2 \rvert$	$S_{1,4,6,8}$	$S_{3,5,6,8}$	V_1+	V_2-
Rev. Mot.	$V_1 < \lvert V_2 \rvert$	$S_{1,4,6,8}$	$S_{3,5,7}$	I_1+	I_2-
Q_{IV} Mode D	$V_1 > \lvert V_2 \rvert$	$S_{3,5,6,8}$	$S_{1,4,7}$	V_1+	V_2-
Rev. Reg.	$V_1 < \lvert V_2 \rvert$	$S_{3,5,6,8}$	$S_{1,4,6,8}$	I_{1-}	I_2+

Each mode has two conditions: $V_1 > V_2$ and $V_1 < V_2$ (or $|V_2|$ for Q_{III} and Q_{IV}). Each condition has two states: "on" and "off." Usually, each state is operating in a different conduction duty k for different currents. As usual, the efficiency of all switched-capacitor dc/dc converters is independent of the conduction duty cycle k. The switching period is T, where $T = 1/f$. The switch status is shown in Table 17.3.

As usual, the transfer efficiency relies only on the ratio of the source and load voltages, and it is independent of R, C, f, and k. We select $k = 0.5$ for our description. Other values for the reference are $f = 5\,\mathrm{kHz}$, $V_1 = 21\,\mathrm{V}$ and $V_2 = 14\,\mathrm{V}$, and total $C = 4000\,\mu\mathrm{F}$, $R = 50\,\mathrm{m}\Omega$.

For Mode A1, condition $V_1 > V_2$ is shown in Fig. 17.45a. Because $V_1 > V_2$, two capacitors C_1 and C_2 are connected in parallel. During the switch-**on** state, switches S_1, S_4, S_6 and S_8 are closed and other switches are open. In this case capacitors $C_1//C_2$ are charged via the circuit V_1–S_1–$C_1//C_2$–S_4, and the voltage across capacitors C_1 and C_2 is increasing. During the switch-**off** state, switches S_2, S_4, S_6 and S_8 are closed and other switches are open. In this case capacitors $C_1//C_2$ are discharged via the circuit S_2–V_2–S_4–$C_1//C_2$, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the source to the load.

The average capacitor voltage,

$$V_C = kV_1 + (1-k)V_2$$

The average current

$$I_2 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{V_C - V_2}{R}$$

and

$$I_1 = \frac{1}{T}\int_{0}^{kT} i_C(t)dt \approx k\frac{V_1 - V_C}{R}$$

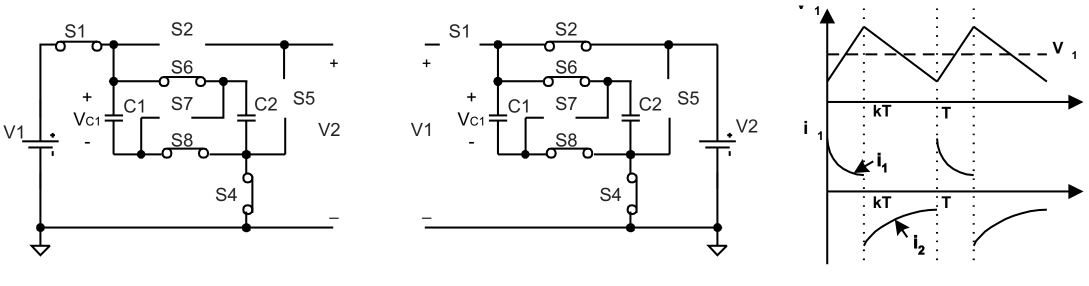
The transfer efficiency is

$$\eta_{A1} = \frac{P_O}{P_I} = \frac{1-k}{k}\frac{V_2}{V_1}\frac{V_C - V_2}{V_1 - V_C} = \frac{V_2}{V_1}$$

For Mode A2, condition $V_1 < V_2$ is shown in Fig. 17.45b. Because $V_1 < V_2$, two capacitors C_1 and C_2 are connected in parallel during switch-on and in series during switch-off. This is the so-called *voltage-lift technique.* During the switch-**on** state, switches S_1, S_4, S_6 and S_8 are closed and other switches are open. In this case capacitors $C_1//C_2$ are charged via the circuit V_1–S_1–$C_1//C_2$–S_4, and the voltage across capacitors C_1 and C_2 is increasing. During the switch-**off** state, switches S_2, S_4 and S_7 are closed and other switches are open. In this case capacitors C_1 and C_2 are discharged via the circuit S_2–V_2–S_4–C_1–S_7–C_2, and the voltage across capacitor C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the source to the load.

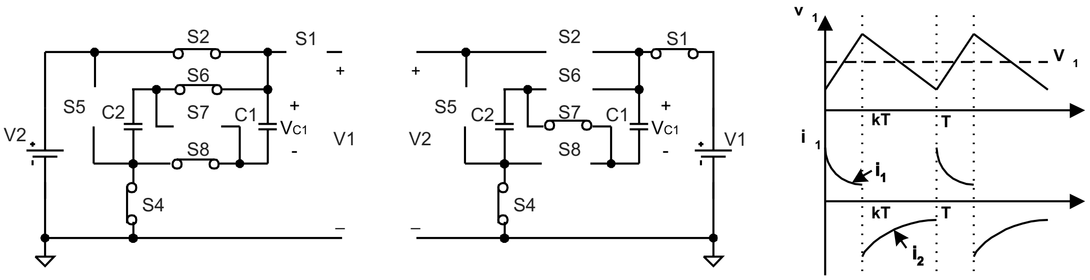
The average capacitor voltage is

$$V_C = \frac{0.5V_1 + V_2}{2.5} = 11.2$$



(i) Switch-on: *S1*, *S4*, *S6* & *S8* on (ii) Switch-off: *S2*, *S4*, *S6* & *S8* on (iii) Waveforms

FIGURE 17.45a Mode A1 (quadrant I): forward motoring with $V_1 > V_2$.



(i) Switch-on: *S2*, *S4*, *S6* & *S8* on (ii) Switch -off: *S1*, *S4*(*S5*) & *S7* on (iii) Waveforms.

FIGURE 17.45b Mode A2 (quadrant I): forward motoring with $V_1 < V_2$.

The average current

$$I_2 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{2V_C - V_2}{R}$$

and

$$I_1 = \frac{1}{T}\int_{0}^{kT} i_C(t)dt \approx k\frac{V_1 - V_C}{R}$$

The transfer efficiency is

$$\eta_{A2} = \frac{P_O}{P_I} = \frac{1-k}{k}\frac{V_2}{V_1}\frac{2V_C - V_2}{V_1 - V_C} = \frac{V_2}{2V_1}$$

For Mode B1, condition $V_1 > V_2$ is shown in Fig. 17.45c. Because $V_1 > V_2$, two capacitors C_1 and C_2 are connected in parallel during switch-on and in series during switch-off. The *voltage-lift technique* is applied. During the switch-**on** state, switches S_2, S_4, S_6 and S_8 are closed. In this case capacitors $C_1//C_2$ are charged via the circuit V_2–S_2–$C_1//C_2$–S_4, and the voltage across capacitors C_1 and C_2 is increasing. During the switch-**off** state, switches S_1, S_4 and S_7 are closed. In this case capacitors C_1 and C_2 are discharged via the circuit S_1–V_1–S_4–C_2–S_7–C_1, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. Therefore, we have $I_2 = 2I_1$.

The average capacitor voltage is

$$V_C = \frac{0.5V_2 + V_1}{2.5} = 11.2$$

The average current

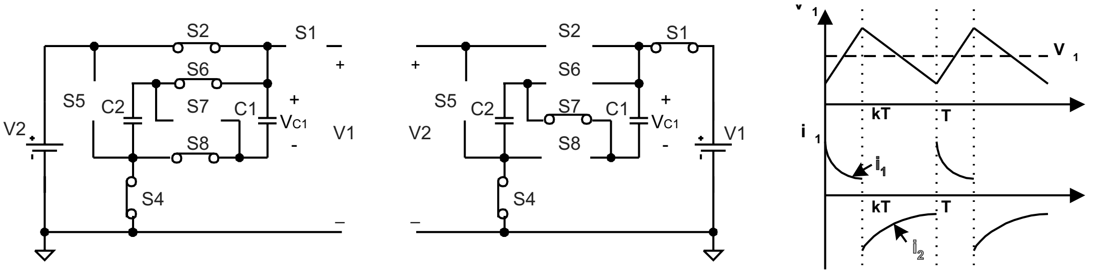
$$I_1 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{2V_C - V_1}{R}$$

and

$$I_2 = \frac{1}{T}\int_{0}^{kT} i_C(t)dt \approx k\frac{V_2 - V_C}{R}$$

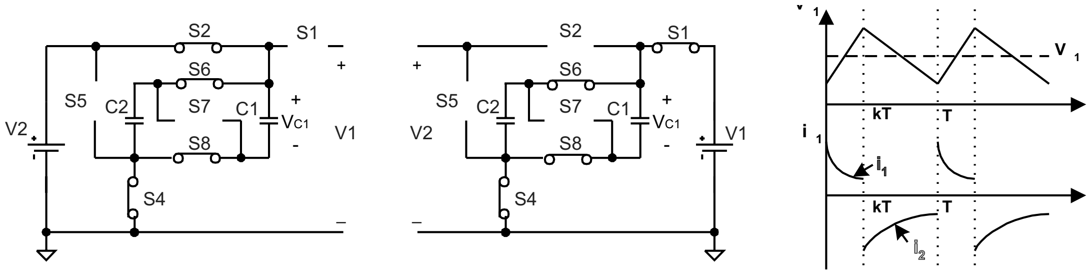
The transfer efficiency is

$$\eta_{B1} = \frac{P_O}{P_I} = \frac{1-k}{k}\frac{V_1}{V_2}\frac{2V_C - V_1}{V_2 - V_C} = \frac{V_1}{2V_2}$$



(i) Switch-on: *S2*, *S4*, *S6* & *S8* on (ii) Switch -off: *S1*, *S4*(*S5*) & *S7* on (iii) Waveforms.

FIGURE 17.45c Mode B1 (quadrant II): forward regenerative braking with $V_1 > V_2$.



(i) Switch-on: *S2*, *S4*, *S6* & *S8* on (ii) Switch -off: *S1*, *S4*(*S5*), *S6* & *S8* on (iii) Waveforms.

FIGURE 17.45d Mode B2 (quadrant II): forward regenerative braking with $V_1 < V_2$.

For Mode B2, condition $V_1 < V_2$ is shown in Fig. 17.45d. Because $V_1 < V_2$, two capacitors C_1 and C_2 are connected in parallel. During the switch-**on** state, switches S_2, S_4, S_6 and S_8 are closed. In this case capacitors $C_1//C_2$ are charged via the circuit V_2–S_2–$C_1//C_2$–S_4, and the voltage across capacitors C_1 and C_2 is increasing. During the switch-**off** state, switches S_1, S_4, S_6 and S_8 are closed. In this case capacitors $C_1//C_2$ are discharged via the circuit S_1–V_1–S_4–$C_1//C_2$, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. Therefore, we have $I_2 = I_1$.

The average capacitor voltage is:

$$V_C = kV_2 + (1-k)V_1$$

The average current

$$I_1 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{V_C - V_1}{R}$$

and

$$I_2 = \frac{1}{T}\int_{0}^{kt} i_C(t)dt \approx k\frac{V_2 - V_C}{R}$$

The transfer efficiency is

$$\eta_{B2} = \frac{P_O}{P_I} = \frac{1-k}{k}\frac{V_1}{V_2}\frac{V_C - V_1}{V_2 - V_C} = \frac{V_1}{V_2}$$

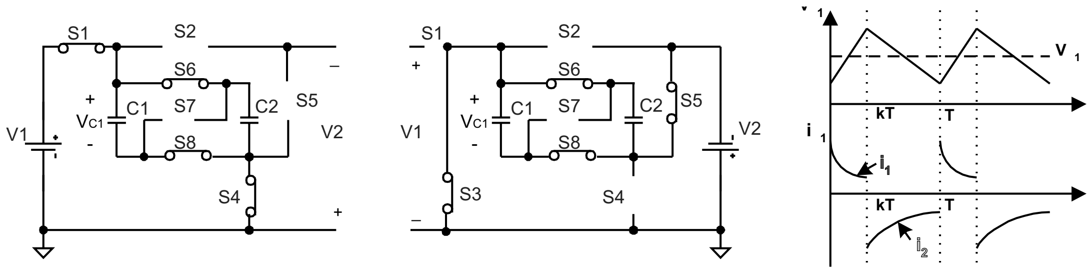
For Mode C1, condition $V_1 > |V_2|$ is shown in Fig. 17.45e. As $V_1 > |V_2|$, two capacitors C_1 and C_2 are connected in parallel. During the switch-**on** state, switches S_1, S_4, S_6 and S_8 are closed. In this case capacitors $C_1//C_2$ are charged via the circuit V_1–S_1–$C_1//C_2$–S_4, and the voltage across capacitors C_1 and C_2 is increasing. During the switch-**off** state, switches S_3, S_5, S_6 and S_8 are closed. Capacitors C_1 and C_2 are discharged via the circuit S_3–V_2–S_5–$C_1//C_2$, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the source to the load. We have $I_1 = I_2$.

The average capacitor voltage is

$$V_C = kV_1 + (1-k)|V_2|$$

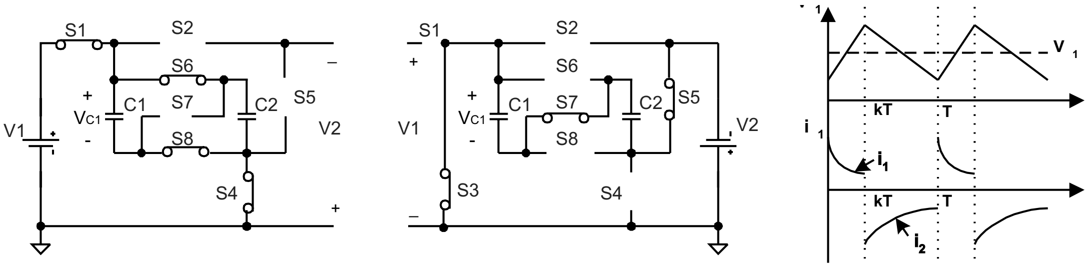
The average current (absolute value) is

$$I_2 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{V_C - |V_2|}{R}$$



(i) Switch-on: *S1*, *S4*, *S6* & *S8* on (ii) Switch-off: *S3*, *S5*, *S6* & *S8* on (iii) Waveforms

FIGURE 17.45e Mode C1 (quadrant III): reverse motoring with $V_1 > |V_2|$.



(i) Switch-on: *S1*, *S4*, *S6* & *S8* on (ii) Switch-off: *S3*, *S5* & *S7* on (iii) Waveforms

FIGURE 17.45f Mode C2 (quadrant III): reverse motoring with $V_1 < |V_2|$.

and the average input current is

$$I_1 = \frac{1}{T}\int_0^{kT} i_C(t)dt \approx k\frac{V_1 - V_C}{R}$$

The transfer efficiency is

$$\eta_{C1} = \frac{P_O}{P_I} = \frac{1-k}{k}\frac{|V_2|}{V_1}\frac{V_C - |V_2|}{V_1 - V_C} = \frac{|V_2|}{V_1}$$

For Mode C2, condition $V_1 < |V_2|$ is shown in Fig. 17.45f. As $V_1 < |V_2|$, two capacitors C_1 and C_2 are connected in parallel during switch-on and in series during switch-off, applying the *voltage-lift technique*. During the switch-**on** state, switches S_1, S_4, S_6 and S_8 are closed. Capacitors C_1 and C_2 are charged via the circuit V_1–S_1–$C_1//C_2$–S_4, and the voltage across capacitors C_1 and C_2 is increasing. During switch-**off** state, switches S_3, S_5 and S_7 are closed. Capacitors C_1 and C_2 are discharged via the circuit S_3–V_2–S_5–C_1–S_7–C_2, and the voltage across capacitor C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the source to the load. We have $I_1 = 2I_2$.

The average capacitor voltage is

$$V_C = \frac{0.5V_1 + |V_2|}{2.5} = 11.2 \text{ V}$$

The average currents

$$I_2 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{2V_C - |V_2|}{R}$$

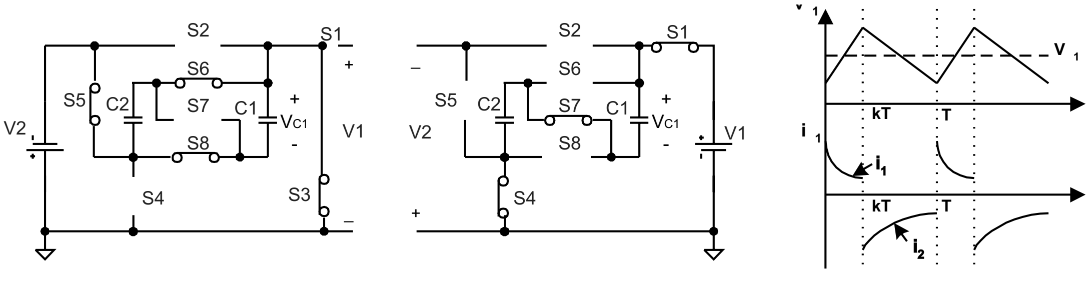
and

$$I_1 = \frac{1}{T}\int_0^{kT} i_C(t)dt \approx k\frac{V_1 - V_C}{R}$$

The transfer efficiency is

$$\eta_{C2} = \frac{P_O}{P_I} = \frac{1-k}{k}\frac{|V_2|}{V_1}\frac{2V_C - |V_2|}{V_1 - V_C} = \frac{|V_2|}{2V_1}$$

For Mode D1, condition $V_1 > |V_2|$ is shown in Fig. 17.45g. Because $V_1 > |V_2|$, two capacitors C_1 and C_2 are connected in parallel during switch-on and in series during switch-off, applying the *voltage-lift technique*. During the switch-**on** state, switches S_3, S_5, S_6 and S_8 are closed. In this case capacitors $C_1//C_2$ are charged via the circuit V_2–S_3–$C_1//C_2$–S_5, and the voltage across capacitors C_1 and C_2 is increasing. During the switch-**off** state, switches S_1, S_4 and S_7 are closed. Capacitors C_1 and C_2 are discharged via the circuit S_1–V_1–S_4–C_2–S_7–C_1, and the voltage across capacitors C_1 and C_2 is



(i) Switch-on: *S3*, *S5*, *S6* & *S8* on (ii) Switch-off: *S1*, *S4* & *S7* on (iii) Waveforms

FIGURE 17.45g Mode D1 (quadrant IV): reverse regenerative braking with $V_1 > |V_2|$.

decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. We have $I_2 = 2I_1$.

The average capacitor voltage is

$$V_C = \frac{0.5|V_2| + V_1}{2.5} = 11.2$$

The average currents

$$I_1 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{2V_C - V_1}{R}$$

and

$$I_2 = \frac{1}{T}\int_{0}^{kT} i_C(t)dt \approx k\frac{|V_2| - V_C}{R}$$

The transfer efficiency is

$$\eta_{D1} = \frac{P_O}{P_I} = \frac{1-k}{k}\frac{V_1}{|V_2|}\frac{2V_C - V_1}{|V_2| - V_C} = \frac{V_1}{2|V_2|}$$

For Mode D2, condition $V_1 < |V_2|$ is shown in Fig. 17.45h. As $V_1 < |V_2|$, two capacitors C_1 and C_2 are connected in parallel. During switch-**on** state, switches S_3, S_5, S_6 and S_8 are closed. In this case capacitors $C_1//C_2$ are charged via the circuit V_2–S_3–$C_1//C_2$–S_5, and the voltage across capacitors C_1 and C_2 is increasing. During the switch-**off** state, switches S_1, S_4, S_6 and S_8 are closed. Capacitors C_1 and C_2 are discharged via the circuit S_1–V_1–S_4–$C_1//C_2$, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. We have $I_2 = I_1$.

The average capacitor voltage is

$$V_C = k|V_2| + (1-k)V_1$$

The average currents

$$I_1 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{V_C - V_1}{R}$$

and

$$I_1 \frac{1}{T}\int_{0}^{kT} i_C(t)dt \approx k\frac{V_1 - V_C}{R}$$

The transfer efficiency is

$$\eta_{D1} = \frac{P_O}{P_I} = \frac{1-k}{k}\frac{|V_2|}{V_1}\frac{2V_C - |V_2|}{V_1 - V_C} = \frac{|V_2|}{2V_1}$$

For Mode D1, condition $V_1 > |V_2|$ is shown in Fig. 17.45g. Because $V_1 > |V_2|$, two capacitors C_1 and C_2 are connected in parallel during switch-on and in series during switch-off, applying the *voltage-lift technique*. During the switch-**on** state, switches S_3, S_5, S_6 and S_8 are closed. In this case capacitors $C_1//C_2$ are charged via the circuit V_2–S_3–$C_1//C_2$–S_5, and the voltage across capacitors C_1 and C_2 is increasing. During the switch-**off** state takes S_1, S_4 and S_7 are closed. Capacitors C_1 and C_2 are discharged via the circuit S_1–V_4–S_4–C_2–S_7–C_1, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. We have $I_2 = 2I_1$.

The average capacitor vaoltage is

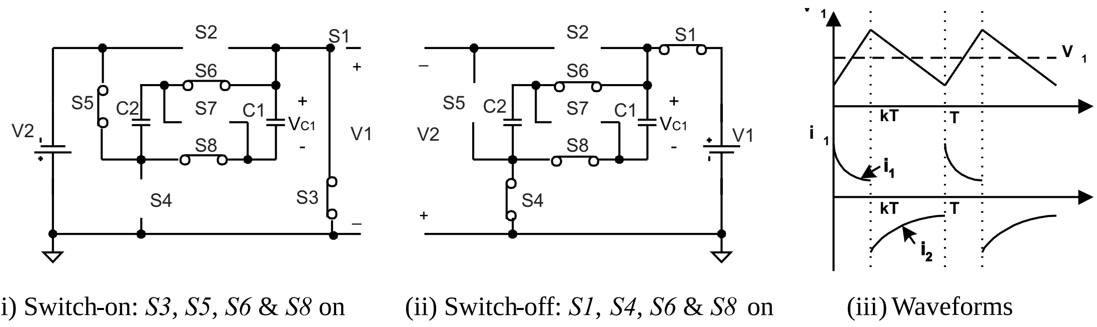
$$V_C = \frac{0.5|V_2| + V_1}{2.5} = 11.2$$

The average currents

$$I_1 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{2V_C - V_1}{R}$$

and

$$I_2 = \frac{1}{T}\int_{0}^{kT} i_C(t)dt \approx k\frac{|V_2| - V_C}{R}$$



(i) Switch-on: *S3*, *S5*, *S6* & *S8* on (ii) Switch-off: *S1*, *S4*, *S6* & *S8* on (iii) Waveforms

FIGURE 17.45h Mode d2 (quadrant IV): reverse regenerative braking with $V_1 < |V_2|$.

The transfer efficiency is

$$\eta_{D1} = \frac{P_O}{P_I} = \frac{1-k}{k}\frac{V_1}{|V_2|}\frac{2V_C - V_1}{|V_2| - V_C} = \frac{V_1}{2|V_2|}$$

For Mode D2, condition $V_1 < |V_2|$ is shown in Fig. 17.45h. As $V_1 < |V_2|$, two capacitors C_1 and C_2 are connected in parallel. During switch-**on** state, switches S_3, S_5, S_6 and S_8 are closed. In this case capacitors $C_1//C_2$ are charged via the circuit V_2–S_3–$C_1//C_2$–S_5, and the voltage across capacitors C_1 and C_2 is increasing. During the switch-**off** state, switches S_1, S_4, S_6 and S_8 are closed. Capacitors C_1 and C_2 are discharged via the circuit S_1–V_1–S_4–$C_1//C_2$, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. We have $I_2 = I_1$.

The average capacitor voltage is

$$V_C = k|V_2| + (1-k)V_1$$

The average capacitor currents

$$I_1 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{V_C - V_1}{R}$$

and

$$I_1 \frac{1}{T}\int_{0}^{kT} i_C(t)dt \approx k\frac{V_1 - V_C}{R}$$

The transfer efficiency is

$$\eta_{D2} = \frac{P_O}{P_I} = \frac{1-k}{k}\frac{|V_2|}{V_1}\frac{2V_C - |V_2|}{V_1 - V_C} = \frac{|V_2|}{2V_1}$$

17.7 Switched-Inductor MultiQuadrant Luo-Converters

Switched-capacitor converters usually have many switches and capacitors, especially for a system with a high ratio between source and load voltages. The switched inductor converter usually has only one inductor even if it works in single-, two- and/or four-quadrant operation. Simplicity is the main advantage of all switched inductor converters.

Switched inductor multiquadrant Luo-converters are third-generation converters, and they have only one inductor. These converters have been derived from chopper circuits, and they have three modes:

- two-quadrant switched-inductor dc/dc Luo-converter in forward operation;
- two-quadrant switched-inductor dc/dc Luo-converter in reverse operation; and
- four-quadrant switched-inductor dc/dc Luo-converter.

The two-quadrant switched-inductor dc/dc Luo-converter in forward operation has been derived for the energy transmission of a dual-voltage system; both source and load voltages are positive polarity. It performs in the first-quadrant Q_{I} and the second quadrant Q_{II} corresponding to the dc motor forward operation in motoring and regenerative braking states.

The two-quadrant switched-inductor dc/dc Luo-converter in reverse operation has been derived for the energy transmission of a dual-voltage system. The source voltage is positive and the load voltage is negative polarity. It performs in the third-quadrant Q_{III} and the fourth-quadrant Q_{IV} corresponding to the dc motor reverse operation in motoring and regenerative braking states.

The four-quadrant switched-inductor dc/dc Luo-converter has been derived for the energy transmission of a dual-voltage system. The source voltage is positive and the load voltage can be positive or negative polarity. It performs four-quadrant operation corresponding to the dc motor forward and reverse operation in motoring and regenerative braking states.

17.7.1 Two-Quadrant Switched-Inductor DC/DC Luo-Converter in Forward Operation

The **F 2Q SI Luo-converter** shown in Fig. 17.46 has two switches with two passive diodes, two inductors and one capacitor. The source voltage (V_1) and load voltage (V_2) are usually considered as constant voltages. The load can be a battery or motor back-electromotive force (EMF). For example, the source voltage is 42 V and load voltage is +14 V. There are two modes of operation:

1. Mode A (Quadrant I) electrical energy is transferred from source side V_1 to load side V_2; and
2. Mode B (Quadrant II) electrical energy is transferred from load side V_2 to source side V_1.

Mode A. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.47a,b. The typical

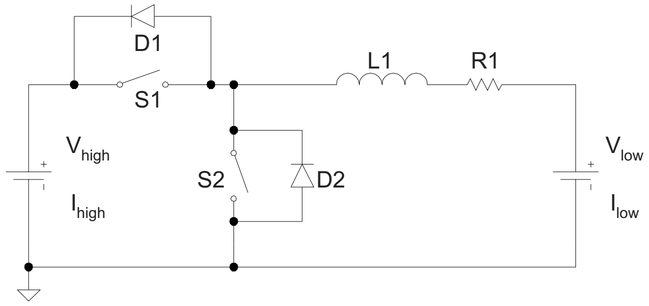


FIGURE 17.46 Switched inductor quadrant I and II dc/dc Luo-converter.

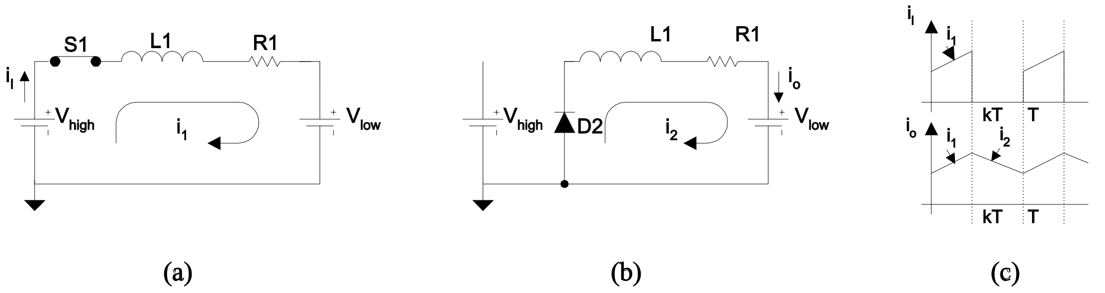

S1
L1
R1
i_I
V_{high}
i_1
V_{low}
(a)
L1
R1
i_o
V_{high}
D2
i_2
V_{low}
(b)
i_I
i_1
kT
T
i_o
i_1
i_2
kT
T
(c)

FIGURE 17.47 Mode A of F 2Q SI Luo-converter: (a) on state-S1 on; (b) off state-S1 off; and (c) input and output current waveforms.

output voltage and current waveforms are shown in Fig. 17.47c.

The average inductor current I_L is

$$I_L = \frac{kV_1 - V_2}{R}$$

The variation ratio of the inductor current i_L is

$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)V_1}{kV_1 - V_2}\frac{R}{2fL}$$

The power transfer efficiency

$$\eta_A = \frac{P_O}{P_I} = \frac{V_2}{kV_1}$$

The boundary between continuous and discontinuous regions is defined: $\zeta \geq 1$, that is,

$$\frac{k(1-k)V_1}{kV_1 - V_2}\frac{R}{2fL} \geq 1$$

or

$$k \leq \frac{V_2}{V_1} + k(1-k)\frac{R}{2fL}$$

The average inductor current I_L in the discontinuous region is

$$I_L = \frac{V_1}{V_2 + RI_L}\frac{V_1 - V_2 - RI_L}{2fL}k^2$$

The power transfer efficiency

$$\eta_{A-dis} = \frac{P_O}{P_I} = \frac{V_2}{V_2 + RI_L}$$

with

$$k \leq \frac{V_2}{V_1} + k(1-k)\frac{R}{2fL}$$

Mode B. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.48a,b. The typical output voltage and current waveforms are shown in Fig. 17.48c.

The average inductor current I_L is

$$I_L = \frac{V_2 - (1-k)V_1}{R}$$

The variation ratio of the inductor current i_L is

$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)V_1}{V_2 - (1-k)V_1}\frac{R}{2fL}$$

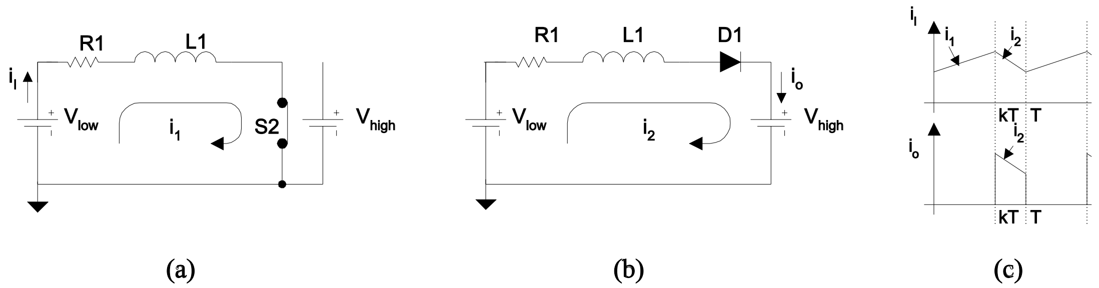

R1
L1
i_I
V_{low}
i_1
S2
V_{high}
(a)
R1
L1
D1
i_o
V_{low}
i_2
V_{high}
(b)
i_I
i_1
i_2
kT
T
i_o
i_2
kT
T
(c)

FIGURE 17.48 Mode B of F 2Q SI Luo-converter: (a) on state-S2 on; (b) off state-D1 on, S2 off; and (c) input and output current waveforms.

The power transfer efficiency

$$\eta_B = \frac{P_O}{P_I} = \frac{(1-k)V_1}{V_2}$$

The boundary between continuous and discontinuous regions is defined: $\zeta \geq 1$ that is

$$\frac{k(1-k)V_1}{V_2-(1-k)V_1}\frac{R}{2fL} \geq 1 \quad \text{or} \quad k \leq \left(1-\frac{V_2}{V_1}\right) + k(1-k)\frac{R}{2fL}$$

The average inductor current I_L in the discontinuous region is

$$I_L = \frac{V_1}{V_1 - V_2 + RI_L}\frac{V_2 - RI_L}{2fL}k^2$$

The power transfer efficiency

$$\eta_{B-dis} = \frac{P_O}{P_I} = \frac{V_2 - RI_L}{V_2}$$

with

$$k \leq \left(1-\frac{V_2}{V_1}\right) + k(1-k)\frac{R}{2fL}$$

17.7.2 Two-Quadrant Switched-Inductor DC/DC Luo-Converter in Reverse Operation

The **R 2Q SI Luo-converter** shown in Fig. 17.49 consists of two switches with two passive diodes, two inductors and one capacitor. The source voltage (V_1) and load voltage (V_2) are usually considered as constant voltages. The load can be a battery or motor back-electromotive force (EMF). For example, the source voltage is 42 V and load voltage is −14 V. There are two modes of operation:

1. Mode C (Quadrant III): electrical energy is transferred from source side V_1 to load side $-V_2$;
2. Mode D (Quadrant IV): electrical energy is transferred from load side $-V_2$ to source side V_1.

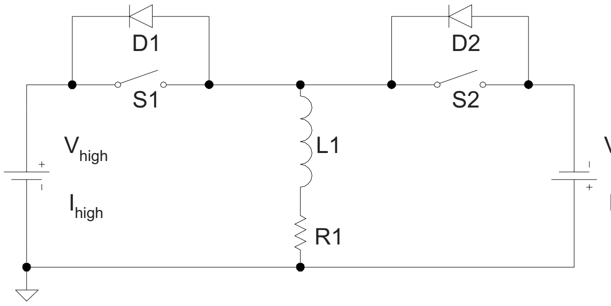


FIGURE 17.49 Switched inductor quadrant III and IV dc/dc Luo-converter.

Mode C. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.50a,b. The typical output voltage and current waveforms are shown in Fig. 17.50c.

The average inductor current I_L is

$$I_L = \frac{kV_1 - (1-k)V_2}{R}$$

The variation ratio of the inductor current i_L is

$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)(V_1+V_2)}{kV_1-(1-k)V_2}\frac{R}{2fL}$$

The power transfer efficiency

$$\eta_C = \frac{P_O}{P_I} = \frac{(1-k)V_2}{kV_1}$$

The boundary between continuous and discontinuous regions is defined: $\zeta \geq 1$

$$\frac{k(1-k)(V_1+V_2)}{kV_1-(1-k)V_2}\frac{R}{2fL} \geq 1 \quad \text{or} \quad k \leq \frac{V_2}{V_1+V_2} + k(1-k)\frac{R}{2fL}$$

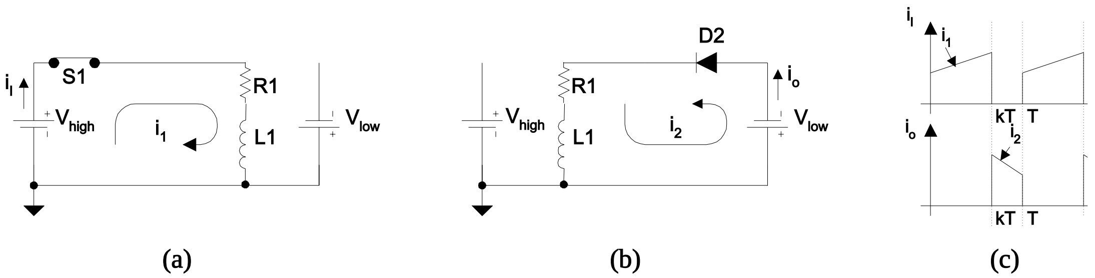


FIGURE 17.50 Mode C of F 2Q SI Luo-converter: (a) on state-S_1on; (b) off state-D_2 on, S_1 off; (c) input and output current waveforms.

The average inductor current I_L in the discontinuous region is

$$I_L = \frac{V_1 + V_2}{V_2 + RI_L}\frac{V_1 - RI_L}{2fL}k^2$$

The power transfer efficiency

$$\eta_{C-dis} = \frac{P_O}{P_1} = \frac{V_2}{V_1}\frac{V_1 - RI_L}{V_2 + RI_L}$$

with

$$k \leq \frac{V_2}{V_1 + V_2} + k(1-k)\frac{R}{2fL}$$

Mode D. The equivalent circuits during switch-on and switch-off periods are shown in Fig. 17.51a,b. typical output voltage and current waveforms are shown in Fig. 17.51c.

The average inductor current I_L is

$$I_L = \frac{kV_2 - (1-k)V_1}{R}$$

The variation ratio of the inductor current i_L is

$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)(V_1 + V_2)}{kV_2 - (1-k)V_1}\frac{R}{2fL}$$

The power transfer efficiency

$$\eta_D = \frac{P_O}{P_I} = \frac{(1-k)V_1}{kV_2}$$

The boundary between continuous and discontinuous regions is defined: $\zeta \geq 1$

$$\frac{k(1-k)(V_1 + V_2)}{kV_2 - (1-k)V_1}\frac{R}{2fL} \geq 1 \quad \text{or} \quad k \leq \frac{V_a}{V_1 + V_2} + k(1-k)\frac{R}{2fL}$$

The average inductor current I_L in the discontinuous region is

$$I_L = \int_0^{t_4} = \frac{V_1 + V_2}{V_1 + RI_L}\frac{V_2 - RI_L}{2fL}k^2$$

The power transfer efficiency

$$\eta_{D-dis} = \frac{P_O}{P_I} = \frac{V_1}{V_2}\frac{V_2 - RI_L}{V_1 + RI_L}$$

with

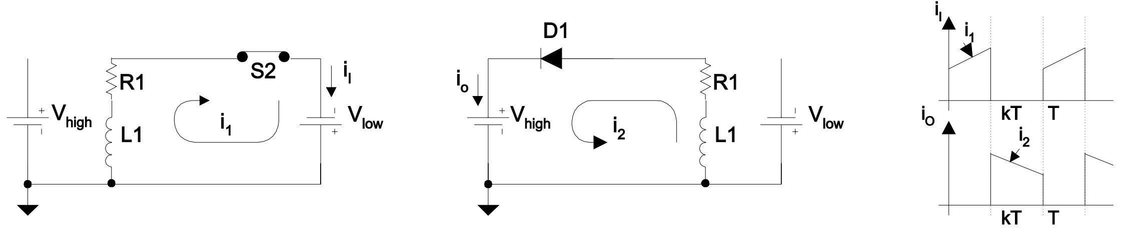
$$k \leq \frac{V_1}{V_1 + V_2} + k(1-k)\frac{R}{2fL}$$

17.7.3 Four-Quadrant Switched-Inductor DC/DC Luo-Converter

Switched inductor dc/dc converters successfully overcome the disadvantage of switched-capacitor converters. Usually, only one inductor is required for each converter with 1- or 2- or 4-quadrant operation no matter how large the difference of the input and output voltages. Therefore, the switched inductor converter has a very simple topology and circuit. Consequently, it has high power density. Here a *switched inductor four-quadrant dc/dc Luo-converter* is introduced.

This converter is shown in Fig. 17.52 and it consists of three switches, two diodes and only one inductor L. The source voltage V_1 and load voltage V_2 (e.g., a battery or dc motor back-EMF) are usually constant voltages; R is the equivalent resistance of the circuit, and it is usually small; $V_1 > |V_2|$, and are assumed to +42 and ±14 V, respectively. Therefore, there are four quadrants (modes) of operation:

1. Mode A the energy is transferred from source to positive voltage load; the first quadrant-operation Q_{I};
2. Mode B the energy is transferred from positive voltage load to source; the second quadrant-operation Q_{II};



(a) (b) (c)

FIGURE 17.51 Mode D of F 2Q SI Luo-converter. (a) on state-S_2 on; (b) off state-D_1 on, S_2 off; (c) input and output current waveforms.

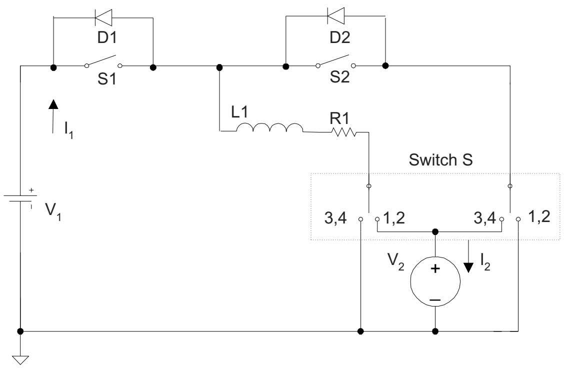


FIGURE 17.52 Four-quadrant switched inductor dc/dc Luo-converter.

3. Mode C the energy is transferred from source to negative voltage load; the third quadrant-operation Q_{III};
4. Mode C the energy is transferred from negative voltage load to source; the fourth quadrant-operation Q_{IV};

The first quadrant is the so-called forward motoring (Forw. Mot.) operation; V_1 and V_2 are positive, and I_1 and I_2 are positive as well. The second quadrant is the so-called forward regenerative (Forw. Reg.) braking operation; V_1 and V_2 are positive, and I_1 and I_2 are negative. The third quadrant is the so-called reverse motoring (Rev. Mot.) operation; V_1 and I_1 are positive, and V_2 and I_2 are negative. The fourth quadrant is the so-called reverse regenerative (Rev. Reg.) braking operation; V_1 and I_2 are positive, and I_1 and V_2 are negative. Each mode has two states: "on" and "off." Usually, each state is operating in a different conduction duty k. The switching period is T where $T = 1/f$. The switch status is shown in Table 17.4.

Mode A is shown in Fig. 17.47. During the switch-**on** state, switch S_1 is closed. In this case the source voltage V_1 supplies the load V_2 and inductor L, and inductor current i_L increases. During the switch-**off** state, diode D_2 is on. In this case current i_L flows through the load V_2 via the freewheeling diode D_2, and it decreases.

Mode B is shown in Fig. 17.48. During the switch-**on** state, switch S_2 is closed. In this case the load voltage V_2 supplies the inductor L, and inductor current i_L increases. During the switch-**off** state, diode D_1 is on, and current i_L flows through the source V_1 and load V_2 via the diode D_1, and it decreases.

TABLE 17.4 Switch status (none of the mentioned switches are off)

Q No.	State	S_1	D_1	S_2	D_2	S_3	Source	Load
Q_I, Mode A	ON	ON				ON 1/2	V_1+	V_2+
Forw. Mot.	OFF				ON	ON 1/2	I_1+	I 2
Q_{II}, Mode B	ON			ON		ON 1/2	V_1+	V_2+
Forw. Reg.	OFF		ON			ON 1/2	I_1-	I_2-
Q_{III}, Mode C	ON	ON				ON 3/4	V_1+	V_2-
Rev. Mot.	OFF				ON	ON 3/4	I_1+	I_2-
Q_{IV}, Mode D	ON			ON		ON 3/4	V_1+	V_2-
Rev. Reg.	OFF		ON			ON 3/4	I_1-	I_2+

Mode C is shown in Fig. 17.50. During the switch-**on** state, switch S_1 is closed. The source voltage V_1 supplies the inductor L, and inductor current i_L increases. During the switch-**off** state, diode D_2 is on. Current i_L flows through the load V_2 via the freewheeling diode D_2, and it decreases.

Mode D is shown in Fig. 17.51. During the switch-**on** state, switch S_2 is closed. The load voltage V_2 supplies the inductor L, and inductor current i_L increases. During the switch-**off** state, diode D_1 is on. Current i_L flows through the source V_1 via the diode D_1, and it decreases.

All descriptions of the Modes A, B, C, and D are the same as in Sections 17.7.1 and 17.7.2.

17.8 Multi uadrant CS uasi-Resonant Luo-Converters

Soft-switching converters are fourth-generation converters, consisting only of an inductor or capacitors. They usually perform in the systems between two voltage sources V_1 and V_2. Voltage source V_1 is positive voltage and voltage V_2 is the load voltage that can be positive or negative. In this study, both voltages are constant voltages. As V_1 and V_2 are constant values, the voltage-transfer gain is constant. Our research will concentrate on the working current and the power transfer efficiency η. The resistance R of the inductor has to be considered for the power transfer efficiency η calculation.

From a review of the literature, we found that almost all the papers investigated switched-component converters working in the single-quadrant operation. Luo and his colleagues have developed this technique into the multiquadrant operation, which will be described in what follows.

Multiquadrant ZCS quasi-resonant Luo-converters are fourth-generation converters. Because these converters implement the zero-current-switching technique, they have the advantages of high power density, high-power transfer efficiency, low EMI, and reasonable EMC. They have three modes:

- two-quadrant ZCS quasi-resonant dc/dc Luo-converter in forward operation;
- two-quadrant ZCS quasi-resonant dc/dc Luo-converter in reverse operation; and
- four-quadrant ZCS quasi-resonant dc/dc Luo-converter.

The two-quadrant ZCS quasi-resonant dc/dc Luo-converter in forward operation is for the energy transmission of a dual-voltage system. Both source and load voltages are positive polarity. It performs in the first-quadrant Q_I and the second-quadrant Q_{II} corresponding to the dc motor forward operation in motoring and regenerative braking states.

The two-quadrant ZCS quasi-resonant dc/dc Luo-converter in reverse operation is also for the energy transmission of a dual-voltage system, but in this case the source voltage is positive and the load voltage is negative polarity. It performs in the third-quadrant Q_{III} and the fourth-quadrant Q_{IV} corresponding to the dc motor reverse operation in motoring and regenerative braking states.

The four-quadrant ZCS quasi-resonant dc/dc Luo-converter is for the energy transmission of a dual-voltage system. The source voltage is positive, and load voltage can be positive or negative polarity. It performs four-quadrant operation corresponding to the dc motor forward and reverse operation in motoring and regenerative braking states.

17.8.1 Two-Quadrant ZCS Quasi-Resonant Luo-Converter in Forward Operation

As both voltages are low, this converter is designed as a zero-current-switching quasi-resonant converter (ZCS-QRC). It is shown in Fig. 17.53. This converter consists of one main inductor L and two switches with their auxiliary components. Assuming that the main inductance is sufficiently large, the current i_L is constant. The source voltage V_1 and load voltage V_2 are usually constant $V_1 = 42\,\text{V}$ and $V_2 = 14\,\text{V}$. There are two modes of operation:

1. Mode A (Quadrant I) — electrical energy is transferred from V_1 side to V_2 side; and
2. Mode B (Quadrant II) — electrical energy is transferred from V_2 side to V_1 side.

Each mode has two states: "on" and "off." The switch status of each state is shown in Table 17.5.

Mode A is a ZCS buck converter. The equivalent circuit, current and voltage waveforms are shown in Fig. 17.54. There are four time regions for the switching-on and switching-off period. The conduction duty cycle is $k = (t_1 + t_2)$ when the input current flows through the switch S_1 and inductor L. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. Some formulas are listed in the following:

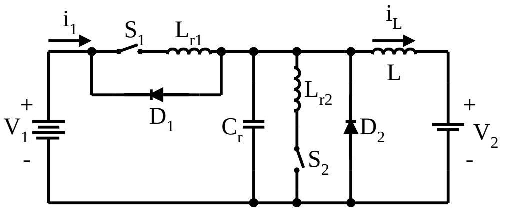


FIGURE 17.53 Two-quadrant $(Q_I + Q_{II})$ dc/dc ZCS quasi-resonant Luo-converter.

TABLE 17.5 Switch status (the blank space means off)

Switch or Diode	Mode A (Q-I)		Mode B (Q-II)	
	State-on	State-off	State-on	State-off
S_1	ON			
D_1				ON
S_2			ON	
D_2		ON		

$$\omega_1 = \frac{1}{\sqrt{L_{r1} C_r}} \qquad Z_1 = \sqrt{\frac{L_{r1}}{C_r}} \quad \text{and} \quad i_{1-peak} = I_L + \frac{V_1}{L_1}$$

$$t_1 = \frac{I_L L_{r1}}{V_1} \quad \text{and} \quad \alpha_1 = \sin^{-1}\left(\frac{I_L z_1}{V_1}\right)$$

$$t_2 = \frac{1}{\omega_1}(\pi + \alpha_1) \quad \text{and} \quad v_{CO} = V_1(1 + \cos\alpha_1)$$

$$t_3 = \frac{v_{CO} C_r}{I_L} \quad \text{and} \quad \frac{I_L V_2}{V_1} = \frac{t_1 + t_2}{T}\left(I_L + \frac{V_1}{Z_1}\frac{\cos\alpha_1}{\pi/2 + \alpha_1}\right)$$

$$t_4 = \frac{V_1(t_1 + t_2)}{V_2 I_L}\left(I_L + \frac{V_1}{Z_1}\frac{\cos\alpha_1}{\pi/2 + \alpha_1}\right) - (t_1 + t_2 t_3)$$

$$k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \qquad T = t_1 + t_2 + t_3 + t_4 \quad \text{and} \quad f = 1/T$$

Mode B is a ZCS boost converter. The equivalent circuit, current and voltage waveforms are shown in Fig. 17.55. There are four time regions for the switching-on and switching-off period. The conduction duty cycle is $k = (t_1 + t_2)$, but the output current flows only through the source V_1 in the period

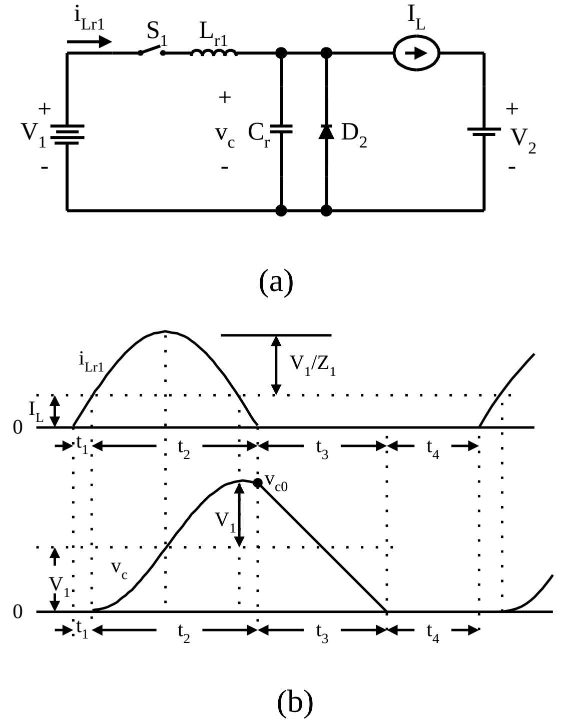
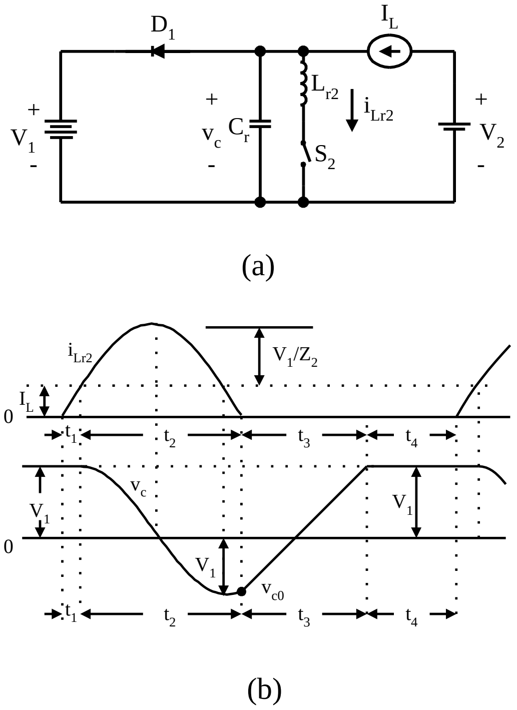


FIGURE 17.54 Mode A operation: (a) equivalent circuit; (b) waveforms.



(a)

(b)

FIGURE 17.55 Mode B operation: (a) equivalent circuit; (b) waveforms.

t_4. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. Some formulas are listed in what follows:

$$\omega_2 = \frac{1}{\sqrt{L_{r2} C_r}} \quad Z_2 = \sqrt{\frac{L_{r2}}{C_r}} \quad \text{and} \quad i_{2-peak} = I_L + \frac{V_1}{Z_2}$$

$$t_1 = \frac{I_L L_{r2}}{V_1} \quad \text{and} \quad \alpha_2 = \sin^{-1}\left(\frac{I_L Z_2}{V_1}\right)$$

$$t_2 = \frac{1}{\omega_2}(\pi + \alpha_2) \quad \text{and} \quad v_{CO} = -V_1 \cos\alpha_2$$

$$t_3 = \frac{(V_1 - v_{CO})C_r}{I_L} \quad \text{and} \quad \frac{I_L V_2}{V_1} = \frac{t_4}{T} I_L \quad \text{or}$$

$$\frac{V_2}{V_1} = \frac{t_4}{T} = \frac{t_4}{t_1 + t_2 + t_3 + t_4}$$

$$t_4 = \frac{t_1 + t_2 + t_3}{\dfrac{V_1}{V_2} - 1}$$

$$k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \quad T = t_1 + t_2 + t_3 + t_4 \quad \text{and} \quad f = 1/T$$

17.8.2 Two- uadrant CS uasi-Resonant Luo-Converter in Reverse Operation

The **two-quadrant CS quasi-resonant Luo-converter** in reverse operation is shown in Fig. 17.56. It is a new soft switching technique with two-quadrant operation, which effectively reduces the power losses and largely increases the power transfer efficiency. It consists of one main inductor L and two switches with their auxiliary components. Assuming that the main inductance L is sufficiently large, the current i_L is constant. The source voltage V_1 and load voltage V_2 are usually constant, for example, $V_1 = 42$ V and $V_2 = -28$ V. There are two modes of operation:

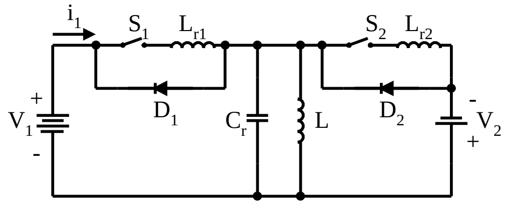


FIGURE 17.56 Two-quadrant (QIII+IV) dc/dc ZCS quasi-resonant Luo-converter.

1. Mode C (Quadrant III) electrical energy is transferred from V_1 side to $-V_2$ side; and
2. Mode D (Quadrant IV) electrical energy is transferred from $-V_2$ side to V_1 side.

Each mode has two states: "on" and "off". The switch status of each state is shown in Table 17.6.

Mode C is a ZCS buck-boost converter. The equivalent circuit, current and voltage waveforms are shown in Fig. 17.57. There are four time regions for the switching-on and switching-off period. The conduction duty cycle is $kT = (t_1 + t_2)$ when the input current flows through the switch S_1 and the main inductor L. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. Some formulas are listed in what follows:

$$\omega_1 = \frac{1}{\sqrt{L_{r1} C_r}} \quad Z_1 = \sqrt{\frac{L_{r1}}{C_r}} \quad \text{and} \quad i_{1-peak} = I_L + \frac{V_1}{Z_1}$$

$$t_1 = \frac{I_L L_{r1}}{V_1 + V_2} \quad \text{and} \quad \alpha_1 = \sin^{-1}\left(\frac{I_L Z_1}{_1 + V_2}\right)$$

$$t_2 = \frac{1}{\omega_1}(\pi + \alpha_1) \quad \text{and} \quad v_{CO} = (V_1 - V_2) + V_1 \sin(\pi/2 + \alpha_1)$$

$$= V_1(1 + \cos\alpha_1) - V_2$$

$$t_3 = \frac{(v_{CO} + V_2)C_r}{I_L} = \frac{V_1(1 + \cos\alpha_1)C_r}{I_L}$$

$$I_1 = \frac{t_1 + t_2}{T}\left(I_L + \frac{V_1}{Z_1}\frac{2\cos\alpha_) 1}{\pi/2 + \alpha_1}\right) \quad \text{and} \quad I_2 = \frac{t_4}{T} I_L$$

$$t_4 = \frac{V - 1(t_1 + t_2)}{V_2 I_L}\left(I_L + \frac{V_1}{Z_1}\frac{2\cos\alpha_1}{\pi/2 + \alpha_1}\right)$$

TABLE 17.6 Switch status (the blank space means off)

Switch or Diode	Mode C (Q-III)		Mode D (Q-IV)	
	State-on	State-off	State-on	State-off
S_1	ON			
D_1				ON
S_2			ON	
D_2		ON		

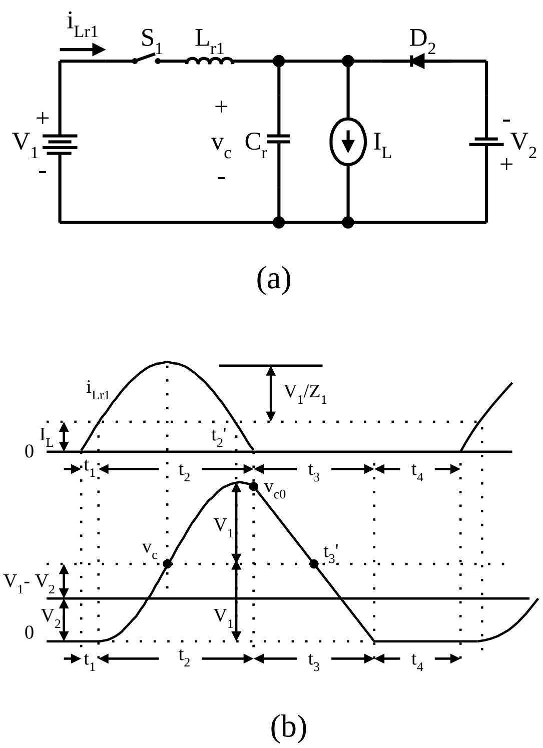

iLr1
S1
Lr1
D2
V1
vc
Cr
IL
V2
(a)
iLr1
V1/Z1
IL
0
t2'
t1
t2
t3
t4
vc0
V1
vc
t3'
V1- V2
V2
0
V1
(b)

FIGURE 17.57 Mode C operation: (a) equivalent circuit; (b) waveforms.

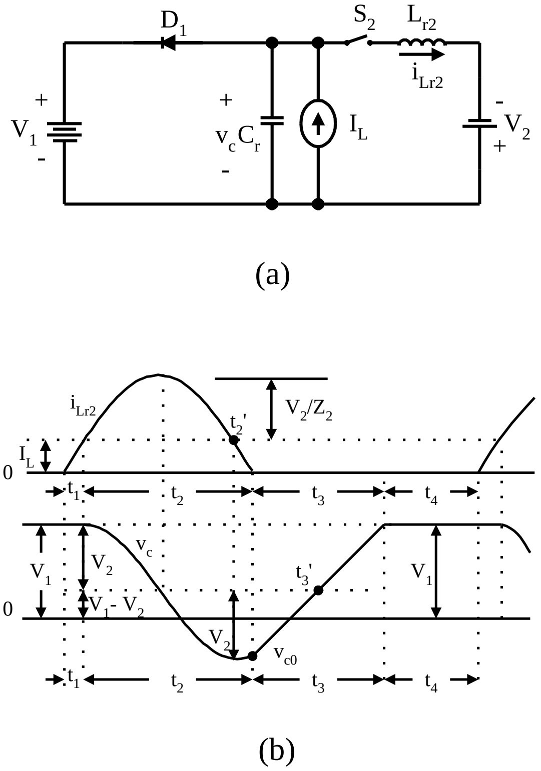

D1
S2
Lr2
iLr2
V1
vc
Cr
IL
V2
(a)
iLr2
V2/Z2
t2'
IL
0
t1
t2
t3
t4
vc
V1
V2
t3'
V1
0
V1- V2
V2
vc0
(b)

FIGURE 17.58 Mode D operation: (a) equivalent circuit; (b) waveforms.

Mode D is a cross ZCS buck-boost converter. The equivalent circuit, current and voltage waveforms are shown in Fig. 17.58. There are four time regions for the switching-on and switching-off period. The conduction duty cycle is $kT = (t_1 + t_2)$, but the output current flows only through the source V_1 in the period t_4. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. Some formulas are listed as follows:

$$\omega_2 = \frac{1}{\sqrt{L_{r2}C_r}} \qquad Z_2 = \sqrt{\frac{L_{r2}}{C_4}} \quad \text{and} \quad i_{2-peak} = I_L + \frac{V_2}{Z_2}$$

$$t_1 = \frac{I_L L_{r2}}{V_1 + V_2} \quad \text{and} \quad \alpha_2 = \sin^{-1}\left(\frac{I_L Z_2}{V_2 + V_2}\right)$$

$$t_2 = \frac{1}{\omega_2}(\pi + \alpha_2) \quad \text{and} \quad v_{CO} = (V_1 - V_2) - V_2 \sin(\pi/2 + \alpha_2)$$

$$= V_1 - V_2(1 + \cos\alpha_2)$$

$$t_3 = \frac{(V_1 - v_{CO})C_r}{I_L} = \frac{V_2(1 + \cos\alpha_2)C_r}{I_L}$$

$$I_2 = \frac{t_1 + t_2}{T}\left(I_L + \frac{V_2}{Z_2}\frac{2\cos\alpha_2}{\pi/2 + \alpha_2}\right) \quad \text{and} \quad I_1 = \frac{t_4}{T} I_L$$

$$t_4 = \frac{V_2(t_1 + t_2)}{V_1 I_L}\left(I_L + \frac{V_2}{Z_2}\frac{2\cos\alpha_2}{\pi/2 + \alpha_2}\right)$$

17.8.3 Four-Quadrant ZCS Quasi-Resonant Luo-Converter

The **four-quadrant ZCS quasi-resonant Luo-converter** is shown in Fig. 17.59. Circuit 1 implements the operation in quadrants I and II, Circuit 2 implements the operation in quadrants III and IV. Circuit 1 and Circuit 2 can be converted to each other by an auxiliary switch. Each circuit consists of one main inductor L and two switches. Assuming that the main inductance L is sufficiently large, the current i_L remains constant. The source and load voltages are usually constant,

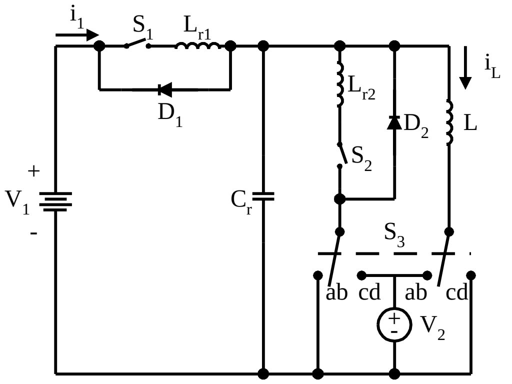

i1
S1
Lr1
D1
iL
Lr2
D2
L
S2
V1
Cr
S3
ab
cd
ab
cd
V2

FIGURE 17.59 Four-quadrant dc/dc ZCS quasi-resonant Luo-converter.

for example, $V_1 = 42\,\text{V}$ and $V_2 = \pm 28\,\text{V}$ [7–9]. There are four modes of operation:

1. Mode A (Quadrant I) electrical energy is transferred from the V_1 side to the V_2 side;
2. Mode B (Quadrant II) electrical energy is transferred from the V_2 side to the V_1 side.
3. Mode C (Quadrant III) electrical energy is transferred from the V_1 side to the $-V_2$ side; and
4. Mode D (Quadrant IV) electrical energy is transferred from the $-V_2$ side to the V_1 side.

Each mode has two states "on" and "off." The switch status of each state is shown in Table 17.7.

The operation of Mode A, B, C, and D is the same as that in the previous Sections 17.8.1 and 17.8.2.

17. Multiquadrant VS Quasi-Resonant Luo-Converters

Multiquadrant ZVS quasi-resonant Luo-converters are fourth-generation converters. Because these converters implement the zero-current-switching technique, they have the advantages of high power density, high-power transfer efficiency, low EMI, and reasonable EMC. They have three modes:

- two-quadrant ZVS quasi-resonant dc/dc Luo-converter in forward operation;
- two-quadrant ZVS quasi-resonant dc/dc Luo-converter in reverse operation; and
- four-quadrant ZVS quasi-resonant dc/dc Luo-converter.

The two-quadrant ZVS quasi-resonant dc/dc Luo-converter in forward operation is derived for the energy transmission of a dual-voltage system. Both source and load voltages are positive polarity. It performs in the first quadrant Q_{I} and the second quadrant Q_{II} corresponding to the dc motor forward operation in motoring and regenerative braking states.

The two-quadrant ZVS quasi-resonant dc/dc Luo-converter in reverse operation is derived for the energy transmission of a dual-voltage system. The source voltage is positive polarity and the load voltage is negative polarity. It performs in the third quadrant Q_{III} and the fourth quadrant Q_{IV} corresponding to the dc motor reverse operation in motoring and regenerative braking states.

The four-quadrant ZVS quasi-resonant dc/dc Luo-converter is derived for the energy transmission of a dual-voltage system. The source voltage is positive polarity, and load voltage can be either positive or negative polarity. It performs four-quadrant operation corresponding to the dc motor forward and reverse operation in motoring and regenerative braking states.

17. .1 Two-Quadrant VS-Quasi-Resonant DC/DC Luo-Converter in Forward Operation

The **two-quadrant VS quasi-resonant Luo-converter** in forward operation is shown in Fig. 17.60. It consists of one main inductor L and two switches with their auxiliary components.

Assuming the main inductance L is sufficiently large, the current i_L is constant. The source voltage V_1 and load voltage V_2 are usually constant, for example, $V_1 = 42\,\text{V}$ and $V_2 = 14\,\text{V}$. There are two modes of operation:

1. Mode A (Quadrant I) electrical energy is transferred from the V_1 side to the V_2 side; and
2. Mode B (Quadrant II) electrical energy is transferred from the V_2 side to the V_1 side.

Each mode has two states "on" and "off." The switch status of each state is shown in Table 17.8.

Mode A is a ZVS buck-converter shown in Fig. 17.61. There are four time-regions for the switching-on and switching-off period. The conduction duty cycle is $kT = (t_3 + t_4)$ when the input current flows through the switch S_1 and the main

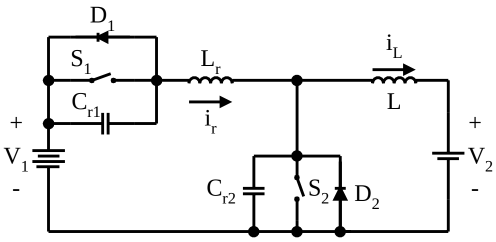


FIGURE 17.60 Two-quadrant (QI+QII) dc/dc ZVS quasi-resonant Luo-converter.

TABLE 17.7 Switch status (the blank space means off)

Circuit // Switch or Diode	Mode A (Q-I)		Mode B (Q-II)		Mode C (Q-III)		Mode D (Q-IV)	
	State-on	State off	State on	State off	State on	State off	State on	State off
Circuit		Circuit 1			Circuit 2			
S_1	ON				ON			
D_1				ON				ON
S_2			ON				ON	
D_2		ON				ON		

TABLE 17.8 Switch status (the blank space means off)

Switch	Mode A (Q-I)		Mode B (Q-II)	
State-on	State-off	State-on	State-off	
S_1	ON			
D_1				ON
S_2			ON	
D_2		ON		

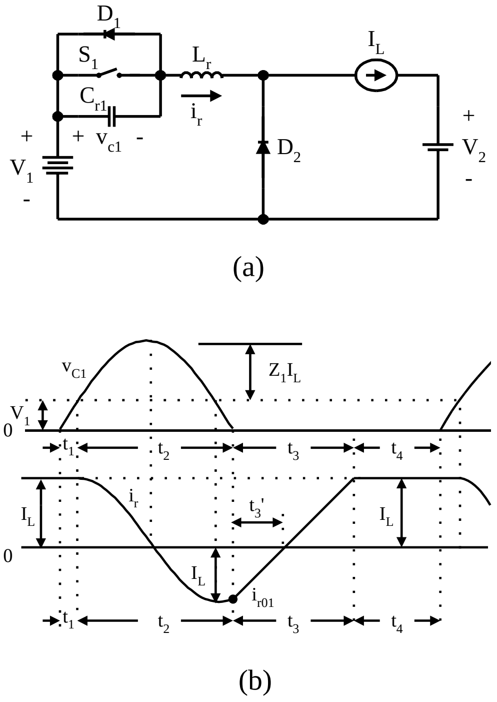


FIGURE 17.61 Mode A operation: (a) equivalent circuit; (b) waveforms.

inductor L. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. Some relevant formulas are listed in the following:

$$\omega_1 = \frac{1}{\sqrt{L_r C_{r1}}} \quad Z_1 = \sqrt{\frac{L_r}{C_{r1}}} \quad \text{and} \quad v_{c1-peak} = V_1 + Z_1 I_L$$

$$t_1 = \frac{V_1 C_{r1}}{I_L} \quad \text{and} \quad \alpha_1 = \sin^{-1}\left(\frac{V_1}{Z_1 I_L}\right)$$

$$t_2 = \frac{1}{\omega_1}(\pi + \alpha_1) \quad \text{and} \quad i_{rO1} = -I_L \cos\alpha_1$$

$$t_3 = \frac{(I_L - i_{rO1})L_r}{V_1} \quad \text{and}$$

$$I_1 = \frac{I_L V_2}{V_1} = \frac{1}{T}\int_{t_3}^{t_4} i_r dt \approx \frac{1}{T}(I_L t_4) = \frac{t_4}{T} I_L$$

$$t_4 = \frac{t_1 + t_2 + t_3}{\frac{V_1}{V_2} - 1} \quad k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4}$$

$$T = t_1 + t_2 + t_3 + t_4 \quad \text{and} \quad f = 1/T$$

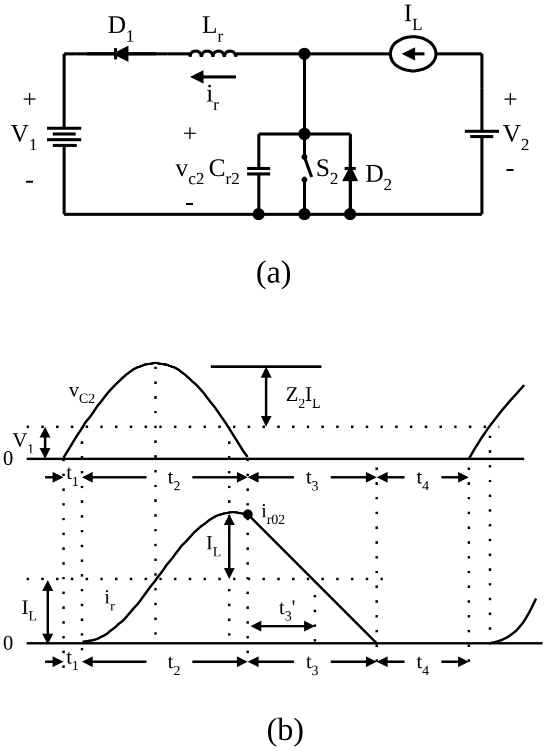


FIGURE 17.62 Mode B operation: (a) equivalent circuit; (b) waveforms.

Mode B is a ZVS boost converter shown in Fig. 17.62. There are four time regions for the switching-on and switching-off period. The conduction duty cycle is $kT = (t_3 + t_4)$, but the output current flows only through the source V_1 in the period $(t_1 + t_2)$. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. Some relevant formulas are listed in the following:

$$\omega_2 \frac{1}{\sqrt{L_r C_{r2}}} \quad Z_2 = \sqrt{\frac{L_r}{C_{r2}}} \quad \text{and} \quad v_{C2-peak} = v_1 + Z_2 I_L$$

$$t_1 = \frac{V_1 C_{r2}}{I_L} \quad \text{and} \quad \alpha_2 = \sin^{-1}\left(\frac{V_1}{Z_2 I_L}\right)$$

$$t_2 = \frac{1}{\omega_2}(\pi + \alpha_2) \quad \text{and} \quad i_{rO2} = I_L(1 + \cos\alpha_2)$$

$$t_3 = \frac{i_{rO2} L_r}{V_1} \quad \text{and} \quad I_1 = \frac{I_L V_2}{V_1} = \frac{1}{T}\int_{t_1}^{t_3} i_r dt$$

$$\approx \frac{1}{T}[I_L(t_2 + t_3)] = \frac{t_2 + t_3}{T} I_L$$

$$\frac{V_2}{V_1} = \frac{1}{T}(t_2 + t_3) = \frac{t_2 + t_3}{t_1 + t_2 + t_3 + t_4}$$

$$t_4 = \left(\frac{V_1}{V_2} - 1\right)(t_2 + t_3) - t_1$$

or

$$k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4} T = t_1 + t_2 + t_3 + t_4 \quad \text{and} \quad f = 1/T$$

17. .2 Two-Quadrant ZVS Quasi-Resonant DC/DC Luo-Converter in Reverse Operation

The **two-quadrant ZVS quasi-resonant Luo-converter** in reverse operation is shown in Fig. 17.63. It consists of one main inductor L and two switches with their auxiliary components. Assuming the main inductance L is sufficiently large, the current i_L is constant. The source voltage V_1 and load voltage V_2 are usually constant, for example, $V_1 = +42$ V and $V_2 = -28$ V. There are two modes of operation:

1. Mode C (Quadrant III) electrical energy is transferred from the V_1 side to the $-V_2$ side; and
2. Mode D (Quadrant IV) electrical energy is transferred from the $-V_2$ side to the V_1 side.

Each mode has two states: "on" and "off." The switch status of each state is shown in Table 17.9.

Mode C is a ZVS buck-boost converter as shown in Fig. 17.64. There are four time regions for the switching-on and switching-off period. The conduction duty cycle is $kT = (t_3 + t_4)$ when the input current flows through the switch S_1 and the main inductor L. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. Some formulas are listed as follows:

$$\omega_1 = \frac{1}{\sqrt{L_r C_{r1}}} \quad Z_1 = \sqrt{\frac{L_r}{C_{R1}}} \quad \text{and} \quad v_{c1-peak} = V_1 + V_2 + Z_1 I_L$$

$$t_1 = \frac{(V_1 + V_2)C_{r1}}{I_L} \quad \text{and} \quad \alpha_1 = \sin^{-1}\left(\frac{V_1 + V_2}{Z_1 I_L}\right)$$

$$t_2 = \frac{1}{\omega_1}(\pi + \alpha_1) \quad \text{and} \quad i_{rO1} = -I_L \sin(\pi/2 + \alpha_1)$$

$$t_3 = \frac{(I_L - i_{rO1})L_r}{V_1} \quad \text{and} \quad I_1 = \frac{I_L V_2}{V_1} = \frac{1}{T}\int_{t_3}^{t_4} i_r dt \approx \frac{1}{T}(I_L t_4) = \frac{t_4}{T} I_L$$

$$t_4 = \frac{t_1 + t_2 + t_3}{\frac{V_1}{V_2} - 1} \quad \text{and} \quad I_2 = \frac{1}{T}\int_{t_2}^{t_3} (I_L - i_r)dt \approx \frac{t_2 + t_3}{T} I_L$$

$$k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4}$$

Mode D is a cross ZVS buck-boost converter as shown in Fig. 17.65. There are four time regions for the switching-on and switching-off period. The conduction duty cycle is $kT =$

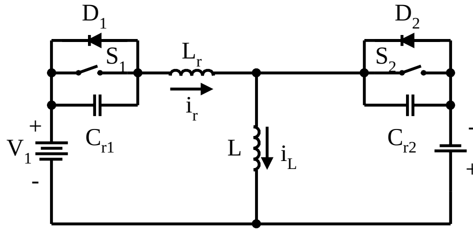


FIGURE 17.63 Two-quadrant (QIII IV) dc/dc ZVS quasi-resonant Luo-converter.

TABLE 17.9 Switch status (the blank space means off)

Switch	Mode C (Q-III)		Mode D (Q-IV)	
	State-on	State-off	State-on	State-off
S_1	ON			
D_1				ON
S_2			ON	
D_2		ON		

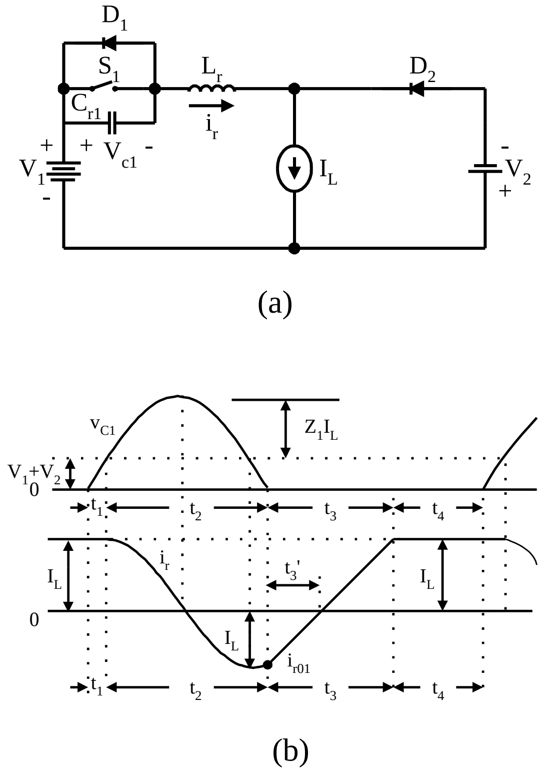


FIGURE 17.64 Mode C operation: (a) equivalent circuit; (b) waveforms.

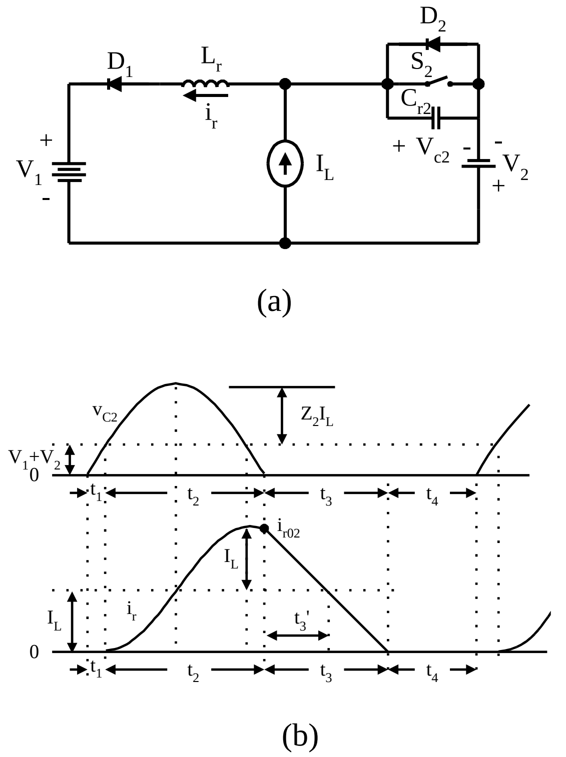


FIGURE 17.65 Mode D operation: (a) equivalent circuit; (b) Wave forms.

$(t_3 + t_4)$, but the output current flows only through the source V_1 in the period $(t_1 + t_2)$. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. Some formulas are listed as follows:

$$\omega_2 = \frac{1}{\sqrt{L_r C_{R2}}} \quad Z_2 = \sqrt{\frac{L_r}{C_{r2}}} \quad \text{and} \quad v_{C2-peak} = V_1 + V_2 + Z_2 I_L$$

$$t_1 = \frac{(V_1 + V_2)C_{r2}}{I_L} \quad \text{and} \quad \alpha_2 = \sin^{-1}\left(\frac{V_1 + V_2}{Z_1 I_L}\right)$$

$$t_2 = \frac{1}{\omega_2}(\pi + \alpha_2) \quad \text{and} \quad i_{rO2} = I_L[1 + \sin(\pi/2 + \alpha_2)]$$

$$t_3 = \frac{i_{rO2} L_r}{V_1 + V_2} \quad I_1 = \frac{1}{T}\int_{t_1}^{t_3} i_r dt \approx \frac{1}{T}[I_L(t_2 + t_3)] = \frac{t_2 + t_3}{T} I_L$$

$$\text{and} \quad I_2 = \frac{1}{T}\int_{t_3}^{t_4} i_r dt \approx \frac{1}{T}(I_L t_4) = \frac{t_4}{T} I_L$$

$$\frac{V_2}{V_1} = \frac{1}{T}(t_2 + t_3) = \frac{t_2 + t_3}{t_1} t_2 + t_3 + t_4$$

$$t_4 = \left(\frac{V_1}{V_2} - 1\right)(t_2 + t_3) - t_1$$

$$k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4}$$

$$T = t_1 + t_2 + t_3 + t_4 \quad \text{and} \quad f = 1/T$$

17. .3 Four-Quadrant ZVS Quasi-Resonant DC/DC Luo-Converter

The four-quadrant ZVS quasi-resonant Luo-converter is shown in Fig. 17.66. Circuit 1 implements the operation in quadrants I and II, and Circuit 2 implements the operation in quadrants III and IV. Circuit 1 and Circuit 2 can be converted to each other by an auxiliary switch. Each circuit consists of one main inductor L and two switches. Assuming that the main inductance L is sufficiently large, the current i_L is constant. The source and load voltages are usually constant, for example, $V_1 = 42$ V and $V_2 = \pm 28$ V. There are four modes of operation:

- Mode A (Quadrant I) electrical energy is transferred from the V_1 side to the V_2 side;
- Mode B (Quadrant II) electrical energy is transferred from the V_2 side to the V_1 side;
- Mode C (Quadrant III) electrical energy is transferred from the V_1 side to the $-V_2$ side; and
- Mode D (Quadrant IV) electrical energy is transferred from the $-V_2$ side to the V_1 side.

Each mode has two states, that is, "on" and "off." The switch status of each state is shown in Table 17.10.

The description of Modes A, B, C and D is same to that in the previous Sections 17.9.1 and 17.9.2.

17.1 Synchronous Rectifier DC/DC Luo-Converters

Synchronous rectifier dc/dc converters are called the fifth-generation converters. The development of microelectronics and computer science requires power supplies with low output voltage and strong current. Traditional diode bridge rectifiers are not available that meet this requirement. The soft-switching technique can be applied in synchronous rectifier dc/dc converters. We have created few converters with very low

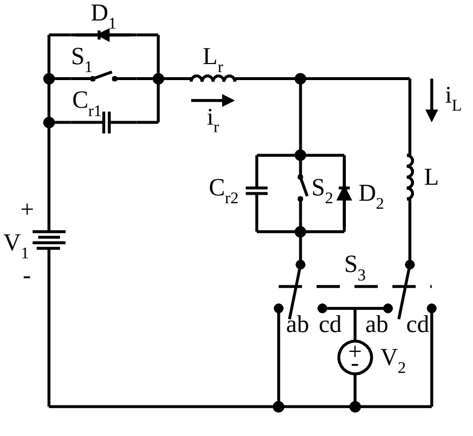


FIGURE 17.66 Four-quadrant dc/dc ZVS quasi-resonant Luo-converter.

TABLE 17.10 Switch status (the blank space means off)

Circuit // Switch or Diode	Mode A (Q-I)		Mode B (Q-II)		Mode C (Q-III)		Mode D (Q-IV)	
State-on	State-off	State-on	State-off	State-on	State-off	State-on		State-off
Circuit	Circuit 1				Circuit 2			
S_1	ON				ON			
D_1				ON				ON
S_2			ON				ON	
D_2		ON				ON		

voltage (5, 3.3, and 1.8 ~ 1.5 V) and strong current (30, 60, up to 200 A) and high-power transfer efficiency (86, 90, up to 93 %). This section introduces a few new circuits that are different from the ordinary synchronous rectifier dc/dc converters:

- flat transformer synchronous rectifier dc/dc Luo-converter;
- double current synchronous rectifier dc/dc Luo-converter with active clamp circuit;
- zero-current-switching synchronous rectifier dc/dc Luo-converter; and
- zero-voltage-switching synchronous rectifier dc/dc Luo-converter.

17.1 .1. Flat Transformer Synchronous Rectifier DC/DC Luo-Converter

A flat transformer **SR dc/dc Luo-converter** is shown in Fig. 17.67. The switches S_1, S_2 and S_3 are the low-resistance MOSFET devices with very low resistance R_S (7–8 mΩ). Because we use a flat transformer, the leakage inductance L_m and resistance R_L are small. Other parameters are $C = 1\ \mu$F, $L_m = 1$ nH, $R_L = 2$ mΩ, $L = 5\ \mu$H, and $C_O = 10\ \mu$F. The input voltage is $V_1 = 30$ V dc, the output voltage is V_2, and the output current is I_O. The transformer turns ratio is $N = 12:1$. The repeating period is $T = 1/f$ and conduction duty is k. There are four working modes:

$$\omega = \frac{1}{\sqrt{L_m C}}$$

The natural resonant frequency is

$$t_1 = \frac{L_m}{V_1}\frac{I_O}{N} \qquad t_2 \approx kT$$

The intervals are:

$$t_3 = \sqrt{L_m C}\left[\frac{\pi}{2} + \frac{V_1}{\sqrt{V_1^2 + \frac{L_m}{C}\left(\frac{I_O}{N}\right)^2}}\right] \qquad t_4 \approx (1-k)T$$

Average output voltage V_2 and input current is I_1 are:

$$V_2 = \frac{kV_1}{N} - \left(R_L + R_S + \frac{L_m}{TN^2}\right)I_O \quad \text{and} \quad I_1 = k\frac{I_O}{N}$$

The power transfer efficiency:

$$\eta = \frac{V_2 I_O}{V_1 I_1} = 1 - \frac{R_L + R_S + \frac{L_m}{TN^2}}{kV_1/N} I_O$$

When we set the frequency $f = 150$–200 kHz, we obtained $V_2 = 1.8$ V, $N = 12$, $I_O = 0$–30 A, Volume = 2.5 (in^3). The average power-transfer efficiency is 92.3 %, and the maximum power density (PD) is 21.6 W/in^3.

17.1 .2 Double Current Synchronous Rectifier DC/DC Luo-Converter with Active Clamp Circuit

The converter in Fig. 17.67 prefers a half-wave rectifier. The **dc SR dc/dc Luo-converter** with an active clamp circuit is shown in Fig. 17.68. The switches S_1–S_4 are the low-resistance MOSFET devices with very low resistance R_S (7–8 mΩ). As S_3 and S_4 plus L_1 and L_2 form a double-current circuit and S_2 plus C is the active clamp circuit, this converter prefers a full-wave rectifier and obtains strong output current. Other parameters are $C = 1\ \mu$F, $L_m = 1$ nH, $R_L = 2$ mΩ, $L = 5\ \mu$H, and $C_O = 10\ \mu$F. The input voltage is $V_1 = 30$ V dc, output voltage is V_2, and the output current is I_O. The transformer turns ratio

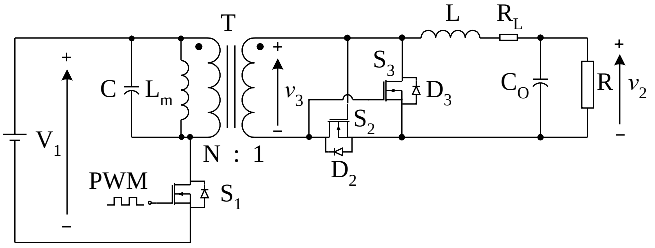


FIGURE 17.67 Flat transformer SR Luo-converter.

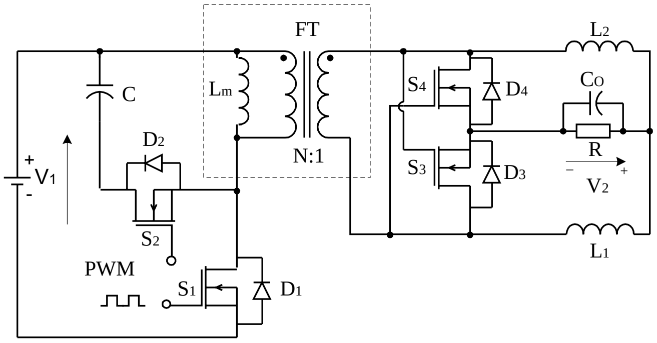


FIGURE 17.68 Double-current SR Luo-converter.

is $N = 12:1$. The repeating period is $T = 1/f$ and conduction duty is k. There are four working modes:

$$\omega = \frac{1}{\sqrt{L_m C}} \qquad V_C = \frac{k}{1-k} V_1$$

The natural resonant frequency is

$$t_1 = \frac{L_m}{V_1}\frac{I_O}{N} \qquad t_2 \approx kT$$

The interval of t_1 is

$$t_3 = \sqrt{L_m C}\left[\frac{\pi}{2} + \frac{V_1}{\sqrt{V_1^2 + \frac{L_m}{C}\left(\frac{I_O}{N}\right)^2}}\right] \qquad t_4 \approx (1-k)T$$

Average output voltage V_2 and input current I_1 are:

$$V_2 = \frac{kV_1}{N} - \left(R_L + R_S + \frac{L_m}{TN^2}\right) I_O \quad \text{and} \quad I_1 = k\frac{I_O}{N}$$

The power transfer efficiency:

$$\eta = \frac{V_2 I_O}{V_1 I_1} = 1 - \frac{R_L + R_S + \frac{L_m}{TN^2}}{kV_1/N} I_O$$

When we set the frequency $f = 200$–250 kHz, we obtained $V_2 = 1.8$ V, $N = 12$, $I_O = 0$–35 A, Volume = 2.5 (in^3). The average power-transfer efficiency is 94% and the maximum power density (PD) is 25 W/in^3.

17.1 .3 Zero-Current-Switching Synchronous Rectifier DC DC Luo-Converter

Because the power loss across the main switch S_1 is high in **dc SR dc/dc Luo-converter**, we designed the **ZCS SR dc/dc Luo-converter** shown in Fig. 17.69. This converter is based on the **dc SR dc/dc Luo-converter** plus the zero-current-switching technique. It employs a double-core flat transformer:

$$\omega_r = \frac{1}{\sqrt{L_r C_r}}$$

The ZCS resonant frequency is

$$Z_r = \sqrt{\frac{L_r}{C_r}} \quad \text{and} \quad \alpha = \sin^{-1}\left(\frac{I_1 Z_r}{V_1}\right)$$

normalized impedance is

$$t_1 = \frac{I_1 L_r}{V_1} \qquad t_2 = \frac{1}{\omega_r}(\pi + \alpha) \qquad t_3 = \frac{V_1(1+\cos\alpha)C_r}{I_1}$$

The intervals are:

$$t_4 = \frac{V_1(t_1+t_2)}{V_2 I_1}\left(I_L + \frac{V_1}{Z_r}\frac{\cos\alpha}{\pi/2+\alpha}\right) - (t_1 + t_2 + t_3)$$

Average output voltage V_2 and input current I_1 are:

$$V_2 = \frac{kV_1}{N} - \left(R_L + R_S + \frac{L_m}{TN^2}\right) I_O \quad \text{and} \quad I_1 = k\frac{I_O}{N}$$

The power transfer efficiency:

$$\eta = \frac{V_2 I_O}{V_1 I_1} = 1 - \frac{R_L + R_S \frac{L_m}{TN^2}}{kV_1/N} I_O$$

When we set $V_1 = 60$ V and frequency $f = 200$–250 kHz, and obtained $V_2 = 1.8$ V, $N = 12$, $I_O = 0$–60 A, Volume = 4 (in^3). The average power transfer efficiency is 94.5% and the maximum power density (PD) is 27 W/in^3.

17.1 .4 Zero-Voltage-Switching Synchronous Rectifier DC/DC Luo-Converter

The **ZVS SR dc/dc Luo-converter** is shown in Fig. 17.70. This converter is based on the **dc SR dc/dc Luo-converter** plus the

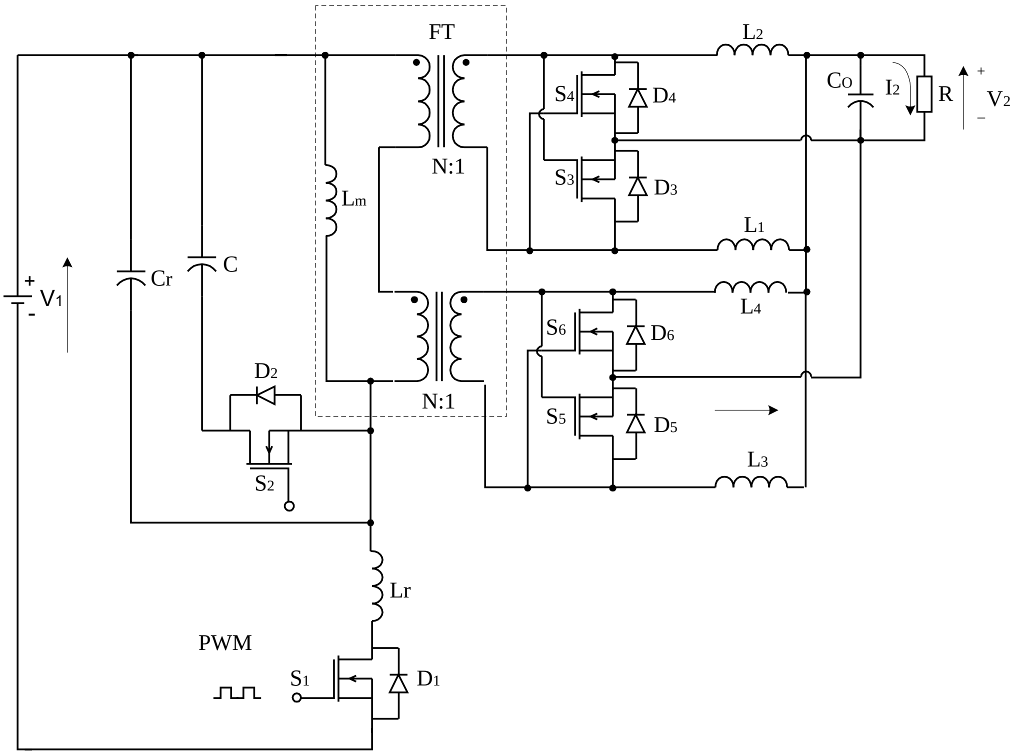

FT
L2
Co
I2
R
V2
+
−
S4
D4
N:1
S3
D3
Lm
L1
Cr
C
V1
+
-
L4
S6
D6
D2
N:1
S5
D5
L3
S2
Lr
PWM
S1
D1

FIGURE 17.69 The ZCS dc SR Luo-converter.

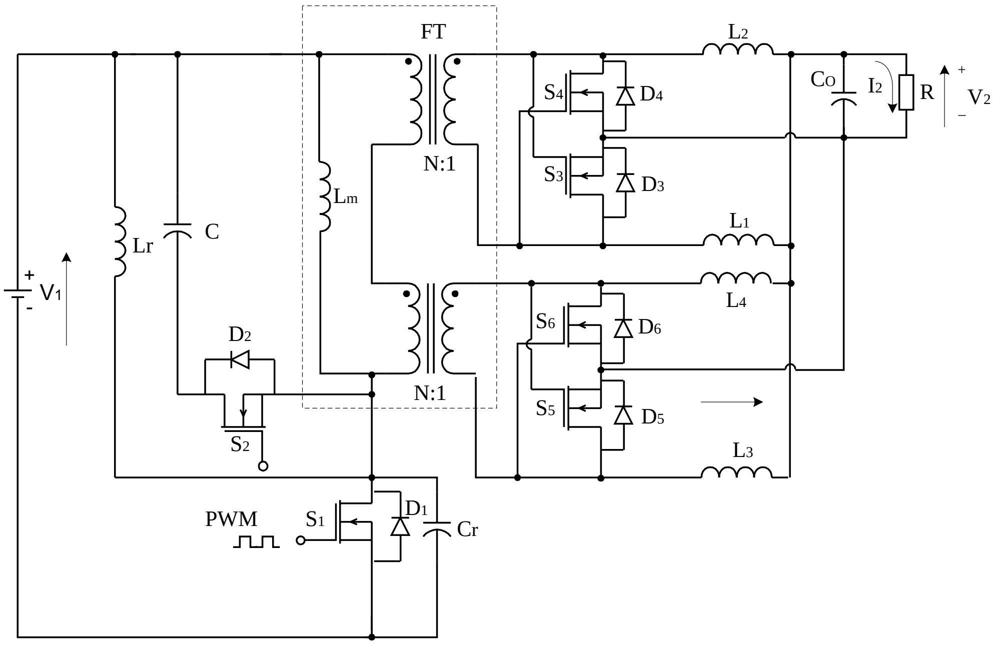

FT
L2
Co
I2
R
V2
+
−
S4
D4
N:1
S3
D3
Lm
L1
Lr
C
V1
+
-
L4
S6
D6
D2
N:1
S5
D5
L3
S2
PWM
S1
D1
Cr

FIGURE 17.70 ZVS dc SR Luo-converter.

zero-voltage-switching technique. It employs a double-core flat transformer:

$$\omega_r = \frac{1}{\sqrt{L_r C_r}}$$

The ZVS resonant frequency is

$$Z_r = \sqrt{\frac{L_r}{C_r}} \quad \text{and} \quad \alpha = \sin^{-1}\left(\frac{V_1}{Z_r I_1}\right)$$

normalized impedance is

$$t_1 = \frac{V_1 C_r}{I_1} \quad t_2 = \frac{1}{\omega_r}(\pi + \alpha) \quad t_3 = \frac{I_1(1+\cos\alpha)L_r}{V_1}$$

The intervals are:

$$t_4 = \frac{t_1 + t_2 + t_3}{\frac{V_1}{V_2} - 1}$$

Average output voltage V_2 and input current I_1 are:

$$V_2 = \frac{kV_1}{N} - \left(R_L + R_S + \frac{L_m}{TN^2}\right) I_O \quad \text{and} \quad I_1 = k\frac{I_O}{N}$$

The power transfer efficiency:

$$\eta = \frac{V_2 I_O}{V_1 I_1} = 1 - \frac{R_L + R_S + \frac{L_m}{TN^2}}{kV_1/N} I_O$$

When we set $V_1 = 60$ V and frequency $f = 200$–250 kHz, we obtained $V_2 = 1.8$ V, $N = 12$, $I_O = 0$–60 A, Volume = 4 (in^3). The average power-transfer efficiency is 94.5 and the maximum power density (PD) is 27 W/in^3.

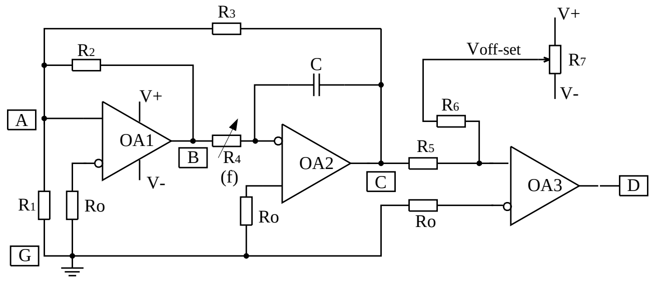


FIGURE 17.71 Luo-resonator.

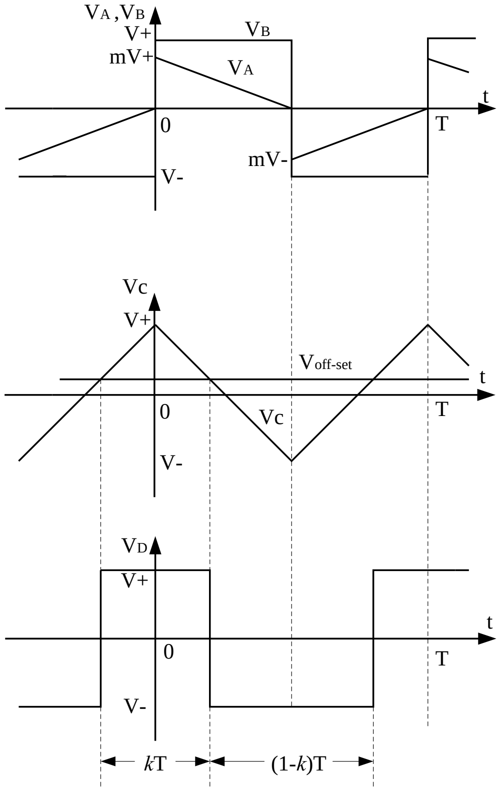


FIGURE 17.72 Voltage waveforms of Luo-resonator.

17.11 Gate Control, Luo-Resonator

The **Luo-resonator** is shown in Fig. 17.71. It generates the PWM pulse train to drive the static switch *S*. The Luo-resonator is a high-efficiency and simple structured circuit with easily adjusting frequency *f* and conduction duty *k*. It consists of three operational amplifiers (**OA**) namely, OA1-3, and an auxiliary. These three 741-type OAs are integrated in a chip TL074 (which contains four OAs). Two potentiometers are applied to adjust the frequency *f* and conduction duty *k*. The voltage waveforms are shown in Fig. 17.72.

The type-741 OA can work at a power supply of ±3–±18 V denoted by $V+$, G and $V-$ with $|V-| = V+$. The OA2 in Fig. 17.71 acts as the integration operation, its output V_C is a triangle waveform with regulated frequency $f = 1/T$ controlled by potentiometer R_4. The OA1 acts as a resonant operation, its output V_B is a square waveform with the frequency f. The OA3 acts as a comparator, and its output V_D is a square-waveform pulse train with regulated conduction duty k controlled by R_7.

First, assume that the voltage $V_B = V+$ at $t = 0$ and feeds positively back to OA1 via R_2. This causes the OA1 output voltage to be maintained at $V_B = V+$. In the meantime, V_B inputs to OA2 via R_4, and the output voltage V_C of OA2 therefore decreases towards $V-$ with the slope $1/R_4C$. Voltage V_C feeds negatively back to OA1 via R_3. Voltage V_A at point A changes from $(mV+)$ to 0 in the period of $2mR_4C$. Usually, R_3 is set slightly smaller than R_2, and the ratio is defined as $m = R_3/R_2$. Thus, voltage V_A tends towards negative. It causes the OA1 output voltage $V_B = V-$ at $t = 2mR_4C$ and voltage V_A jumps to $mV-$. Conversely, the voltage $V_B = V-$ at $t = 2mR_4C$ and feeds positively back to OA1 via R_2. This causes the OA1 output voltage to be maintained at $V_B = V-$. In the meantime, V_B inputs to OA2 via R_4, the output voltage V_C of OA2 therefore increases towards $V+$ with the slope $1/R_4C$. Voltage V_C feeds negatively back to OA1 via R_3. Voltage V_A at point A changes from $(mV-)$ to 0 in the period of $2mR_4C$. Thus, voltage V_A tends towards positive. It causes the OA1 output voltage $V_B = V+$ at $t = 4mR_4C$ and voltage V_A jumps to $mV+$.

Voltage V_C inputs to OA3 and compares with shift signal $V_{off\text{-}set}$ regulated by the potentiometer R_7 via R_6. When $V_{off\text{-}set} = 0$, OA3 yields its output voltage V_D as a pulse train with conduction duty $k = 0.5$. Positive $V_{off\text{-}set}$ shifts the zero cross point of voltage V_C downwards. Hence, OA3 yields its output voltage V_D as a pulse train with conduction duty $k > 0.5$. Conversely, negative $V_{off\text{-}set}$ shifts the zero cross point of voltage V_C upwards. Hence, OA3 yields its output voltage V_D as a pulse train with conduction duty $k < 0.5$ as shown in Fig. 17.72. Conduction duty k is controlled by $V_{off\text{-}set}$ via the potentiometer R_7. The calculation formulas are:

$$m = \frac{R_3}{R_2} \qquad f = \frac{1}{4mR_4C} \qquad k = 0.5 + \frac{R_5 V_{off\text{-}set}}{2R_6V+}$$

This PWM pulse train V_D is applied to the dc/dc converter switch such as a transistor, MOSFET or IGBT via a coupling circuit.

A design example: A Luo-resonator was designed as shown in Fig. 17.71 with the component values of $R_0 = 10\,\mathrm{k\Omega}$; $R_1 = R_2 = R_5 = 100\,\mathrm{k\Omega}$; $R_3 = R_6 = 95\,\mathrm{k\Omega}$; $R_4 = 510\,\Omega$–$5.1\,\mathrm{k\Omega}$; $R_7 = 20\,\mathrm{k\Omega}$; and $C = 5.1\,\mathrm{nF}$. The results are $m = 0.95$, frequency $f = 10$–$100\,\mathrm{kHz}$, and conduction duty $k = 0$–1.0.

17.12 Applications

The dc/dc conversion technique has been rapidly developed and has been widely applied in industrial applications and computer peripheral equipment. Three examples are listed in what follows:

- 1000-V insulation test bench;
- MIT 42/14-V dc/dc converter; and
- IBM 1.8-V/200-A power supply.

17.12.1 Thousand-Volt Insulation Test Bench

The traditional power supply for a high-voltage insulation test is costly, the power-transfer efficiency is very low, and the size is large. A newly designed 1000-V dc power supply is built by using a positive output Luo-converter quadruple-lift circuit plus a general IC-chip TL494. It is much smaller, cheaper, and highly efficient. The circuit is shown in Fig. 17.73. The source voltage is 24-V dc, and the output voltage is usually required to be $100 \sim 1000\,\mathrm{V}$ dc. It is used for an insulation test bench. Output voltage V_O was calculated as

$$V_O = \frac{V_{ref}}{R_9 + R_{W1}}(R_9 + R_W + R_8)$$

The wiper of the pot R_W can move from $3.9\,\mathrm{k\Omega}$ to 0. The corresponding output voltage changes from 98 to 1048 V.

The experimental results are listed in Table 17.11. The measured data verified the advantages of this power supply.

17.12.2 MIT 42/14-V 3-kW DC/DC Converter

This is a **two-quadrant ZCS-QR Luo-converter** that is shown in Fig. 17.74. This converter consists of one main inductor L and two switches with their auxiliary components. Assuming the main inductance is sufficiently large, the current i_L is constant. The source voltage V_1 and load voltage V_2 are usually constant, that is, $V_1 = 42\,\mathrm{V}$ and $V_2 = 14\,\mathrm{V}$. There are two modes of operation:

- Mode A (Quadrant I) electrical energy is transferred from the V_1 side to the V_2 side; and
- Mode B (Quadrant II) electrical energy is transferred from the V_2 side to the V_1 side.

Mode A is a ZCS buck converter. The output current can be 220 A. Mode B is a ZCS boost converter. The output current can be nearly 70 A. This converter has the volume of $270\,\mathrm{in}^3$. It can transfer the power of 3 kW between two batteries of 42 and 14 V with high power density ($22.85\,\mathrm{W/in}^3$), high efficiency (93%), and low EMI and reasonable EMC. The measured data are shown in Table 17.12.

17.12.3 IBM 1.8-V/200-A Power Supply

This is a **ZCS SR dc/dc Luo-converter** as shown in Fig. 17.75. This converter is based on the **dc SR dc/dc Luo-converter** plus the zero-current-switching (ZCS) technique. It employs a hixaploid-core flat transformer.

The ZCS resonant frequency is

$$\omega_r = \frac{1}{\sqrt{L_r C_r}}$$

and normalized impedance is

$$Z_r = \sqrt{\frac{L_r}{C_r}} \quad \text{and} \quad \alpha = \sin^{-1}\left(\frac{I_1 Z_r}{V_1}\right)$$

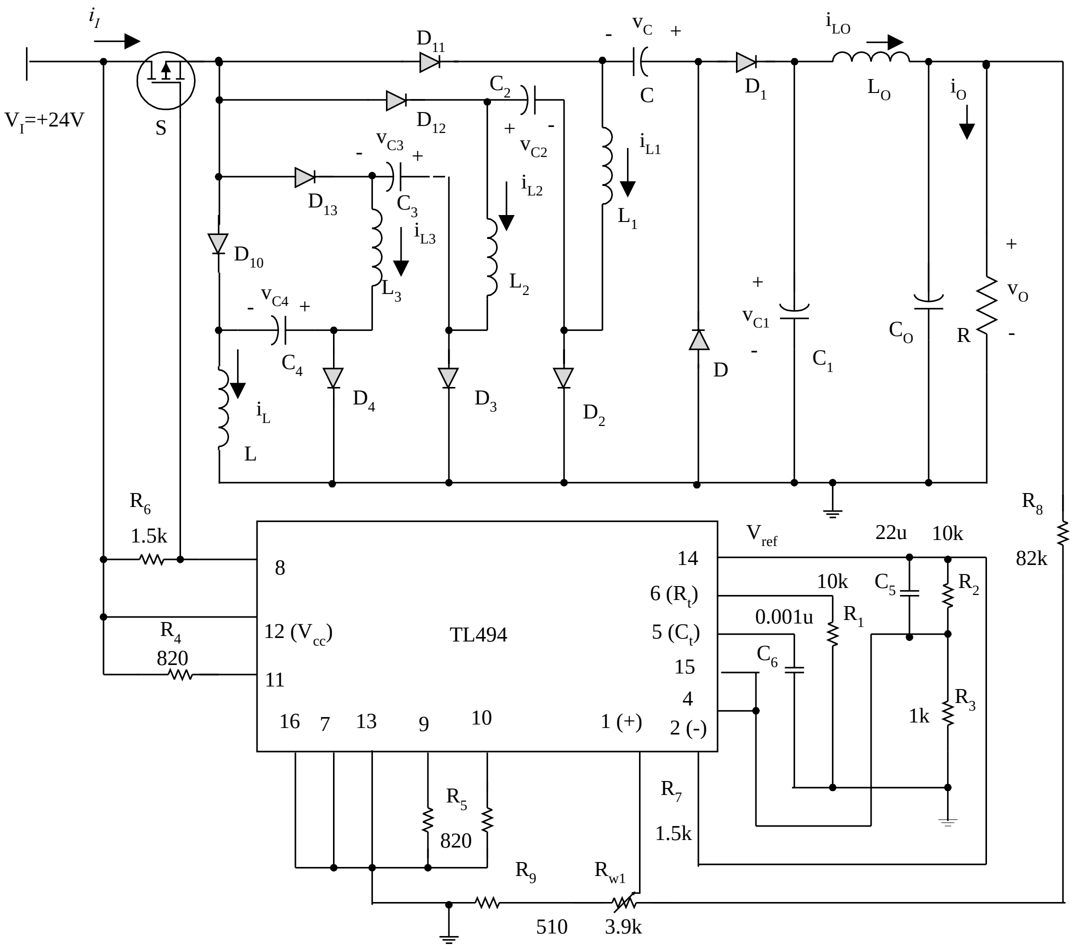

i_I
V_I=+24V
S
D_{11}
D_{12}
D_{13}
D_{10}
C_2
v_{C2}
C_3
v_{C3}
C_4
v_{C4}
v_C
C
i_{L1}
L_1
i_{L2}
L_2
i_{L3}
L_3
i_L
L
D_4
D_3
D_2
D
D_1
i_{LO}
L_O
i_O
v_{C1}
C_1
C_O
R
v_O
R_6
1.5k
R_4
820
TL494
8
12 (V_{cc})
11
16
7
13
9
10
1 (+)
2 (-)
14
6 (R_t)
5 (C_t)
15
4
V_{ref}
22u
10k
C_5
R_2
10k
R_1
0.001u
C_6
1k
R_3
R_8
82k
R_5
820
R_7
1.5k
R_9
R_{w1}
510
3.9k

FIGURE 17.73 The 1000-V insulation test bench.

TABLE 17.11 The measured experimental results

Item	Test Conditions	Data
Source effect ratio	$V_O = 300$ V, $R_L = 5$ kΩ, V_I varies between 20–24 V	0.001
Load effect ratio	$V_O = 300$ V, $V_I = 24$ V, R_L varies between 5 kΩ–1 MΩ	0.005
Power efficiency	$V_I = 24$ V, $V_O = 150$ V, $R_L = 5$ kΩ, $k \approx 0.36$	0.95
Power efficiency	$V_I = 24$ V, $V_O = 800$ V, $R_L = 5$ kΩ, $k \approx 0.88$	0.96
Power efficiency	$V_I = 24$ V, $V_O = 300$ V, $R_L = 5$ kΩ, $k \approx 0.68$	0.95

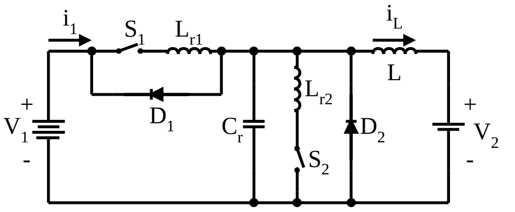

i_1
S_1
L_{r1}
i_L
L
V_1
D_1
C_r
L_{r2}
S_2
D_2
V_2

FIGURE 17.74 The MIT 42/14-V 3-kW dc/dc converter.

The intervals are:

$$t_1 = \frac{I_1 L_r}{V_1} \quad t_2 = \frac{1}{\omega_r}(\pi + \alpha) \quad t_3 = \frac{V_1(1 + \cos\alpha)C_r}{I_1}$$

$$t_4 = \frac{V_1(t_1 + t_2)}{V_2 I_1}\left(I_L + \frac{V_1}{Z_r}\frac{\cos\alpha}{\pi/2 + \alpha}\right) - (t_1 + t_2 + t_3)$$

Average output voltage V_2 and input current I_1 are:

$$V_2 = \frac{kV_1}{N} - \left(R_L + R_S + \frac{L_m}{TN^2}\right)I_O$$

TABLE 17.12 Experimental results for different frequency

Mode	f (kHz)	$L_{r1} = L_{r2}$ (μH)	C_r (μF)	I_I (A)	I_O (A)	I_L (A)	P_I (W)	P_O (W)	η ( )	PD (W/in^3)
A	20.5	1	4	77.1	220	220	3239	3080	95.1	23.40
A	21	1	4	78.3	220	220	3287	3080	93.7	23.58
A	21.5	1	4	81.0	220	220	3403	3080	90.5	24.01
B	16.5	1	4	220	69.9	220	3080	2935	95.3	22.28
B	17	1	4	220	68.3	220	3080	2871	93.2	22.04
B	17.5	1	4	220	66.6	220	3080	2797	90.8	21.77

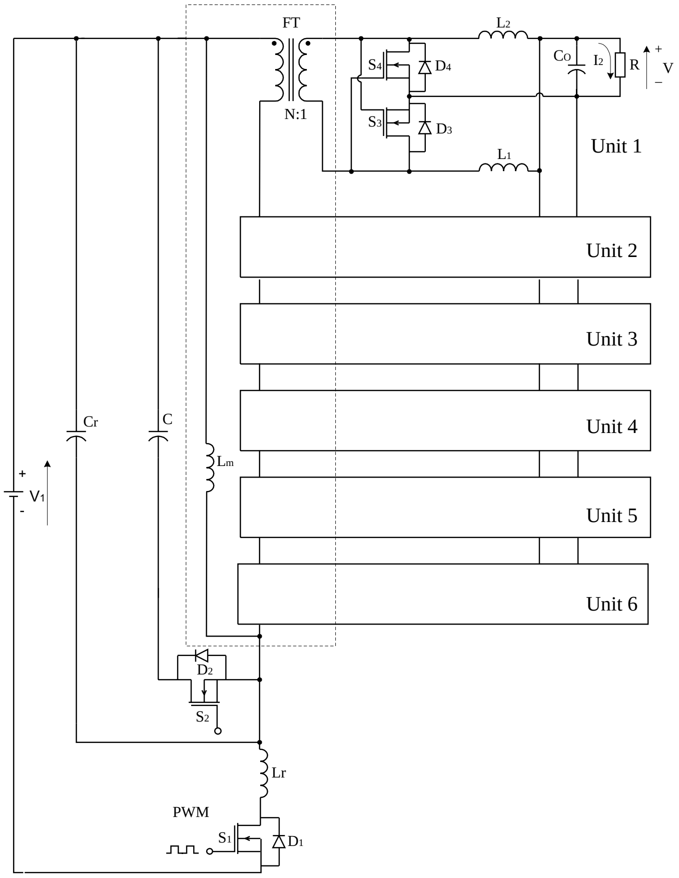


FIGURE 17.75 The IBM 1.8-V/200-A power supply.

and

$$I_1 = k\frac{I_O}{N}$$

The power transfer efficiency is

$$\eta = \frac{V_2 I_O}{V_1 I_1} = 1 - \frac{R_L + R_S + \dfrac{L_m}{TN^2}}{kV_1/N} I_O$$

When we set $V_1 = 180$ V and frequency $f = 200$–250 kHz, we obtained $V_2 = 1.8$ V, $N = 12$, $I_O = 0$–200 A, Volume = 14 (in^3). The average power-transfer efficiency is 94 and the maximum power density (PD) is 25.7 W/in^3.

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18

Gate Drive Circuits

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18.1 Introduction

A gate signal is required for every power semiconductor-controlled device to bring it into the conduction state. However, the nature of the gate drive requirement (or the base drive requirement for power bipolar junction transistor (BJT) and Darlington power transistor) of each device varies, depending on the voltage and current rating and also on the type of the device (i.e., thyristors or gate-commutation devices). The gate drive requirements of thyristors (silicon controlled rectifier, SCR), Triac, etc. are different from the gate drive requirements of the gate-commutation devices, viz. gate-turn-off thyristor (GTO), power BJT, metal-oxide field effect transistor (MOSFET), insulated-gate bipolar transistor (IGBT), static induction transistor (SIT), MOS-controlled thyristor (MCT), and so forth. Therefore, gate drive circuits of thyristors and gate-commutation devices are discussed here separately.

18.2 Thyristor Gate Requirements

A thyristor can be triggered by the application of a positive gate voltage (V_G) and hence a gate current (I_G) supplied from a gate drive circuit as shown in Fig. 18.1. However, the choice of V_G and I_G is not restricted to a particular value, rather it varies over a wide range. It depends on the gate characteristics of the device as shown in Fig. 18.2. Any operating point (V_G, I_G) may be selected within the permissible or preferred gate drive area bounded by curves 1, 2, 3, 4, 5, and the rectangle *mnop*. Curve 3 represents a constant value of the maximum permissible gate power dissipation P_{GM}. Moreover, there is a nontrigger gate voltage (V_{GD}), which is a minimum gate voltage below which a thyristor cannot be triggered at any temperature (normally up to 100 °C). This gives a permissible noise level of the gate drive circuit that will not trigger the thyristor. The rectangle *mnop* is prescribed by the manufacturers to avoid both unsuccessful and undesirable triggering in the worst cases. It corresponds to the threshold condition of triggering (V_{GT}, I_{GT}). Also, it is related to forward anode voltage (V_{AK}) and junction temperature (T_j). For lower temperature, V_{GT} and I_{GT} increase and therefore the size of the rectangle *mnop* increases. Similarly, it should be ensured that the gate-circuit load-line (*wxyz*) should pass above this area. However, the most preferred zone for the operating point is close to curve 3. This, in turn, increases the di/dt capability, minimizes the switching-on time, and hence reduces the switching loss of the thyristor.

Gate trigger circuits can be designed with the help of both Figs. 18.1 and 18.2. Curve 6 shows the gate-to-cathode forward v–i characteristics of the device at given V_{AK} and T_j. This is the same as the forward-conducting characteristics of a silicon diode. The load-line *wxyz* of the gate trigger circuit intersects the device characteristics at q. Thus operating gate voltage (V_G) and gate current (I_G) are given by *or* and *os* respectively. The permissible range of the operating point is between x and y. The maximum or short-circuit current of the trigger source is $E_S/(R_S + R_1)$, which is shown by *ow*; R_1

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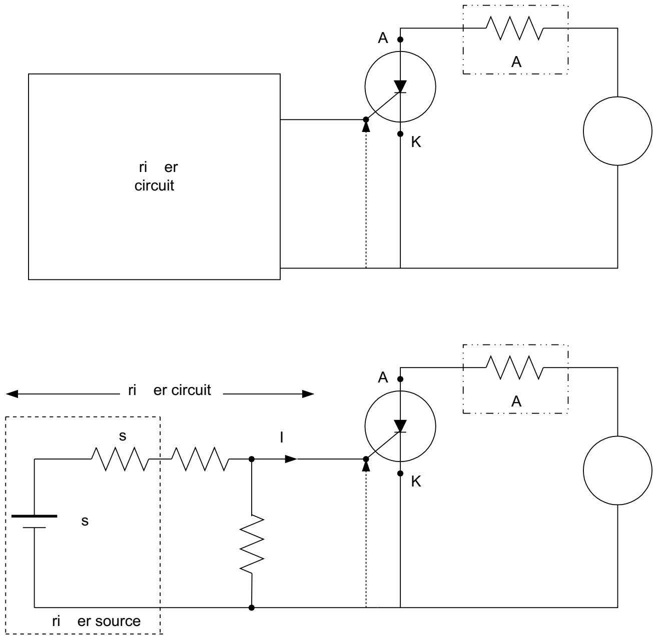


FIGURE 18.1 A typical switching arrangement for an SCR.

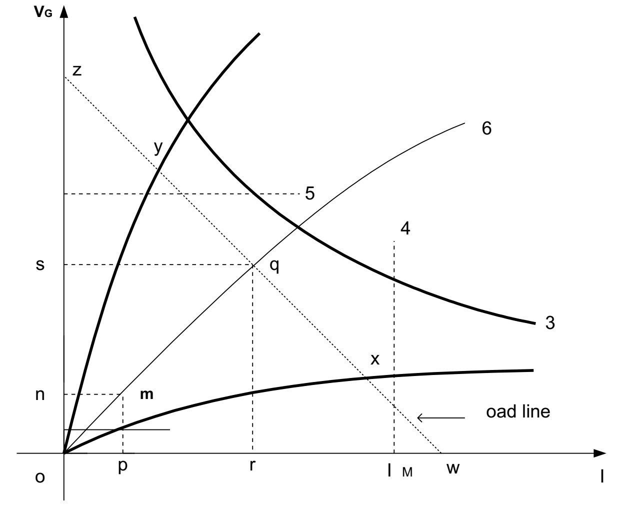


FIGURE 18.2 Typical gate characteristics of an SCR.

should be selected such that this current is not harmful to the source as well as to the gate-to-cathode junction (J_3). Similarly, *oz* shows the maximum trigger source voltage E_S. The presence of R_2 is optional, however, if E_S is greater than V_{GM}, it helps to clip V_G not to exceed the V_{GM} level, otherwise J_3 may be damaged. Moreover, R_2 provides a low gate-to-cathode impedance in the off-state of the device, thus improving the thyristor noise immunity.

When R_2 is connected across *G* and *K* terminals, the maximum V_G should be less than V_{GM}. Thus

$$\frac{R_2}{R_S + R_1 + R_2} E_S \le V_{GM} \tag{18.1}$$

Also,

$$E_s = V_G + (R_s + R_1)\left(I_G + \frac{V_G}{R_2}\right) \tag{18.2}$$

The preceding design considerations are in terms of continuous or dc values of gate voltage and gate current. However, a single pulse or a train of pulses are also used to trigger a thyristor. The forementioned design considerations (with dc values of V_G and I_G) are also valid for a pulsewidth up to 100 μs. For a short pulsewidth, V_G (peak) and I_G (peak) should be increased. In the case of a single pulse, the width of the gate pulse should be wide enough such that anode current would reach the latching current level of the thyristor. This consideration is important for a highly inductive load, where due to inductance the rise time of anode current is significant. For a train of pulses, it is found in practice that a 50-μs pulsewidth at 10 kHz with 50 duty cycle is sufficient for switching a highly inductive load. However, the average value of the peak gate drive power P_G (peak) should be less than P_{GM} (dc value), which is given by

$$P_{GM} \ge P_G\,(\text{peak}) \times \text{duty ratio} = P_G\,(\text{peak}) \times \text{pulsewidth} \times \text{frequency of pulses} \tag{18.3}$$

Similarly, there is a permissible limit to the maximum negative gate voltage that may appear across the gate-to-cathode junction. This is exactly like the peak inverse voltage (PIV) rating of an ordinary *p–n* junction diode. For this purpose either a diode is connected in series with a gate (between R_1 and *G*), or a diode (or a Zener diode) is connected across R_2 where the cathode of the diode is connected to *G*. The Zener diode clips the positive overshoot of the gate voltage above the V_{GM} level.

EXAMPLE 18.1. Design a suitable gate trigger circuit for an 800-V, 110-A SCR (OE-C50N), connected with a 6-V dc power supply. The maximum permissible current and the short-circuit current of the dc source are 200 and 500 mA, respectively. The SCR has the following gate parameters: $V_G = 2.5$ V; $I_G = 50$ mA; $V_{GM} = 3$ V; $I_{GM} = 100$ mA; and $P_{GM} = 0.5$ W.

SOLUTION. (i) For the gate drive circuit shown in Fig. 18.1 (without R_2). Short-circuit current $I_{Sh} = 500$ mA. Therefore,

$$R_S = \frac{E_S}{I_{Sh}} = \frac{6}{0.5} = 12\ \Omega$$

To protect the source from excessive current, the minimum value of resistor R_1 is given by

$$R_S + R_1 \ge \frac{E_S}{0.2} = \frac{6}{0.2} = 30\ \Omega$$

that is,

$$R_1 \geq 30 - 12 = 18\ \Omega$$

Also, to protect the gate-to-cathode junction of the SCR, the minimum value of the resistor is given by

$$R_S + R_1 \geq \frac{E_S}{I_{GM}} = \frac{6}{0.1} = 60\ \Omega$$

that is,

$$R_1 \geq 60 - 12 = 48\ \Omega$$

Therefore, R_1 should be greater than $48\,\Omega$.

Now corresponding to the typical gate characteristics, that is, $V_G = 2.5\,\text{V}$ and $I_G = 50\,\text{mA}$, the maximum value of resistor R_1 is given by

$$R_S + R_1 \leq \frac{E_S - V_G}{I_G}$$

$$R_1 \leq \frac{E_S - V_G}{I_G} - R_S = \frac{6 - 2.5}{0.05} - 12 = 58\ \Omega$$

Thus, R_1 should be selected within 58 and $48\,\Omega$. Depending on the availability of resistors of different values on the market, we may choose $R_1 = 56\ \Omega$.

Solution. (ii) Resistor R_2 is also incorporated (Fig. 18.1). As V_G should not exceed the V_{GM} level, therefore,

$$\frac{R_2}{R_S + R_1 + R_2} E_S \leq V_{GM}$$

or

$$R_2 \leq \frac{V_{GM}}{E_S}(R_S + R_1 + R_2) = \frac{3}{6}(12 + 56 + R2) = 69\ \Omega$$

Therefore, we choose $R_2 = 68\ \Omega$.

18.3 Trigger Circuits for Thyristors

Normally, thyristors are switched on by the application of a voltage signal at the gate terminal of the device as shown in Fig. 18.1. The gate voltage (v_G) is generated with the help of a gate drive circuit, which is called a firing or triggering circuit. Thus, thyristors can be switched on by a slow-rising rectified ac signal, a sharp single pulse, a constant-magnitude dc signal, or a train of high-frequency pulses as shown in Fig. 18.3. The thyristor switches on as soon as v_G exceeds the critical gate trigger voltage (V_{GT}) level. This depends on the gate-to-cathode junction temperature (T_j), anode current (i_A), and the supply voltage. The ideal switching signal for a thyristor should have an adequate amplitude of current for sufficient duration with a short rise time as shown in Fig. 18.4. The initial high magnitude and rapid rise of the gate current quickly turn on the device completely. Thus, carriers spread rapidly throughout the surface of blocking junction (J_2). This decreases switching losses and increases the initial di/dt capability of the device. After a few microseconds, a small gate current (slightly higher than the minimum value required for triggering I_{GT}) can be maintained. Ordinarily, a continuous gate signal is not required, but inductive circuits necessitate a sustained gate signal initially, until successful triggering takes place. For reliable operation of controllers, gate trigger signals are normally supplied during the entire on period (e.g., converters of dc drive). However, for a resistive load, a single sharp rising pulse is sufficient for triggering. For high-power applications, it is a common practice to isolate the control and triggering circuits from the power circuit (consisting of

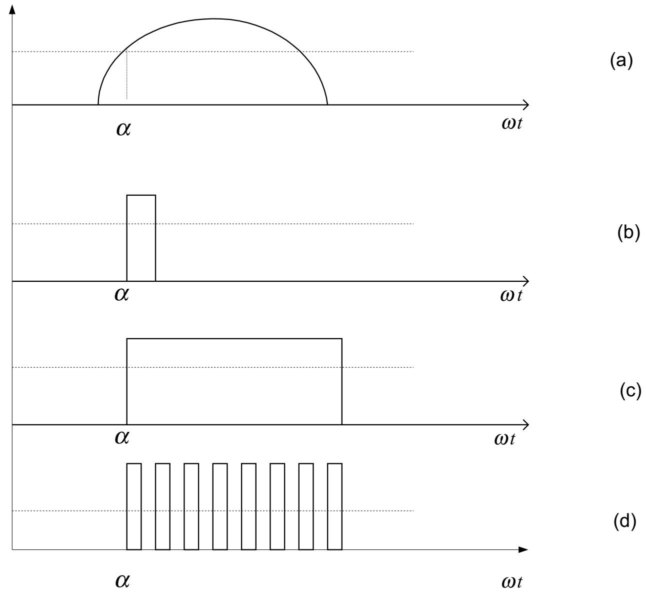


FIGURE 18.3 Different types of trigger signals for switching a thyristor.

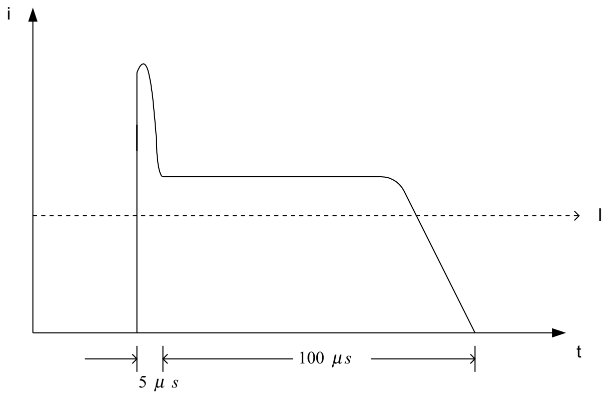


FIGURE 18.4 An ideal gate current required for a thyristor.

thyristors). Otherwise, the effects of high voltage and high current transients may cause misoperation or damage to the low-power control and trigger circuits. For this purpose, pulse transformers or optocouplers are used for low- and medium-power semiconductor devices. For higher power applications, for example, HVDC transmission systems, fiber-optic cables are used to isolate the control circuit from the power circuit. A 5-mW light trigger power source was found sufficient for switching a light-activated silicon-controlled rectifier (LASCR) with a rating of 4 kV, 3 kA.

In general, a thyristor conducts when it is properly biased and the trigger source of a trigger circuit supplies the required the minimum gate voltage (V_{GT}) and gate current (I_{GT}).

18.4 Simple Gate Trigger Circuits for Thyristors

Simple trigger circuits can be realized by R or RC network. They are cheap and consume little power. However, the control and hence the load output voltage (v_o), are susceptible to the device temperature variations. Moreover, feedback control cannot easily be incorporated.

18.4.1 Resistance Trigger Circuits

A step dc voltage, a slow rising dc signal, or a rectified positive half-wave signal can be used to trigger thyristors. When the voltage applied to the gate terminal exceeds the V_{GT} level, triggering takes place. Figure 18.5 shows a trigger circuit and waveforms for an ac circuit. Before conduction of the SCR, the input supply voltage (v) appears across the SCR.

Neglecting R_2 and the voltage drop across D_1, the gate voltage is given by

$$V_G = \frac{R_{GK}}{R_1 + R_{GK} + R_{\min}} v \tag{18.4}$$

where $v = V_m \sin \omega t$ denotes the supply voltage, and R_{GK} is forward gate-to-cathode resistance.

As soon as V_G reaches the V_{GT} level and supplies the required gate current, conduction of SCR takes place. The voltage v_{AK} collapses and therefore v_G also reduces to almost zero level, and v appears across the load. Now, R_1 can be increased to reduce v_{R_2} and thus to increase α. However, with a larger R_1, eventually the circuit fails to trigger the device as shown by curve 3. Here, the control of α is restricted to 90° only (curve 2 of V_G in Fig. 18.5). Similarly, I_G should not

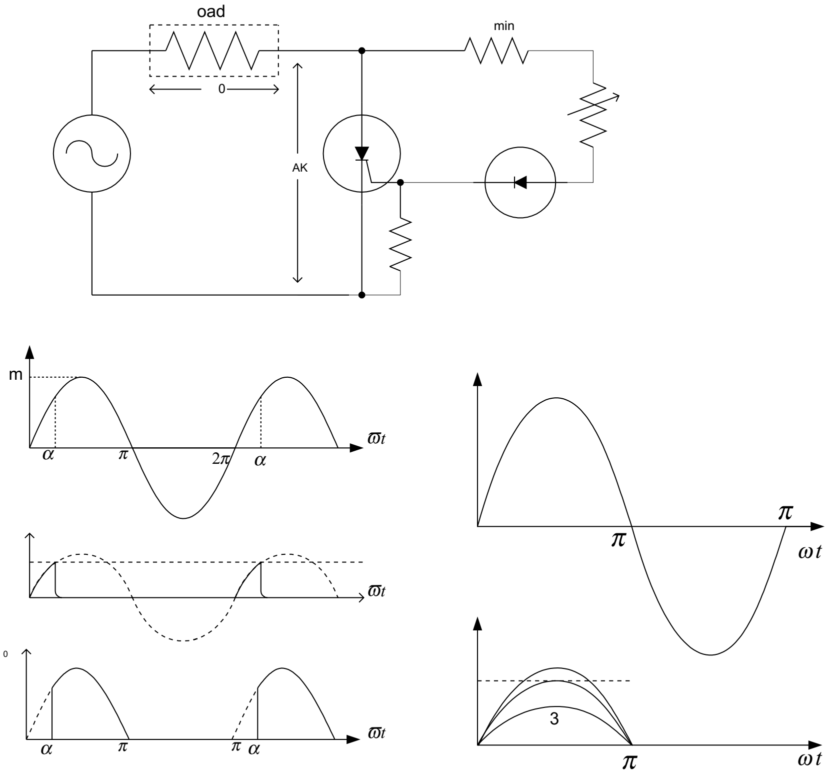


FIGURE 18.5 Resistance trigger circuit for an SCR.

exceed the I_{GM} level. Therefore, the minimum value of the resistor $R_{\min}$ is given by

$$\frac{V_m}{R_{\min}} \leq I_{GM} \tag{18.5}$$

This circuit is further improved by adding a resistor R_2 across G and K terminals of the SCR. Then the worst-case voltage across R_2 should not exceed the V_{GM} level. Therefore, the maximum value of the resistor R_2 is given by

$$\frac{R_2}{R_{\min} + R_2} V_m \leq V_{GM} \tag{18.6}$$

The same circuit also is applicable for Triac. However, diode D_1 has to be removed such that a trigger signal will be available at the gate terminal during both half-cycles. Because the gate of a Triac is not equally sensitive in all four of its modes of switching, α and hence v_o are usually different in the positive and negative half-cycles of the supply voltage.

18.4.2 RC Trigger Circuits

A phase-shifted signal in an ac circuit and a slow rising signal in a dc circuit generated by an RC network are used to trigger the thyristors. In these cases the range of α is extendable beyond 90°.

18.4.2.1 AC-Type

Figure 18.6 shows a trigger circuit and related vector diagram. The supply voltage appears across the RC branch. Neglecting the discharge of the capacitor during the conduction period of the thyristor, the circuit can be analyzed by the sinusoidal steady-state response of a linear RC circuit. Thus, the phase angle of the capacitor voltage (θ), can be controlled from 0° to almost 90° (Fig. 18.6). However, the rms value of the capacitor voltage (V_C), which is equal to ($V \cos\theta$), decreases drastically for a higher value of θ. By variation of R_1, the phase angle (θ) as well as the magnitude of V_C change. The power-factor angle (ϕ) of the RC circuit is given by

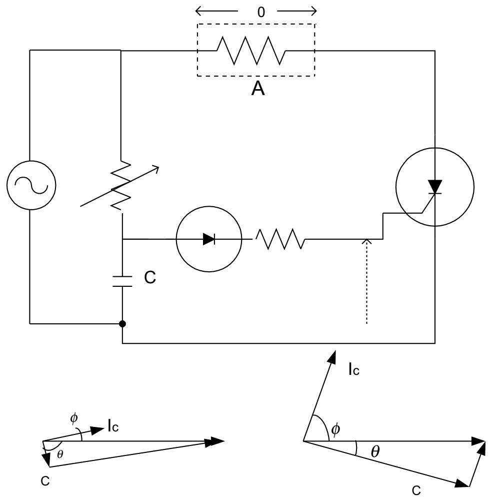


FIGURE 18.6 A typical RC trigger circuit.

$$\phi = \tan^{-1}(X_c/R) = \tan^{-1}(1/\omega CR) \tag{18.7}$$

Also, from trigonometry, when $\theta = (\pi/2) - \phi$,

$$\tan\theta = (1/\tan\phi) \text{ and } \theta = \tan^{-1}(\omega CR) \tag{18.8}$$

The instantaneous value of the voltage across capacitor (v_C) is given by

$$v_C = \sqrt{2} V_C \sin(\omega t - \theta) = (\sqrt{2} V \cos\theta)\sin(\omega t - \theta) \tag{18.9}$$

During the positive half-cycle when v_C hence v_G exceeds the V_{GT} level, conduction of the thyristor takes place (Fig 18.6). In fact v_G is the rectified capacitor voltage. Thus, α can be controlled over wide range beyond 90°. By variation of R, phase angle (θ) as well as the magnitude of V_C change as shown in Fig. 18.6. Furthermore, the magnitude of v_G can also be controlled by gate current limiting resistance R_2, as in the case of a resistance-trigger circuit.

An improvement in the circuit configuration is possible when the RC branch is connected across the SCR. When the SCR conducts, voltage across the RC branch also reduces to a very low level (ideally zero). The power dissipation in the gate circuit therefore reduces significantly.

EXAMPLE 18.2. A 240-V, 50-Hz supply is connected to an RC trigger circuit (Fig. 18.6). If R is variable from 1 to 22 kΩ, $V_{GT} = 2$ V and $C = 0.47$ μF, what are the minimum and maximum triggering or switching angle (α)?

SOLUTION. The phase angle of V_C is given by

$$\begin{aligned}\theta &= \tan^{-1}(\omega CR)\\ &= \tan^{-1}(2\pi f C)\\ &= \tan^{-1}(2\pi \times 50 \times 0.47 \times 10^{-6} \times R)\end{aligned}$$

Furthermore,

$$V_C = V\cos\theta \quad \text{and} \quad v_c(\omega t) = \sqrt{2} V_C \sin(\omega t - \theta).$$

(i) When $R = 1\text{k}\Omega$, it gives $\theta = 8.4°$, $\cos\theta = 0.989$ and $V_C = 240 \times 0.989 = 237.4$ V. Therefore,

$$v_c(\omega t) = \sqrt{2} V_C \sin(\omega t - 8.4°) = 335.77 \sin(\omega t - 8.4°)$$

Conduction of SCR takes place at $v_c = V_{GT} = 2$ V and $\omega t = \alpha$. Therefore,

$$v_c(\alpha) = 2 = 335.77 \sin(\omega t - 8.4°)$$

The minimum value of α is given by

$$\alpha_{\min} = 8.4^\circ + \sin^{-1}(2/335.77) = 8.7^\circ$$

(ii) When $R = 22\ \text{k}\Omega$, it gives $\theta = 72.9^\circ$, $\cos\theta = 0.296$ and $V_C = 240 \times 0.296 = 70.97$ V. Because

$$\begin{aligned} v_c(\alpha) = 2 &= \sqrt{2} \times 70.97 \sin(\omega t - 72.8^\circ) \\ &= 100.36 \sin(\omega t - 72.8^\circ) \end{aligned}$$

the maximum value of α is given by

$$\alpha_{\max} = 72.8^\circ + \sin^{-1}(2/100.36) = 73.9^\circ$$

18.4.2.2 alf- ave Type

This circuit has been realized by incorporating an additional diode (D_2) in the circuit shown in Fig. 18.6. As illustrated in Fig. 18.7, the capacitor is charged (upper plate negative) by v through D_2. The charging starts from the negative-zero-crossover instant to the negative peak of v, that is, $-\sqrt{2}$ V. Then the voltage at the anode of D_2 (i.e. v_c) becomes equal to the voltage at the cathode (i.e. v), therefore the current through D_2 ceases and D_2 becomes reverse-biased. Now the charging of the capacitor (with upper plate positive) takes place through R and the charging rate depends on the time-period RC. When v_G (rectified v_C) becomes slightly higher than V_{GT}, conduction of the SCR takes place. Simply by controlling R, the charging rate of the capacitor α varies; D_1 prevents a large negative supply voltage from appearing at the gate terminal of the thyristor. For a wide range of α, charging of the capacitor is required for almost a three-fourths time-period (T) of the supply voltage. However, for 50 or 60 Hz mains supply applications, the following empirical equation had been reported:

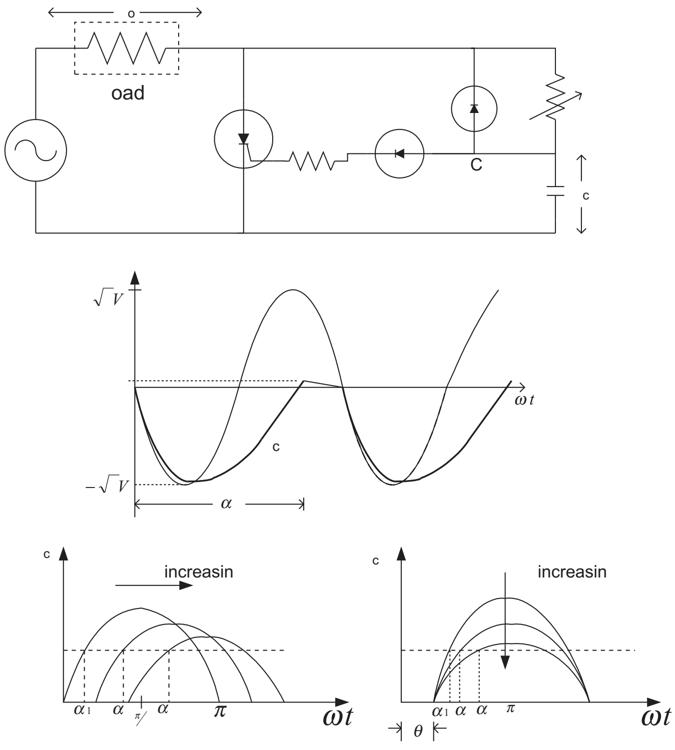


FIGURE 18.7 Another RC trigger circuit.

$$\text{RC} \geq 0.65T = 4/\omega \tag{18.10}$$

where the angular frequency of ac mains $\omega = 2\pi/T$.

The value of R_2 is chosen such that the required I_{GT} and V_{GT} are supplied to the gate terminal:

$$R_2 \leq \frac{v - v_{GT} + v_D}{I_{GT}} \tag{18.11}$$

where v is the voltage at the switching instant of thyristor and v_D is forward voltage drop of diode D_1.

Also, the maximum value of R_2 is given by

$$R_{2\max} \leq \frac{\sqrt{2}V - V_{GT} - V_{D1}}{I_{GT}} \cong \frac{\sqrt{2}V}{I_{GT}} \tag{18.12}$$

With an approximation, the previous analysis of the trigger circuit holds good even for this case.

18.4.2.3 ull- ave Type

This circuit has been realized by incorporating a diode bridge in the previous circuit (Fig. 18.6). As illustrated in Fig. 18.8, charging of capacitor takes place through R and the charging rate depends on RC (time period). When v_G (rectified v_C) becomes slightly higher than v_{GT}, conduction of SCR takes place. Simply by controlling R, the charging rate of the capacitor α varies.

In this circuit, charging of the capacitor starts from each zero-crossover instant and the capacitor experiences only a half-wave rectified voltage until the thyristor is triggered. The circuit can be analyzed by the complete response of an RC circuit with a sinusoidal (half-wave) excitation. The voltage expression is given by

$$v(t) = V_m \sin\omega t = Ri(t) + (1/C)\int i(t)dt$$

where

$$0 \leq t \geq \frac{T}{2} = \frac{\pi}{\omega} \tag{18.13}$$

differentiating,

$$\omega V_m \cos\omega t = R\frac{di(t)}{dt} + \frac{i(t)}{C} \tag{18.14}$$

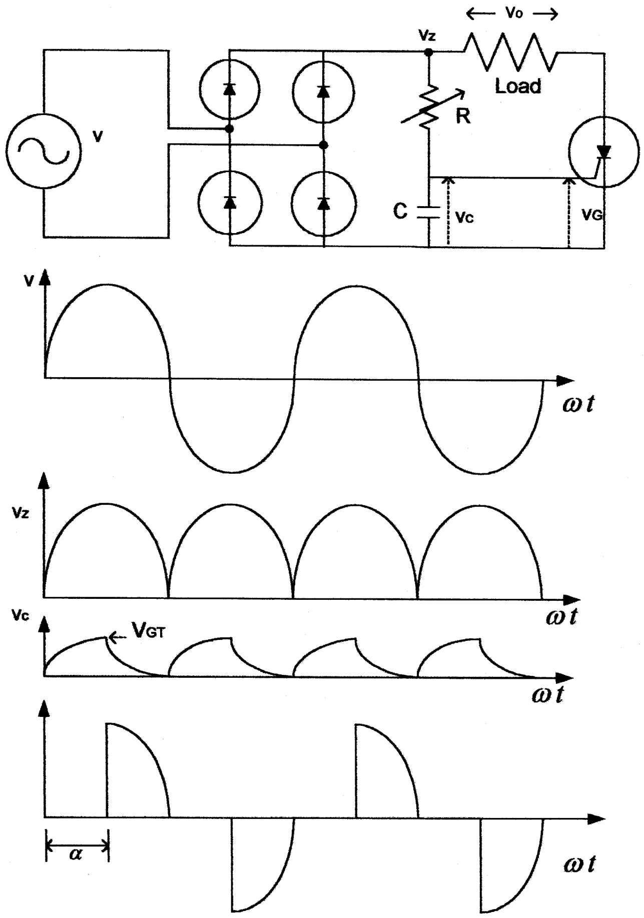


FIGURE 18.8 Full-wave RC trigger circuit.

With zero initial condition, the total current response is given by

$$i(t) = (V_m/Z)[\sin(\omega t + \phi) - \sin\phi \cdot \exp(-\omega t/\tan\phi)] \tag{18.15}$$

and

$$\begin{aligned} v_R(t) = i(t)R &= (V_m R/Z)[\sin(\omega t + \phi) \\ &\quad - \sin\phi \cdot \exp(-\omega t/\tan\phi)] && (18.16) \\ &= V_m \cos\phi[\sin(\omega t + \phi) \\ &\quad - \sin\phi \cdot \exp(-\omega t/\tan\phi)] && (18.17) \end{aligned}$$

Also,

$$v_C(t) = v(t) - v_R(t), \text{ or } v_C(\omega t) = v(\omega t) - v_R(\omega t) \tag{18.18}$$

As soon as v_C reaches the V_{GT} level, triggering of the thyristor takes place.

Example 18.3. If the RC branch of Example 18.2 (Fig. 18.6) is used in a full-wave trigger circuit, what are the minimum and maximum firing or switching angle, α?

Solution. (i) When $R = 1$ kΩ, it gives $\phi = 81.6°$. Because

$$\begin{aligned} v_C(t) = v(t) - v_R(t) = V_m \sin\omega t - V_m \cos\phi \\ \times [\sin(\omega t + \phi) - \sin\phi \cdot \exp(-\omega t/\tan\phi)] \end{aligned}$$

therefore,

$$\begin{aligned} v_C(\omega t) &= V_m[\sin\omega t - \cos\phi\{\sin(\omega t + \phi) \\ &\quad - \sin\phi \cdot \exp(-\omega t/\tan\phi)\}] = \sqrt{2} \times 240 \\ &\quad \times [\sin\omega t - \cos(81.6°)\{\sin(\omega t + 81.6°) \\ &\quad - \sin(81.6°)\exp(-\omega t/\tan(81.6°))\}]. \end{aligned}$$

Now the value of $v_C(\omega t)$ can be computed for $\omega t = 0$ to 180° by the direct substitution method. The required value of $\omega t = \alpha$ corresponds to the condition when v_C becomes equal to $V_{GT} = 2$ V.

It gives $\omega t = \alpha_{\min} = 2.5°$.

(ii) When $R = 22$ kΩ, it gives $\phi = 17.1°$. Therefore,

$$\begin{aligned} v_C(\omega t) = \sqrt{2} \times 240[\sin\omega t - \cos(17.1°)\{\sin(\omega t + 17.1°) \\ - \sin(17.1°)\exp(-\omega t/\tan(17.1°))\}] \end{aligned}$$

It gives $\omega t = \alpha_{\max} = 11.35°$.

18.4.3 Diac Trigger Circuit

This circuit is commonly used for Triac where the trigger signal is required in both half-cycles of the supply voltage (Fig. 18.9). Basically, it is similar to an RC trigger circuit (Fig. 18.6). Here both SCR and diode D_1 are replaced by a Triac and a Diac, respectively. The capacitor is charged through the resistance R during each half-cycle. When v_c reaches the breakover voltage of Diac ($V_{BO} \cong 30$ V), conduction of Diac takes place and the required gate current is supplied. Triac conducts and voltage across the capacitor (hence v_G) collapses for the remaining portion of the half-cycle. In the next half-cycle the same phenomenon repeats. Here, Triac conducts in positive half-cycle by positive gate current and in the negative half-cycle by the negative gate current. Thus, Triac operates in the first and third modes of its switching characteristics. However, the gate sensitivity of Triac is not the same in both these modes. Therefore, for commercial circuits, an additional RC branch is added between the capacitor and Diac to make α the same in both half-cycles. In this circuit the charging of the capacitor starts from each zero-crossover instant of the supply voltage, and the RC circuit experiences only a half-wave voltage before triggering of the thyristor. The circuit can be analyzed by the complete response of an RC circuit with a sinusoidal (half-wave) excitation as discussed in the previous section.

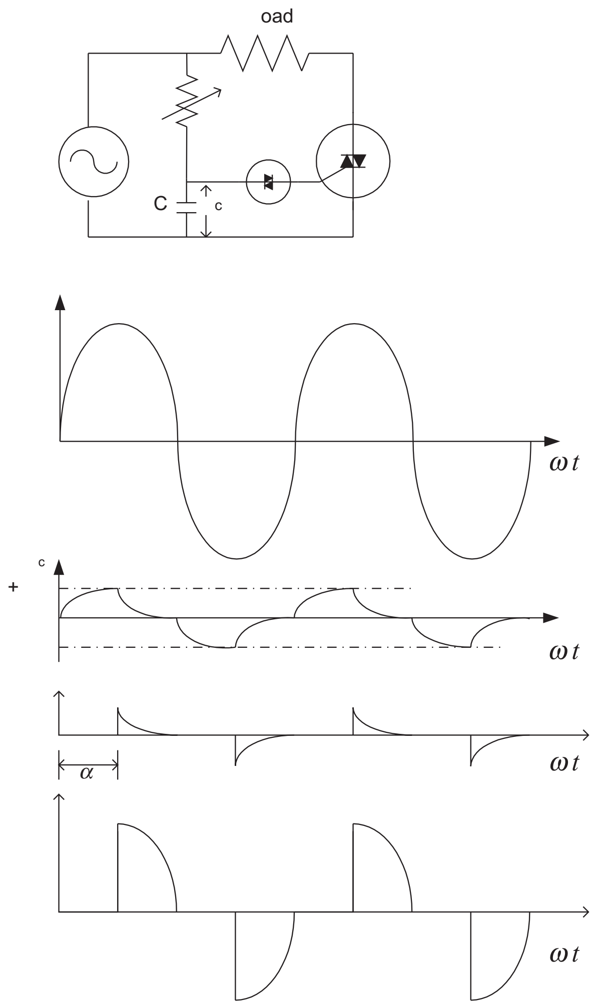


FIGURE 18.9 A Diac RC trigger circuit used in ac regulators.

EXAMPLE 18.4. If the RC branch of Example 18.3 (Fig. 18.6) is used in a Diac trigger circuit (with $V_{BO} = 30\,\text{V}$), what are the minimum and maximum firings or switching angle α?

SOLUTION. Equation (18.18) for v_C holds good even for this case. However, here, triggering takes place at $v_C(\omega t) = v_C(\alpha) = V_{BO} = 30\,\text{V}$ instead of $V_{GT} = 2\,\text{V}$. Now, the value of $v_C(\omega t)$ can be computed for $\omega t = 0$ to 180° by the direct substitution method as was done for the previous case. A simple computer program in QBASIC is given in what follows for Diac trigger circuits to find the required value of α. It corresponds to the condition when v_C becomes equal to V_{BO}.

```
CLS
REM Program for switching angle, Alpha in
Diac trigger circuit
PRINT "Program developed by Jamil Asghar,
EED,AMU,Aligarh,India"
PRINT "Give: R in K-Ohm, C in uF, VBO of
Diac, Supply Voltage"
INPUT R, C, VBO, V
pi = 4 * ATN(1)
phi = ATN(1000 / (2 * pi * 50 * R * C))
Vm = SQR(2) * V
phid = phi * 180 / pi
FOR wtd = 0 TO 180 STEP 0.1
phi = pi * phid / 180
wt = pi * wtd / 180
vR1 = SIN(wt + phi) - SIN(phi) * EXP(-wt *
TAN(phi))
vR = Vm * vR1 * COS(phi)
vC = Vm * SIN(wt) - vR
IF vC >= VBO GOTO 33
NEXT wtd
IF wtd >= 180 THEN PRINT " NO TRIGGERING
— VALUE OF RC TOO HIGH"
GOTO 44
33 PRINT "For diac: R in kOhms=", R, "C -
in uF=", C, "VBO =", VBO
PRINT "Alpha in deg.=", wtd, "Phi -in
deg=", phid, "vC=", vC
44 STOP
END
```

Result: (i) R 1kΩ, Value of alpha 11.33°
(ii) R 22kΩ, Value of alpha 46.5°

18.4.4 AC-Thyratron Type Trigger Circuit

This trigger circuit is similar to the circuit shown in Fig. 18.6, except that the phase-shifting RC network is energized from a separate center-tapped transformer. A simple RC trigger circuit is disadvantageous in that V_c does not remain constant for all values of θ (Fig. 18.6). Therefore, for higher values of θ (near 90°), V_c becomes very small eventually failing to trigger the thyristor. Thus the control range of α becomes small. While in this case the rms value of the voltage v_B remains constant and its phase angle β varies from 0 to almost 180° (lagging) as shown in Fig. 18.10. From the phasor diagram of the secondary of the transformer and the RC circuit,

$$\angle \text{ADB} = \pi/2 - \phi = \theta \quad \text{and} \quad V_{OA} = V_{OB} \tag{18.19}$$

therefore,

$$\phi = \angle \text{BAO} = \pi/2 - \angle \text{ADB} = \angle \text{ABO} \tag{18.20}$$

Also, from triangle OAB,

$$\begin{aligned} \beta &= \pi - 2\phi = 2(\pi/2 - \phi) = 2\theta \\ &= 2\tan^{-1}(\omega \text{CR}) \end{aligned} \tag{18.21}$$

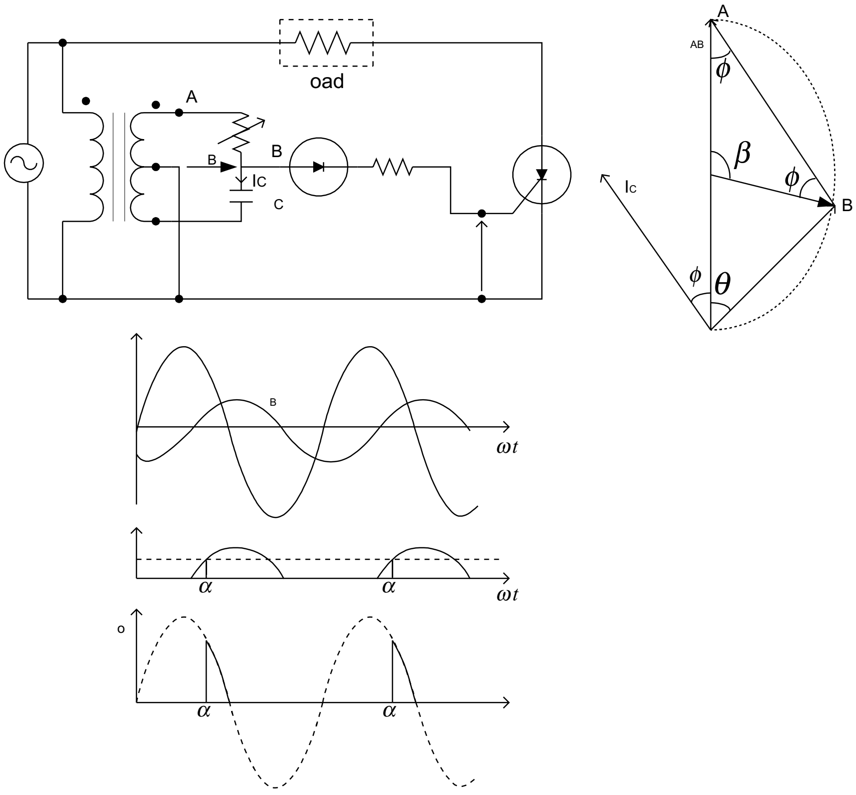


FIGURE 18.10 An ac-thyratron type trigger circuit.

The same circuit can also be used to trigger two thyristors in a bridge. In this case, gate current flows during the entire conduction period of the thyristor. It unnecessarily increases the temperature of gate-to-cathode junction (T_j), which may reduce the voltage withstand (blocking) capability of the thyristor.

18.4.5 Unijunction Transistor-based Trigger Circuit

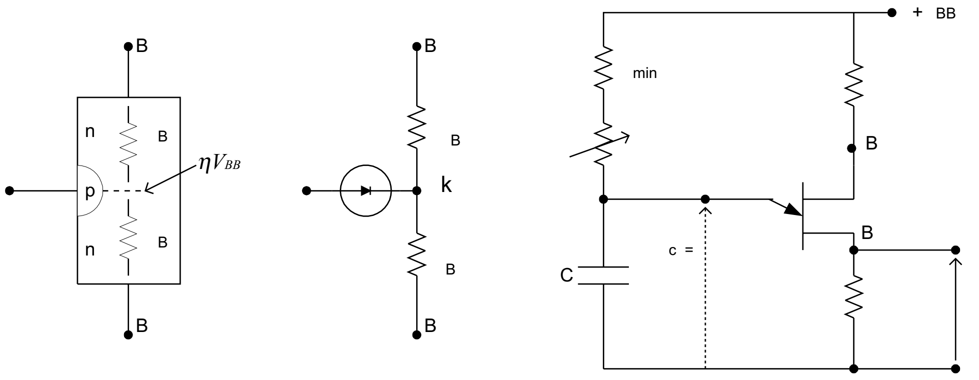
A unijunction transistor (UJT)-based oscillator provides constant-frequency, sharp pulses with small rise-time. The UJT is a three-terminal, two-layer *PN* device (Fig. 18.11). It has an *N*-type semiconductor (between two base terminals B_1 and B_2) with a small *P*-type doping (at emitter terminal *E*). The emitter terminal divides the interbase resistance (V_{BB}) into two parts (say, R_{B1} and R_{B2}). If a dc biasing voltage (V_{BB}) is applied across the base terminals, the voltage in *N*-type material near emitter terminal (**k**) is given by

$$V\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} = \eta V_{BB} \qquad (18.22)$$

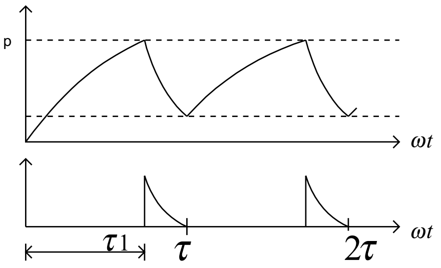
where η is called the intrinsic-standoff ratio of UJT and its value is less than unity (typical value varies between 0.5 and 0.85).

When the emitter voltage (v_E) is less than V_k (or ηV_{BB}), the emitter-B1 junction behaves as a diode in the reverse-biased condition, and thus it offers a very high impedance. A small reverse leakage current (few microamps) flows through the emitter terminal. A UJT oscillator is shown in Fig. 18.11c. When a dc supply voltage (V_{BB}) is connected, charging of the capacitor starts through resistance $R_{\min}$ and R. The voltage across the capacitor v_C (or v_E) increases. As soon as v_E slightly exceeds the V_k or ($\eta V_{BB} + V_D$) level, the *P-N* junction behaves as a diode in the forward-biased condition. Then emitter to base1 impedance collapses and the flow of I_E through R_1 takes place. The capacitor is discharged through R_1 and therefore a voltage pulse appears across R_1 (Fig. 18.11d). At the trailing edge of the pulse, v_E becomes very small (valley voltage V_v), depletion layer forms again and the *P-N* junction (between E and B1) becomes reverse-biased. Ideally, no current flows between E and B1 terminals (except the reverse leakage current) and they behave as open-circuited. Now charging of the capacitor starts and v_E again increases. The charging rate depends on ($R_{\min} + R$)C and the discharge rate of the capacitor depends on R_1C. The delay period (τ_1) and the time period (τ) of the pulse are given by

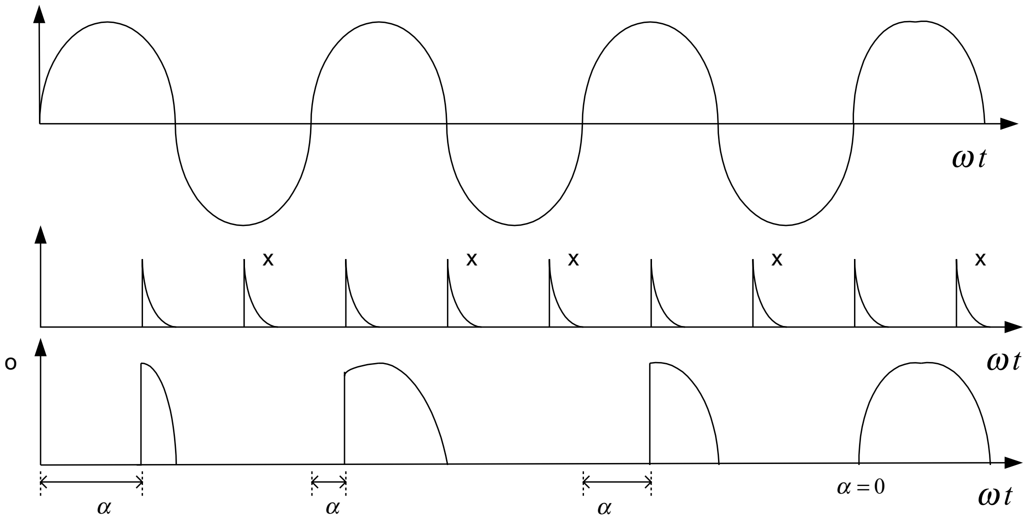
$$\tau = \tau_1 + R_1 C \qquad (18.23)$$



(a) UJT structure (b) Equivalent circuit model (c) UJT oscillator



(d) Wave forms of oscillator



(e) Unsynchronised trigger pulses with dc biasing voltage.

FIGURE 18.11 A UJT-based oscillator circuit and waveforms.

and

$$\tau_1 = (R_{\min} + R)C \ln \frac{1}{1-\eta} \tag{18.24}$$

Also, the switching angle depends on the delay period τ_1 of the oscillator, which is given by

$$\alpha = \omega\tau_1 \tag{18.25}$$

However, in a trigger circuit, α may not be equal in each cycle of the supply voltage (v) as shown in Fig. 18.11e. Some pulses arrive when the thyristor is already conducting while some arrive when the thyristor is in the reverse-biased condition; these pulses are marked “ .” They make no contribution toward triggering of the thyristor. Thus, α does not remain the same but varies randomly in each cycle. To get a constant value of α, synchronization of the trigger pulse with supply voltage is necessary. Figure 18.12 shows a UJT-based trigger circuit

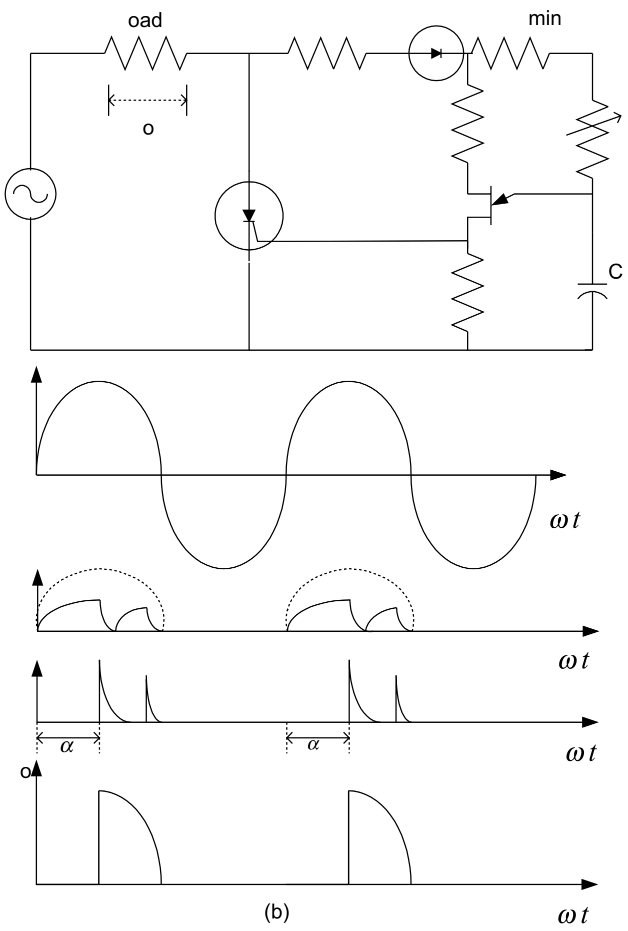


FIGURE 18.12 A UJT trigger circuit with waveforms.

synchronized with mains voltage (***v***) through a diode bridge. The charging of the capacitor starts from each zero crossover instant only. The first pulse in each half-cycle that triggers the thyristor is synchronized with ***v***, and therefore α becomes equal in each cycle. By controlling R, the time period of oscillator (τ), or the delay period of the first pulse (τ), α can be adjusted. The UJT trigger circuit may also be energized from a separate transformer (for biasing) and the same performance can be achieved.

18.4.5.1 Design Considerations

Selection of R_1. It should be low enough to prevent undesirable triggering of the thyristor. Therefore, R_1 is related to the maximum gate voltage (V_{GD}) that will not trigger the thyristor at any temperature:

$$V_{GD} \geq \frac{R_1}{R_1 + R_2 + R_{BB(\min)}} V_{BB} \tag{18.26}$$

Selection of R_2. It is selected from the stability consideration of the circuit because V_p decreases with temperature. The following equation gives the approximate value of R_2 for compensation over a temperature range of 40 to 100°C:

$$R_2 = \frac{10^4}{\eta V_{BB}} \tag{18.27}$$

Selection of capacitor C. It should store sufficient charge to trigger the thyristor. The typical values are between 0.01 to 0.7 μF. It can be calculated with the help of Eq. (18.22). The time period τ of the output pulse is $\tau_1 + R_1 C$, while the delay period that corresponds to the switching angle (α) is τ_1, as given in Eq. (18.24).

Selection of $R_{\min}$. It should be large enough so that the load line formed by R and V_{BB} intersect the emitter characteristics of UJT to the left of the valley point. Therefore,

$$R_{\min} \geq \frac{V_{BB} - V_V}{I_V} \tag{18.28}$$

Selection of R. The total charging resistance ($R + R_{\min}$) must be sufficiently small to allow peak point current drawn from the supply. Therefore,

$$R_{\max} = R + R_{\min} \leq \frac{V_{BB} - V_P}{I_P} \tag{18.29}$$

EXAMPLE 18.5. Parameters and ratings of a UJT (2N2646) at $T_j = 25\,^\circ\mathrm{C}$ are given below:

Maximum interbase voltage (V_{BB}) = 35 V
Maximum average power dissipation = 300 mW
Range of interbase resistance (R_{BB}) = 4.7 to 9.1 kΩ (typical 5.6 kΩ at $V_{BB} = 12$ V)
Valley point current $I_V = 4$ mA at $V_{BB} = 20$ V
Intrinsic standoff ratio, $\eta = 0.56$ to 0.75 (0.63 typical)
Valley point voltage $V_V = 2$ V at $V_{BB} = 20$ V
Peak point current $I_P = 5$ μA (maximum) at $V_{BB} = 25$ V
The maximum gate voltage (V_{GD}) that will not trigger on the SCR = 0.18 V

Design a suitable UJT-base trigger circuit for a single-phase-controlled converter (rectifier) operating with 50-Hz ac mains supply.

SOLUTION. The switching angle α varies from 0 to 180°, that is, for half time-period of the ac mains supply. Therefore,

$$\frac{T}{2} = \frac{1}{2f} = \frac{1}{2 \times 50} = 10 \text{ ms}$$

Let $V_{BB} = 12$ V. Then

$$\text{(i) } r_{\min} > \frac{V_{BB} - V_V}{I_V} = \frac{12 - 2}{4 \times 10^{-3}} = 2.5 \text{ k}\Omega$$

Take $R_{\text{min}} = 2.7\ \text{k}\Omega$

(ii) $V_p \cong \eta V_{BB} = 0.63 \times 12\ \text{V} = 7.56\ \text{V}$,

$$R_{\text{max}} < \frac{V_{BB} - V_P}{I_P} = \frac{12 - 7.56}{5 \times 10^{-6}} = 888\ \text{k}\Omega$$

Then the value of R is given by

$$R = R_{\text{max}} - R_{\text{min}} = 888 - 2.7 = 885.3\ \text{k}\Omega$$

Take $R = 1\ \text{M}\Omega$; then the new value of $R_{\text{max}} = 1002.7\ \text{k}\Omega$.

(iii) Selection of Base-Resistances. The empirical formula for R_2 is given by

$$R_2 = \frac{10{,}000}{\eta V_{BB}} = \frac{10{,}000}{0.63 \times 12} = 1.32\ \text{k}\Omega$$

Therefore, the nearest value is taken $R_2 = 1.2\ \text{k}\Omega$. Then R_1 can be found as

$$\frac{V_{BB}}{R_1 + R_2 + R_{BB(\text{min})}} R_1 < V_{GD}$$

or

$$\frac{12}{R_1 + 1200 + 5600} R_1 < 0.18$$

It gives R_1 less than 103 Ω; therefore take $R_1 = 100\ \Omega$.

(iv) Selection of Capacitor. Let the triggering circuit be designed for a maximum delay period $(1/f)$ of 10 ms. The maximum delay period corresponds to the minimum frequency of the oscillator, which is given by

$$\tau = 10\ \text{ms} = R_{\text{max}} C \ln\left(\frac{1}{1-\eta}\right)$$

Therefore,

$$C = \frac{10^{-2}}{R_{\text{max}} \times \ln\left(\frac{1}{1-\eta}\right)} = \frac{10^{-2}}{1002.7 \times 10^3 \times \ln\left(\frac{1}{1-0.63}\right)}$$
$$= 0.01\ \mu\text{F}$$

Although a capacitor of 0.01 μF can be selected, the pulsewidth of the triggering pulse will be small ($R_2C = 100 \times 0.01 = 1\ \mu\text{F}$). However, this may not be sufficient to trigger a thyristor successfully. Then it should be increased (about 5μs). Moreover, sometimes the voltage pulse across R_1 is not sufficient to drive the thyristor; then the value of R_1 may be increased.

The minimum delay period is given by

$$\tau_{\text{min}} = R_{\text{min}} \times C \times \ln\left(\frac{1}{1-\eta}\right) = 2.7 \times 10^3 \times 0.01 \times 10^{-6}$$
$$\times\ 0.99425 = 0.0268\ \text{ms}$$

The minimum value of

$$\alpha = \text{minimum delay period (in ms)} \times \frac{360^\circ}{20\ \text{ms}}$$
$$= \frac{0.0268 \times 360}{20} = 0.483^\circ$$

Similarly, the maximum delay period is given by

$$\tau_{\text{max}} = R_{\text{max}} \times C \times \ln\left(\frac{1}{1-\eta}\right)$$
$$= 1002.7 \times 10^3 \times 0.01 \times 10^{-6} \times 0.994 = 9.967\ \text{ms}$$

The actual maximum value of

$$\alpha = \text{maximum delay period (in ms)} \times \frac{360^\circ}{20\ \text{ms}}$$
$$= \frac{9.967 \times 360^\circ}{20} = 179.4^\circ$$

18.4.6 Advanced Triggering Circuits for Thyristors

Although RC trigger circuits are very simple and economical, they depend on gate trigger characteristics of the thyristor used, and they cannot be used easily in self-programmed, automatic or feedback controlled systems. Because the use of power-electronic controllers is increasing steadily in industry as well as in power systems, different types of controllers are required for specific applications. In a controller, a group of thyristors or power-semiconductor devices are required to be switched at different switching instants for different durations and in a particular sequence. Different three-phase converters, for example, dual converters, cycloconverters, and regenerative reversible drive, may require 12 to 36 such devices. Thus, switching a large number of these power devices with different control strategies by a simple trigger circuit becomes almost impossible. Moreover, incorporation of feedback and/or different control approaches for same load/drive system requires an intelligent controller. Therefore, the advanced triggering circuits become necessary.

Some modules of power semiconductor devices include a gate drive as well as transient protection circuitry. Such commercially available modules are called *intelligent module* or *smart power*. They include input-output isolation and gate drive circuits, microcomputer control, a protection and diagnostic circuit (for overcurrent, short-circuit, open load, overloading and excess voltage) and a controlled power supply.

Similarly, custom-built driver integrated circuits (ICs) are also available for thyristors as well as MOSFETs and IGBTs.

18.4.7 Buffer and Driver Circuits for Thyristors

In most power electronic circuits, a difference of potential exists between the gates of the various thyristors as well as between the control circuit and thyristors. The control electronics normally consist of linear ICs (e.g., operational amplifiers, timers) and digital ICs (e.g., TTL, CMOS), discrete passive elements, and active devices. Basically, they are low-voltage (few tens of volts) and low-power (few watts) circuits. The power circuit that consists of thyristors is a high-voltage circuit (normally of the order of several hundreds of volts). Therefore, it becomes necessary for the output channels of the gate-pulse generating circuit to be isolated from one another as well as from thyristors. The isolation can be provided either by a small high-frequency pulse transformer or by an optocoupler IC. Then it becomes possible to switch on several thyristors simultaneously (e.g., in a series connection or switching an ac load by two antiparallel thyristors). Similarly, control electronics, which control the conduction period of each thyristor, give an output of very low power (few milliwatts, for example the output of a CMOS logic gate). In general, in most cases output power is not sufficient to drive the gate directly. Therefore, an amplifier circuit is required that amplifies the weak gate drive control signal. For this purpose, a transistor amplifier is used.

For isolation between control and power circuit, the use of a pulse transformer is common. Normally, it has two or three windings, and it is a small low-power and high-frequency transformer; the turns ratio are normally 1 : 1 or 2 : 1. When a high-frequency pulse is applied to the primary winding, an output pulse appears at one or more output secondary windings. The optocoupler IC circuit is also used for this purpose. In this arrangement, an infrared light-emitting diode (I-LED) turns on a photosensitive device (photo-SCR, photo-Triac, photologic gate, or phototransistor), which ultimately turns on the thyristor. However, a separate dc power supply is normally required for each thyristor. For high-voltage applications, the optical-fiber technique is applicable. In this case, the output of the control electronic circuit is supplied in the form of a light signal through the optical-fiber cable to the thyristor. Optical fiber offers a very high level of insulation between the control circuit and the power circuit consisting of thyristors.

Figure 18.13 shows different driver and buffer circuits (DBC). In Fig. 18.13a, pulses are generated by a differentiator circuit ($R_1 C_1$), which converts a step input signal into sharp positive and negative pulses. The positive pulse is then amplified by a transistor amplifier circuit. The isolation is provided by a pulse transformer. Diode D_3 allows only the positive portion of the amplified signal to be applied between gate and cathode terminals of a thyristor; D_2 provides a freewheeling path for the inductive current of the primary winding of the pulse transformer. This protects the transistor from the high-voltage spike (Ldi/dt) that could be generated due to the snap of inductive current by the turn-off of the transistor.

The anode current of a thyristor reaches the latching current level after a certain delay period. Therefore, for an inductive load, a long pulse is required for successful triggering. For this purpose, the triggering pulse is stretched by connecting a capacitor in parallel with R_2. However, to avoid saturation of the core of the pulse transformer due to stretched unidirectional current, the pulse duration is restricted to 50 to 100 μs.

Often in converter circuits with inductive loads the load current is discontinuous within the assigned conduction period and therefore it is required to trigger the thyristor more than once. Similarly,the conduction period (or commutation instant) of each thyristor depends on the load current flowing through it, which varies with respect to the load power factor. Therefore, for reliable triggering, a continuous gate signal is required but it increases thyristor losses and decreases voltage withstand or blocking capability. Alternatively, a train of trigger pulses of high frequency (e.g., 10 kHz) is supplied during the entire conduction period. In this case the switching may be delayed by one time period (0.1 ms for a 10-kHz signal) of the pulse train. However, this delay is negligible for power frequency (e.g., 1.8° for 50 Hz or 2.0° for 60 Hz).

Figure 18.13b shows a commonly used driver and buffer circuit (DBC). A high-frequency (5 to 20 kHz) positive pulse (or square-wave signal) from an oscillator is applied to an AND gate continuously. These pulses are allowed to reach the base of transistor only when the input drive control signal is high. The transistor basically acts as a switch to energize the primary winding of the pulse transformer corresponding to each pulse. Moreover, these pulses also are amplified. Their magnitudes are restricted by the current-limiting resistor (R_2) connected in series with the dc source. In the secondary windings pulses of almost the same strength are produced due to transformer action. Due to the snap of inductive current in the primary winding (when the transistor is switched off), a negative pulse is also generated in the secondary winding. This pulse is blocked by the diode D_2. Thus amplified positive pulses become available between G and K terminals of the thyristor.

Figure 18.13c shows an optocoupler IC chip-based isolation circuit. An infrared light-emitting diode (I-LED) and a photo-SCR are fabricated in a single IC chip. On arrival of the input drive control signal, I-LED conducts and emits light to bring the photo-SCR into the conduction mode. Thus switching of the main SCR takes place.

Figure 18.13d shows another optocoupler-based circuit where a phototransistor is used. Because the output of the phototransistor cannot drive a thyristor, an additional transistor (BJT) is used for amplification. This type of circuit requires an additional electrically isolated dc power supply for each thyristor.

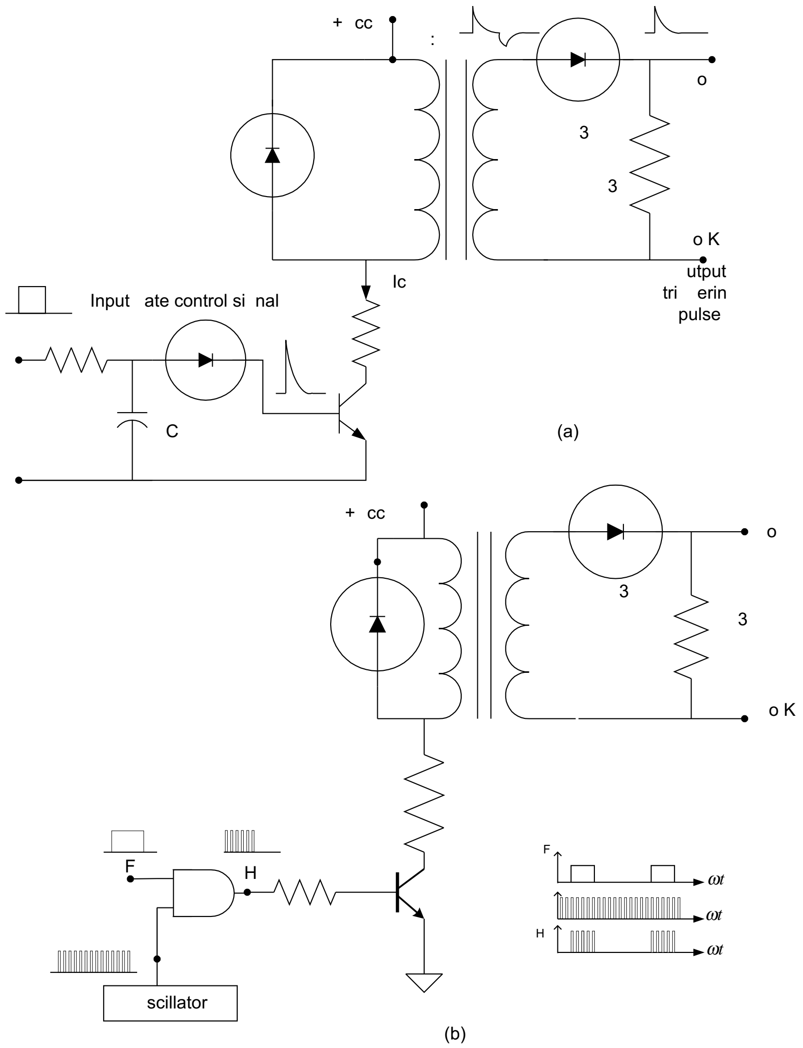


FIGURE 18.13 (a) Driver and buffer circuits for thyristors; (b) driver and buffer circuit in common use.

Figure 18.13e shows a fiber-optic cable-based driver circuit. It provides the very high electrical isolation and large creepage distance required between a low-power control circuit and a high-voltage power circuit. In the case of an optocoupler, I-LED and the receiving phototransistor both are fabricated on the same IC chip. Therefore, capacitance between them should be as small as possible to avoid retriggering at both turn-on and turn-off of the power devices (e.g., power transistors, power MOSFET and IGBT), because of the jump of potential across the devices (dv/dt). To avoid this problem, the fiber-optic technique is used. The first amplifier is a receiver (fiber optic integrated detector/preamplifier), and the second amplifies the control signal to the required level for triggering of the thyristor. Here, the driver circuit is linked to the control circuit only through the fiber-optic cable, thus galvanic isolation is provided between them.

EXAMPLE 18.6. Design a suitable pulse transformer-based driver circuit for gating a given SCR. The worst-case requirements of the SCR are given in the following:

$$I_{G\min} = 100 \text{ mA}, \;\; V_{G\min} = 2.5 \text{ V@} - 65\,^{\circ}\text{C}$$

The input drive control signal is an output of AND gate (IC7408). The specification of a TTL gate (general type) is given by

Output current and voltage at the logic “1” level: $I_{OH} = 0.4$ mA, @$V_{OH} = 2.4$ V, and

Output current and voltage at the logic “0” level: $I_{OL} = 16$ mA, @$V_{OL} = 0.4$ V

SOLUTION. The gate current requirements of the thyristor are important for design considerations. Then the

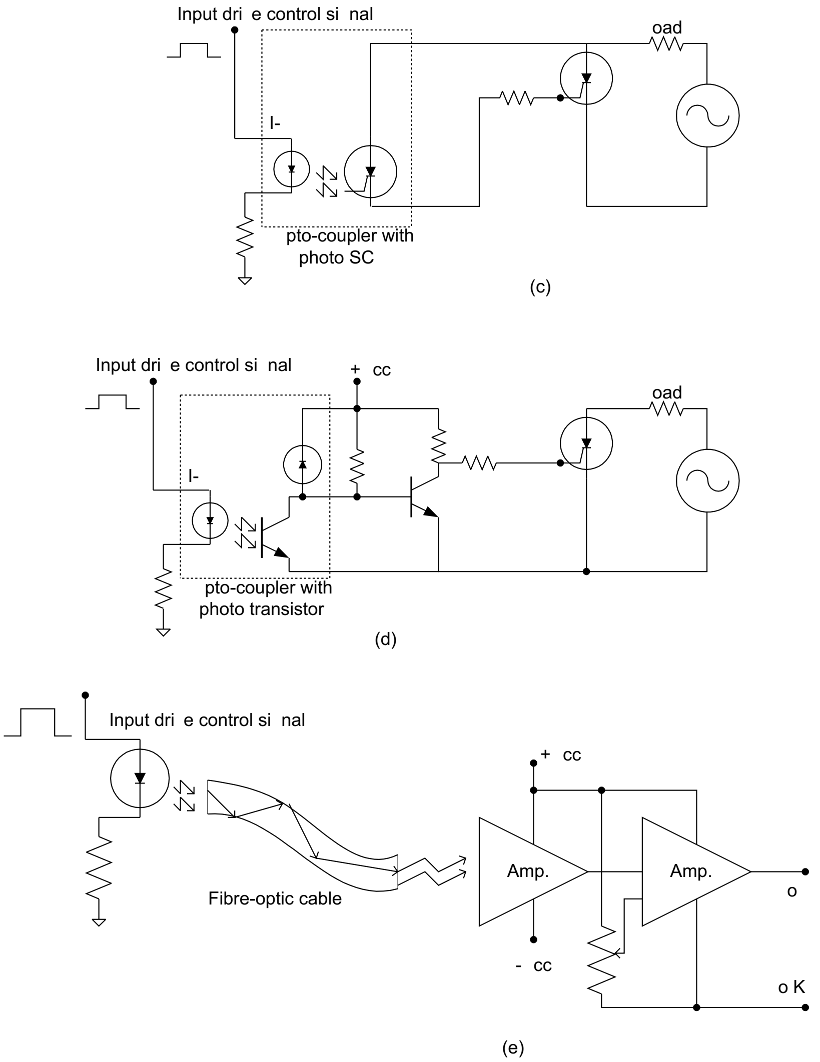

Input drive control signal
oad
I-
pto-coupler with
photo SC
(c)
Input drive control signal
+ cc
oad
I-
pto-coupler with
photo transistor
(d)
Input drive control signal
+ cc
Amp.
Amp.
Fibre-optic cable
o
- cc
o K
(e)

FIGURE 18.13 (c) optocoupler IC chip-based isolation circuit; (d) optocoupler with phototransistor; and (e) optical fiber cable-based driver circuit.

desired gate current and hence the secondary current of the pulse transformer (I_2) should be 100 mA. Let the turns ratio of the pulse transformer be 2 : 1 (Fig. 18.13b). Therefore, the primary current (I_1) of the pulse transformer can be taken as

$$\frac{I_2}{I_1} = \frac{2}{1} \quad \text{or} \quad I_1 = \frac{100}{2} = 50 \text{ mA}$$

Here, the maximum output current of TTL IC is limited to 0.4 mA for logic "1" level. Neglecting the small V_{BE} voltage drop during the switching of the transistor,

$$R_B \geq \frac{V_{OH}}{I_{OH}} = \frac{2.4}{0.4 \times 10^{-3}} = 6 \text{ k}\Omega$$

We thus choose $R_B = 6.8$ kΩ.

For this purpose, a switching transistor (BC 107, BC 148, BEL100N, 2N222 or similar) may be selected according to voltage and current ratings (V_{CC} and I_C). Let BEL100N (or SL 100) transistor be taken whose specifications are $V_{CBO} = 60 \text{ V}_{(\max)}$, $I_C = 500 \text{ mA}_{(\max)}$, h_{fe} (at $I_C = 150$ mA, $V_{CE} = 1$ V, $T_J = 25\,°\text{C}) = 50$ to 280.

Because the required primary winding current of the pulse transformer $I_1 = I_C = 50$ mA, the value of resistor R_1 (which is used to limit the collector current within the allowable range) is given by

$$R_1 = \frac{V_{CC}}{Ic} = \frac{12}{50 \times 10^{-3}} = 240 \ \Omega$$

Then we choose $R_1 = 220$ Ω.

The power rating of the resistor $= I_C^2 R_1 = (50 \times 10^{-3})^2 \times 220 = 0.65$ W.

Therefore, a 220-Ω, 1-W resistor will be a good choice.

18.5 Drivers for Gate Commutation Switches

Devices from the thyristor family differ from those of the transistor family with respect to their input or drive characteristics. In the case of a thyristor, once it is triggered it continues to be in the same mode unless current through it reduces below its holding current level. However, in the case of transistors, to keep them in the conduction mode, a continuous base or gate signal is required. Basically, transistors or other gate commutation devices are either current controlled (e.g., BJT) or voltage controlled (e.g., MOSFET, IGBT). Similarly, for turn-on operation, GTO behaves as an SCR, while the turn-off operation (or gate current requirements for turn-off) is totally different from the SCR. A GTO requires a large negative gate current and a high power sink for successful commutation (similar to driving requirements of power BJTs). As discussed earlier, normally the driver circuit has to provide an electrically isolated gate/base signal. For the power BJT, the current gain (h_{fe} or β) of the transistor is low ($\beta = 5$ to 10). Therefore, the power capability of the driver circuit should be as high as 20 of the power circuit. However, driving a power MOSFET is similar to driving a very high-impedance capacitive network, thus a carefully designed very low power drive circuit is required. Most gate-voltage-controlled (or gate-commutation-controlled) power semiconductor devices require a very low power driver circuit. Normally, a unipolar drive signal (a positive voltage pulse) is sufficient for normal turn-on and turn-off of the devices. However, for rapid turn-on and turn-off, bipolar signals (both positive and negative voltage pulses) are required. Moreover, for high switching performance, similar circuits with high (source and sink) capabilities are required for MOSFET, IGBT, and BJT alike. For MOSFET/IGBT, the transition current capability should be high (with low output power). However, for BJT, a sustained high base current (in the high output power) is required. For GTO, a very low power circuit is required for turn-on. However, the turn-off circuit capability should be very high (compatible with the power BJT drive circuit). Although it is required for a very small period, the gate power requirement of the negative pulse is about one-third of the power circuit.

18.5.1 Gate Drive Circuits for Power MOSFETs

The input gate characteristics of a MOSFET differ from its bipolar counterparts. The gate is isolated electrically from the source by a layer of silicon dioxide. Ideally, no current flows into the gate when a dc voltage is applied. However, a small leakage current (of the order of 10^{-10} A) flows to maintain the gate voltage and also during the transition periods (off-to-on and on-to-off). Therefore, a small current is enough to charge and discharge the device capacitances. However, the device capacitances and gate-drive source impedance determine the device switching speed. There are three capacitances and they are nonlinear and voltage-dependent (Fig. 18.14). If the gate voltage is reduced to zero for turn-off operation, V_{DS} attains the supply voltage magnitude (V_{DD}), the potential at D swings from 0 to V_{DD} and C_{gd} is charged up to to V_{DD} (say, 100 V) through a low gate source impedance (R_g) as shown in Fig. 18.15a. Now if a gate drive signal is applied (higher than the threshold value), the device will be on. Ideally, the voltage across D and S reduces to zero (neglecting small V_{DS}) and terminal D will swing to ground potential (which earlier was at $V_{DD} = 100$ V). The decreasing V_{DS} produces a feedback current ($i = C_{gd} \cdot dV_{DS}/dt$) through C_{gd} to the gate circuit as shown in Fig. 18.15b. This feedback mechanism is called the "Miller effect." Thus, the source and sink capabilities of the gate drive are required: (i) due to the charging and discharging of C_{gs}; and (ii) due to the large swing in the gate-to-drain voltage. Although C_{gs} is an important parameter, C_{gd} is more significant due to the Miller effect.

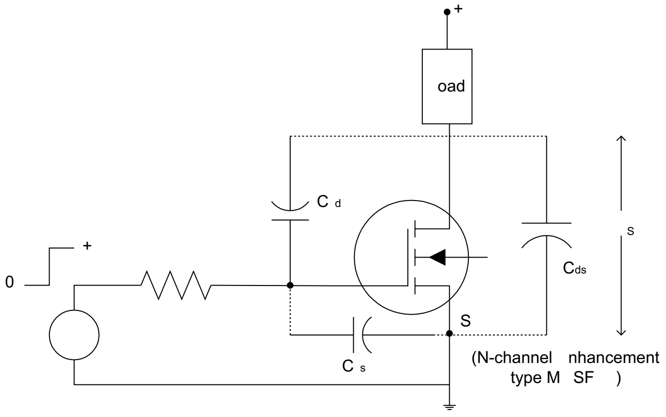


FIGURE 18.14 An *N*-channel enhancement-type MOSFET with voltage-dependent device capacitances.

As the source resistance (R_g) is in series with C_{gs} and C_{gd}, the turn-on time and the turn-off time are affected by this resistance. Therefore, both periods can be controlled independently (Fig. 18.16). Similarly, a bipolar gate drive signal allows rapid turn-on and turn-off.

Low-power digital logic circuits (TTL or CMOS) can easily be used to drive directly the gate of power MOSFET (Fig. 18.17). Because CMOS has limited source current and sink current capabilities (2 and 4 mA $V_{DD} = 12$ V respectively), the modest delay in rise time and fall time are expected due to the Miller effect (charging and discharging current requirements). However, the CMOS IC can directly drive the gate with required magnitude of the drive voltage. For a TTL device with a totem pole output, the output voltage available is approximately 3.5 V (when $V_{cc} = 5$ V). This voltage (3.5 V) may be insufficient to drive the MOSFET into the conduction mode. However, TTL has better source and sink capabilities than its counterpart CMOS, which speeds up the switching

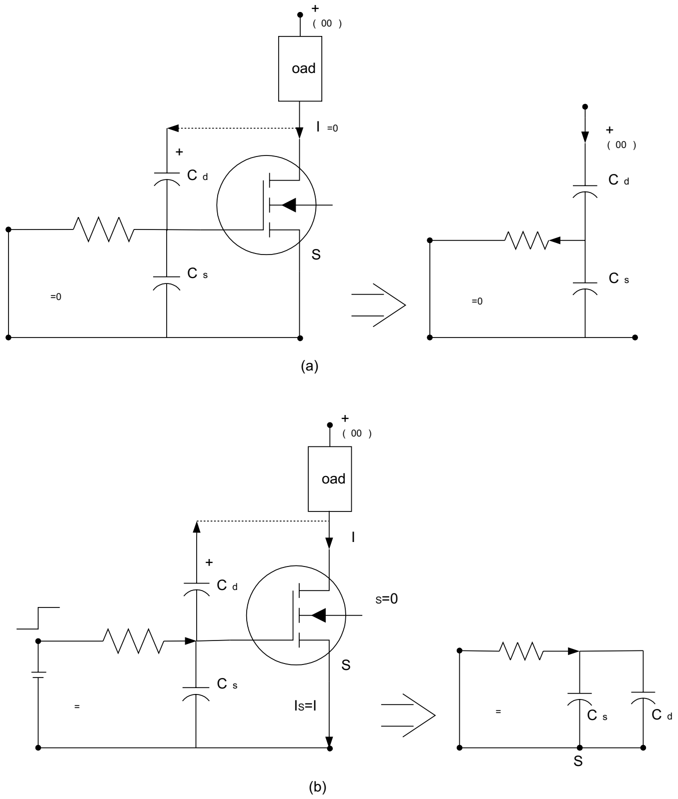


FIGURE 18.15 Large voltage swing at *D*: (a) during turn-off; and (b) during turn-on.

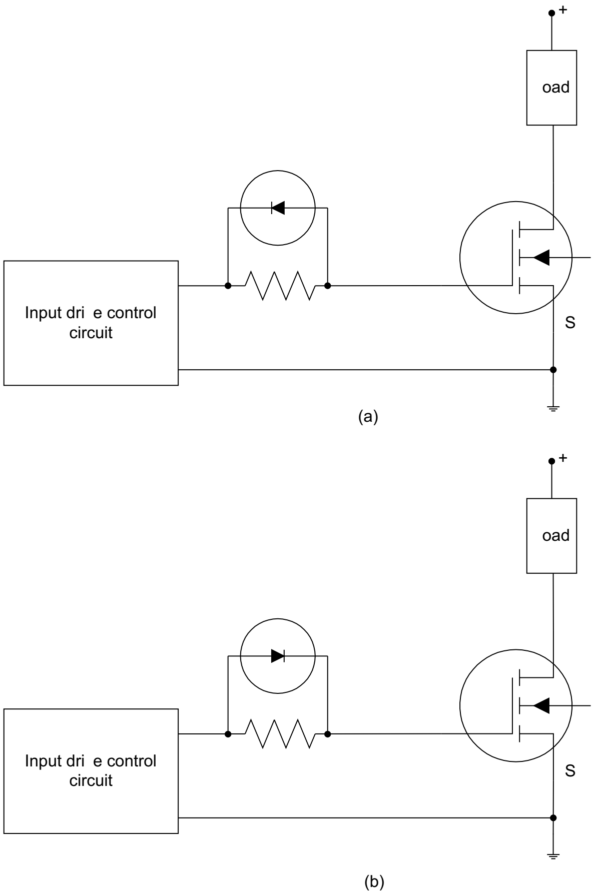
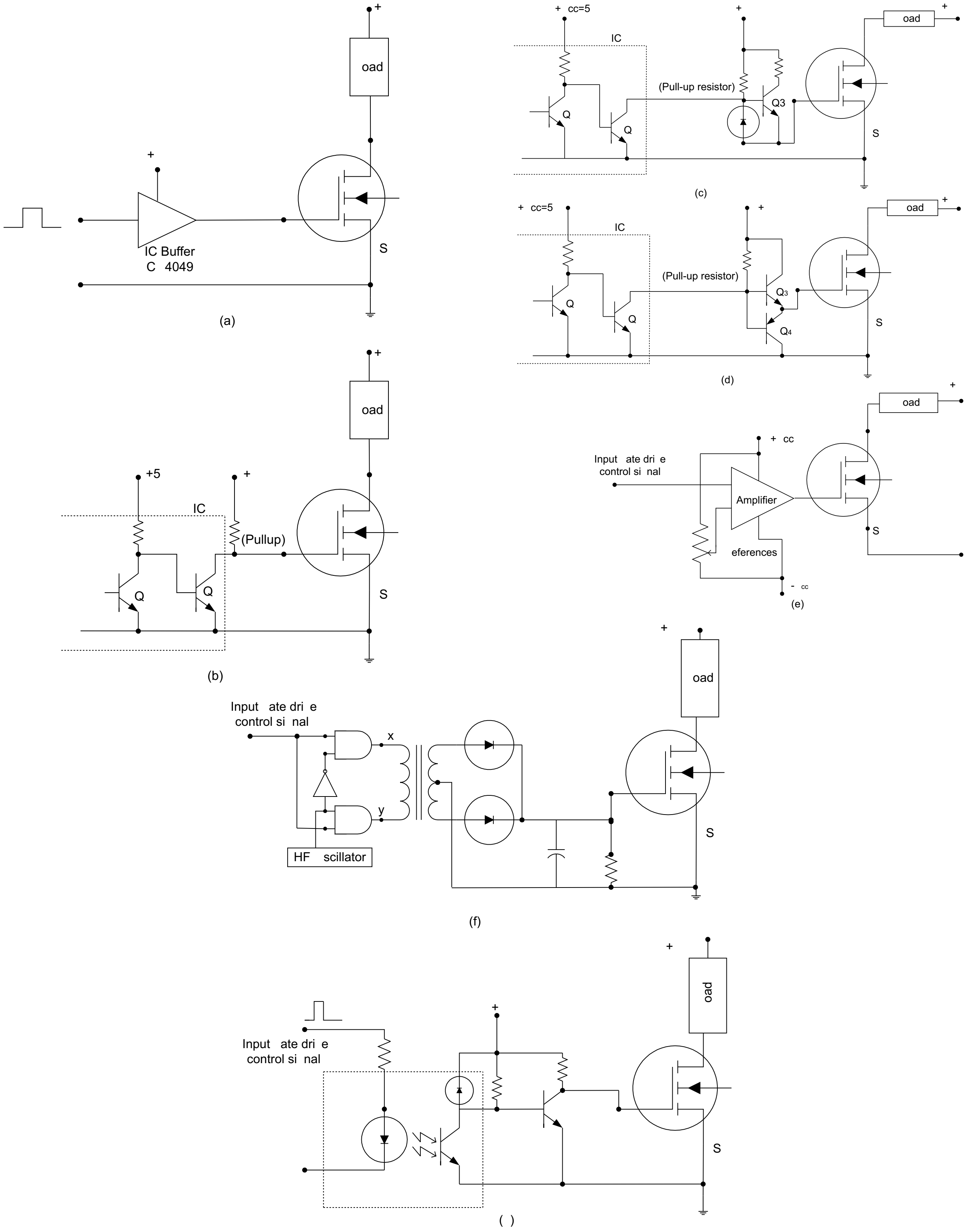


FIGURE 18.16 Driver circuits for (a) delayed turn-on; and (b) delayed turn-off.

transition and reduces turn-on and turn-off times. Thus the output voltage magnitude can be raised by the open-collector TTL device with a pull-up resistor connected to a separate +10 to +15 V dc power supply. It can guarantee rapid gate turn-off due to large sink capability when the output transistor of TTL (inside the TTL IC) is conducting at the logic "0" level (Fig. 18.17). Moreover, this arrangement ensures sufficient gate voltage (10 to 15 V) to turn on the MOSFET fully. However, the turn-on is not as rapid as turn-off because the pull-up resistor delays charging of the device capacitor C_{gs}. Figure 18.17a shows a CMOS-based driver circuit. The output voltage (+10 to +15 V) of CMOS logic is large enough to drive the MOSFET. To increase source and sink capabilities CMOS buffers (CD4049 and CD1450) are used. Thus performance is achieved with respect to switching speeds and low output impedance. To increase the switching speed further, more buffers can be connected in parallel to increase the sink current capabilities for fast turn-off.

Figure 18.17b shows the connection of an open-collector TTL-based driver circuit. The drawback of the TTL output due to its lower magnitude of output (which is the input drive control signal) has been removed. Although an additional dc power supply (+10 to +15 V) will be required, this provides rapid turn-off and ensures sufficient gate voltage to turn on the MOSFET fully.

Figure 18.17c shows a configuration for fast turn-on with reduced power dissipation in TTL. When the TTL output is at the logic "1" level, transistor Q_2 conducts. The output point (cathode of diode and base of Q_2) comes to about the ground potential, and Q_3 remains in the off state. A very small power loss (few milliwatts) occurs in *R* whose value is large, and it behaves as base resistance of Q_3. Similarly, when the TTL output is at the logic "1" level, Q_3 conducts due to the high voltage at its base and the diode becomes reverse-biased. Thus a high voltage (approximately 12 V) reaches the gate of the MOSFET. The conducting Q_3 provides a lower source impedance than *R* (as in the previous case, Fig. 18.17b). Thus the source capability increases, which enables a fast turn-on. The turn-off period depends on the conduction of the TTL output or pull-down transistor Q_2 (by shunting the input gate capacitance of MOSFET to ground). Although the sink and source capability of different types of TTL families varies, the 74AC00 series (logic type) offers better performance for driving the MOSFET. The typical source current and sink current are 24 mA with a 7-ns propagation delay. Only the Schottky (74S00 series) and the low-Schottky (74LS00 series)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Q3
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Q
S
(c)
+ cc=5
IC
+
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(Pull-up resistor)
Q3
Q
Q
Q4
S
(d)
+
oad
+ cc
Input ate dri e
control si nal
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FIGURE 18.17 (a)–(g): CMOS and TTL IC-based driver circuits for MOSFET.

offer less propagation delay (4 ns) but their source and sink current magnitudes are significantly low.

Figure 18.17d shows an open-collector TTL driving a complementary emitter follower (push-pull configuration). This circuit removes the drawback of the lower sink capability of the previous circuit (Fig. 18.17c). Thus, very fast turn-off (hence high switching speed) is attained by using an outboard transistor (Q_4) to clamp the gate-to-ground. Both Q_3 and Q_4 are operating as emitter followers. As they are never driven into saturation, their associated storage times do not significantly affect the switching frequency limit of the gate drive circuit.

Figure 18.17e shows a bipolar driver circuit, where during on and off periods, the input drive signal varies between $+V_{cc}$ to $-V_{cc}$. This type of driver circuit is required for fast switching applications. In this case the turn-on time and turn-off time are small and the configuration is similar to a complementary emitter-follower circuit. Here, source and sink capabilities are increased by providing low output impedance of the operational amplifier. Due to the negative voltage rail ($-V_{cc}$), the input gate capacitor of MOSFET discharges quickly and hence the turn-off time decreases.

Figure 18.17f shows a pulse transformer-based driver circuit. The pulse transformer provides the isolation needed to drive the MOSFETs at different voltage levels (e.g., in a bridge configuration) or to control an *N*-channel MOSFET driving a grounded or source-follower load. The size of the transformer reduces significantly when the operating frequency becomes very high (100 kHz or more). As current and hence the power requirement for the gate driver circuit is very small at steady-state condition (few microwatts only), a separate driver circuit and additional independent dc power supply are not required. However, at the dynamic condition, that is, during turn-on or turn-off transitions, large current (high source and sink capability) is required for fast switching. Another limiting factor is the switching capability of the diode. Thus the Schottky diode can be used because its turn-off time is very small (about 0.23 μs). Here, the high-frequency carrier signal reaches the logic gates when the input drive control signal is high. The output voltage of logic gates become alternately high and low, and therefore current flows in the primary winding of the transformer from *x* to *y* and vice versa. Thus ac voltage, generated in the secondary winding of the transformer, is rectified and filtered. This dc voltage is ultimately used for driving the gate of a MOSFET. Recently, instead of a pulse transformer, a miniturized coreless (planar) transformer of about 1 cm^2, fabricated on a printed-circuit board, was used at 1 MHz for the same application

Figure 18.17g shows an optocoupler-based electrical isolation circuit. This circuit is similar to the optocoupler-based driver circuit discussed for the thyristor (Section 18.4.7).

Moreover, custom-built integrated driver circuits are also available for such applications. Figure 18.18 shows connections of the DS0026 or MMH0026 clock driver, which has been designed for high capacitive loads (high sink and source capability). It has a capability of ±1.5 A output peak current (source and sink) with a typical 15-ns propagation delay, and is compatible with series 54/74 TTL devices.

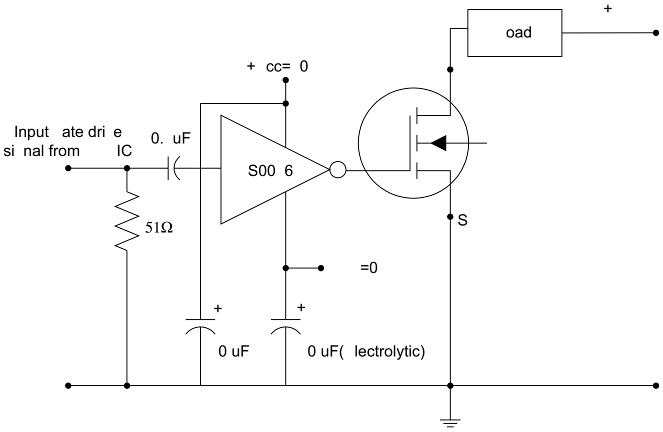

FIGURE 18.18 The DS0026 cloak driver as driver for MOSFET.

Similarly, a large range of such custom-built integrated driver circuits are also available for such applications.

18.5.2 Design Considerations of MOSFET Driver Circuits

Normally, manufacturers do not specify the device capacitances (Fig. 18.14), rather they quote input, output, and reverse common source capacitances (C_{iss}, C_{oss}, and C_{rss}, respectively). All these capacitances are related according to the following:

$$C_{iss} = C_{gs} + C_{gd} \quad \text{where } C_{ds} \text{ shorted} \tag{18.30}$$

$$C_{oss} = C_{ds} + C_{gd} \quad \text{where } C_{gs} \text{ shorted} \tag{18.31}$$

$$C_{rss} = C_{gd} \tag{18.32}$$

The device switching speed depends largely on C_{rss} (or C_{gd}) and the gate drive source impedance. However, two considerations make accurate estimation of switching time (turn-on and turn-off) difficult. First, the magnitude of C_{iss} varies with V_{DS}, particularly large variation at low drain voltage levels. The switching time constant (RC) determined by C_{iss} and gate-drive impedance changes even during the switching cycle. The second consideration is due to the Miller effect. The switching transition can be divided into three distinct periods as shown in Fig. 18.19.

The gate drive requirements for these three periods may be expressed as follows:

$$\begin{aligned} i_G &= C_{iss} \cdot V_{GS(Th)}/(t_1 - t_0) && \text{for } t_0 \le t \le t_1 \\ &= C_{iss}\{(V_{DD} - V_{DS(\text{on})}\}/(t_2 - t_1) && \text{for } t_1 \le t \le t_2 \\ &= C_{iss}\{(V_{GS(\text{on})} - V_{GS(Th)})\}/(t_3 - t_2) && \text{for } t_2 \le t \le t_3 \end{aligned} \tag{18.33}$$

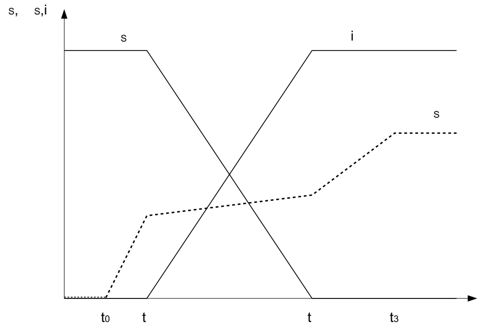

FIGURE 18.19 Ideal switching characteristics of MOSFET with resistive load.

The value of capacitances may be found from the manufacturers data book. For the first two periods, C_{iss} and C_{rss} values may be assumed corresponding to $V_{DS} = 1/2V_{DD}$. While for the third period, assume C_{iss} corresponding to $V_{DS} = V_{DS(\text{on})}$. A small-valued gate resistor of considerable power rating (5 to 20-W range) is used in high-speed switching circuits. This is because the stray inductance of the device assembly connecting wire from driver circuit/chip (on printed circuit board to the gate of MOSFET) and the gate capacitances cause oscillation of input gate current. It behaves as an underdamped series RLC circuit. If there is no gate resistance on the gate driving circuit (ideally), then undamped oscillation will cause a gate voltage (V_{GS}) twice the size of V_{GG}. When the driver chip or circuit operates at $V_{GG} = 12\,\text{V}$, then V_{GS} would be 24 V. However, it could be destructive as maximum V_{GS} is normally 20 V.

The interconnection from the gate driver to the MOSFET can be modeled with a lumped inductance of the following value:

$$L_P = \mu_0 \frac{l_d}{w} \tag{18.34}$$

where $\mu_0 = 4\pi \times 10^{-7}\,\text{H/m} = 4\pi \times 10^{-9}\,\text{H/cm}$, l is the trace length in centimeters, w is the trace width in centimeters, and d is the distance from the trace to the ground plane (that should be under the trace). Let $l = 2\,\text{cm}$, $w = 0.1\,\text{cm}$ and $d = 0.16\,\text{cm}$. Then $L_P = 40\ \eta\text{H}$.

The damping ratio is given by

$$\zeta = \frac{R}{2\sqrt{L_P/C_g}} \tag{18.35}$$

For the total gate input capacitance, let $C_g = 1\,\text{nF}$. Then the resonance frequency of this circuit $(2\sqrt{L_p/C_g})$ is about 25 MHz.

The fastest response of the circuit without overshoot will be for critical damping ($\zeta = 1.0$). Then

$$R = 2\sqrt{\frac{L_p}{C_g}} = 2\sqrt{\frac{40 \times 10^{-9}}{1 \times 10^{-9}}} = 12.6\ \Omega. \tag{18.36}$$

A higher-value gate resistor may efficiently damp out the oscillation but simultaneously it slows down the switching speed of the MOSFET. Because most of the driver chips operate from a 12-V source, they supply or absorb about 1 A or more during the switching transitions. Therefore, 12 Ω is a suitable upper value for the gate resistance to damp out oscillation.

However, the gate drive circuit response will be faster when it is an underdamped circuit. Therefore, if a small overshoot, say, 10 , is allowed, then the corresponding value of $\zeta = 0.6$ (which is found from the universal response curve of a second-order underdamped circuit) is obtained.

Therefore,

$$\zeta = 0.6 = \frac{R}{2\sqrt{L_p/C_g}} \tag{18.37}$$

or $R = 7.56\ \Omega$.

Therefore, normally, a 10-Ω resistor is a suitable choice.

18.5.3 Driver Circuits for IGBT

Basically, an IGBT is a MOSFET-driven power BJT. Thus the same driver circuits used for MOSFET are applicable to the IGBT. It includes fabricated driver circuits as well as custom-built driver circuits as discussed in previous sections.

18.5.4 Transistor-Base Drive Circuits

A properly designed base drive circuit improves reliability by minimizing switching times and hence switching losses, and allows the device to operate in its most robust modes. Ideal base current and voltage waveforms are shown in Fig. 18.20. Initially, a high current pulse should superimpose over the normal turn-on base current supplied from a current source, bringing the BJT rapidly into conduction. This reduces the turn-on switching (transition) time and the switching losses. Similarly, the turn-off switching (transition) time can be

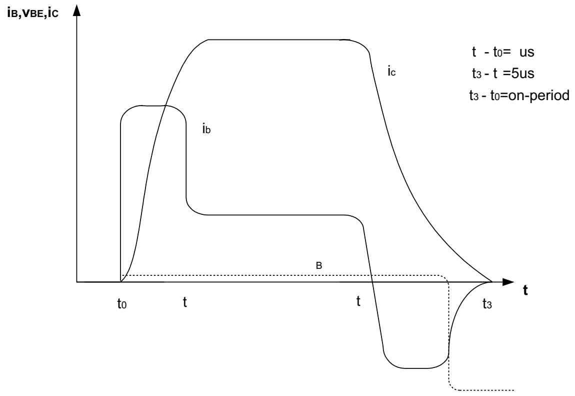

FIGURE 18.20 Ideal base current and voltage requirement of power BJT.

reduced by applying a negative or reverse base current instead of simply ceasing the input drive base current.

Because a high-current, high-power source is required for driving the base of a power BJT, difficulty arises when the emitter is not at ground level (or at a fixed voltage). When the BJTs are connected in a bridge configuration or a load is connected between the emitter and ground, emitter terminal has a floating potential. This potential changes from zero to supply voltage and from supply voltage to zero when the BJT is switched off and switched on, respectively. Figure 18.21 shows simple base drive circuits for a power BJT. The input drive signal is amplified by a *PNP* transistor (Fig. 18.21a), whose I_c ultimately drives the main power BJT. Basically, it is similar to the Darlington circuit. Figure 18.21b shows a transistor to totem-pole arrangement, which reduces power dissipation in the base drive circuit. Although this circuit operates even with unipolar dc power supply (with a 0-V rail instead of $-V_{CC}$), a negative voltage rail speeds up the turn-off transition (turn-off time reduces as in the case of MOSFET). Figure 18.21c shows a *p*-channel MOSFET-based driver circuit. The BJTs are driven by both unipolar as well as bipolar dc supply voltage. The emitter-to-base breakdown voltage rating (V_{ebo}) specifies the maximum negative rail voltage. Normally, −6 to −8 V are used. Therefore, either a ±6 or +12 and −6 V rails may be selected.

18.5.5 Gate Drive Circuit for GTO

The gate drive circuit (shown in Fig. 18.22) for commutation (turn-off) GTO is very similar to the transistor drive circuits discussed in the previous section. The design procedure is the same except that the antisaturation circuit (e.g., BJT in the push-pull mode) and base-to-emitter low-impedance circuit are not necessary. The gate turn-off loop (circuit) should have minimum inductance (including *L*), to increase reverse gate *di*/*dt* and the shorter turn-off time. Therefore, the commutation (turn-off) circuit should be fabricated as close as possible to the gate terminal of the GTO. However, with a shorter turn-off time, the turn-off gain reduces (up to unity). Therefore, the reverse commutating gate current must be almost of the same magnitude as the anode current. A high turn-off gain (over 20) can be achieved at the cost of turn-off switching losses when a slow reverse commutating gate current (slow *di*/*dt*) is applied.

18.6 Some Practical Driver Circuits

An actual drive circuit depends strongly on the type as well as the rating (power handling capability) of the power semiconductor devices. However, the basic circuit configuration does not change significantly. Figure 18.23 shows circuit diagrams for various devices. Figure 18.23a shows a Diac-based trigger circuit. Its performance is better than the previous circuit shown in Fig. 18.9. In this case an RC branch is added to make the switching angle the same in both half-cycles. Figure 18.23b shows a custom-built IC785 used for triggering the SCR, Triac, and so forth. Figure 18.23c shows a simple driver circuit for both MOSFET and IGBT. It works satisfactorily up to several kilohertz of the switching frequency. Figure 18.23f shows a

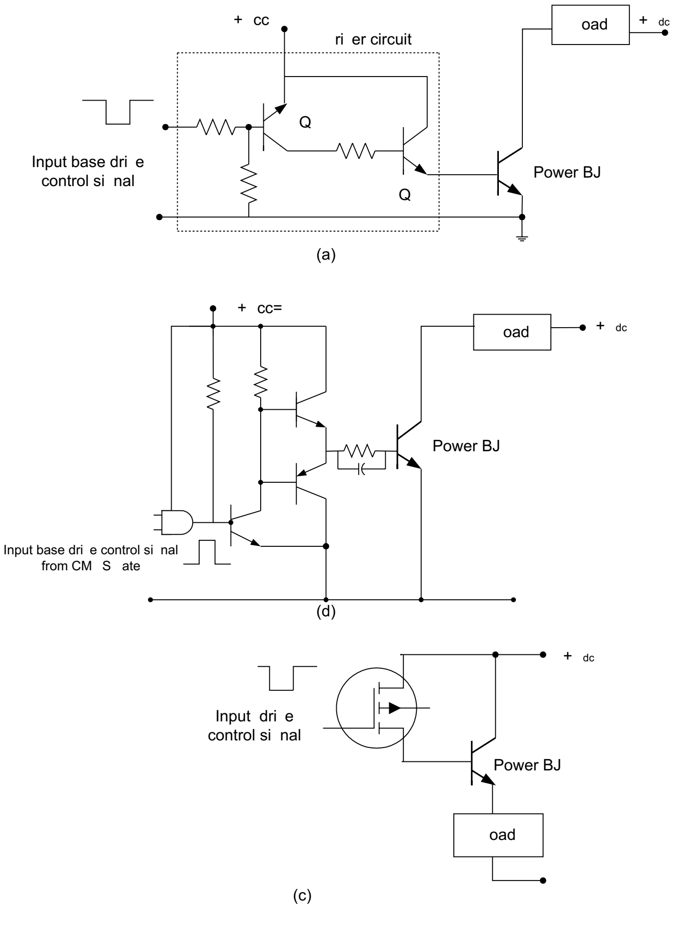

FIGURE 18.21 Base driver circuits for power BJT.

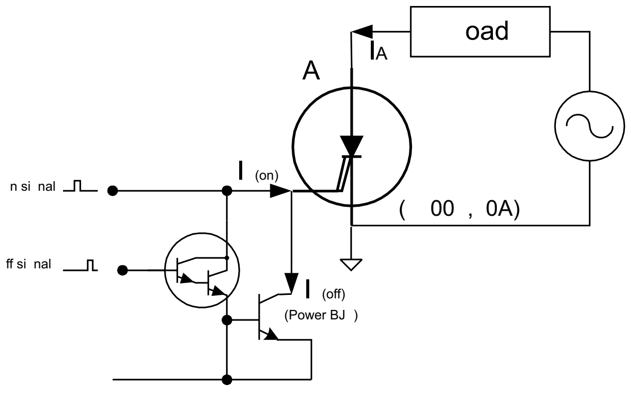

FIGURE 18.22 A typical driver (commutation) circuit for GTO.

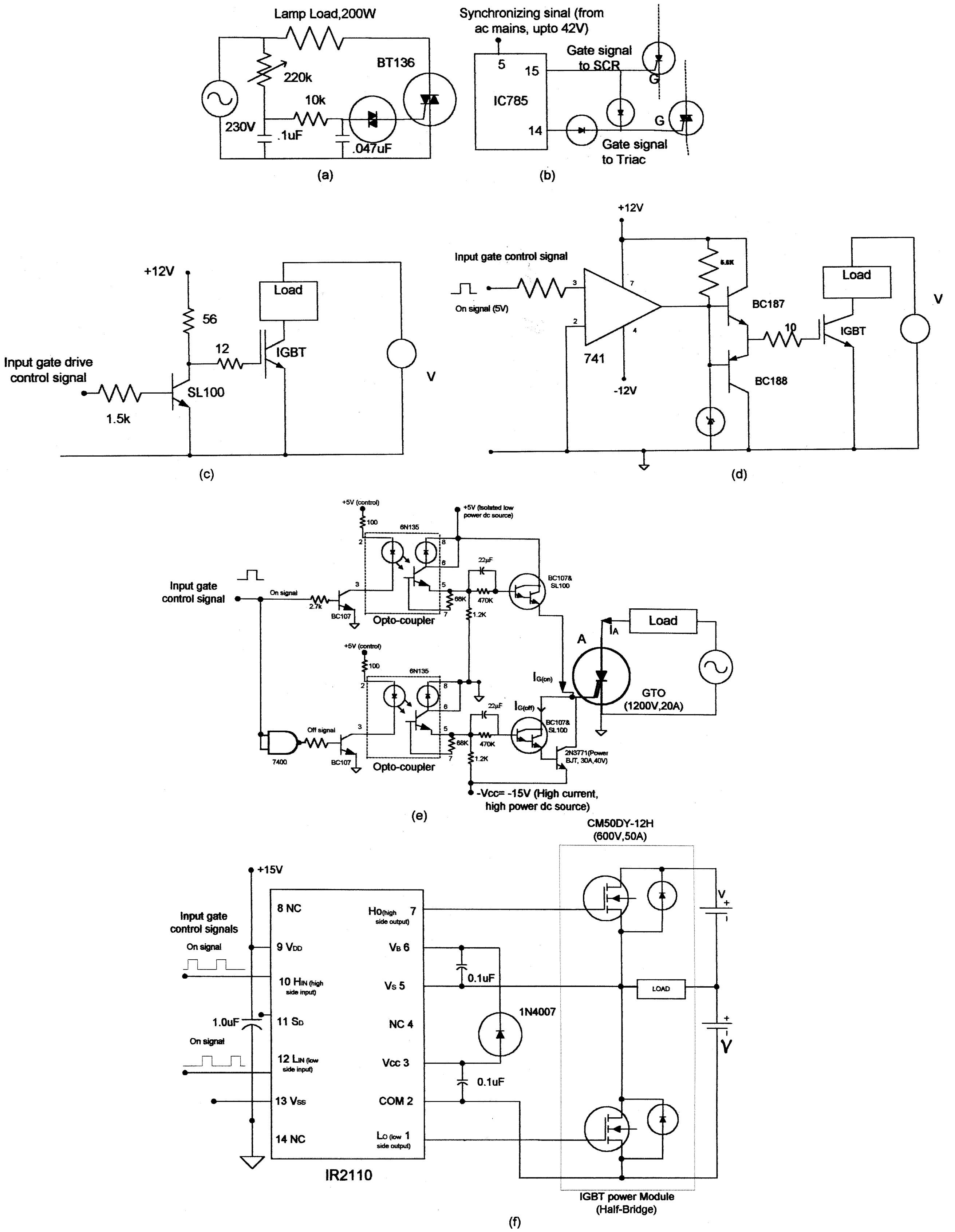
Lamp Load,200W
220k
BT136
10k
230V
.1uF
.047uF
(a)
Synchronizing sinal (from ac mains, upto 42V)
5
15
IC785
14
Gate signal to SCR
G
G
Gate signal to Triac
(b)
+12V
56
Load
12
IGBT
Input gate drive control signal
SL100
1.5k
V
(c)
+12V
Input gate control signal
On signal (5V)
3
2
7
4
741
-12V
5.6K
BC187
10
BC188
Load
IGBT
V
(d)
+5V (control)
100
6N135
+5V (isolated low power dc source)
Input gate control signal
On signal
2.7k
BC107
Opto-coupler
22μF
470K
68K
1.2K
BC107& SL100
Load
A
I_A
$I_{G(on)}$
GTO (1200V,20A)
+5V (control)
100
6N135
Off signal
7400
BC107
Opto-coupler
22μF
$I_{G(off)}$
470K
68K
1.2K
BC107& SL100
2N3771(Power BJT, 30A,40V)
-Vcc= -15V (High current, high power dc source)
(e)
CM50DY-12H (600V,50A)
+15V
Input gate control signals
On signal
On signal
1.0uF
8 NC
9 VDD
10 HIN (high side input)
11 SD
12 LIN (low side input)
13 VSS
14 NC
Ho (high side output) 7
VB 6
Vs 5
NC 4
Vcc 3
COM 2
Lo (low side output) 1
IR2110
0.1uF
1N4007
0.1uF
LOAD
V
V
IGBT power Module (Half-Bridge)
(f)

FIGURE 18.23 Various practical driver circuits.

custom-built driver circuit using IC chip IR2110 for driving an IGBT power module of a half-bridge inverter circuit. Such custom-built driver circuits have high source and sink capability (2A for IR2110).

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19

Control Methods for Power Converters

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1 .1 Introduction

Electronic power converters must be suitably controlled in order to supply the voltages, currents, or frequency ranges needed for the load and to guarantee the requested dynamics.[1] Furthermore, they can be designed to serve as "clean" interfaces between most loads and the electrical utility system. Thereafter, the electrical utility seems to feed almost pure resistive loads.

This chapter provides basic and some advanced skills to control electronic power converters, taking into account that the control of power converters is a vast and interdisciplinary subject. Control designers for power converters should know the static and dynamic behavior of the electronic power converter and how to design its elements for the intended operating modes. Designers must be experts on control techniques, especially the nonlinear ones, since power converters are nonlinear, time variant, discrete systems, and designers must be capable of analog or digital implementation of the derived modulators, regulators, or compensators. Powerful modeling methodologies and sophisticated control processes must be used to obtain stable controlled power converters not only with satisfactory static and dynamic performance, but also with low sensitivity against load or line disturbances or, preferably, robustness.

In Section 19.2, techniques to obtain suitable nonlinear and linear state-space models, for most power converters, are presented and illustrated through examples. The derived linear models are used to create equivalent circuits, and to design linear feedback control methods for converters operating in the continuous or discontinuous mode. The classical linear systems control theory, based on Laplace transform, transfer function concepts, Bode plots, and root locus, is best used with state-space averaged models, or derived circuits, and the well-known triangular wave modulators for generating the switching functions or the trigger signals for the power semiconductors.

Nonlinear state-space models and sliding-mode controllers, presented in Section 19.3, provide a more consistent way of handling the control problem of power converters, since sliding mode is aimed at variable structure systems, as are power converters. Chattering, a characteristic of sliding mode, is inherent in switching power converters, even if they are controlled with linear methods. Chattering is very hard to remove and is acceptable in certain converter variables. The explained sliding-mode control law defines exactly the variables that need to be measured, while providing the necessary equations (control law and switching law) whose implementation gives the modulator and compensator low-level hardware (or software). Therefore, sliding-mode control integrates the

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design of the power converter modulator and controller electronics, reducing the needed designer expertise. This approach requires measurement of the state variables, but eliminates conventional modulators and linear feedback compensators, enabling better performance and robustness, while reducing the converter cost, control complexity, volume, and weight (the power density figure increases). The so-called main drawback of sliding mode, variable switching frequency, is also addressed, providing fixed-frequency auxiliary functions and suitable augmented control laws to null steady-state errors due to the use of constant switching frequency.

Fuzzy control of power converters (Section 19.4) is a control technique needing no converter models, parameters, or operating conditions, but only an expert knowledge of the converter dynamics. Fuzzy controllers can be used in a diverse array of power converters with only small adaptations, since the controllers, based on fuzzy sets, are obtained simply from a knowledge of the system dynamics, using a model reference adaptive control philosophy. Obtained fuzzy control rules can be built into a decision lookup table, in which the control processor simply picks up the control input corresponding to the sampled measurements. Fuzzy controllers are almost immune to system parameter fluctuations, since they do not take into account their values. The steps to obtain a fuzzy controller are described, and the example provided compares the fuzzy controller performance to current mode control.

1 .2 Power Converter Control using State-Space Averaged Models

1 .2.1 Introduction

State-space models provide a general and strong basis for dynamic modeling of various systems including power converters[6,7]. State-space models are useful to design the needed linear control loops, and can also be used to computer simulate the steady state, as well as the dynamic behavior of the power converter, fitted with the designed feedback control loops and subjected to external perturbations. Furthermore, state-space models are the basis for applying powerful nonlinear control methods such as sliding mode. State-space averaging and linearization provides an elegant solution for the application of widely known linear control techniques to most power converters.

1 .2.2 State-Space Modeling

Consider a power converter with sets of power semiconductor structures, each one with two different circuit configurations, according to the state of the respective semiconductors, and operating in the continuous mode of conduction. Supposing the power semiconductors as controlled ideal switches (zero on-state voltage drops, zero off-state currents, and instantaneous commutation between the on and off states), the time (t) behavior of the circuit, over period T, can be represented by the general form of the state-space model (19.1):

$$\begin{aligned} \dot{\ } &= \mathbf{A}\ \ + \mathbf{Bu} \\ \mathbf{y} &= \mathbf{C}\ \ + \mathbf{Du} \end{aligned} \qquad (19.1)$$

where is the state vector, $\dot{\ } = \mathrm{d}\ /\mathrm{d}t$, $\mathbf{u}$ the input or control vector, and $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, $\mathbf{D}$ are respectively the dynamics (or state), the input, the output and the direct transmission (or feedforward) matrices.

Since the power semiconductors will either be conducting or blocking, the time-dependent switching function $\delta(t)$ can be used to describe the allowed switch states of each structure (e.g., $\delta(t) = 1$ for the on state circuit and $\delta(t) = 0$ for the off state circuit). Then, two subintervals must be considered: subinterval 1 for $0 \le t \le \delta_1 T$, where $\delta(t) = 1$ and subinterval 2 for $\delta_1 T \le t \le T$ where $\delta(t) = 0$. The state equations of the circuit, in each of the circuit configurations, can be written as:

$$\begin{aligned} \dot{\ } &= \mathbf{A}_1\ \ + \mathbf{B}_1\mathbf{u} \\ \mathbf{y} &= \mathbf{C}_1\ \ + \mathbf{D}_1\mathbf{u} \end{aligned} \quad \text{for } 0 \le t \le \delta_1 T \text{ where } \delta(t) = 1 \qquad (19.2a)$$

$$\begin{aligned} \dot{\ } &= \mathbf{A}_2\ \ + \mathbf{B}_2\mathbf{u} \\ \mathbf{y} &= \mathbf{C}_2\ \ + \mathbf{D}_2\mathbf{u} \end{aligned} \quad \text{for } \delta_1 T \le t \le T \text{ where } \delta(t) = 0 \qquad (19.2b)$$

1 .2.2.1 Switched State-Space Model

Given the two binary values of the switching function $\delta(t)$, (19.2a) and (19.2b) can be combined to obtain the nonlinear and time-variant switched state-space model of the power converter circuit, (19.3) or (19.4):

$$\begin{aligned} \dot{\ } &= [\mathbf{A}_1\delta(t) + \mathbf{A}_2(1 - \delta(t)]\ \ + [\mathbf{B}_1\delta(t) + \mathbf{B}_2(1 - \delta(t))]\mathbf{u} \\ \mathbf{y} &= [\mathbf{C}_1\delta(t) + \mathbf{C}_2(1 - \delta(t))]\ \ + [\mathbf{D}_1\delta(t) + \mathbf{D}_2(1 - \delta(t))]\mathbf{u} \end{aligned} \qquad (19.3)$$

$$\begin{aligned} \dot{\ } &= \mathbf{A}_S\ \ + \mathbf{B}_S\mathbf{u} \\ \mathbf{y} &= \mathbf{C}_S\ \ + \mathbf{D}_S\mathbf{u} \end{aligned} \qquad (19.4)$$

where

$$\begin{aligned} \mathbf{A}_S &= [\mathbf{A}_1\delta(t) + \mathbf{A}_2(1 - \delta(t))] \\ \mathbf{B}_S &= [\mathbf{B}_1\delta(t) + \mathbf{B}_2(1 - \delta(T))] \\ \mathbf{C}_S &= [\mathbf{C}_1\delta(t) + \mathbf{C}_2(1 - \delta(T))] \end{aligned}$$

and

$$\mathbf{D}_S = [\mathbf{D}_1\delta(t) + \mathbf{D}_2(1 - \delta(t))].$$

1 .2.2.2 State-Space Averaged Model

Since the state variables of the vector are continuous, using (19.3), with the initial conditions $_1(0) = {}_2(T)$, $_2(\delta_1 T) = {}_1(\delta_1 T)$, and considering the duty cycle δ_1 as the average value of $\delta(t)$, the time evolution of the converter state variables can be obtained, integrating (19.3) over the intervals

$0 \le t \le \delta_1 T$ and $\delta_1 T \le t \le T$, although it often requires excessive calculation effort. However, a convenient approximation can be devised, considering $\lambda_{\max}$ the maximum of the absolute values of all eigenvalues of $\mathbf{A}$ (usually $\lambda_{\max}$ is related to the cutoff frequency f_c of an equivalent low-pass filter with $f_c \ll 1/T$). For $\lambda_{\max} T \ll 1$, the exponential matrix (or state transition matrix) $e^{\mathbf{A}t} = \mathbf{I} + \mathbf{A}t + \mathbf{A}^2 t^2/2 + \cdots + \mathbf{A}^n t^n/n!$, where $\mathbf{I}$ is the identity or unity matrix, can be approximated by $e^{\mathbf{A}t} \approx \mathbf{I} + \mathbf{A}t$. Therefore,

$$\mathbf{e}^{\mathbf{A}_1\delta_1 t}\mathbf{e}^{\mathbf{A}_2(1-\delta_1)t} \approx \mathbf{I} + [\mathbf{A}_1\delta_1 + \mathbf{A}_2(1-\delta_1)]t.$$

Hence, the solution over the period T, for the system represented by (19.3), is found to be:

$$\begin{aligned}(T) &\cong e^{[\mathbf{A}_1\delta_1+\mathbf{A}_2(1-\delta_1)]T}\ {}_1(0)\\ &+ \int_0^T e^{[\mathbf{A}_1\delta_1+\mathbf{A}_2(1-\delta_1)](T-\tau)}[\mathbf{B}_1\delta_1 + \mathbf{B}_2(1-\delta_1)]\mathbf{u}\,d\tau \quad (19.5)\end{aligned}$$

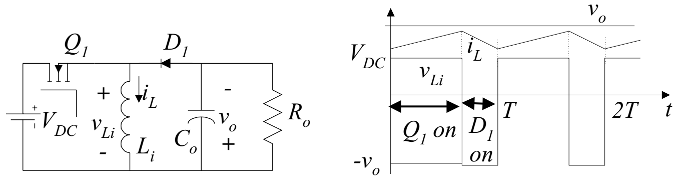
This approximate response of (19.3) is identical to the exact response obtained from the nonlinear continuous time invariant state space model (19.6), supposing that the average values of , denoted $\bar{}$, are the new state variables, and considering $\delta_2 = 1 - \delta_1$. Moreover, if $\mathbf{A}_1\,\mathbf{A}_2 = \mathbf{A}_2\,\mathbf{A}_1$ the approximation is exact.

$$\begin{aligned}\dot{\bar{}} &= [\mathbf{A}_1\delta_1 + \mathbf{A}_2\delta_2]^{-} + [\mathbf{B}_1\delta_1 + \mathbf{B}_2\delta_2]\bar{\mathbf{u}}\\ \bar{\mathbf{y}} &= [\mathbf{C}_1\delta_1 + \mathbf{C}_2\delta_2]^{-} + [\mathbf{D}_1\delta_1 + \mathbf{D}_2\delta_2]\bar{\mathbf{u}}\end{aligned} \quad (19.6)$$

For $\lambda_{max} T \ll 1$, the most often referred to as the state space averaged model (19.6), is also said to be obtained by "averaging" (19.3) over one period, under small ripple and slow variations, as the average of products is approximated by products of the averages. By comparing (19.6) to (19.1), the relations (19.7), defining the state-space averaged model, are obtained.

$$\begin{aligned}\mathbf{A} &= [\mathbf{A}_1\delta_1 + \mathbf{A}_2\delta_2]; &\quad \mathbf{B} &= [\mathbf{B}_1\delta_1 + \mathbf{B}_2\delta_2];\\ \mathbf{C} &= [\mathbf{C}_1\delta_1 + \mathbf{C}_2\delta_2]; &\quad \mathbf{D} &= [\mathbf{D}_1\delta_1 + \mathbf{D}_2\delta_2].\end{aligned} \quad (19.7)$$

Example 19.1. State-Space Models for the Buck-Boost dc/dc Converter. Consider the simplified circuitry of the buck-boost converter of Fig. 19.1 switching at $f_s = 20$ kHz ($T = 50$ μs) with $V_{DC\max} = 28$ V, $V_{DC\min} = 22$ V, $V_o = 24$ V, $L_i = 400$ μH, $C_o = 2700$ μF, $R_o = 2\ \Omega$.



a) b)

FIGURE 19.1 (a) Basic circuit of the buck-boost dc/dc converter; (b) ideal waveforms.

The differential equations governing the dynamics of the state vector $= [i_L, v_o]^T$ (^{T} denotes the transpose of vectors or matrices) are:

$$\begin{aligned}L_i\frac{di_L}{dt} &= V_{DC}\\ C_o\frac{dv_o}{dt} &= -\frac{v_o}{R_o}\end{aligned}\qquad \begin{aligned}&\text{for } 0 \le t \le \delta_1 T\ \delta(t) = 1,\\ &Q_1 \text{ is on and } D_1 \text{ is off)}\end{aligned} \quad (19.8a)$$

$$\begin{aligned}L_i\frac{di_L}{dt} &= -v_o\\ C_o\frac{dv_o}{dt} &= i_L - \frac{v_o}{R_o}\end{aligned}\qquad \begin{aligned}&\text{for } \delta_1 T \le t \le T\ (\delta(t) = 0,\\ &Q_1 \text{ is off and } D_1 \text{ is on)}\end{aligned} \quad (19.8b)$$

Comparing (19.8) to (19.2) and considering $\mathbf{y} = [v_o, i_L]^T$ the following matrices can be identified:

$$\mathbf{A}_1 = \begin{bmatrix} 0 & 0\\ 0 & -1/(R_oC_o)\end{bmatrix};\ \mathbf{A}_2 = \begin{bmatrix} 0 & -1/L_i\\ 1/C_o & -1/(R_oC_o)\end{bmatrix};$$

$$\mathbf{B}_1 = [1/L_i, 0]^T;\ \mathbf{B}_2 = [0, 0]^T;\ \mathbf{u} = [V_{DC}];$$

$$\mathbf{C}_1 = \begin{bmatrix} 0 & 1\\ 1 & 0\end{bmatrix};\ \mathbf{C}_2 = \begin{bmatrix} 0 & 1\\ 1 & 0\end{bmatrix};\ \mathbf{D}_1 = [0, 0]^T;\ \mathbf{D}_2 = [0, 0]^T$$

From (19.3) and (19.4), the switched state space model of this power converter is:

$$\begin{aligned}\begin{bmatrix}\dot{i}_L\\ \dot{v}_o\end{bmatrix} &= \begin{bmatrix} 0 & -(1-\delta(t))/L_i\\ (1-\delta(T))/C_o & -1/(R_oC_o)\end{bmatrix}\begin{bmatrix} i_L\\ v_o\end{bmatrix} + \begin{bmatrix}\delta(t)/L_i\\ 0\end{bmatrix}V_{DC}\\ \begin{bmatrix} v_o\\ i_L\end{bmatrix} &= \begin{bmatrix} 0 & 1\\ 1 & 0\end{bmatrix}\begin{bmatrix} i_L\\ v_o\end{bmatrix} + \begin{bmatrix}0\\ 0\end{bmatrix}[V_{DC}]\end{aligned} \quad (19.9)$$

Now applying (19.6), Eqs. (19.10a) and (19.10b) can be obtained:

$$\begin{aligned}\begin{bmatrix}\dot{\bar{i}}_L\\ \dot{\bar{v}}_o\end{bmatrix} &= \left[\begin{bmatrix} 0 & 0\\ 0 & \dfrac{-1}{R_oC_o}\end{bmatrix}\delta_1 + \begin{bmatrix} 0 & \dfrac{-1}{L_i}\\ \dfrac{1}{C_o} & \dfrac{-1}{R_oC_o}\end{bmatrix}\delta_2\right]\begin{bmatrix}\bar{i}_L\\ \bar{v}_o\end{bmatrix}\\ &+ \left[\begin{bmatrix}\dfrac{1}{L_i}\\ 0\end{bmatrix}\delta_1 + \begin{bmatrix}0\\ 0\end{bmatrix}\delta_2\right][\bar{V}_{DC}]\end{aligned} \quad (19.10a)$$

$$\begin{aligned}\begin{bmatrix}\bar{v}_o\\ \bar{i}_L\end{bmatrix} &= \left[\begin{bmatrix} 0 & 1\\ 1 & 0\end{bmatrix}\delta_1 + \begin{bmatrix} 0 & 1\\ 1 & 0\end{bmatrix}\delta_2\right]\begin{bmatrix}\bar{i}_L\\ \bar{v}_o\end{bmatrix}\\ &+ \left[\begin{bmatrix}0\\ 0\end{bmatrix}\delta_1 + \begin{bmatrix}0\\ 0\end{bmatrix}\delta_2\right][\bar{V}_{DC}]\end{aligned} \quad (19.10b)$$

From (19.10), the state space averaged model, written as function of δ_1, is:

$$\begin{bmatrix}\dot{\bar{i}}_L\\ \dot{\bar{v}}_o\end{bmatrix} = \begin{bmatrix}0 & -\dfrac{1-\delta_1}{L_i}\\ \dfrac{1-\delta_1}{C_o} & \dfrac{-1}{R_oC_o}\end{bmatrix}\begin{bmatrix}\bar{i}_L\\ \bar{v}_o\end{bmatrix} + \begin{bmatrix}\dfrac{\delta_1}{L_i}\\ 0\end{bmatrix}[\bar{V}_{DC}] \qquad (19.11a)$$

$$\begin{bmatrix}\bar{v}_o\\ \bar{i}_L\end{bmatrix} = \begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}\begin{bmatrix}\bar{i}_L\\ \bar{v}_o\end{bmatrix} + \begin{bmatrix}0\\ 0\end{bmatrix}[\bar{V}_{DC}] \qquad (19.11b)$$

The eigenvalues $s_{bb_{1,2}}$, or characteristic roots of **A**, are the roots of $|\mathbf{sI} - \mathbf{A}|$. Therefore:

$$s_{bb_{1,2}} = \frac{-1}{2R_oC_o} \pm \sqrt{\frac{1}{4(R_oC_o)^2} - \frac{(1-\delta_1)^2}{L_iC_o}} \qquad (19.12)$$

Since $\lambda_{\max}$ is the maximum of the absolute values of all the eigenvalues of **A**, the model (19.11) is valid for switching frequencies f_s ($f_s = 1/T$) that verify $\lambda_{\max} T \ll 1$. Therefore, as $T \ll 1/\lambda_{\max}$ the values of T that approximately verify this restriction are $T \ll 1/\max(|s_{bb_{1,2}}|)$. Given this buck-boost converter data, $T \ll 2$ ms is obtained. Therefore, the converter switching frequency must obey $f_s \gg \max(|s_{f_{1,2}}|)$, implying switching frequencies above, say, 5 kHz. Consequently, the buck-boost switching frequency, the inductor value and the capacitor value, were chosen accordingly.

This restriction can be further used to discuss the maximum frequency $\omega_{\max}$ for which the state-space averaged model is still valid, given a certain switching frequency. As $\lambda_{\max}$ can be regarded as a frequency, the preceding constraint brings $\omega_{\max} \ll 2\pi f_s$, say, $\omega_{\max} < 2\pi f_s/10$, which means that the state-space averaged model is a good approximation at frequencies under one tenth of the power converter switching frequency.

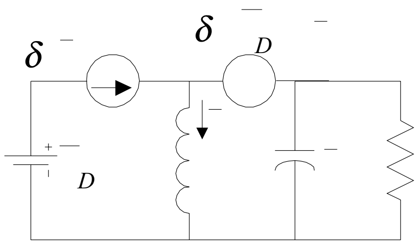
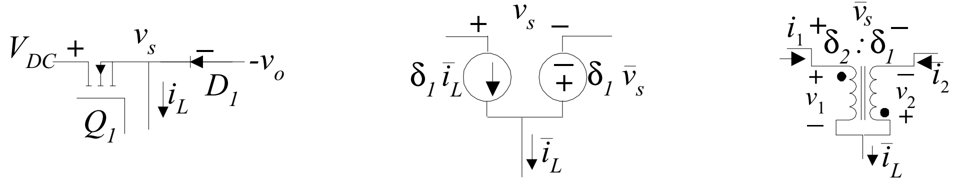


FIGURE 19.2 Equivalent circuit of the averaged state-space model of the buck-boost converter.

The state-space averaged model (19.11) is also the state-space model of the circuit represented in Fig. 19.2. Hence, this circuit is designated as the averaged equivalent circuit of the buck-boost converter and allows the determination, under small ripple and slow variations, of the average equivalent circuit of the converter switching cell (power transistor plus diode).

The average equivalent circuit of the switching cell (Fig. 19.3a) is represented in Fig. 19.3b and emerges directly from the state space averaged model (19.11). This equivalent circuit can be viewed as the model of an "ideal transformer" (Fig. 19.3c), whose primary to secondary ratio (v_1/v_2) can be calculated applying Kirchhoff voltage laws to obtain $-v_1 + v_s - v_2 = 0$. As $v_2 = \delta_1 v_s$, it follows that $v_1 = v_s(1-\delta_1)$, giving $(v_1/v_2) = (1-\delta_1)/\delta_1$. The same ratio could be obtained beginning with $i_L = i_1 + i_2$, and $i_1 = \delta_1 i_L$ (Fig. 19.3b), which gives $i_2 = i_L(1-\delta_1)$ and $(i_2/i_1) = \delta_2/\delta_1$.

The average equivalent circuit concept, obtained from (19.6) or (19.11), can be applied to other power converters, with or without a similar switching cell, to obtain transfer functions or to computer simulate the converter average behavior. The average equivalent circuit of the switching cell can be applied to converters with the same switching cell operating in the continuous conduction mode. However, note that the state variables of (19.6) or (19.11) are mean values of the converter instantaneous variables and, therefore, do not represent their ripple components. The inputs of the state-space averaged model are the mean values of the inputs over one switching period.



a) b) c)

FIGURE 19.3 Average equivalent circuit of the switching cell. (a) Switching cell; (b); average equivalent circuit; (c) average equivalent circuit using an ideal transformer.

1 .2.2.3 Linearized State-Space Averaged Model

Since the converter outputs $\bar{\mathbf{y}}$ must be regulated actuating on the duty cycle $\delta(t)$, and the converter inputs $\bar{\mathbf{u}}$ usually present perturbations due to load and power supply variations, state variables are decomposed in small ac perturbations (denoted by "$\sim$") and dc steady-state quantities (represented by uppercase letters). Therefore:

$$\begin{aligned} \bar{\ } &= \mathbf{X} + \tilde{\ } \\ \bar{\mathbf{y}} &= \quad + \tilde{\mathbf{y}} \\ \bar{\mathbf{u}} &= \mathbf{U} + \tilde{\mathbf{u}} \\ \delta_1 &= \Delta_1 + \tilde{\delta} \\ \delta_2 &= \Delta_2 - \tilde{\delta} \end{aligned} \tag{19.13}$$

Using (19.13) in (19.6) and rearranging terms, we obtain

$$\begin{aligned} \dot{\tilde{\ }} = {} & [\mathbf{A}_1\Delta_1 + \mathbf{A}_2\Delta_2]\mathbf{X} + [\mathbf{B}_1\Delta_1 + \mathbf{B}_2\Delta_2]\mathbf{U} \\ & + [\mathbf{A}_1\Delta_1 + \mathbf{A}_2\Delta_2]\tilde{\ } + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}]\tilde{\delta} \\ & + [\mathbf{B}_1\Delta_1 + \mathbf{B}_2\Delta_2]\tilde{\mathbf{u}} + [(\mathbf{A}_1 - \mathbf{A}_2)\tilde{\ } + (\mathbf{B}_1 - \mathbf{B}_2)\tilde{\mathbf{u}}]\tilde{\delta} \end{aligned} \tag{19.14}$$

$$\begin{aligned} + \tilde{\mathbf{y}} = {} & [\mathbf{C}_1\Delta_1 + \mathbf{C}_2\Delta_2]\mathbf{X} + [\mathbf{D}_1\Delta_1 + \mathbf{D}_2\Delta_2]\mathbf{U} \\ & + [\mathbf{C}_1\Delta_1 + \mathbf{C}_2\Delta_2]\tilde{\ } + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{D}_1 - \mathbf{D}_2)\mathbf{U}]\tilde{\delta} \\ & + [\mathbf{D}_1\Delta_1 + \mathbf{D}_2\Delta_2]\tilde{\mathbf{u}} + [(\mathbf{C}_1 - \mathbf{C}_2)\tilde{\ } + (\mathbf{D}_1 - \mathbf{D}_2)\tilde{\mathbf{u}}]\tilde{\delta} \end{aligned} \tag{19.15}$$

The terms

$$[\mathbf{A}_1\Delta_1 + \mathbf{A}_2\Delta_2]\mathbf{X} + [\mathbf{B}_1\Delta_1 + \mathbf{B}_2\Delta_2]\mathbf{U}$$

and

$$[\mathbf{C}_1\Delta_1 + \mathbf{C}_2\Delta_2]\mathbf{X} + [\mathbf{D}_1\Delta_1 + \mathbf{D}_2\Delta_2]\mathbf{U},$$

respectively from (19.14) and from (19.15), represent the steady-state behavior of the system. As in steady state $\dot{\mathbf{X}} = \mathbf{0}$, the following relationships hold:

$$\mathbf{0} = [\mathbf{A}_1\Delta_1 + \mathbf{A}_2\Delta_2]\mathbf{X} + [\mathbf{B}_1\Delta_1 + \mathbf{B}_2\Delta_2]\mathbf{U} \tag{19.16}$$

$$= [\mathbf{C}_1\Delta_1 + \mathbf{C}_2\Delta_2]\mathbf{X} + [\mathbf{D}_1\Delta_1 + \mathbf{D}_2\Delta_2]\mathbf{U} \tag{19.17}$$

Neglecting higher order terms $([\mathbf{A}_1 - \mathbf{A}_2)\tilde{\ } + (\mathbf{B}_1 - \mathbf{B}_2)\tilde{\mathbf{u}}]\tilde{\delta} \approx 0)$ of (19.14) and (19.15), the linearized small-signal state-space averaged model is:

$$\begin{aligned} \dot{\tilde{\ }} &= [\mathbf{A}_1\Delta_1 + \mathbf{A}_2\Delta_2]\tilde{\ } + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}]\tilde{\delta} \\ &\quad + [\mathbf{B}_1\Delta_1 + \mathbf{B}_2\Delta_2]\tilde{\mathbf{u}} \\ \tilde{\mathbf{y}} &= [\mathbf{C}_1\Delta_1 + \mathbf{C}_2\Delta_2]\tilde{\ } + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{D}_1 - \mathbf{D}_2)\mathbf{U}]\tilde{\delta} \\ &\quad + [\mathbf{D}_1\Delta_1 + \mathbf{D}_2\Delta_2]\tilde{\mathbf{u}} \end{aligned} \tag{19.18}$$

or:

$$\begin{aligned} \dot{\tilde{\ }} &= \mathbf{A}_{av}\tilde{\ } + \mathbf{B}_{av}\tilde{\mathbf{u}} + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}]\tilde{\delta} \\ \tilde{\mathbf{y}} &= \mathbf{C}_{av}\tilde{\ } + \mathbf{D}_{av}\tilde{\mathbf{u}} + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{D}_1 - \mathbf{D}_2)\mathbf{U}]\tilde{\delta} \end{aligned} \tag{19.19}$$

with:

$$\begin{aligned} \mathbf{A}_{av} &= [\mathbf{A}_1\Delta_1 + \mathbf{A}_2\Delta_2] \\ \mathbf{B}_{av} &= [\mathbf{B}_1\Delta_1 + \mathbf{B}_2\Delta_2] \\ \mathbf{C}_{av} &= [\mathbf{C}_1\Delta_1 + \mathbf{C}_2\Delta_2] \\ \mathbf{D}_{av} &= [\mathbf{D}_1\Delta_1 + \mathbf{D}_2\Delta_2] \end{aligned} \tag{19.20}$$

1 .2.3 Converter Transfer Functions

Using (19.16) in (19.17) the input $\mathbf{U}$ to output steady state relations (19.21), needed for open-loop and feed-forward control, can be obtained:

$$\frac{\ }{\mathbf{U}} = -\mathbf{C}_{av}\mathbf{A}_{av}^{-1}\mathbf{B}_{av} + \mathbf{D}_{av} \tag{19.21}$$

Applying Laplace transforms to (19.19) with zero initial conditions, and using the superposition theorem, the small signal duty-cycle $\tilde{\delta}$ to output $\tilde{\mathbf{y}}$ transfer functions (19.22) can be obtained considering zero line perturbations ($\tilde{u} = 0$).

$$\begin{aligned} \frac{\tilde{\mathbf{y}}(s)}{\tilde{\delta}(s)} = {} & \mathbf{C}_{av}[s\mathbf{I} - \mathbf{A}_{av}]^{-1}[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}] \\ & + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X} + (\mathbf{D}_1 - \mathbf{D}_2)\mathbf{U}] \end{aligned} \tag{19.22}$$

The line to output transfer function (or audio susceptibility transfer function) (19.23) is derived using the same method, considering now zero small signal duty-cycle perturbations ($\tilde{\delta} = 0$).

$$\frac{\tilde{\mathbf{y}}(s)}{\tilde{\mathbf{u}}(s)} = \mathbf{C}_{av}[s\mathbf{I} - \mathbf{A}_{av}]^{-1}\mathbf{B}_{av} + \mathbf{D}_{av} \tag{19.23}$$

EXAMPLE 19.2. BUCK-BOOST DC/DC CONVERTER TRANSFER FUNCTIONS. From (19.11) of Example 19.1 and (19.19), making $\mathbf{X} = [I_L, V_o]^{\mathrm{T}}$, $\ = [V_o, I_L]^{\mathrm{T}}$ and $\mathbf{U} = [V_{DC}]$, the linearized state space model of the buck-boost converter is:

$$\begin{bmatrix} \dot{\tilde{i}}_L \\ \dot{\tilde{v}}_o \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1-\Delta_1}{L_i} \\ \dfrac{1-\Delta_1}{C_o} & \dfrac{-1}{R_o C_o} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_o \end{bmatrix} + \begin{bmatrix} \dfrac{\Delta_1}{L_i} \\ 0 \end{bmatrix} [\tilde{v}_{DC}]$$

$$+ \begin{bmatrix} 0 & \dfrac{\tilde{\delta}}{L_i} \\ -\dfrac{\tilde{\delta}}{C_o} & 0 \end{bmatrix} \begin{bmatrix} I_L \\ v_o \end{bmatrix} + \begin{bmatrix} \dfrac{V_{DC}}{L_i} \\ 0 \end{bmatrix} [\tilde{\delta}]$$

$$\begin{bmatrix} \tilde{v}_0 \\ \tilde{i}_L \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_o \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [\tilde{v}_{DC}] \tag{19.24a}$$

From (19.20) and (19.24) the following matrices are identified:

$$\mathbf{A}_{av} = \begin{bmatrix} 0 & -\dfrac{1-\Delta_1}{L_i} \\ \dfrac{1-\Delta_1}{C_o} & \dfrac{-1}{R_o C_o} \end{bmatrix}; \mathbf{B}_{av} = \begin{bmatrix} \dfrac{\Delta_1}{L_i} \\ 0 \end{bmatrix}; \tag{19.24b}$$

$$\mathbf{C}_{av} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}; \qquad \mathbf{D}_{av} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}.$$

The averaged linear equivalent circuit, resulting from (19.24a) or from the linearization of the averaged equivalent circuit (Fig. 19.2) derived from (19.11), now includes the small signal current source $\tilde{\delta} I_L$ in parallel with the current source $\Delta_1 \tilde{i}_L$, and the small signal voltage source $\tilde{\delta}(V_{DC} + V_o)$ in series with the voltage source $\Delta_1(\tilde{v}_{DC} + \tilde{v}_o)$. The supply voltage source $\bar{V}_{DC}$ is replaced by the voltage source $\tilde{v}_{DC}$.

Using (19.24b) in (19.21), the **input U to output steady-state relations** are:

$$\frac{I_L}{V_{DC}} = \frac{\Delta_1}{R_o(\Delta_1 - 1)^2} \tag{19.25a}$$

$$\frac{V_o}{V_{DC}} = \frac{\Delta_1}{1 - \Delta_1} \tag{19.25b}$$

These relations are the known steady-state transfer relationships of the buck-boost converter [13]. For open-loop control of the V_o output, knowing the nominal value of the power supply V_{DC} and the required V_o, the value of Δ_1 can be off-line calculated from (19.25b) ($\Delta_1 = V_o/(V_o + V_{DC})$). A modulator such as that described in Section 19.2.4, with the modulation signal proportional to Δ_1, would generate the signal $\delta(t)$. Open-loop control for fixed output voltages is possible, if the power supply V_{DC} is almost constant and the converter load does not change significantly. If the V_{DC} value presents disturbances, then feed-forward control can be used, calculating Δ_1 on-line, so that its value will always be in accordance with (19.25b). The correct V_o value will be attained at steady state, despite input voltage variations. However, because of converter parasitic reactances, not modeled here (see Example 19.3), in practice a steady-state error would appear. Moreover, the transient dynamics imposed by the converter would present overshoots, being often not suited for demanding applications.

From (19.23), the **line to output transfer functions** are:

$$\frac{\tilde{i}_L(s)}{\tilde{v}_{DC}(s)} = \frac{\Delta_1(1 + sC_oR_o)}{s^2 L_i C_o R_o + sL_i + R_o(1 - \Delta_1)^2} \tag{19.26a}$$

$$\frac{\tilde{v}_o(s)}{\tilde{v}_{DC}(s)} = \frac{R_o \Delta_1(1 - \Delta_1)}{s^2 L_i C_o R_o + sL_i + R_o(1 - \Delta_1)^2} \tag{19.26b}$$

From (19.22), **the small-signal duty-cycle $\tilde{\delta}$ to output $\tilde{\mathbf{y}}$ transfer functions** are:

$$\frac{\tilde{i}_L(s)}{\tilde{\delta}(s)} = \frac{V_{DC}(1 + \Delta_1 + sC_oR_o)/(1 - \Delta_1)}{s^2 L_i C_o R_o + sL_i + R_o(1 - \Delta_1)^2} \tag{19.27a}$$

$$\frac{\tilde{v}_o(s)}{\tilde{\delta}(s)} = \frac{V_{DC}(R_o - sL_i\Delta_1/(1 - \Delta_1)^2)}{s^2 L_i C_o R_o + SL_i + R_o(1 - \Delta_1)^2} \tag{19.27b}$$

These transfer functions enable the choice and feedback loop design of the compensation network. Note the positive zero in $\tilde{v}_o(s)/\tilde{\delta}(s)$, pointing out a nonminimum-phase system. These equations could also be obtained using the small signal equivalent circuit derived from (19.24), or from the linearized model of the switching cell (Fig. 19.3.b), substituting the current source $\delta_1 \bar{i}_L$ by the current sources $\Delta_1 \tilde{i}_L$ and $\tilde{\delta} I_L$ in parallel, and the voltage source $\delta_1 \bar{v}_s$ by the voltage sources $\Delta_1(\tilde{v}_{DC} + \tilde{v}_o)$ and $\tilde{\delta}(V_{DC} + V_o)$ in series.

EXAMPLE 19.3. TRANSFER FUNCTIONS OF THE FORWARD DC–DC CONVERTER. Consider the forward (buck-derived) converter of Fig. 19.4 switching at $f_s = 100$ kHz ($T = 10$ μs) with $V_{DC} = 300$ V, $n = 30$, $V_o = 5$ V, $L_i = 20$ μH, $r_L = 0.01$ Ω, $C_o = 2200$ μF, $r_C = 0.005$ Ω, $R = 0.1$ Ω.

Assuming $\quad = [i_L, v_C]^{\mathrm{T}}$, $\delta(t) = 1$ when both Q_1, D_1 are on and D_2 is off ($0 \leq t \leq \delta_1 T$), $\delta(t) = 0$ when both Q_1, D_1 are off and D_2 is on ($\delta_1 T \leq t \leq T$), the switched

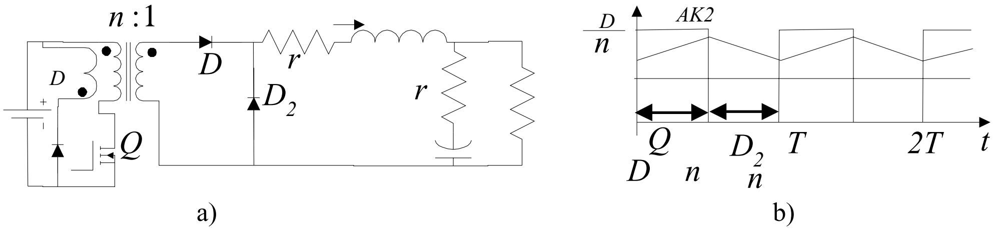


FIGURE 19.4 (a) Basic circuit of the forward dc–dc converter; (b) circuit main waveforms.

state-space model of the forward converter, considering as output vector $\mathbf{y} = [i_L, v_o]^{\mathrm{T}}$, is:

$$\begin{aligned}\frac{\mathrm{d}i_L}{\mathrm{d}t} &= -\frac{(R_o r_C + R_o r_L + r_L r_C)}{L_i(R_o + r_C)} i_L \\ &\quad - \frac{R_o}{L_i(R_o + R_C)} v_C + \frac{\delta(t)}{n} V_{DC} \\ \frac{\mathrm{d}v_C}{\mathrm{d}t} &= \frac{R_o}{(R_o + r_C)C_o} i_L - \frac{1}{(R_o + r_C)C_o} v_C \\ v_o &= \frac{r_C}{1 + r_C/R_o} i_L + \frac{1}{1 + r_C/R_o} v_C\end{aligned} \tag{19.28}$$

Making $r_{cm} = r_C/(1 + r_C/R_o)$, $R_{oc} = R_o + r_C$, $k_{oc} = R_o/R_{oc}$, $r_P = r_L + r_{cm}$ and comparing (19.28) to (19.2), the following matrices can be identified:

$$\mathbf{A}_1 = \mathbf{A}_2 = \begin{bmatrix} -r_P/L_i & -k_{oc}/L_i \\ k_{oc}/C_o & -1/(R_{oc}C_o) \end{bmatrix};$$

$$\mathbf{B}_1 = [1/(nL_i), 0]^{\mathrm{T}}; \mathbf{B}_2 = [0, 0]^{\mathrm{T}}; \mathbf{u} = [V_{DC}]$$

$$\mathbf{C}_1 = \mathbf{C}_2 = \begin{bmatrix} 1 & 0 \\ r_{cm} & k_{oc} \end{bmatrix}; \mathbf{D}_1 = \mathbf{D}_2 = [0, 0]^{\mathrm{T}}$$

Now, applying (19.6), the exact (since $\mathbf{A}_1 = \mathbf{A}_2$) state-space averaged model (19.29) is obtained:

$$\begin{bmatrix} \dot{\bar{i}}_L \\ \dot{\bar{v}}_C \end{bmatrix} = \begin{bmatrix} -r_P/L_i & -k_{oc}/L_i \\ k_{oc}/C_o & -1/(R_{oc}C_o) \end{bmatrix} \begin{bmatrix} \bar{i}_L \\ \bar{v}_C \end{bmatrix} + \begin{bmatrix} \dfrac{\delta_1}{nL_i} \\ 0 \end{bmatrix} [\bar{V}_{DC}] \tag{19.29a}$$

$$\begin{bmatrix} \bar{i}_L \\ \bar{v}_o \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ r_{cm} & k_{oc} \end{bmatrix} \begin{bmatrix} \bar{i}_L \\ \bar{v}_o \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [\bar{V}_{DC}] \tag{19.29b}$$

Since $\mathbf{A}_1 = \mathbf{A}_2$, this model is valid for $\omega_{max} < 2\pi f_s$. The converter eingenvalues $s_{f_{1,2}}$ are:

$$s_{f_{1,2}} = - \frac{L_i + C_o R_{oc} r_P \pm \sqrt{-4R_{oc}L_iC_o(R_{oc}k_{oc}^2 + r_P) + (L_i + C_o R_{oc} r_P)^2}}{2R_{oc}L_iC_o} \tag{19.30}$$

The equivalent circuit arising from (19.29) is represented in Fig. 19.5. It could also be obtained with the concept of the switching cell equivalent circuit (Fig. 19.3 of Example 19.1).

Making $\mathbf{X} = [I_L, V_C]^{\mathrm{T}}$, $= [I_L, V_o]^{\mathrm{T}}$ and $\mathbf{U} = [V_{DC}]$, from (19.19) the small-signal state-space averaged model is:

$$\begin{bmatrix} \dot{\tilde{i}}_L \\ \dot{\tilde{v}}_C \end{bmatrix} = \begin{bmatrix} -r_P/L_i & -k_{oc}/L_i \\ k_{oc}/C_o & -1/(R_{oc}C_o) \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_C \end{bmatrix} + \begin{bmatrix} \dfrac{\Delta_1}{nL_i} \\ 0 \end{bmatrix} [\tilde{v}_{DC}] + \begin{bmatrix} \dfrac{V_{DC}}{nL_i} \\ 0 \end{bmatrix} [\tilde{\delta}] \tag{19.31a}$$

$$\begin{bmatrix} \tilde{i}_L \\ \tilde{v}_o \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ r_{cm} & k_{oc} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [\tilde{v}_{DC}] \tag{19.31b}$$

From (19.21) the input $\mathbf{U}$ to output steady-state relations are:

$$\frac{I_L}{V_{DC}} = \frac{\Delta_1}{n(k_{oc}^2 R_{oc} + r_P)} \tag{19.32a}$$

$$\frac{V_o}{V_{DC}} = \frac{\Delta_1(k_{oc}^2 R_{oc} + r_{cm})}{n(k_{oc}^2 R_{oc} + r_P)} \tag{19.32b}$$

Making $r_C = 0$, $r_L = 0$ and $n = 1$, the former relations give the well-known dc transfer relationships of the buck dc–dc converter. Relations (19.32) allow the open-loop and feed-forward control of the converter, as discussed in Example 19.2, provided that all the modeled parameters are time invariant and accurate enough.

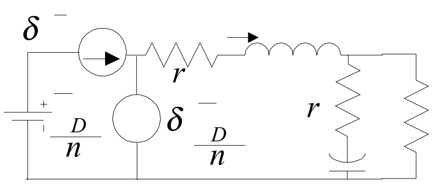


FIGURE 19.5 Equivalent circuit of the averaged state-space model of the forward converter.

From (19.23) the line to output transfer functions are derived:

$$\frac{\tilde{i}_L(s)}{\tilde{v}_{DC}(s)}=\frac{\frac{\Delta_1}{n}(1+sC_oR_{oc})}{s^2L_iC_oR_{oc}+s(L_i+C_oR_{oc}r_P)+k_{oc}^2R_{oc}+r_P} \tag{19.33a}$$

$$\frac{\tilde{v}_o(s)}{\tilde{v}_{DC}(s)}=\frac{\frac{\Delta_1}{n}(k_{oc}^2R_{oc}+r_{cm}+sC_oR_{oc}r_{cm})}{s^2L_iC_oR_{oc}+s(L_i+C_oR_{oc}r_P)+k_{oc}^2R_{oc}+r_P} \tag{19.33b}$$

Using (19.22), the small-signal duty cycle $\tilde{\delta}$ to output $\tilde{\mathbf{y}}$ transfer functions are:

$$\frac{\tilde{i}_L(s)}{\tilde{\delta}(s)}=\frac{\frac{V_{DC}}{n}(1+sC_oR_{oc})}{s^2L_iC_oR_{oc}+s(L_i+C_oR_{oc}r_P)+k_{oc}^2R_{oc}+r_P} \tag{19.34a}$$

$$\frac{\tilde{v}_o(s)}{\tilde{\delta}(s)}=\frac{\frac{V_{DC}}{n}(k_{oc}^2R_{oc}+r_{cm}+sC_oR_{oc}r_{cm})}{s^2L_iC_oR_{oc}+s(L_i+C_oR_{oc}r_P)+k_{oc}^2R_{oc}+r_P} \tag{19.34b}$$

The real zero of (19.34b) is due to r_C, the equivalent series resistance (ESR) of the output capacitor. A similar zero would occur in the buck-boost converter (Example 19.2), if the ESR of the output capacitor was included in the modeling.

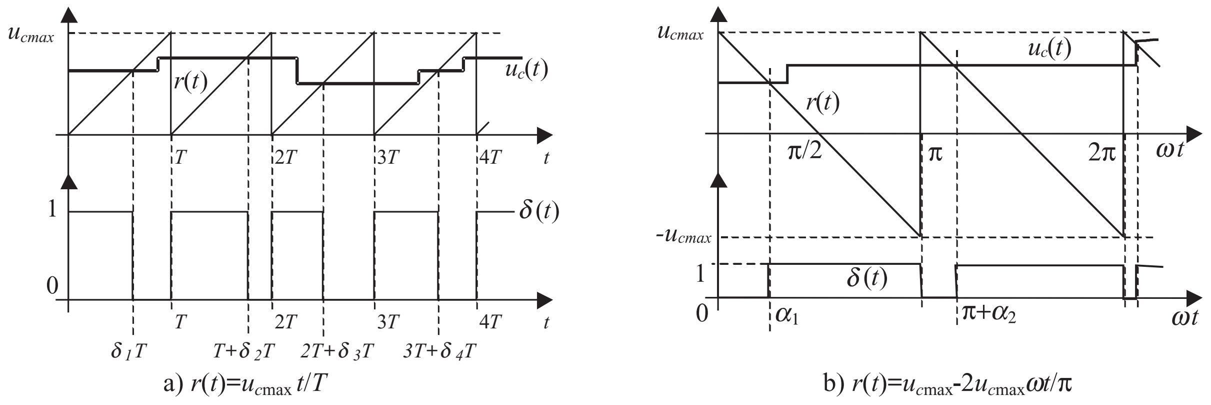
19.2.4 Pulse Width Modulator Transfer Functions

In what is often referred to as pulse width modulation (PWM) voltage mode control, the output voltage $u_c(t)$ of the error (between desired and actual output) amplifier plus regulator, processed if needed, is compared to a repetitive or carrier waveform $r(t)$, to obtain the switching function $\delta(t)$ (Fig. 19.6a). This function controls the power switch, turning it on at the beginning of the period and turning it off when the ramp exceeds the $u_c(t)$ voltage. In Fig. 19.6b the opposite occurs (turn-off at the end of the period, turn-on when the $u_c(t)$ voltage exceeds the ramp).

Considering $r(t)$ as represented in Fig. 19.6a ($r(t)=u_{c\max}t/T$), δ_k is obtained equating $r(t)=u_c$ giving $\delta_k=u_c(t)/u_{c\max}$ or $\delta_k/u_c(t)=G_M$ ($G_M=1/u_{c\max}$). In Fig. 19.6b the switching-on angle α_k is obtained from $r(t)=u_{c\max}-2u_{c\max}\omega t/\pi$, $u_c(t)=u_{c\max}-2u_{c\max}\alpha_k/\pi$, giving $\alpha_k=(\pi/2)\times(1-u_c/u_{c\max})$ and $G_M=\partial\alpha_k/\partial u_c=-\pi/(2u_{c\max})$. Since, after turn-off or turn-on, any control action variation of $u_c(t)$ will only affect the converter duty cycle in the next period, a time delay is introduced in the control loop. For simplicity, with small signal perturbations around the operating point, this delay is assumed almost constant and equal to its mean value ($T/2$). Then, the transfer function of the PWM modulator is:

$$\begin{aligned}\frac{\tilde{\delta}(s)}{\tilde{u}_c(s)}&=G_M\mathrm{e}^{-sT/2}=\frac{G_M}{\mathrm{e}^{sT/2}}\\&=\frac{G_M}{1+s\frac{T}{2}+\frac{s^2}{2!}\left(\frac{T}{2}\right)^2+\cdots+\frac{s^j}{j!}\left(\frac{T}{2}\right)^j+\cdots}\\&\approx\frac{G_M}{1+s\frac{T}{2}}\end{aligned} \tag{19.35}$$

The final approximation of (19.35), valid for $\omega T/2<\sqrt{2}/2$, [2] suggests that the PWM modulator can be considered as an amplifier with gain G_M and a dominant pole. Notice that this pole occurs at a frequency doubling the switching frequency, and most state-space averaged models are valid only for frequencies below one-tenth of the switching frequency. Therefore, in most situations this modulator pole can be neglected, being simply $\delta(s)=G_M\,u_c(s)$, as the dominant



a) $r(t)=u_{c\max}\,t/T$

b) $r(t)=u_{c\max}-2u_{c\max}\omega t/\pi$

FIGURE 19.6 Waveforms of pulse width modulators showing the variable time delays of the modulator response.

pole of (19.35) stays, at least one decade to the left of the dominant poles of the converter.

1 .2.5 Linear Feedback Design Ensuring Stability

In the application of classical linear feedback control to power converters, Bode plots and root-locus are usually suitable methods to assess system performance and stability. General rules for the design of the compensated open-loop transfer function are as follows:

(i) The low-frequency gain should be high enough to minimize output steady-state errors.
(ii) The frequency of 0 dB gain (unity gain), ω_{odB}, should be placed close to the maximum allowed by the modeling approximations ($\lambda_{\max} T \ll 1$). In practice, this frequency should be almost an order of magnitude lower than the switching frequency.
(iii) To ensure stability, the phase margin, defined as the additional phase shift needed to render the system unstable without gain changes (or the difference between the open loop system phase at ω_{0dB} and -180°) must be positive, and in general greater than 30° ($45^\circ-70^\circ$ is desirable). In the root locus, no poles should enter the right half of the complex plane.
(iv) To increase stability, at the frequency where the phase reaches -180°, the gain should be less than -30 dB (gain margin greater than 30 dB).

Transient behavior and stability margins are related: The obtained damping factor is generally 0.01 times the phase margin (in degrees), and overshoot (in percent) is given approximately by 75° minus the phase margin. The product of the rise time (in seconds) and the closed loop bandwidth (in rad/s) is close to 2.8.

To guarantee gain and phase margins the following series compensation transfer functions (usually implemented with operational amplifiers) are often used.

1 .2.5.1 Lag or Lead Compensation

Lag compensation should be used in converters with good stability margin but poor steady state accuracy. If the frequencies $1/T_p$ and $1/T_z$ ((19.36) with $1/T_p < 1/T_z$) are chosen well below the unity gain frequency, lag–lead compensation lowers the loop gain at high frequency but maintains the phase unchanged for $\omega \gg 1/T_z$. Then, the dc gain can be increased to reduce the steady-state error without significantly decreasing the phase margin.

$$C_{LL}(s) = k_{LL}\frac{1+sT_z}{1+sT_p} = k_{LL}\frac{T_z}{T_p}\left(\frac{s+1/T_z}{s+1/T_p}\right) \tag{19.36}$$

Lead compensation can be used in converters with good steady-state accuracy but poor stability margin. If the frequencies $1/T_p$ and $1/T_z$ ((19.36) with $1/T_p > 1/T_z$) are chosen below the unity gain frequency, lead–lag compensation increases the phase margin without significantly affecting the steady-state error. The T_p and T_z values are chosen to increase the phase margin, fastening the transient response and increasing the bandwidth.

1 .2.5.2 Proportional-Integral Compensation

Proportional-integral (PI) compensators (19.37) are used to guarantee null steady-state error with acceptable rise times. PI compensators are a particular case of lag-lead compensators, therefore suitable for converters with good stability margin but poor steady-state accuracy.

$$\begin{aligned} C_{PI}(s) &= \frac{1+sT_z}{sT_p} = \frac{T_z}{T_p} + \frac{1}{sT_p} \\ &= K_p + \frac{K_i}{s} = K_p\left(1+\frac{K_i}{K_p s}\right) \\ &= k_p\left(1+\frac{1}{sT_z}\right) = \frac{1+sT_z}{sT_z/K_p} \end{aligned} \tag{19.37}$$

1 .2.5.3 Proportional-Integral plus High-Frequency Pole Compensation

This integral plus zero-pole compensation (19.38) combines the advantages of a PI with lead or lag compensation. Can be used in converters with good stability margin but poor steady-state accuracy. If the frequencies $1/T_M$ and $1/T_z$ ($1/T_z < 1/T_M$) are carefully chosen, compensation lowers the loop gain at high frequency, while only slightly lowering the phase to achieve the desired phase margin.

$$\begin{aligned} C_{ILD}(s) &= \frac{1+sT_z}{sT_p(1+sT_M)} = \frac{T_z}{T_p T_M}\frac{s+1/T_z}{s(s+1/T_M)} \\ &= W_{cp}\frac{s+\omega_z}{s(s+\omega_M)} \end{aligned} \tag{19.38}$$

1 .2.5.4 Proportional Integral Derivative PID , plus High-Frequency Poles

The PID notch filter type (19.39a) scheme is used in converters with two lightly damped complex poles, to increase the response speed, while ensuring zero steady-state error. In most power converters, the two complex zeros are selected to have a damping factor greater than the converter complex poles, but on oscillating frequency that is slightly smaller. The high-frequency pole is placed to achieve the needed phase margin. The design is correct if the complex pole loci, heading to the

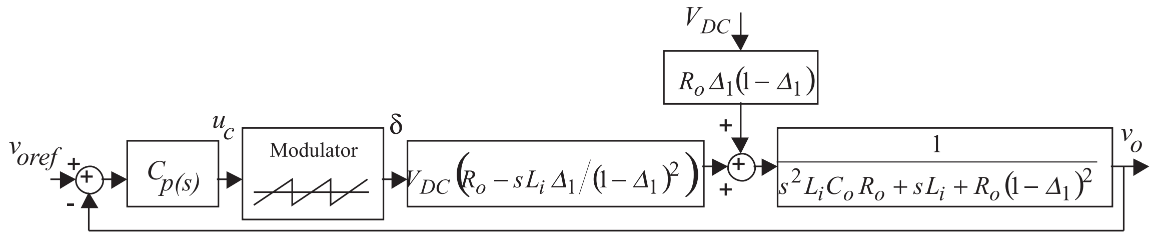

V_{DC}
$R_o \Delta_1 (1-\Delta_1)$
v_{oref}
+
-
u_c
$C_{p(s)}$
Modulator
δ
$V_{DC}\left(R_o - sL_i \Delta_1 / (1-\Delta_1)^2\right)$
+
+
$\frac{1}{s^2 L_i C_o R_o + sL_i + R_o (1-\Delta_1)^2}$
v_o

FIGURE 19.7 Block diagram of the linearized model of the closed loop buck-boost converter.

complex zeros in the system root locus, never enter the right half-plane.

$$
\begin{aligned}
C_{PIDnf}(s) &= T_{cp} \frac{s^2 + 2\xi_{cp}\omega_{0cp}s + \omega_{0cp}^2}{s(1+s/\omega_{p1})} \\
&= \frac{T_{cp}s}{1+s/\omega_{p1}} + \frac{2T_{cp}\xi_{cp}\omega_{0cp}}{1+s/\omega_{p1}} + \frac{T_{cp}\omega_{0cp}^2}{s(1+s/\omega_{p1})} \\
&= \frac{T_{cp}s}{1+s/\omega_{p1}} + \frac{T_{cp}\omega_{0cp}^2(1+2s\xi_{cp}/\omega_{0cp})}{s(1+s/\omega_{p1})} \qquad (19.39\text{a})
\end{aligned}
$$

For systems with a high frequency zero placed at least one decade above the two lightly damped complex poles, the compensator (19.39b), with $\omega_{z1} \approx \omega_{z2} < \omega_p$, can be used. Usually, the two real zeros present frequencies slightly lower than the frequency of the converter complex poles. The two high frequency poles are placed to obtain the desired phase margin [4]. The obtained overall performance will be inferior to that of the PID type notch filter.

$$
C_{PID}(s) = W_{cp} \frac{(1+s/\omega_{z1})(1+s/\omega_{z2})}{s(1+s/\omega_p)^2} \qquad (19.39\text{b})
$$

EXAMPLE 19.4. FEEDBACK DESIGN FOR THE BUCK-BOOST DC–DC CONVERTER. Consider the converter output voltage v_o (Fig. 19.1) to be the controlled output. From Example 19.2 (19.26b) and (19.27b), the block diagram of Fig. 19.7 is obtained. The modulator transfer function is considered a pure gain ($G_M = 0.1$). The magnitude and phase of the open loop transfer function v_o/u_c (Fig. 19.8a) traces 1), shows a resonant peak due to the two lightly damped complex poles and the associated −12 dB/octave roll-off. The right half-plane zero changes the roll-off to −6 dB/octave and adds −90° to the converter phase (nonminimum phase converter).

The procedure to select the compensator and to design its parameters can be outlined as follows:

1. Compensator selection. Since V_{DC} perturbations exist, null steady-state error guarantee is needed. High-frequency poles are usually needed, given the −6 dB/octave final slope of the transfer function. Therefore, two ((19.38) and (19.39a)) compensation schemes with integral action can be tried. Compensator (19.39a) is usually convenient for systems with lightly damped complex poles.

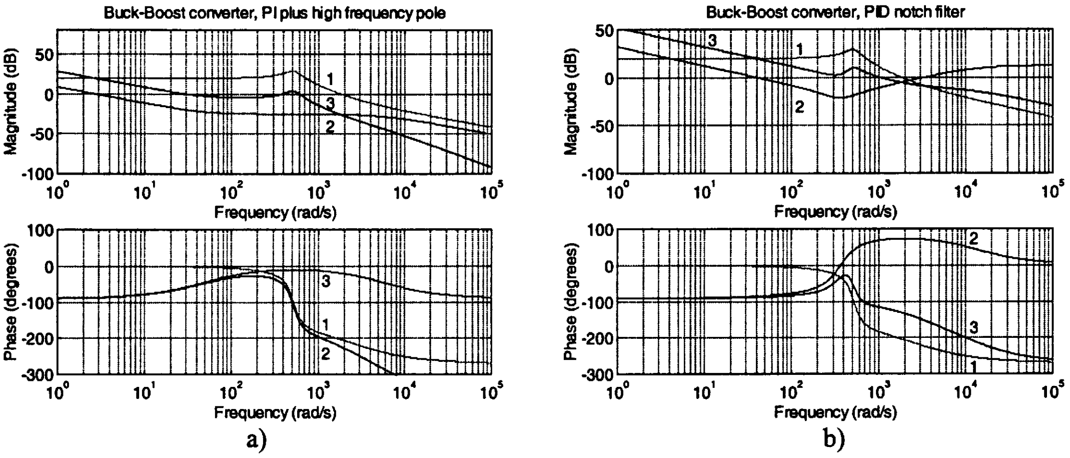


FIGURE 19.8 Bode plots for the buck-boost converter. Trace 1, power converter magnitude and phase; trace 2, compensator magnitude and phase; trace 3, resulting magnitude and phase of the compensated converter. (a) PI plus high-frequency pole compensation with 30° phase margin, $\omega_{0dB} = 50\,\text{rad/s}$, selected $W_{cp} = 300\,\text{rad/s}$, $\omega_z = 45\,\text{rad/s}$, $\omega_M = 45\,\text{rad/s}$; (b) PID notch filter compensation with 64° phase margin, $\omega_{0dB} = 1000\,\text{rad/s}$ and obtained $T_{cp} \approx 0.000305$ s. $2T_{cp}\zeta_{cp}\omega_{0cp} \approx 0.083$ rad, $T_{cp}\omega_{0cp}^2 \approx 40.2\,\text{rad/s}$, $\omega_{p1} \approx 12900\,\text{rad/s}$.

2. Unity gain frequency ω_{0dB} choice:
   - If the selected compensator has no complex zeros, it is better to be conservative choosing ω_{0dB} well below the frequency of the converter lightly damped poles. However, because of the resonant peak of the converter transfer function, the phase margin can be obtained at a frequency near the resonance. If the phase margin is not enough, the compensator gain must be lowered.
   - If the selected compensator has complex zeros, ω_{0dB} can be chosen slightly above the frequency of the lightly damped poles.
3. Desired phase margin (ϕ_M) specification $\phi_M \geq 30°$ (preferably between 45° and 70°).
4. Compensator pole zero placement to achieve the desired phase margin:
   - With the integral plus zero-pole compensation (19.38), the compensator phase ϕ_{cp}, at the maximum frequency of unity gain (often ω_{0dB}), equals the phase margin (ϕ_M) minus 180° and minus the converter phase ϕ_{cv}, ($\phi_{cp} = \phi_M - 180° - \phi_{cv}$). The zero-pole position can be obtained calculating the factor $f_{ct} = \mathrm{tg}(\pi/2 + \phi_{cp}/2)$ being $\omega_z = \omega_{0dB}/f_{ct}$ and $\omega_M = \omega_{0dB} f_{ct}$.
   - In the PID notch filter (19.29a), the two complex zeros are placed to have a damping factor equal to two times the damping of the converter complex poles, and oscillating frequency ω_{0cp} 30 smaller. The high-frequency pole ω_{p1} is placed to achieve the needed phase margin ($\omega_{p1} \approx (\omega_{0cp}\ \omega_{0dB})^{1/2} f_{ct}^2$ with $f_{ct}^2 = \mathrm{tg}(\pi/2 + \phi_{cp}/2)$ and $\phi_{cp} = \phi_M - 180° - \phi_{cv}$) [10].
5. Needed compensator gain calculation (the product of the converter and compensator gains at the ω_{0dB} frequency must be 1).
6. Stability margins verification using Bode plots and root locus.
7. Results evaluation. Restarting the compensator selection and design, if the attained results are not suitable.

The buck-boost converter controlled with integral plus zero-pole compensation presents, in closed loop, two complex poles closer to the imaginary axes than in open-loop. These poles should not dominate the converter dynamics. Instead, the real pole resulting from the open-loop pole placed at the origin should be almost the dominant one, thus slightly lowering the calculated compensator gain. If the ω_{0dB} frequency is chosen too low, the integral plus zero-pole compensation turns into a pure integral compensator ($\omega_z = \omega_M = \omega_{0dB}$). However, the obtained gains are too low, leading to very slow transient responses.

Results showing the transient responses to v_{oref} and V_{DC} step changes, using the selected compensators (Fig. 19.8) are shown (Fig. 19.9). The compensated real converter transient behavior occurs in the buck and in the boost regions. Notice the nonminimum phase behavior of the converter (mainly in Fig. 19.9b), the superior performance of the PID notch filter compensator, and the unacceptable behavior of the PI with high-frequency pole. Care should be taken with load changes, when using this compensator, since instability can easily occur.

The compensator critical values, obtained with root-locus studies, are $W_{cpcrit} = 700$ for the integral plus zero-pole compensator, $T_{cpcrit} = 0.0012$ for the PID notch filter, and $W_{Icprit} = 18$, for the integral compensation derived from the integral plus zero-pole compensator

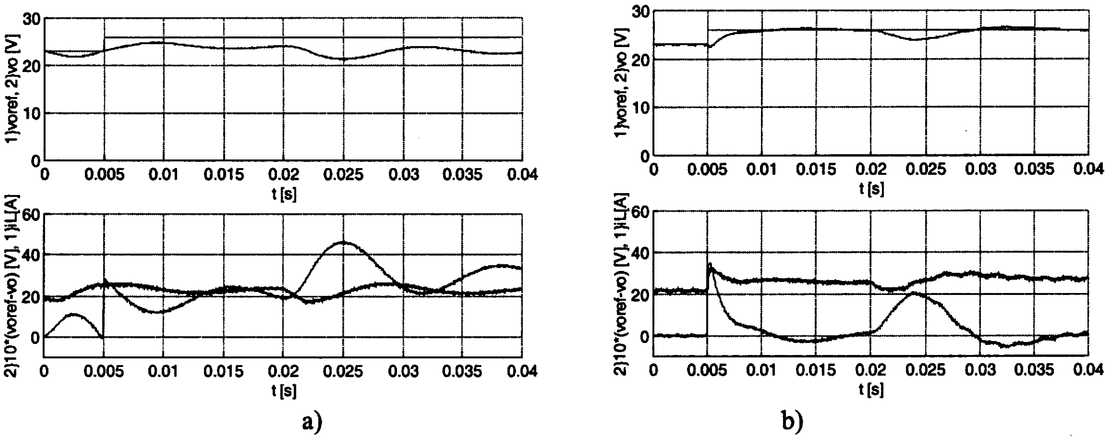


FIGURE 19.9 Transient responses of the compensated buck-boost converter. At $t = 0.005$ s v_{oref} step from 23 V to 26 V. At $t = 0.02$ s V_{DC} step from 26 V to 23 V. Top graphs: square reference v_{oref} and output voltage v_o. Bottom graphs: traces around 20, i_L current; traces starting at zero, $10 \times (v_{oref} - v_o)$. (a) PI plus high-frequency pole compensation with 60° phase margin and $\omega_{0dB} = 500$ rad/s; (b) PID notch filter compensation with 64° phase margin and $\omega_{0dB} = 1000$ rad/s.

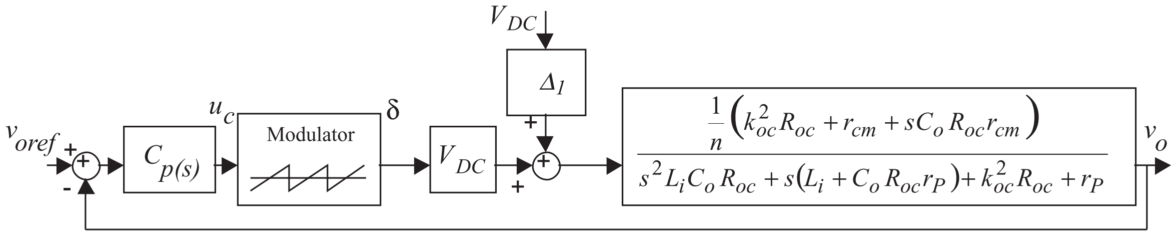

V_{DC}
Δ_I
u_c
δ
v_{oref}
+
-
$C_{p(s)}$
Modulator
V_{DC}
+
+
$\frac{\frac{1}{n}\left(k_{oc}^2 R_{oc} + r_{cm} + sC_o R_{oc} r_{cm}\right)}{s^2 L_i C_o R_{oc} + s\left(L_i + C_o R_{oc} r_P\right) + k_{oc}^2 R_{oc} + r_P}$
v_o

FIGURE 19.10 Block diagram of the linearized model of the closed-loop controlled forward converter.

($\omega_z = \omega_M$). This confirms the Bode plot design and allows stability estimation with changing loads and power supply.

Example 19.5. Feedback Design for the Forward dc/dc Converter. Consider the output voltage v_o of the forward converter (Fig. 19.4a) to be the controlled output. From Example 19.3 (19.33b) and (19.34b), the block diagram of Fig. 19.10 is obtained. As in Example 19.4, the modulator transfer function is considered a pure gain ($G_M = 0.1$). The magnitude and phase of the open-loop transfer function v_o/u_c (Fig. 19.11a, trace 1) shows an open-loop stable system. Since integral action is needed to have some disturbance rejection of the voltage source V_{DC}, the compensation schemes used in Example 19.4, obtained using the same procedure (Fig. 19.11), were also tested.

Results, showing the transient responses to v_{oref} and V_{DC} step changes, are shown (Fig. 19.12). Both compensators ((19.38) and (19.39a)) are easier to design than the ones for the buck-boost converter, and both have acceptable performances. Moreover, the PID notch filter presents a much faster response.

Alternatively, a PID feedback controller such as (19.39b) can be easily hand adjusted, starting with the proportional, integral, and derivative gains all set to zero. In the first step, the proportional gain is increased until the output presents an oscillatory response with nearly 50 overshoot. Next, the derivative gain is slowly increased until the overshoot is eliminated. Lastly, the integral gain is increased to eliminate the steady-state error as quickly as possible.

Example 19.6. Feedback Design for Phase-controlled Rectifiers in the Continuous Mode. Phase controlled, p pulse ($p > 1$), thyristor rectifiers (Fig. 19.13a), operating in the continuous mode, present an output voltage with p identical segments within the mains period T. Given this cyclic waveform, the **A**, **B**, **C**, and **D** matrices for all these p intervals can be written with the same form, in spite of the topological variation. Hence, the state-space averaged model is obtained simply by averaging all the variables within period

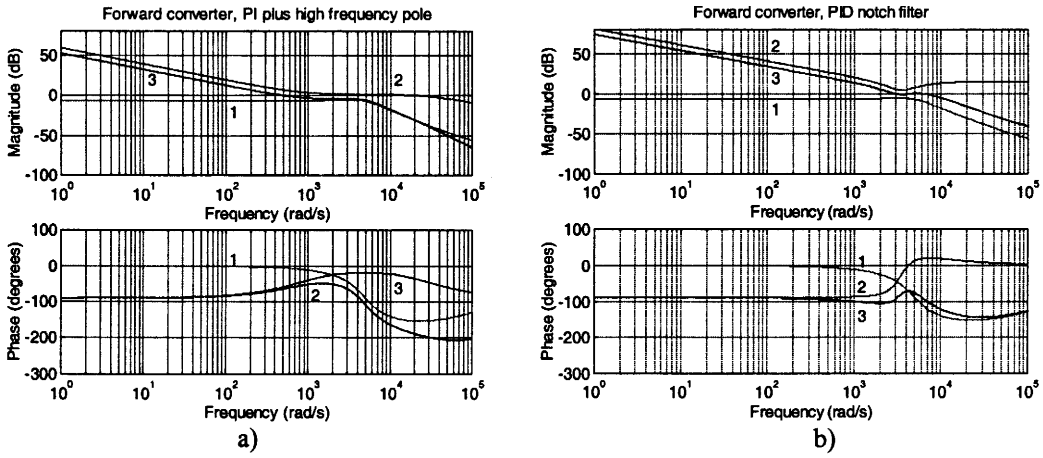


FIGURE 19.11 Bode plots for the forward converter. Trace 1, power converter magnitude and phase; trace 2, compensator magnitude and phase; trace 3, resulting magnitude and phase of the compensated converter. (a) PI plus high-frequency pole compensation with 115° phase margin, $\omega_{0dB} = 500\,\text{rad/s}$ and calculated $W_{cp} = 36{,}000\,\text{rad/s}$, $\omega_z = 770\,\text{rad/s}$, $\omega_M = 30{,}600\,\text{rad/s}$; (b) PID notch filter compensation with 85° phase margin, $\omega_{0dB} = 6000\,\text{rad/s}$ and selected $T_{cp} \approx 0.001$ s, $2T_{cp}\zeta_{cp} \approx 1.9\,\text{rad}$, $T_{cp}\omega_{0cp}^2 \approx 10{,}000\,\text{rad/s}$, $\omega_{p1} \approx 600\,\text{rad/s}$.

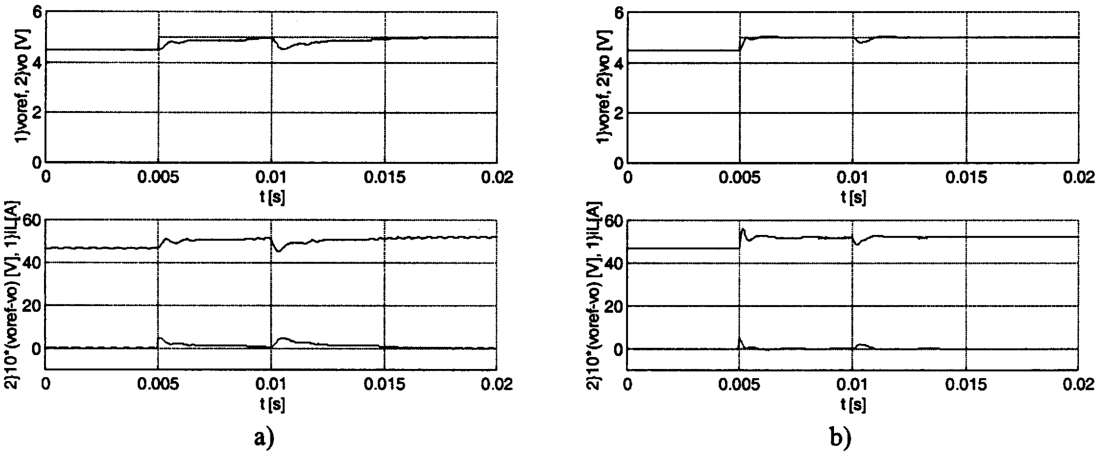


FIGURE 19.12 Transient responses of the compensated forward converter. At $t = 0.005$ s v_{oref} step from 4.5 V to 5 V. At $t = 0.01$ s V_{DC} step from 300 V to 260 V. Top graphs: square reference v_{oref} and output voltage v_o. Bottom graphs: top traces i_L current; bottom traces $10 \times (v_{oref} - v_o)$. (a) PI plus high-frequency pole compensation with 115° phase margin and $\omega_{0dB} = 500$ rad/s; (b) PID notch filter compensation with 85° phase margin and $\omega_{0dB} = 6000$ rad/s.

T/p. Assuming small variations, the mean value of the rectifier output voltage U_{DC} can be written [8]:

$$U_{DC} = U_p \frac{p}{\pi} \sin\left(\frac{\pi}{p}\right) \cos\alpha \qquad (19.40)$$

where α is the triggering angle of the thyristors, and U_p the maximum peak value of the rectifier output voltage, determined by the rectifier topology and the ac supply voltage. The α value can be obtained $(\alpha = (\pi/2) \times (1 - u_c/u_{c\max}))$ using the modulator of Fig. 19.6b, where $\omega = 2\pi/T$ is the mains frequency. From (19.40), the incremental gain K_R of the modulator plus rectifier yields:

$$K_R = \frac{\partial U_{DC}}{\partial u_c} = U_p \frac{p}{2u_{c\max}} \sin\left(\frac{\pi}{p}\right) \cos\left(\frac{\pi u_c}{2u_{c\max}}\right) \qquad (19.41)$$

For a given rectifier, this gain depends on u_c and should be calculated for a certain quiescent point. However, for feedback design purposes, keeping in mind that the rectifier could be required to be stable in all operating points, the maximum value of K_R, denoted K_{RM}, can be used:

$$K_{RM} = U_p \frac{p}{2u_{c\max}} \sin\left(\frac{\pi}{p}\right) \qquad (19.42)$$

The operation of the modulator, coupled to the rectifier thyristors, introduces a time delay, with mean value $T/2p$. Therefore, from (19.35) the modulator–rectifier transfer function $G_R(s)$ is:

$$G_R(s) = \frac{U_{DC}(s)}{u_c(s)} = K_{RM} e^{-s(T/2p)} \approx \frac{K_{RM}}{1 + s\dfrac{T}{2p}} \qquad (19.43)$$

Considering zero U_p perturbations, the rectifier equivalent averaged circuit (Fig. 19.13b) includes the loss-free rectifier output resistance R_i, due to the overlap in the commutation phenomenon caused by the mains inductance [8,14]. Usually, $R_i \approx p\omega l/\pi$ where l is the equiva-

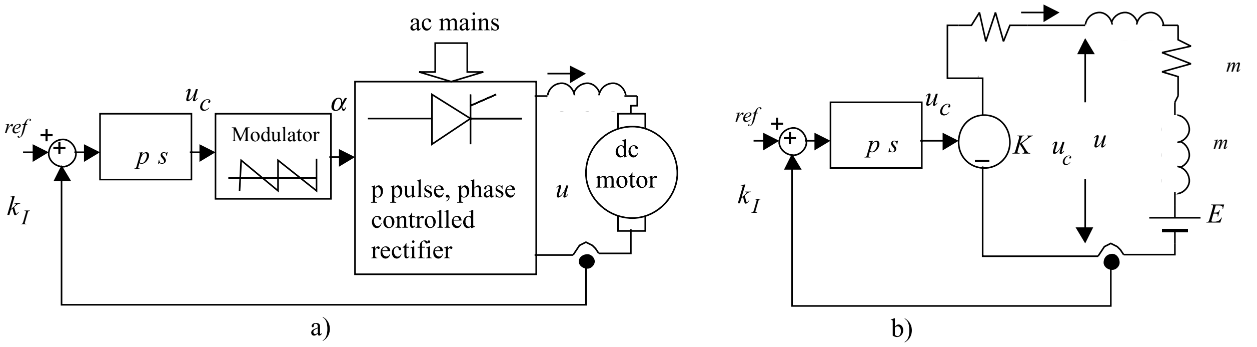


FIGURE 19.13 (a) Block diagram of a p pulse phase controlled rectifier feeding a separately excited dc motor. (b) Equivalent averaged circuit.

lent inductance of the lines paralleled during the overlap, half the equivalent line inductance for most rectifiers, except for single-phase bridge rectifiers where l is the line inductance. L_o is the smoothing reactor and R_m, L_m, and E_o are respectively the armature internal resistance, inductance, and back electromotive force of a separately excited dc motor (typical load). Assuming the mean value of the output current as the controlled output, making $L_t = L_o + L_m$, $R_t = R_i + R_m$, $T_t = L_t/R_t$, and applying Laplace transforms to the differential equation obtained from the circuit of Fig. 19.13b, the output current transfer function is:

$$\frac{i_o(s)}{U_{DC}(s) - E_o(s)} = \frac{1}{R_t(1 + sT_t)} \tag{19.44}$$

The rectifier and load are now represented by a perturbed (E_o) second-order system (Fig. 19.14). To achieve zero steady-state error, which ensures steady state insensitivity to the perturbations, and to obtain closed-loop second-order dynamics, a PI controller (19.37) was selected for $C_p(s)$ (Fig. 19.14). Canceling the load pole ($-1/T_t$) with the PI zero ($-1/T_z$) yields:

$$T_z = L_t/R_t \tag{19.45}$$

The rectifier closed-loop transfer function $i_o(s)/i_{oref}(\mathrm{s})$, with zero E_o perturbations, is:

$$\frac{i_o(s)}{i_{oref}(s)} = \frac{2pK_{RM}k_I(R_tT_pT)}{s^2 + (2p/T)s + 2pK_{RM}k_I/(R_tT_pT)} \tag{19.46}$$

The final value theorem enables the verification of the zero steady-state error. Comparing the denominator of (19.46) to the second-order polynomial $s^2 + 2\zeta\omega_n s + \omega_n^2$ yields:

$$\begin{aligned} \omega_n^2 &= 2pK_{RM}k_I/(R_tT_pT) \\ 4\zeta^2\omega_n^2 &= (2p/T)^2 \end{aligned} \tag{19.47}$$

Since only one degree of freedom is available (T_p), the damping factor ζ is imposed. Usually $\zeta = \sqrt{2}/2$ is selected, since it often gives the best compromise between response speed and overshoot. Therefore, from (19.47), (19.48) arises:

$$T_p = 4\zeta^2K_{RM}k_IT/(2pR_t) = K_{RM}k_IT/(pR_t) \tag{19.48}$$

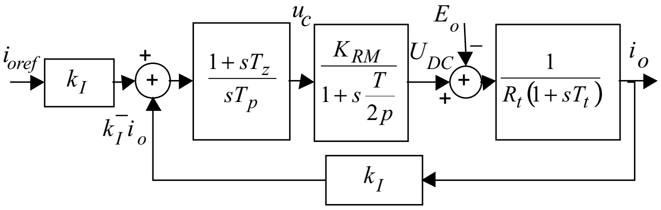


FIGURE 19.14 Block diagram of a PI controlled p pulse rectifier.

Note that both T_z (19.45) and T_p (19.48) are dependent upon circuit parameters. They will have the correct values-only for dc motors with parameters closed to the nominal load value. Using (19.48) in (19.46) yields (19.49), the second-order closed-loop transfer function of the rectifier, showing that, with loads close to the nominal value, the rectifier dynamics depend only on the mean delay time $T/2p$.

$$\frac{i_o(s)}{i_{oref}(s)} = \frac{1}{2(T/2p)^2s^2 + sT/p + 1} \tag{19.49}$$

From (19.49) $\omega_n = \sqrt{2}p/T$ results, which is the maximum frequency allowed by $\omega T/2p < \sqrt{2}/2$, the validity limit of (19.43). This implies that $\zeta \geq \sqrt{2}/2$, which confirms the preceding choice. For $U_p = 310$ V, $p = 6$, $T = 20$ ms, $l = 0.8$ mH, $R_m = 0.5\,\Omega$, $L_t = 50$ mH, $E_o = -150$ V, $u_{c\max} = 10$ V, $k_I = 0.1$, Fig. 19.15a shows the rectifier output voltage $u_{oN}(u_{oN} = u_o/U_p)$ and the step response of the output current i_{oN}, ($i_{oN} = i_o/40$) in accordance with (19.49). Notice that the rectifier is operating in the inverter mode. Figure 19.15b shows the effect, in the i_o current, of a 50 reduction in the E_o value. The output current is initially disturbed but the error vanishes rapidly with time.

This modeling and compensator design are valid for small perturbations. For large perturbations either the rectifier will saturate or the firing angles will originate large current overshoots. For large signals, antiwindup schemes (Fig. 19.16a) or error ramp limiters (or soft starters) and limiters of the PI integral component (Fig. 19.16b) must be used. These solutions will also work with other power converters.

To use this rectifier current controller as the inner control loop of a cascaded controller for the dc motor speed regulation, a useful first-order approximation of (19.49) is $i_o(s)/i_{oref}(s) \approx 1/(sT/p + 1)$.

Although allowing a straightforward compensator selection and precise calculation of its parameters, the rectifier modeling presented here is not suited for stability studies. The rectifier root locus will contain two complex conjugate poles in branches parallel to the imaginary axis. To study the current controller stability, at least the second-order term of (19.43) is needed. Alternative ways include

$$\mathrm{e}^{-sT/2p} \approx (1 - sT/4p)/(1 + sT/4p),$$

the first-order Padé approximation of $\mathrm{e}^{-sT/2p}$ or the second-order approximation,

$$\mathrm{e}^{-sT/2p} \approx (1 - sT/4p + (sT/2p)^2/12)/(1 + sT/4p + (sT/2p)^2/12).$$

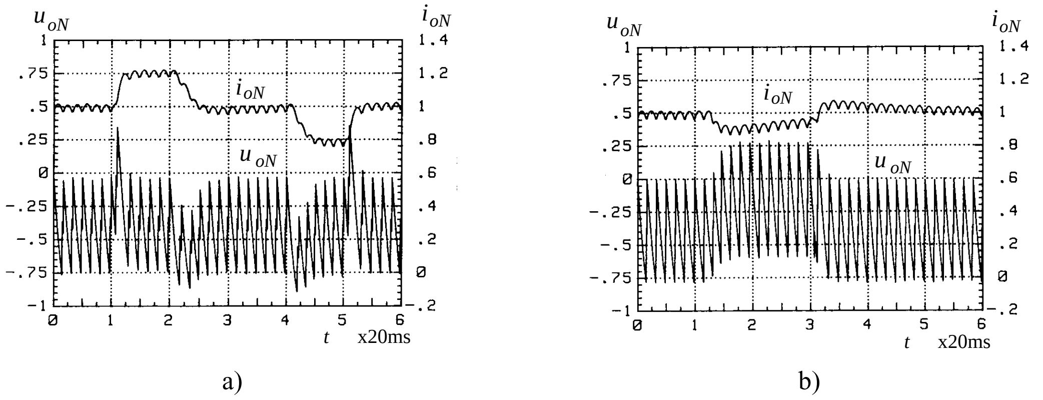


FIGURE 19.15 Transient response of the compensated rectifier. (a) Step response of the controlled current i_o; (b) the current i_o response to a step chance to 50 of the E_o nominal value during 1.5T.

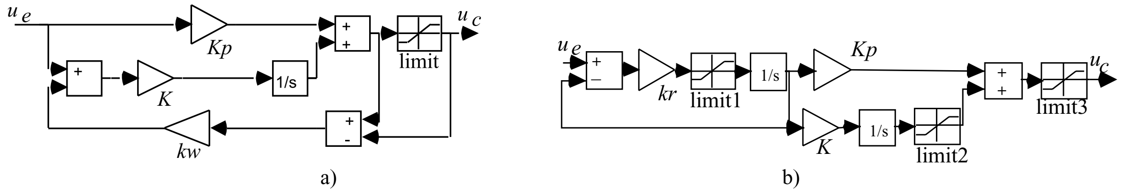


FIGURE 19.16 (a) PI implementation with antiwindup (usually $1/K_p \le k_w \le K_i/K_p$) to deal with rectifier saturation; (b) PI with ramp limiter/soft starter ($k_r \gg K_p$) and integral component limiter to deal with large perturbations.

These approaches introduce zeros in the right half-plane (nonminimum phase systems), and/or extra poles, giving more realistic results. Taking a first-order approximation and root-locus techniques, it is found that the rectifier is stable for $T_p > K_{RM}k_lT/(4pR_t)$ ($\zeta > 0.25$). Another approach uses the conditions of magnitude and angle of the delay function $e^{-sT/2p}$ to obtain the system root locus. Also, the power converter can be considered a sampled data system, at frequency p/T, and Z transform can be used to determine the critical gain and first frequency of instability $p/(2T)$, usually half the switching frequency of the rectifier.

Example 19.7. Buck-Boost dc/dc Converter Feedback Design in the Discontinuous Mode. The methodologies just described do not apply to power converters operating in the discontinuous mode. However, the derived equivalent averaged circuit approach can be used, calculating the mean value of the discontinuous current supplied to the load, to obtain the equivalent circuit. Consider the buck-boost converter of Example 19.1 (Fig. 19.1) with the new values $L_i = 40$ μH, $C_o = 1000$ μF, $r_o = 15$ Ω. The mean value of the current i_{Lo} (Fig. 19.17b), supplied to the output capacitor and resistor of the circuit operating in the discontinuous mode, can be calculated noting that, if the input V_{DC} and output v_o voltages are essentially constant (low ripple), the inductor current rises linearly from zero, peaking at $I_P = (V_{DC}/L_i)\delta_1 T$ (Fig. 19.17a). As the mean value of i_{Lo}, supposed linear, is $I_{Lo} = (I_P\delta_2 T)/2T)$, using the steady state input–output

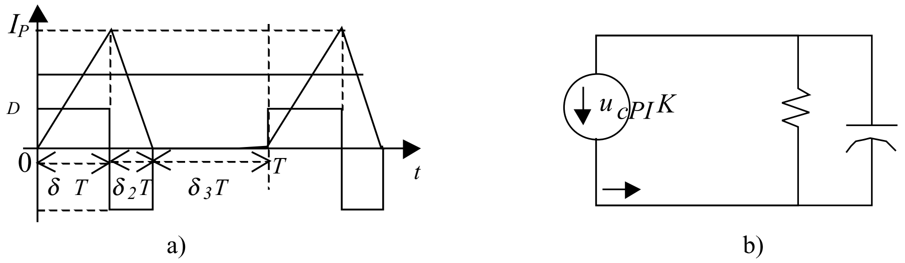


FIGURE 19.17 (a) Waveforms of the buck-boost converter in the discontinuous mode; (b) equivalent averaged circuit.

relation $V_{DC}\delta_1 = V_o\delta_2$ and the above I_P value, I_{Lo} can be written:

$$I_{Lo} = \frac{\delta_1^2 V_{DC}^2 T}{2L_i V_o} \tag{19.50}$$

This is a nonlinear relation that could be linearized around an operating point. However, power converters in the discontinuous mode seldom operate just around an operating point. Therefore, using a quadratic modulator (Fig. 19.18), obtained integrating the ramp $r(t)$ (Fig. 19.6a) and comparing the quadratic curve to the term $u_{cPI}v_o/V_{DC}^2$ (which is easily implemented using the Unitrode UC3854 integrated circuit), the duty cycle δ_1 is $\delta_1 = \sqrt{u_{cPI}V_o/(u_{c\max}V_{DC}^2)}$, and a constant incremental factor K_{CV} can be obtained:

$$K_{CV} = \frac{\partial I_{Lo}}{\partial u_{cPI}} = \frac{T}{2u_{c\max}L_i} \tag{19.51}$$

Considering zero voltage perturbations, the equivalent averaged circuit (Fig. 19.17b) can be used to derive the output voltage to input current transfer function $v_o(s)/i_{Lo}(s) = R_o/(sC_oR_o + 1)$. Using a PI controller (19.37), the closed-loop transfer function is:

$$\frac{v_o(s)}{v_{oref}(s)} = \frac{K_{CV}(1 + sT_z)/C_oT_p}{s^2 + s(T_p + T_zK_{CV}k_vR_o)/C_oR_oT_p + K_{CV}k_v/C_oT_p} \tag{19.52}$$

Since two degrees of freedom exist, the PI constants are derived imposing ζ and ω_n for the second-order denominator of (19.52), usually $\zeta \geq \sqrt{2}/2$ and $\omega_n \leq 2\pi f_s/10$. Therefore:

$$\begin{aligned} T_p &= K_{CV}k_v/(\omega_n^2 C_o) \\ T_z &= T_p(2\zeta\omega_n C_o R_o - 1)/(K_{CV}k_vR_o) \end{aligned} \tag{19.53}$$

The transient behavior of this converter, with $\zeta = 1$ and $\omega_n \approx \pi f_s/10$, is shown in Fig. 19.20a. Compared to Example 19.2, the operation in the discontinuous conduction mode reduces, by one, the order of the state-space averaged model and eliminates the zero in the right half of the complex plane. The inductor current does not behave as a true state variable, since during the interval $\delta_3 T$ this current is zero, and this value is always the i_{Lo} current initial condition. Given the differences between these two examples, care should be taken to avoid the operation in the continuous mode of converters designed and compensated for the discontinuous mode. This can happen during turn-on or step load changes and, if not prevented, the feedback design should guarantee stability in both modes (Example 19.8, Fig. 19.20a).

EXAMPLE 19.8. FEEDBACK DESIGN FOR THE BUCK-BOOST DC/DC CONVERTER OPERATING IN THE DISCONTINUOUS MODE AND USING CURRENT MODE CONTROL. The performances of the buck-boost converter operating in the discontinuous mode can be greatly enhanced if a **current mode control** scheme is used, instead of the voltage mode controller designed in Eample 19.7. Current mode control in power converters is the simplest form of state feedback. Current mode needs the measurement of the current i_L (Fig. 19.1) but greatly simplifies the modulator design (compare Fig. 19.18 to 19.19), since no modulator linearization is used. The measured value, proportional to the current i_L, is compared to the value u_{cPI} given by the output voltage controller (Fig. 19.19). The modulator switches off the power semiconductor when $k_I I_P = u_{cPI}$.

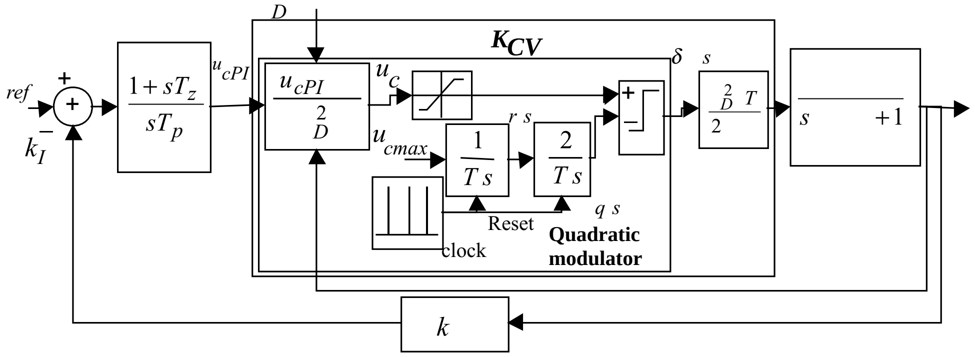


FIGURE 19.18 Block diagram of a PI controlled (feed-forward linearized) buck-boost converter operating in the discontinuous mode.

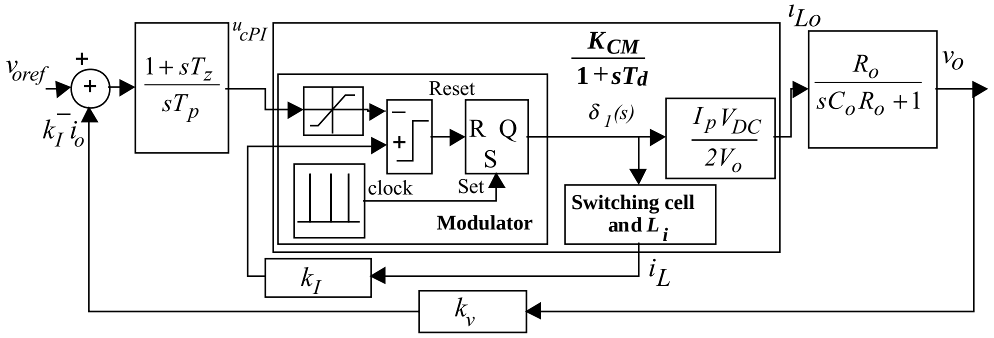


FIGURE 19.19 Block diagram of a current mode controlled buck-boost converter operating in the discontinuous mode.

Expressed as a function of the peak i_L current I_P, I_{Lo} becomes (see the previous example) $I_{Lo} = I_P\delta_1 V_{DC}/(2V_o)$, or considering the modulator task $I_{Lo} = u_{cPI}\delta_1 V_{DC}/(2k_I V_o)$. For small perturbations, the incremental gain is $K_{CM} = \partial I_{Lo}/\partial u_{cPI} = \delta_1 V_{DC}/(2K_I V_o)$. An I_{Lo} current delay $T_d = 1/(2f_s)$, related to the switching frequency f_s can be assumed. The current mode control transfer function $G_{CM}(s)$ is:

$$G_{CM}(s) = \frac{I_{Lo}(s)}{u_{cPI}(s)} \approx \frac{K_{CM}}{1+sT_d} \approx \frac{\delta_1 V_{DC}}{2k_I V_o(1+sT_d)} \tag{19.54}$$

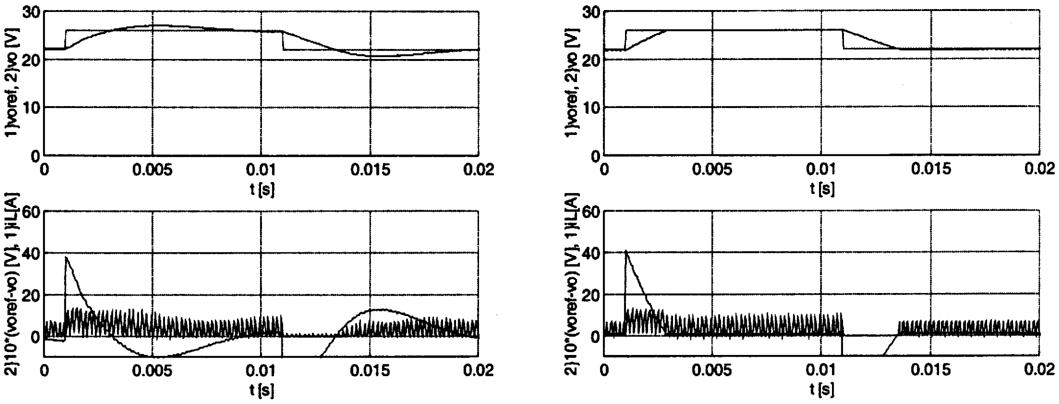
Using the approach of Example 19.6, the values for T_z and T_p are given by (19.55).

$$\begin{aligned} T_z &= R_o C_o \\ T_p &= 4\zeta^2 K_{CM} k_v R_o T_d \end{aligned} \tag{19.55}$$

The transient behavior of this converter, with $\zeta = 1$ and maximum value for I_p, $I_{p\max} = 15\,\text{A}$, is shown in Fig. 19.20b. The output voltage step response presents no overshoot, no steady-state error, and better dynamics, compared to the response (Fig. 19.20a) obtained using the quadratic modulator (Fig. 19.18). Notice that, with current mode control, the converter behaves like a reduced-order system and the right half-plane zero is not present.

The current mode control scheme can be advantageously applied to converters operating in the continuous mode, guarantying short-circuit protection, system order reduction, and better performances. However, for converters operating in the step-up (boost) regime, a stabilizing ramp with negative slope is required, to ensure stability (the stabilizing ramp will transform the signal u_{cPI} in a new signal $u_{cPI} - \text{rem}(k_{sr}t/T)$ where k_{sr} is the needed amplitude for the compensation ramp and the function rem is the remainder of the division of $k_{sr}t$ by T. In the next section, current control of power converters will be detailed.

Closed-loop control of resonant converters can be achieved using the outlined approaches, if the resonant



a) b)

FIGURE 19.20 Transient response of the compensated buck-boost converter in the discontinuous mode. At $t = 0.001$ s v_{oref} step from 23 V to 26 V. At $t = 0.011$ s v_{oref} step from 26 V to 23 V. Top graphs: square reference v_{oref} and output voltage v_o. Bottom graphs: pulses, i_L current; trace peaking at 40, $10 \times (v_{oref} - v_o)$. (a) PI controlled and feed-forward linearized buck-boost converter with $\zeta = 1$ and $\omega_n \approx \pi f_s/10$; (b) current mode controlled buck-boost with $\zeta = 1$ and maximum value $I_{p\max} = 15$ A.

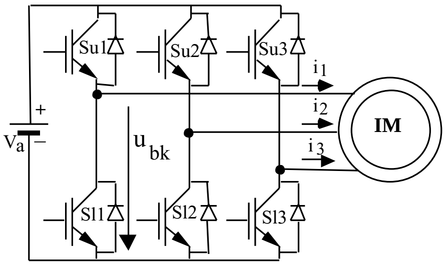


FIGURE 19.21 IGBT based voltage-sourced three-phase inverter with induction motor.

phases of operation last for small intervals compared to the fundamental period. Otherwise, the equivalent averaged circuit concept can often be used and linearized, now considering the resonant converter input–output relations, normally functions of the driving frequency and input or output voltages, to replace the δ_1 variable.

EXAMPLE 19.9. OUTPUT VOLTAGE CONTROL IN THREE-PHASE VOLTAGE-SOURCE INVERTERS USING SINUSOIDAL WAVE PWM (SWPWM) AND SPACE VECTOR MODULATION (SVM)

Sinusoidal Wave PWM

Voltage-source three-phase inverters (Fig. 19.21) are often used to drive squirrel-cage induction motors (IMs) in variable speed applications.

Considering almost ideal power semiconductors, the output voltage u_{bk} ($k \in \{1, 2, 3\}$) dynamics of the inverter is negligible as the output voltage can hardly be considered a state variable in the time scale describing the motor behavior. Therefore, the best-known method to create sinusoidal output voltages uses an open-loop modulator with low-frequency sinusoidal waveforms $\sin(\omega t)$, with amplitude defined by the modulation index m_i ($m_i \in [0, 1]$), modulating high-frequency triangular waveforms $r(t)$ (carriers), Fig. 19.22, a process similar to the described in (19.4).

This sinusoidal wave PWM (SWPWM) modulator generates the variable γ_k, represented in Fig. 19.22 by the rectangular waveform, which describes the inverter k leg state:

$$\gamma_k = \begin{cases} 1 \rightarrow \text{when } m_i \sin(\omega t) > r(t) \\ 0 \rightarrow \text{when } m_i \sin(\omega t) < r(t) \end{cases} \tag{19.56}$$

The turn-on and turn-off signals for the k leg inverter switches are related with the variable γ_k as follows:

$$\gamma_k = \begin{cases} 1 \rightarrow \text{then } \mathrm{Su}_k \text{ is on and } \mathrm{Sl}_k \text{ is off} \\ 0 \rightarrow \text{then } \mathrm{Su}_k \text{ is off and } \mathrm{Sl}_k \text{ is on} \end{cases} \tag{19.57}$$

This applies constant-frequency sinusoidally weighted PWM signals to the gates of each insulated gate bipolar transistor (IGBT). The PWM signals for all the upper IGBTs (Su_k, $k \in \{1, 2, 3\}$) must be 120° out of phase and the PWM signal for the lower IGBT Sl_k must be the complement of the Su_k signal. Since transistor turn-on times are usually shorter than turn-off times, some dead time must be included between the Su_k and Sl_k pulses to prevent internal short circuits.

Sinusoidal PWM can be easily implemented using a microprocessor or two digital counters/timers generating the addresses for two lookup tables (one for the triangular function, another for supplying the per unit basis of the sine, whose frequency can vary). Tables can be stored in read only memories, ROM, or erasable programmable ROM, EPROM. One multiplier for the modulation index (perhaps into the digital-to-analog (D/A) converter for the sine ROM output) and one hysterisis comparator must also be included.

With SWPWM the first harmonic maximum amplitude of the obtained line to line voltage is only about 86 of the inverter dc supply voltage V_a. Since it is expectable that this amplitude should be closer to V_a, different modulating voltages (for example, adding a third-order harmonic with 1/4 of the fundamental sine amplitude) can be used as long as the fundamental harmonic of the line to line voltage is kept sinusoidal. Another way is to leave SWPWM and consider the eight

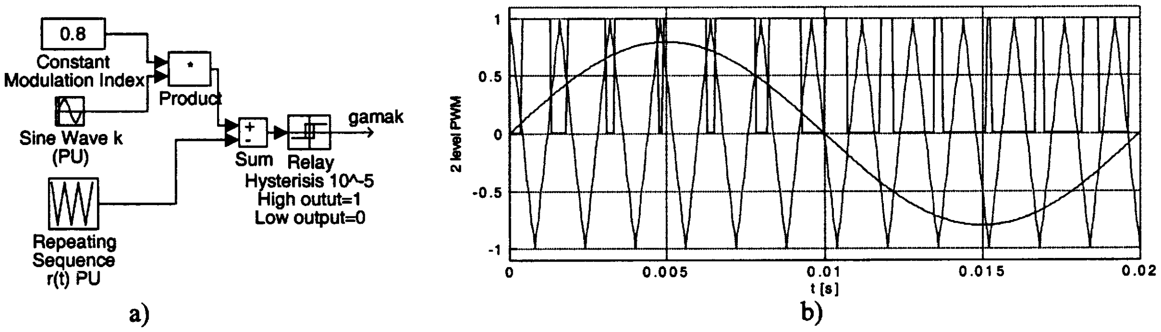


FIGURE 19.22 (a) SWPWM modulator schematic; (b) main SWPWM signals.

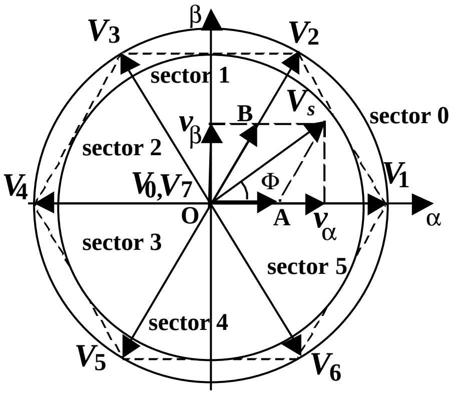


FIGURE 19.23 α–β space vector representation of the three-phase bridge inverter leg base vectors.

possible inverter output voltages trying to directly use then. This will lead to space vector modulation.

Space Vector Modulation

Space vector modulation (SVM) is based on the polar representation (Fig. 19.23) of the eight possible base output voltages of the three-phase inverter (Table 19.1, where v_α, v_β are the vector components of vector $\vec{V}_g$, $g \in \{0, 1, 2, 3, 4, 5, 6, 7\}$, obtained with (19.58)). Therefore, as all the available voltages can be used, SVM does not present the voltage limitation of SWPWM. Furthermore, being a vector technique, SVM fits nicely with vector control methods often used in IM drives.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \gamma_1 \\ \gamma_2 \\ \gamma_3 \end{bmatrix} V_a \tag{19.58}$$

Consider that the vector $\vec{V}_s$ (magnitude V_s, angle Φ) must be applied to the IM. Since there is no such vector available directly, SVM uses an averaging technique to apply the two vectors, $\vec{V}_1$ and $\vec{V}_2$, closest to $\vec{V}_s$. The vector V_1 will be applied during $\delta_A T_s$, while vector $\vec{V}_2$ will last $\delta_B T_s$ (where $1/T_s$ is the inverter switching frequency, δ_A and δ_B are duty cycles, δ_A, δ_B $\in [0, 1]$).

TABLE 19.1 The three-phase inverter 8 possible γ_k combinations, vector numbers, and respective $\alpha\beta$ components

γ_1	γ_2	γ_3	u_{bk}	$u_{bk} - u_{bk+1}$	v_α	v_β	Vector
0	0	0	0	0	0	0	$\vec{V}_0$
1	0	0	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$\sqrt{2/3}V_a$	0	$\vec{V}_1$
1	1	0	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$V_a/\sqrt{6}$	$V_a/\sqrt{2}$	$\vec{V}_2$
0	1	0	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$-V_a/\sqrt{6}$	$V_a/\sqrt{2}$	$\vec{V}_3$
0	1	1	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$-\sqrt{2/3}V_a$	0	$\vec{V}_4$
1	1	1	V_a	0	0	0	$\vec{V}_7$
1	0	1	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$V_a/\sqrt{6}$	$-V_a/\sqrt{2}$	$\vec{V}_6$
0	0	1	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$-V_a/\sqrt{6}$	$-V_a/\sqrt{2}$	$\vec{V}_5$

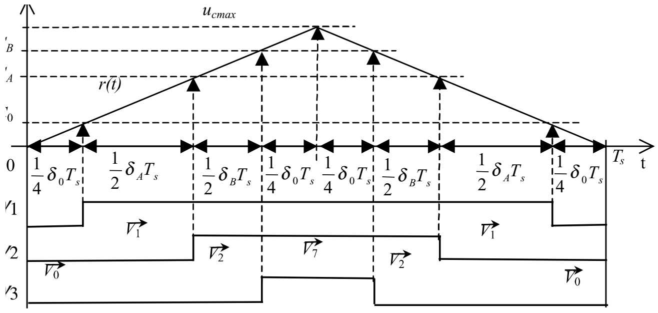

u_{cmax}
B
A
$r(t)$
0
0
$\frac{1}{4}\delta_0 T_s$
$\frac{1}{2}\delta_A T_s$
$\frac{1}{2}\delta_B T_s$
$\frac{1}{4}\delta_0 T_s$
$\frac{1}{4}\delta_0 T_s$
$\frac{1}{2}\delta_B T_s$
$\frac{1}{2}\delta_A T_s$
$\frac{1}{4}\delta_0 T_s$
T_s
t
1
$\vec{V}_1$
$\vec{V}_1$
2
$\vec{V}_2$
$\vec{V}_7$
$\vec{V}_2$
$\vec{V}_0$
$\vec{V}_0$
3

FIGURE 19.24 Symmetrical SVM.

If there is any leftover time in the PWM period T_s, then the zero vector is applied during time $\delta_0 T_s = T_s - \delta_A T_s - \delta_B T_s$. Since there are two zero vectors ($\vec{V}_0$ and $\vec{V}_7$) a symmetric PWM can be devised, which uses both $\vec{V}_0$ and $\vec{V}_7$, as shown in Fig. 19.24. Such a PWM arrangement minimizes the power semiconductor switching frequency and IM torque ripples.

The input to the SVM algorithm is the space vector $\vec{V}_s$, into the sector s_n, with magnitude V_s and angle Φ_s. This vector can be rotated to fit into sector 0 (Fig. 19.23) reducing Φ_s to the first sector, $\Phi = \Phi_s - s_n\,\pi/3$. For any $\vec{V}_s$ that is not exactly along one of the six nonnull inverter base vectors (Fig. 19.23), SVM must generate an approximation by applying the two adjacent vectors during an appropriate amount of time. The algorithm can be devised considering that the projections of $\vec{V}_s$ onto the two closest base vectors are values proportional to δ_A and δ_B duty cycles. Using simple trigonometric relations in sector 0 ($0 < \Phi < \pi/3$) of Fig. 19.23, and considering K_T the proportional ratio, δ_A and δ_B are, respectively, $\delta_A = K_T\overline{\mathrm{OA}}$ and $\delta_B = K_T\overline{\mathrm{OB}}$, yielding:

$$\begin{aligned} \delta_A &= K_T \frac{2V_s}{\sqrt{3}} \sin\left(\frac{\pi}{3} - \Phi\right) \\ \delta_B &= K_T \frac{2V_s}{\sqrt{3}} \sin\Phi \end{aligned} \tag{19.59}$$

The K_T value can be found if we notice that when $\vec{V}_s = \vec{V}_1$, $\delta_A = 1$ and $\delta_B = 0$ (or when $\vec{V}_s = \vec{V}_2$, $\delta_A = 0$ and $\delta_B = 1$). Therefore, since when $\vec{V}_s = \vec{V}_1$, $V_s = \sqrt{v_\alpha^2 + v_\beta^2} = \sqrt{2/3}V_a$. $\Phi = 0$, or when $\vec{V}_s = \vec{V}_2$, $V_s = \sqrt{2/3}V_a$, $\Phi = \pi/3$, the K_T constant is $K_T = \sqrt{3}/(\sqrt{2}V_a)$. Hence:

$$\begin{aligned} \delta_A &= \frac{\sqrt{2}V_s}{V_a} \sin\left(\frac{\pi}{3} - \Phi\right) \\ \delta_B &= \frac{\sqrt{2}V_s}{V_a} \sin\Phi \\ \delta_0 &= 1 - \delta_A - \delta_B \end{aligned} \tag{19.60}$$

The obtained resulting vector $\vec{V}_s$ cannot extend beyond the hexagon of Fig. 19.23. This can be understood if the maximum magnitude V_{sm} of a vector with $\Phi = \pi/6$ is calculated. Since, for $\Phi = \pi/6$, $\delta_A = 1/2$ and $\delta_B = 1/2$ are the maximum duty cycles, from (19.60) $V_{sm} = V_a/\sqrt{2}$ is obtained. This magnitude is lower than that of vector $\vec{V}_1$ since the ratio between these magnitudes is $\sqrt{3}/2$. To generate sinusoidal voltages, the vector $\vec{V}_s$ must be inside the inner circle of Fig. 19.23, so that it can be rotated without crossing the hexagon boundary. Vectors with tips between this circle and the hexagon are reachable, but produce nonsinusoidal line-to-line voltages.

For sector 0 (Fig. 19.23), SVM symmetric PWM switching variables (γ_1, γ_2, γ_3) and intervals (Fig. 19.24) can be obtained by comparing a triangular wave with amplitude $u_{c\max}$ (Fig. 19.24 where $r(t) = 2u_{c\max}t/T_s$, $t \in [0, T_s/2]$) with the following values:

$$
\begin{aligned}
C_0 &= \frac{u_{c\max}}{2}\delta_0 = \frac{u_{c\max}}{2}(1 - \delta_A - \delta_B)\\
C_A &= \frac{u_{c\max}}{2}\left(\frac{\delta_0}{2} + \delta_A\right) = \frac{u_{c\max}}{2}(1 + \delta_A - \delta_B) \qquad (19.61)\\
C_B &= \frac{u_{c\max}}{2}\left(\frac{\delta_0}{2} + \delta_A + \delta_B\right) = \frac{u_{c\max}}{2}(1 + \delta_A + \delta_B)
\end{aligned}
$$

Extension of Eq. (19.61) to all six sectors can be done if the sector number s_n is considered, together with the auxiliary matrix Ξ:

$$
\Xi^{\mathrm{T}} = \begin{bmatrix} -1 & -1 & 1 & 1 & 1 & -1 \\ -1 & 1 & 1 & 1 & -1 & -1 \end{bmatrix} \qquad (19.62)
$$

Generalization of values C_0, C_A, and C_B, denoted C_{0sn}, C_{Asn}, and C_{Bsn}, are written in (19.63), knowing that, for example, $\Xi_{((s_n+4)\bmod 6+1)}$ is the Ξ matrix row with number $1 + (s_n + 4)\bmod 6$.

$$
\begin{aligned}
C_{0sn} &= \frac{u_{c\max}}{2}\left(1 + \Xi_{((s_n)_{\bmod} 6+1)}\begin{bmatrix}\delta_A\\ \delta_B\end{bmatrix}\right)\\
C_{Asn} &= \frac{u_{c\max}}{2}\left(1 + \Xi_{((s_n+4)_{\bmod} 6+1)}\begin{bmatrix}\delta_A\\ \delta_B\end{bmatrix}\right) \qquad (19.63)\\
C_{Bsn} &= \frac{u_{c\max}}{2}\left(1 + \Xi_{((s_n+2)_{\bmod} 6+1)}\begin{bmatrix}\delta_A\\ \delta_B\end{bmatrix}\right)
\end{aligned}
$$

Therefore, γ_1, γ_2, γ_3 are:

$$
\begin{aligned}
\gamma_1 &= \begin{cases} 0 \rightarrow \text{when } r(t) < C_{0sn} \\ 1 \rightarrow \text{when } r(t) > C_{0sn} \end{cases}\\
\gamma_2 &= \begin{cases} 0 \rightarrow \text{when } r(t) < C_{Asn} \\ 1 \rightarrow \text{when } r(t) > C_{Asn} \end{cases} \qquad (19.64)\\
\gamma_3 &= \begin{cases} 0 \rightarrow \text{when } r(t) < C_{Bsn} \\ 1 \rightarrow \text{when } r(t) > C_{Bsn} \end{cases}
\end{aligned}
$$

Supposing that the space vector $\vec{V}_s$ is now specified in the orthogonal coordinates $\alpha\beta\,(v_\alpha,\ \vec{v}_\beta)$, instead of magnitude V_s and angle Φ_s, the duty cycles δ_A, δ_B can be easily calculated knowing that $v_\alpha = V_s \cos\Phi$, $v_\beta = V_s$ sen Φ and using (19.60):

$$
\begin{aligned}
\delta_A &= \frac{\sqrt{2}}{2V_a}(\sqrt{3}v_\alpha - v_\beta)\\
\delta_B &= \frac{\sqrt{2}}{V_a}v_\beta
\end{aligned} \qquad (19.65)
$$

This equation enables the use of (19.63) and (19.64) to obtain SVM in orthogonal co-ordinates.

Using SVM or SWPWM, the closed-loop control of the inverter output currents (induction motor stator currents) can be performed using an approach similar to that outlined in Example 19.6 and decoupling the currents expressed in a *dq* rotating frame.

1 .3 Sliding Mode Control of Power Converters

1 .3.1 Introduction

All the designed controllers for power converters are in fact variable structure controllers, in the sense that the control action changes rapidly from one to another of, usually, two possible δ values, cyclically changing the converter topology. This is accomplished by the modulator (Fig. 19.6), which creates the switching function $\delta(t)$ imposing $\delta(t) = 1$ or $\delta(t) = 0$, to turn on or off the power semiconductors. As a consequence of this discontinuous control action, indispensable for efficiency reasons, state trajectories move back and forth around a certain average surface in the state space, and variables present some ripple. To avoid the effects of this ripple in the modeling and to apply linear control methodologies to time variant systems, average values of state variables and state space averaged models or circuits were presented (Section 19.2). However, a nonlinear approach to the modeling and control problem, taking advantage of the inherent ripple and variable structure behavior of power converters, instead of just trying to live with them, would be desirable, especially if enhanced performances could be attained.

In this approach power converter topologies, as discrete nonlinear time-variant systems, are controlled to switch from one dynamics to another when just needed. If this switching occurs at a very high frequency (theoretically infinite), the state dynamics, described as (19.2) or (19.3), can be enforced to slide along a certain prescribed state space trajectory. The converter is said to be in sliding mode, the allowed deviations from the trajectory (the ripple) imposing the practical switching frequency.

Sliding-mode control of variable structure systems, such as power converters, is particular interesting because of the inherent robustness, capability of system order reduction, and appropriateness to the on–off switching of power semiconductors [15,16]. The control action, being the control equivalent of the management paradigm "just in time" (JIT), provides timely and precise control actions, determined by the control law and the allowed ripple. Therefore, the switching frequency is not constant over all operating regions of the converter.

This section treats the derivation of the control (sliding surface) and switching laws, robustness, stability, constant-frequency operation, and steady-state error elimination necessary for sliding-mode control of power converters, also giving some examples.

1 .3.2 Principles of Sliding-Mode Control

Consider the state-space switched model (19.3) of a power converter subsystem, and input–output linearization or another technique, to obtain, from state-space equations, one equation (19.66), for each controllable subsystem output $\mathbf{y} = \ $. In the controllability canonical form [11] (also known as input–output decoupled or companion form), (19.66) is:

$$\frac{\mathrm{d}}{\mathrm{d}t}[x_h,\ldots,x_{j-1},x_j]^{\mathrm{T}} = [x_{h+1},\ldots,x_j,-f_h(\ )-p_h(t)+b_h(\ )u_h(t)]^{\mathrm{T}} \qquad (19.66)$$

where $\ = [x_h,\ldots,x_{j-1},x_j]^{\mathrm{T}}$ is the subsystem state vector, $f_h(\ )$ and $b_h(\ )$ are functions of , $p_h(t)$ represents the external disturbances, and $u_h(t)$ is the control input. In this special form of state-space modeling, the state variables are chosen so that the x_{i+1} variable ($i \in \{h,\ldots,j-1\}$) is the time derivative of x_i, that is $\ = [x_h,\dot{x}_h,\ddot{x}_h,\ldots,\overset{m}{x}_h]^{\mathrm{T}}$, where $m = j - h$ [9].

1 .3.2.1 Control law Sliding Surface

The required closed-loop dynamics for the subsystem output vector $\mathbf{y} = \ $ can be chosen to verify (19.67) with selected k_i values. This is a model reference adaptive control approach to impose a state trajectory that advantageously reduces the system order $j - h + 1$.

$$\frac{\mathrm{d}x_j}{\mathrm{d}t} = -\sum_{i=h}^{j-1}\frac{k_i}{k_j}x_{i+1} \qquad (19.67)$$

Effectively, in a single-input/single-output (SISO) subsystem the order is reduced by one unity, applying the restriction (19.67). In a multiple-input/multiple-output (MIMO) system, in which v independent restrictions could be imposed (usually with v degrees of freedom), the order could often be reduced in v units. Indeed, from (19.67), the dynamics of the jth term of   is linearly dependent from the $j - h$ first terms:

$$\frac{\mathrm{d}x_j}{\mathrm{d}t} = -\sum_{i=h}^{j-1}\frac{k_i}{k_j}x_{i+1} = -\sum_{i=h}^{j-1}\frac{k_i}{k_j}\frac{\mathrm{d}x_i}{\mathrm{d}t} \qquad (19.68)$$

The controllability canonical model allows the direct calculation of the needed control input to achieve the desired dynamics (19.67). In fact, as the control action should enforce the state vector , to follow the reference vector $_r = [x_{h_r},\dot{x}_{h_r},\ddot{x}_{h_r},\ldots,\overset{m}{x}_{h_r}]^{\mathrm{T}}$, the tracking error vector will be $\mathbf{e} = [x_{h_r}-x_h,\ldots,x_{j-1_r}-x_{j-1},\ x_{j_r}-x_j]^{\mathrm{T}}$ or $\mathbf{e} = [e_{x_h},\ldots,e_{xj-1},e_{xj}]^{\mathrm{T}}$. Thus, if we equate the subexpressions for $\mathrm{d}x_j/\mathrm{d}t$ of (19.66) and (19.67), the necessary control input $u_h(t)$ is:

$$u_h(t) = \frac{p_h(t)+f_h(\ )+\dfrac{\mathrm{d}x_j}{\mathrm{d}t}}{b_h(\ )} = \frac{p_h(t)+f_h(\ )-\sum\limits_{i=h}^{j-1}\dfrac{k_i}{k_j}x_{i+1_r}+\sum\limits_{i=h}^{j-1}\dfrac{k_i}{k_j}e_{x_{i+1}}}{b_h(\ )} \qquad (19.69)$$

This expression is the required closed-loop control law, but unfortunately it depends on system parameters and external perturbations and is difficult to compute. Moreover, for some output requirements, Eq. (19.69) would give extremely high values for the control input $u_h(t)$, which would be impractical or almost impossible.

In most power converters $u_h(t)$ is discontinuous. Yet, if we assume one or more discontinuity borders dividing the state space into subspaces, the existence and uniqueness of the solution is guaranteed out of the discontinuity borders, since in each subspace the input is continuous. The discontinuity borders are subspace switching hypersurfaces, whose order is the space order minus one, along which the subsystem state slides, since its intersections of the auxiliary equations defining the discontinuity surfaces can give the needed control input.

Within the sliding-mode control (SMC) theory, assuming a certain dynamic error tending to zero, one auxiliary equation (sliding surface) and the equivalent control input $u_h(t)$ can be obtained, integrating both sides of (19.68) with null initial conditions:

$$k_jx_j + \sum_{i=h}^{j-1}k_ix_i = \sum_{i=h}^{j}k_ix_i = 0 \qquad (19.70)$$

This equation represents the discontinuity surface (hyperplane) and just defines the necessary sliding surface $S(x_i, t)$ to obtain the prescribed dynamics of (19.67):

$$S(x_i, t) = \sum_{i=h}^{j}k_ix_i = 0 \qquad (19.71)$$

In fact, by taking the first time derivative of $S(x_i, t)$, $\dot{S}(x_i, t) = 0$, solving it for $\mathrm{d}x_j/\mathrm{d}t$, and substituting the result in (19.69), the dynamics specified by (19.67) is obtained. This means that the control problem is reduced to a first-order problem, since it is only necessary to calculate the time derivative of (19.71) to obtain the dynamics (19.67) and the needed control input $u_h(t)$.

$$B_I(s)_m = (s+\omega_o)^m = \begin{cases} m=0 \Rightarrow B_I(s) = 1 \\ m=1 \Rightarrow B_I(s) = s+\omega_o \\ m=2 \Rightarrow B_I(s) = s^2+2\omega_o s+\omega_o^2 \\ m=3 \Rightarrow B_I(s) - s^3+3\omega_o s^2+3\omega_o^2 s+\omega_o^3 \\ m=4 \Rightarrow B_I(s) = s^4+4\omega_o s^3+6\omega_o^2+4\omega_o^2 s^2+4\omega_o^3 s+\omega_o^4 \\ \qquad \qquad \qquad \ldots \end{cases} \tag{19.72a}$$

$$I_{TAE}(s)_m = \begin{cases} m=0 \Rightarrow I_{TAE}(s) = 1 \\ m=1 \Rightarrow I_{TAE}(s) = s+\omega_o \\ m=2 \Rightarrow I_{TAE}(s) = s^2+1.4\omega_o s+\omega_o^2 \\ m=3 \Rightarrow I_{TAE}(s) = s^3+1.75\omega_o s^2+2.15\omega_o^2 s+\omega_o^3 \\ m=4 \Rightarrow I_{TAE}(s) = s^4+2.1\omega_o s^3+3.4\omega_o^2 s^2+2.7\omega_o^3 s+\omega_o^4 \\ \ldots \end{cases} \tag{19.72b}$$

$$B_E(s)_m = \begin{cases} m=0 \Rightarrow B_E(s) = 1 \\ m=1 \Rightarrow B_E(s) = st_r+1 \\ m=2 \Rightarrow B_E(s) = \dfrac{(st_r)^2+3st_r+3}{3} \\ m=3 \Rightarrow B_E(s) = \dfrac{((st_r)^2+3.678st_r+6.459)(st_r+2.322)}{15} \\ \qquad \qquad \qquad = \dfrac{(st_r)^3+6(st_r)^2+15st_r+15}{15} \\ m=4 \Rightarrow B_E(s) = \\ \quad \dfrac{(st_r)^4+10(st_r)^3+45(st_r)^2+105(st_r)+105}{105} \end{cases} \tag{19.72c}$$

The sliding surface (19.71), as the dynamics of the converter subsystem, must be a Routh–Hurwitz polynomial and verify the sliding manifold invariance conditions, $S(x_i, t) = 0$ and $\dot{S}(x_i, t) = 0$. Consequently, the closed-loop controlled system behaves as a stable system of order $j - h$, whose dynamics is imposed by the coefficients k_i, which can be chosen by pole placement of the poles of the order $m = j - h$ polynomial. Alternatively, certain kinds of polynomials can be advantageously used (19.77): Butterworth, Bessel, Chebyshev, elliptic (or Cauer), binomial, and minimum integral of time absolute error product (ITAE). Most useful are Bessel polynomials $B_E(s)$, which minimize the system response time t_r, providing no overshoot, the polynomials $I_{TAE}(s)$ that minimize the ITAE criterion for a system with desired natural oscillating frequency ω_o, and binomial polynomials $B_I(s)$. For $m > 1$, ITAE polynomials give faster responses than binomial polynomials.

These polynomials can be the reference model for this model reference adaptive control method.

1 .3.2.2 Closed-Loop Control Input Output Decoupled orm

For closed-loop control applications, instead of the state variables x_i, it is worthy to consider, as new state variables, the errors e_{x_i}, components of the error vector $\mathbf{e} = [e_{x_h}, \dot{e}_{x_h}, \ddot{e}_{x_h}, \ldots, \overset{m}{e}_{x_h}]^{\mathrm{T}}$ of the state-space variables x_i, relative to a given reference x_{i_r} (19.74). The new controllability canonical model of the system is:

$$\frac{\mathrm{d}}{\mathrm{d}t}[e_{x_h}, \ldots, e_{x_{j-1}}, e_{x_j}]^{\mathrm{T}} = [e_{x_{h+1}}, \ldots, e_{x_j}, -f_e(\mathbf{e}) + p_e(t) - b_e(\mathbf{e})u_h(t)]^{\mathrm{T}} \tag{19.73}$$

where $f_e(\mathbf{e})$, $p_e(t)$, and $b_e(\mathbf{e})$ are functions of the error vector $\mathbf{e}$.

As the transformation of variables

$$e_{x_i} = x_{i_r} - x_i \qquad \text{with } i = h, \ldots, j \tag{19.74}$$

is linear, the Routh–Hurwitz polynomial for the new sliding surface $S(e_{x_i}, t)$ is

$$S(e_{x_i}, t) = \sum_{i=h}^{j} k_i e_{x_i} = 0 \tag{19.75}$$

Since $e_{x_{i+1}}(s) = s e_{x_i}(s)$, this **control law**, that from (19.72) can be written $S(\mathbf{e}, s) = e_{x_i}(s+\omega_o)^m$, does not depend on circuit parameters, disturbances or operating conditions, but only on the imposed k_i parameters and on the state variable errors e_{x_i}, which can usually be measured or estimated. The control law (19.75) enables the desired dynamics of the output variable(s), if the semiconductor switching strategy is designed to guarantee the system stability. In practice, the finite switching frequency of the semiconductors will impose a certain dynamic error ε tending to zero. The control law (19.75) is the required controller for the closed loop SISO subsystem with output $\mathbf{y}$.

1 .3.2.3 Stability

. . . . Existence Condition

The existence of the operation in sliding mode implies $S(e_{x_i}, t) = 0$. Also, to stay in this regime, the control system should guarantee $\dot{S}(e_{x_i}, t) = 0$. Therefore, the semiconductor switching law must ensure the stability condition for the system in sliding mode, written as

$$S(e_{x_i}, t)\dot{S}(e_{x_i}, t) < 0 \tag{19.76}$$

The fulfillment of this inequality ensures the convergence of the system state trajectories to the sliding surface $S(e_{x_i}, t) = 0$, since

- If $S(e_{x_i}, t) > 0$ and $\dot{S}(e_{x_i}, t) < 0$, then $S(e_{x_i}, t)$ will decrease to zero
- If $S(e_{x_i}, t) < 0$ and $\dot{S}(e_{x_i}, t) > 0$, then $S(e_{x_i}, t)$ will increase toward zero

Hence, if (19.76) is verified, then $S(e_{x_i}, t)$ will converge to zero. The condition (19.76) is the manifold $S(e_{x_i}, t)$ invariance condition, or the sliding mode existence condition.

Given the state-space model (19.73), the function of the error vector $\mathbf{e}$, and, from $\dot{S}(e_{x_i}, t) = 0$, the equivalent average control input $U_{eq}(t)$ that must be applied to the system in order that the system state slides along the surface (19.75), is given by[5]

$$U_{eq}(t) = \frac{k_h \dfrac{\mathrm{d}e_{x_h}}{\mathrm{d}t} + k_{h+1}\dfrac{\mathrm{d}e_{x_{h+1}}}{\mathrm{d}t} + \cdots + k_{j-1}\dfrac{\mathrm{d}e_{x_{j-1}}}{\mathrm{d}t} + k_j(-f_e(\mathbf{e}) + p_e(t))}{k_j b_e(\mathbf{e})} \tag{19.77}$$

This control input $U_{eq}(t)$ ensures converter subsystem operation in the sliding mode.

. . . . Reaching Condition

The fulfillment of $S(e_{x_i}, t)\dot{S}(e_{x_i}, t) < 0$, as $S(e_{x_i}, t)\dot{S}(e_{x_i}, t) = (1/2)\dot{S}^2(e_{x_i}, t)$ implies that the distance between the system state and the sliding surface will tend to zero, since $S^2(e_{x_i}, t)$ can be considered a measure for this distance. This means that the system will reach sliding mode. Additionally, from (19.73) it can be written

$$\frac{\mathrm{d}e_{x_j}}{\mathrm{d}t} = -f_e(\mathbf{e}) + p_e(t) - b_e(\mathbf{e})u_h(t) \tag{19.78}$$

From (19.75), Eq. (19.79) is obtained.

$$\begin{aligned} S(e_{x_i}, t) &= \sum_{i=h}^{j} k_i e_{x_i} \\ &= k_h e_{x_h} + k_{h+1}\frac{\mathrm{d}e_{x_h}}{\mathrm{d}t} + k_{h+2}\frac{\mathrm{d}^2 e_{x_h}}{\mathrm{d}t^2} + \cdots + k_j \frac{\mathrm{d}^m e_{x_h}}{\mathrm{d}t^m} \end{aligned} \tag{19.79}$$

If $S(e_{x_i}, t) > 0$, from the Routh–Hurwitz property of (19.75), then $e_{x_j} > 0$. In this case, to reach $S(e_{x_i}, t) = 0$ it is necessary to impose $-b_e(\mathbf{e})u_h(t) = -U$ in (19.78), with U chosen to guarantee $\mathrm{d}e_{x_j}\mathrm{d}t < 0$. After a certain time, e_{x_j} will be $e_{x_j} = \mathrm{d}^m e_{x_h}/\mathrm{d}t^m < 0$, implying along with (19.79) that $\dot{S}(e_{x_i}, t) < 0$, thus verifying (19.76). Therefore, every term of $S(e_{x_i}, t)$ will be negative, which implies, after a certain time, an error $e_{x_h} < 0$ and $S(e_{x_i}, t) < 0$. Hence, the system will reach sliding mode, staying there if $U = U_{eq}(t)$. This same reasoning can be made for $S(e_{x_i}, t) < 0$, it now being necessary to impose $-b_e(\mathbf{e})u_h(t) = +U$, with U high enough to guarantee $\mathrm{d}e_{x_j}/\mathrm{d}t > 0$.

To ensure that the system always reaches sliding-mode operation, it is necessary to calculate the maximum value of $U_{eq}(t)$, U_{eqmax}, and also impose the reaching condition:

$$U > U_{eqmax} \tag{19.80}$$

This means that the power supply voltage values U should be chosen high enough to additionally account for the maximum effects of the perturbations. With step inputs, even with $U > U_{eqmax}$, the converter usually loses sliding mode, but it will reach it again, even if the U_{eqmax} is calculated considering only the maximum steady-state values for the perturbations.

1 .3.2.4 Switching Law

From the foregoing considerations, supposing a system with two possible structures, the semiconductor switching strategy must ensure $S(e_{x_i}, t)\dot{S}(e_{x_i}, t) < 0$. Therefore, if $S(e_{x_i}, t) > 0$, then $\dot{S}\,(e_{x_i}, t) < 0$, which implies, as seen, $-b_e(\mathbf{e})u_h(t) = -U$ (the sign of $b_e(\mathbf{e})$ must be known). Also, if $S(e_{x_i}, t) < 0$, then $\dot{S}(e_{x_i}, t) > 0$, which implies $-b_e(\mathbf{e})u_h(t) = +U$. This imposes the switching between two structures at infinite frequency. Since power semiconductors can switch only at finite frequency, in practice, a small enough error for $S(e_{x_i}, t)$ must be allowed $(-\varepsilon < S(e_{x_i}, t) < +\varepsilon)$. Hence, the switching law between the two possible system structures must be

$$u_h(t) = \begin{cases} U/b_e(\mathbf{e}) \text{ for } S(e_{x_i}, t) > +\varepsilon \\ -U/b_e(\mathbf{e}) \text{ for } S(e_{x_i}, t) < -\varepsilon \end{cases} \tag{19.81}$$

The condition (19.81) determines the control input to be applied and therefore represents the semiconductor switching strategy or switching function. This law determines a two-level pulse width modulator with "just in time" switching (variable frequency).

1 .3.2.5 Robustness

The dynamics of a system with closed-loop control using the control law (19.75) and the switching law (19.81), does not depend on the system operating point, load, circuit parameters, power supply, or bounded disturbances, as long as the control input $u_h(t)$ is large enough to maintain the converter subsystem in sliding mode. Therefore, it is said that the power converter dynamics, operating in sliding mode, is robust against changing operating conditions, variations of circuit parameters, and external disturbances. The desired dynamics for the output variable(s) is determined only by the k_i coefficients of the control law (19.75), as long as the switching law (19.81) maintains the converter in sliding mode.

1 .3.3 Constant-Frequency Operation

Prefixed switching frequency can be achieved, even with sliding-mode controllers, at the cost of losing the JIT action. As the sliding-mode controller changes the control input when needed, and not at a certain prefixed rhythm, applications needing constant switching frequency (such as thyristor rectifiers or resonant converters) must compare $S(e_{x_i}, t)$ (hysteresis width 2ι much narrower than 2ε) with auxiliary triangular waveforms (Fig. 19.25a), auxiliary sawtooth functions (Fig. 19.25c), three-level clocks (Fig. 19.25d), or phase-locked loop control of the comparator hysterisis variable width 2ε. However, as illustrated in Fig. 19.25b, steady-state errors do appear. Often, they should be eliminated as described in the next section.

1 .3.4 Steady-state Error Elimination in Converters with Continuous Control Inputs

In the ideal sliding mode, state trajectories are directed toward the sliding surface (19.75) and move exactly along the discontinuity surface, switching between the possible system structures, at infinite frequency. Practical sliding modes cannot switch at infinite frequency, and therefore exhibit phase plane trajectory oscillations inside a hysterisis band of width 2ε, centered in the discontinuity surface.

The switching law (19.75) permits no steady-state errors as long as $S(e_{x_i}, t)$ tends to zero, which implies no restrictions on the commutation frequency. Control circuits operated at constant frequency, or needed continuous inputs, or particular limitations of the power semiconductors, such as minimum on or off times, can originate $S(e_{x_i}, t) = \varepsilon_1 \neq 0$. The steady-state error (e_{x_h}) of the x_h variable, $x_{h_r} - x_h = \varepsilon_1/k_h$, can be eliminated, increasing the system order by 1. The new state space controllability canonical form, considering the error e_{x_i}, between the variables and their references, as the state vector, is

$$\frac{\mathrm{d}}{\mathrm{d}t}\left[\int e_{x_h}\mathrm{d}t, e_{x_h}, \dots, e_{x_{j-1}}, e_{x_j}\right]^{\mathrm{T}} = [e_{x_h}, e_{x_{h+1}}, \dots, e_{x_j} - f_e(\mathbf{e}) - p_e(t) - b_e(\mathbf{e})u_h(t)]^{\mathrm{T}} \qquad (19.82)$$

The new sliding surface $S(e_{x_i}, t)$, written from (19.75) considering the new system (19.82), is

$$S(e_{x_i}, t) = k_0 \int e_{x_h}\mathrm{d}t + \sum_{i=h}^{j} k_i e_{x_i} = 0 \qquad (19.83)$$

This sliding surface offers zero-state error, even if $S(e_{x_i}, t) = \varepsilon_1$ due to hardware errors or fixed (or limited) frequency switching. Indeed, in the steady state, the only nonnull term is $k_0 \int e_{x_h}\mathrm{d}t = \varepsilon_1$. Also, like (19.75), this closed-loop control law does not depend on system parameters or perturbations to ensure a prescribed closed-loop dynamics similar to (19.67) with an error approaching zero.

The approach outlined herein precisely defines the control law (sliding surface (19.75) or (19.83)) needed to obtain the selected dynamics, and the switching law (19.81). As the control law allows the implementation of the system controller, and the switching law gives the PWM modulator, there is no need to design linear or nonlinear controllers, based on linear converter models, or devise off-line PWM modulators. Therefore, sliding-mode control theory, applied to power converters, provides a systematic method to generate both the controller(s) (usually nonlinear) and the modulator(s) that will ensure a model reference robust dynamics, solving the control problem of power converters.

In the next examples, it is shown that sliding-mode controllers use (nonlinear) state feedback, therefore needing to measure the state variables and often other variables, since they use more system information. This is a disadvantage since more sensors are needed. However, the straightforward control design and obtained performances are much better than those obtained with the averaged models, the use of more sensors

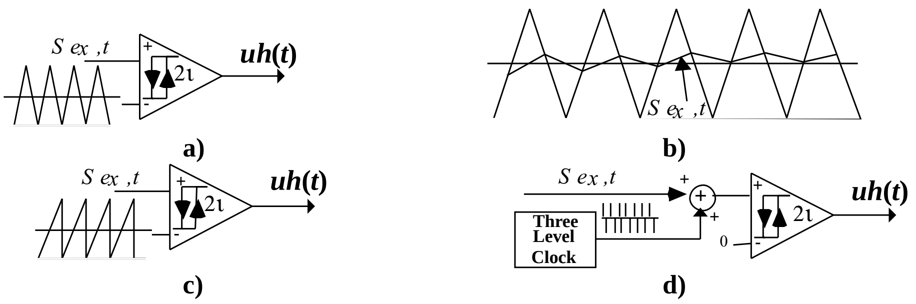


FIGURE 19.25 Auxiliary functions and methods to obtain constant switching frequency with sliding-mode controllers.

being really valued. Alternatively to the extra sensors, state observers can be used [9].

EXAMPLE 19.10. SLIDING-MODE CONTROL OF THE BUCK-BOOST DC/DC CONVERTER. Consider again the buck-boost converter of Fig. 19.1 and assume the converter output voltage v_o to be the controlled output. From Section 19.2, using the switched state-space model (19.9), making $\mathrm{d}v_o/\mathrm{d}t = \theta$, and calculating the first time derivative of θ, the controllability canonical model (19.84), where $i_o = v_o/R_o$, is obtained:

$$\begin{aligned}\frac{\mathrm{d}v_o}{\mathrm{d}t} &= \theta = \frac{1-\delta(t)}{C_o} i_L - \frac{i_o}{C_o}\\ \frac{\mathrm{d}\theta}{\mathrm{d}t} &= -\frac{(1-\delta(t))^2}{L_i C_o} v_o - \frac{C_o\theta + i_o}{C_o(1-\delta(t))}\frac{\mathrm{d}\delta(t)}{\mathrm{d}t}\\ &\quad - \frac{1}{C_o}\frac{\mathrm{d}i_o}{\mathrm{d}t} + \frac{\delta(t)(1-\delta(t))}{C_o L_i} V_{DC}\end{aligned} \tag{19.84}$$

This model, written in the form of (19.66), contains two state variables, v_o and θ. Therefore, from (19.75) and considering $e_{v_o} = v_{o_r} - v_o$, $e_\theta = \theta_r - \theta$, the control law (sliding surface) is

$$\begin{aligned}S(e_{x_i}, t) &= \sum_{i=1}^{2} k_i e_{x_i}\\ &= k_1(v_{o_r} - v_o) + k_2\frac{\mathrm{d}v_{o_r}}{\mathrm{d}t} - k_2\frac{\mathrm{d}v_o}{\mathrm{d}t}\\ &= k_1(v_{o_r} - v_o) + k_2\frac{\mathrm{d}v_{o_r}}{\mathrm{d}t} - \frac{k_2}{C_o}(1-\delta(t))i_L\\ &\quad + \frac{k_2}{C_o} i_o = 0\end{aligned} \tag{19.85}$$

This sliding surface depends on the variable $\delta(t)$, which should be precisely the result of the application, in (19.85), of a switching law similar to (19.81). Assuming an ideal up–down converter and slow variations, from (19.25b) the variable $\delta(t)$ can be averaged to $\delta_1 = v_o/(v_o + V_{DC})$. By substituting this relation in (19.85), and rearranging, (19.86) is derived:

$$\begin{aligned}S(e_{x_i}, t) &= \frac{C_o k_1}{k_2}\left(\frac{v_o + V_{DC}}{v_o}\right)\\ &\quad \times \left((v_{o_r} - v_o) + \frac{k_2}{k_1}\frac{\mathrm{d}v_{o_r}}{\mathrm{d}t} + \frac{k_2}{k_1}\frac{1}{C_o} i_o\right)\\ &\quad - i_L = 0\end{aligned} \tag{19.86}$$

This control law shows that the power supply voltage V_{DC} must be measured, as well as the output voltage v_o and the currents i_o and i_L.

To obtain the switching law from stability considerations (19.76), the time derivative of $S(e_{x_i}, t)$, supposing $(v_o + V_{DC})/v_o$ almost constant, is

$$\begin{aligned}\dot{S}(e_{x_i}, t) &= \frac{C_o k_1}{k_2}\left(\frac{v_o + V_{DC}}{v_o}\right)\\ &\quad \times \left(\frac{\mathrm{d}e_{v_o}}{\mathrm{d}t} + \frac{k_2}{k_1}\frac{\mathrm{d}^2 v_{o_r}}{\mathrm{d}t^2} + \frac{k_2}{k_1 C_o}\frac{\mathrm{d}i_o}{\mathrm{d}t}\right) - \frac{\mathrm{d}i_L}{\mathrm{d}t}\end{aligned} \tag{19.87}$$

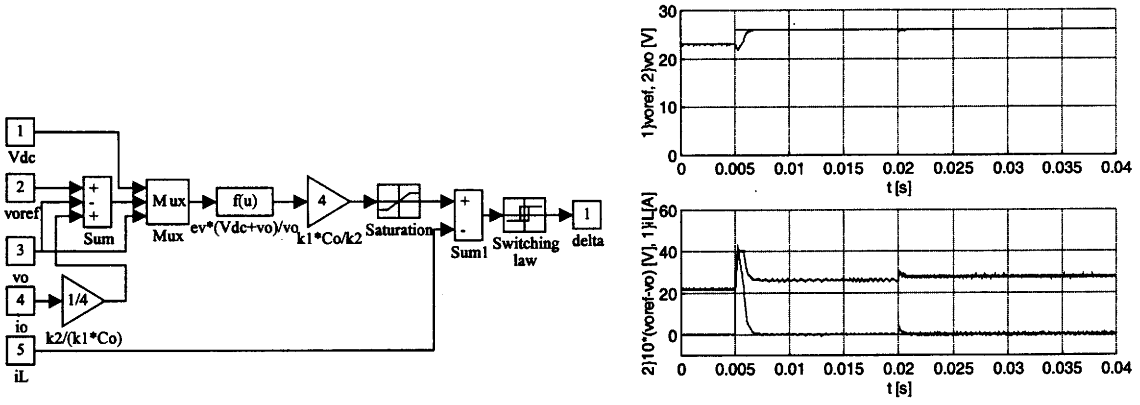
If $S(e_{x_i}, t) > 0$ then, from (19.76), $\dot{S}(e_{x_i}, t) < 0$ must hold. Analyzing (19.87), we can conclude that, if $S(e_{x_i}, t) > 0$, $\dot{S}(e_{x_i}, t)$ is negative if, and only if, $\mathrm{d}i_L/\mathrm{d}t > 0$. Therefore, for positive errors $e_{v_o} > 0$ the current i_L must be increased, which implies $\delta(t) = 1$. Similarly, for $S(e_{x_i}, t) < 0$, $\mathrm{d}i_L/\mathrm{d}t < 0$ and $\delta(t) = 0$. Thus, a switching law similar to (19.81) is obtained:

$$\delta(t) = \begin{cases} 1 & \text{for } S(e_{x_i}, t) > +\varepsilon \\ 0 & \text{for } S(e_{x_i}, t) < -\varepsilon \end{cases} \tag{19.88}$$

The same switching law could be obtained from knowing the dynamic behavior of this nonminimum-phase up–down converter: to increase (decrease) the output voltage, a previous increase (decrease) of the i_L current is mandatory.

Equation (19.85) shows that, if the buck-boost converter is into sliding mode ($S(e_{x_i}, t) = 0$), the dynamics of the output voltage error tends exponentially to zero with time constant k_2/k_1. Since during step transients, the converter is in the reaching mode, the time constant k_2/k_1 cannot be designed to originate error variations larger than allowed by the self-dynamics of the converter excited by a certain maximum permissible i_L current. Given the polynomials (19.72) with $m = 1$, $k_1/k_2 = \omega_o$ should be much lower than the finite switching frequency $(1/T)$ of the converter. Therefore, the time constant must obey $k_2/k_1 \gg T$. Then, knowing that k_2 and k_1 are both imposed, the control designer can tailor the time constant as needed, provided that the preceding restrictions are observed.

Short-circuit-proof operation for the sliding-mode controlled buck-boost converter can be derived from (19.86), noting that all the terms to the left of i_L represent the set point for this current. Therefore, limiting these terms (Fig. 19.26, saturation block, with $i_{L\max} = 40$ A), the switching law (19.88) ensures that the output current will not rise above the maximum imposed limit. Given the converter nonminimum-phase



a) b)

FIGURE 19.26 (a) Block diagram of the sliding-mode nonlinear controller for the buck-boost converter; (b) transient responses of the sliding-mode controlled buck-boost converter. At $t = 0.005$ s v_{oref} step from 23 V to 26 V. At $t = 0.02$ s V_{DC} step from 26 V to 23 V. Top graph: square reference v_{oref} and output voltage v_o. Bottom graph: trace around 20, i_L current; trace starting at zero, $10 \times (v_{oref} - v_o)$.

behavior, this i_L current limit is fundamental to reach the sliding-mode of operation with step disturbances.

The block diagram (Fig. 19.26a) of the implemented control law ((19.86) with $C_o k_1/k_2 = 4$) and switching law ((19.88) with $\varepsilon = 0.3$) does not included the time derivative of the reference (dv_{on}/dt) since, in a dc–dc converter its value is considered zero. The controller hardware (or software), derived using just the sliding-mode approach, operates only in closed loop.

The resulting performance (Fig. 19.26b) is much better than that obtained with the PID notch filter (compare to Example 19.4, Fig. 19.9b), with a higher response speed and robustness against power-supply variations.

EXAMPLE 19.11. SLIDING-MODE CONTROL OF THE SINGLE-PHASE HALF-BRIDGE CONVERTER. Consider the half-bridge four quadrant converter of Fig. 19.27 with output filter and inductive load ($V_{DCmax} = 300$ V; $V_{DCmin} = 230$ V; $R_i = 0.1\ \Omega$; $L_o = 4$ mH; $C_o = 470\ \mu$F; inductive load with nominal values $R_o = 7\ \Omega$, $L_o = 1$ mH).

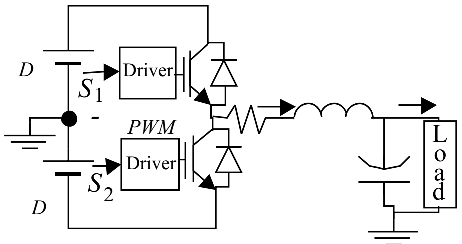


FIGURE 19.27 Half bridge power inverter with insulated gate bipolar transistors, output filter and load.

Assuming that power switches, output filter capacitor, and power supply are all ideal, and a generic load with allowed slow variations, the switched state-space model of the converter, with state variables v_o and i_L, is

$$\frac{d}{dt}\begin{bmatrix} v_o \\ i_L \end{bmatrix} = \begin{bmatrix} 0 & 1/C_o \\ -1/L_o & -R_i/L_o \end{bmatrix}\begin{bmatrix} v_o \\ i_L \end{bmatrix} + \begin{bmatrix} -1/C_o & 0 \\ 0 & 1/L_o \end{bmatrix}\begin{bmatrix} i_o \\ \delta(T)V_{DC} \end{bmatrix} \qquad (19.89)$$

where i_o is the generic load current and $v_{PWM} = \delta(t)V_{DC}$ is the extended PWM output voltage ($\delta(t) = +1$ when one of the upper main semiconductors of Fig. 19.27 is conducting and $\delta(t) = -1$ when one of the lower semiconductors is on).

Output Current Control (Current Mode Control)

To perform as a v_{i_L} voltage controlled i_L current source (or sink) with transconductance g_m ($g_m = i_L/v_{i_L}$), this converter must supply a current i_L to the output inductor, obeying $i_L = g_m v_{i_L}$. Using a bounded v_{i_L} voltage to provide output short-circuit protection, the reference current for a sliding-mode controller must be $i_{L_r} = g_m v_{i_L}$. Therefore, the controlled output is the i_L current and the controllability canonical model (19.90) is obtained from the second equation of (19.89), since the dynamics of this subsystem, being governed by $\delta(t)V_{DC}$, is already in the controllability canonical form for this chosen output.

$$\frac{di_L}{dt} = -\frac{R_i}{L_o}i_L - \frac{1}{L_o}v_o + \frac{\delta(t)V_{DC}}{L_o} \qquad (19.90)$$

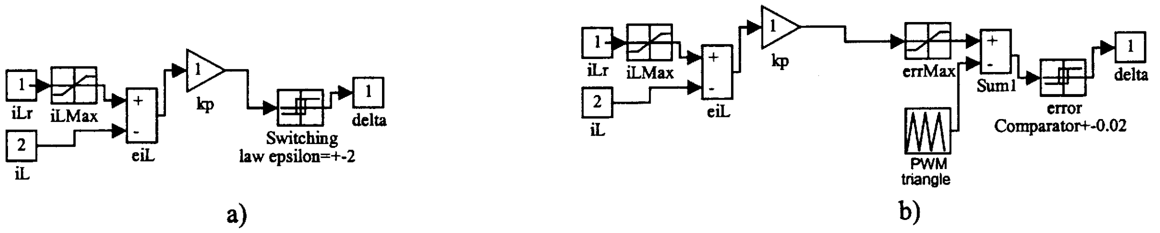


FIGURE 19.28 (a) Implementation of short-circuit-proof sliding-mode current controller (variable frequency); (b) implementation of fixed-frequency, short-circuit-proof, sliding-mode current controller using a triangular waveform.

A suitable sliding surface (19.91) is obtained from (19.90), making $e_{i_L} = i_{L_r} - i_L$.

$$\begin{aligned} S(e_{i_L}, t) &= k_p e_{i_L} = k_p(i_{L_r} - i_L) \\ &= k_p(g_m v_{i_L} - i_L) = 0 \end{aligned} \tag{19.91}$$

The switching law (19.92) can be devised calculating the time derivative of (19.91) $\dot{S}(e_{i_L}, t)$, and applying (19.76). If $S(e_{i_L}, t) > 0$, then $\mathrm{d}_{i_L}/dt > 0$ must hold to obtain $\dot{S}(e_{i_L}, t) < 0$, implying $\delta(t) = 1$.

$$\delta(t) = \begin{cases} 1 & \text{for } S(e_{i_L}, t) > +\varepsilon \\ -1 & \text{for } S(e_{i_L}, t) < -\varepsilon \end{cases} \tag{19.92}$$

The k_p value and allowed ripple ε define the instantaneous value of the variable switching frequency. The sliding mode controller is represented in Fig. 19.28a. Step response (Fig. 19.29a) shows variable-frequency operation and a very short rise time (limited only by the available power supply) and confirms the expected robustness against supply variations.

For systems where fixed frequency operation is needed, a triangular wave, with frequency (10 kHz) slightly greater than the maximum variable frequency, can be added (Fig. 19.28b) to the sliding-mode controller, as explained in Section 19.3.3. Performances (Fig. 19.29b), comparable to those of the variable-frequency sliding-mode controller show the constant switching frequency, but also a steady-state error dependent on the operating point.

To eliminate this error, a new sliding surface (19.93), based on (19.83), should be used. The constants k_p and k_0 can be calculated, as discussed in Example 19.10.

$$S(e_{i_L}, t) = k_0 \int e_{i_L} \mathrm{d}t + k_p e_{i_L} = 0 \tag{19.93}$$

The new constant-frequency sliding-mode current controller (Fig. 19.30a), with added antiwindup techniques (Example 19.6), since a saturation (errMax) is

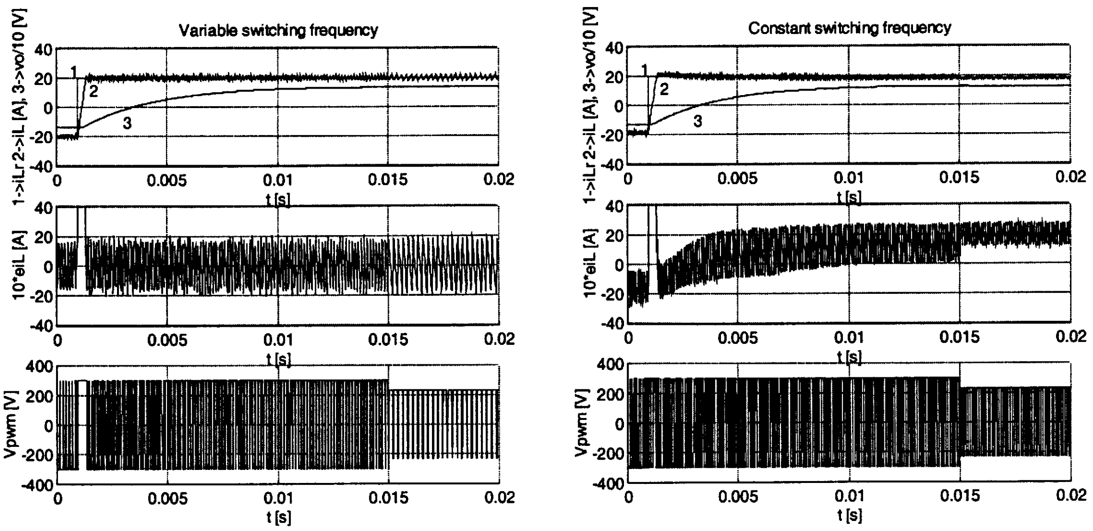


FIGURE 19.29 Performance of the transconductance amplifier; response to a i_{L_r} step from −20 A to 20 A at $t = 0.001$ s and to a V_{DC} step from 300 V to 230 V at $t = 0.015$ s.

needed to keep the frequency constant, now presents no steady-state error (Fig. 19.30b). Performances are comparable to those of the variable frequency controller, and no robustness loss is visible. The applied sliding-mode approach led to the derivation of the known **average current-mode controller**.

Output voltage control

To obtain a power operational amplifier suitable for building uninterruptible power supplies, power filters, power gyrators, inductance simulators, or power factor active compensators, v_o must be the controlled converter output. Therefore, using the input–output linearization technique, it is seen that the first time derivative of the output $(\mathrm{d}v_o/\mathrm{d}t) = (i_L - i_o)/C_o = \theta$, does not explicitly contain the control input $\delta(t)V_{DC}$. Then, the second derivative must be calculated. Taking into account (19.89), as $\theta = (i_L - i_o)/C_o$, (19.94) is derived

$$\begin{aligned}\frac{\mathrm{d}^2 v_o}{\mathrm{d}t^2} &= \frac{\mathrm{d}}{\mathrm{d}t}\theta = \frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{i_L - i_o}{C_o}\right)\\ &= -\frac{R_i}{L_o}\theta - \frac{1}{L_oC_o}v_o - \frac{R_i}{L_oC_o}i_o - \frac{1}{C_o}\frac{\mathrm{d}i_o}{\mathrm{d}t}\\ &\quad + \frac{1}{L_oC_o}\delta(t)V_{DC} \qquad (19.94)\end{aligned}$$

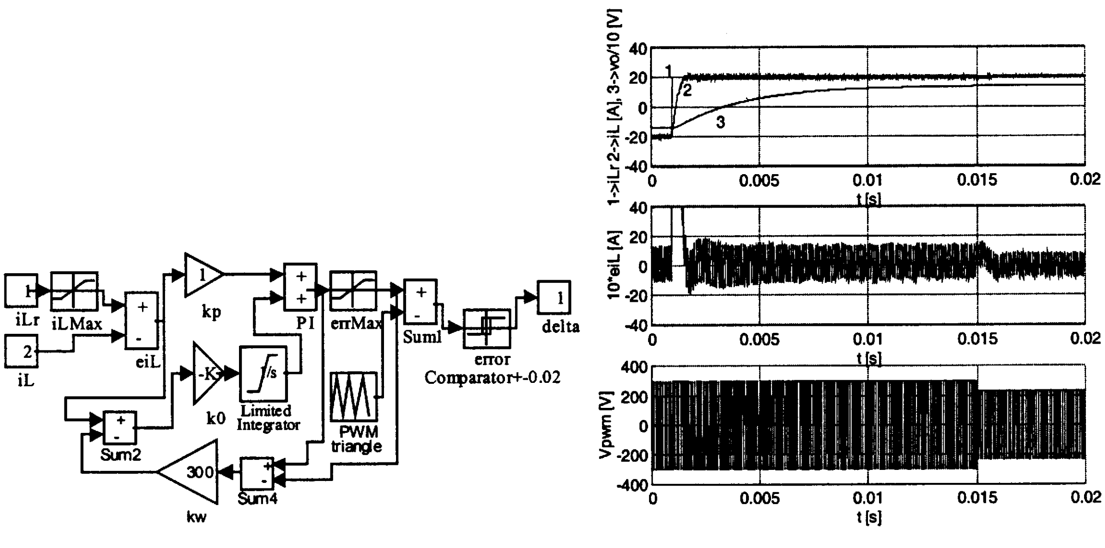
This expression shows that the second derivative of the output depends on the control input $\delta(t)V_{DC}$. No further time derivative is needed, and the state-space equations of the equivalent circuit, written in the phase canonical form, are

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} v_o \\ \theta \end{bmatrix} = \begin{bmatrix} \theta \\ -\frac{R_i}{L_o}\theta - \frac{1}{L_oC_o}v_o - \frac{R_i}{L_oC_o}i_0 - \frac{1}{C_o}\frac{\mathrm{d}i_o}{\mathrm{d}t} + \frac{1}{L_oC_o}\delta(t)V_{DC} \end{bmatrix} \qquad (19.95)$$

According to (19.75), (19.95), and (19.89), considering that e_{v_o} is the feedback error $e_{v_o} = v_{o_r} - v_o$, a sliding surface $S(e_{v_o}, t)$, can be chosen:

$$\begin{aligned}S(e_{v_o}, t) &= k_1 e_{v_o} + k_2\frac{\mathrm{d}e_{v_o}}{\mathrm{d}t}\\ &= e_{v_o} + \frac{k_2}{k_1}\frac{\mathrm{d}e_{v_o}}{\mathrm{d}t} = e_{v_o} + \beta\frac{\mathrm{d}e_{v_o}}{\mathrm{d}t}\\ &= \frac{C_o}{\beta}(v_{o_r} - v_o) + C_o\frac{\mathrm{d}v_{o_r}}{\mathrm{d}t} + i_o - i_L = 0\end{aligned} \qquad (19.96)$$

where β is the time constant of the desired first-order response of output voltage ($\beta \gg T > 0$), as the strong relative degree [9] of this system is 2, and sliding-mode operation reduces by one the order of this system (the strong relative degree represents the number of times the



a) b)

FIGURE 19.30 (a) Block diagram of the average current-mode controller (sliding mode); (b) performance of the fixed-frequency sliding-mode controller with removed steady-state error: response to an i_{L_r} step from -20 A to 20 A at $t = 0.001$ s and to a V_{DC} step from 300 V to 230 V at $t = 0.015$ s.

output variable must be time differentiated until a control input explicitly appears).

Calculating $\dot{S}(e_{v_o}, t)$, the control strategy (switching law) (19.97) can be devised since, if $S(e_{v_o}, t) > 0$, $\mathrm{d}i_L/\mathrm{d}t$ must be positive to obtain $\dot{S}(e_{i_L}, t) < 0$, implying $\delta(t) = 1$. Otherwise, $\delta(t) = -1$.

$$\delta(t) = \begin{cases} 1 \text{ for } S(e_{v_o}, t) > 0 \ (v_{PWM} = +V_{DC}) \\ -1 \text{ for } S(e_{v_o}, t) < 0 \ (v_{PWM} = -V_{DC}) \end{cases} \tag{19.97}$$

In the ideal sliding-mode dynamics, the filter input voltage v_{PWM} switches between V_{DC} and $-V_{DC}$ with infinite frequency. This switching generates the equivalent control voltage V_{eq} that must satisfy the sliding manifold invariance conditions, $S(e_{v_o}, t) = 0$ and $\dot{S}(e_{v_o}, t) = 0$. Therefore, from $\dot{S}(e_{v_o}, t) = 0$, using (19.96) and (19.89), (or from (19.94)), V_{eq} is:

$$V_{eq} = L_o C_o \left[\frac{\mathrm{d}^2 v_{o_r}}{\mathrm{d}t^2} + \frac{1}{\beta} \frac{\mathrm{d}v_{o_r}}{\mathrm{d}t} + \frac{v_o}{L_o C_o} \right.$$
$$\left. + \frac{(\beta R_i - L_o) i_L}{\beta L_o C_o} + \frac{i_o}{\beta C_o} + \frac{1}{C_o} \frac{\mathrm{d}i_o}{\mathrm{d}t} \right] \tag{19.98}$$

This equation shows that only smooth input v_{o_r} signals ("smooth" functions) can be accurately reproduced at the inverter output, as it contains derivatives of the v_{o_r} signal. This fact is a consequence of the stored electromagnetic energy. The existence of the sliding-mode operation implies the following necessary and sufficient condition:

$$-V_{DC} < V_{eq} < V_{DC} \tag{19.99}$$

Equation (19.99) enables the determination of the minimum input voltage V_{DC} needed to enforce the sliding-mode operation. Nevertheless, even in the case of $|V_{eq}| > |V_{DC}|$, the system experiences only a saturation transient and eventually reaches the region of sliding-mode operation, except if, in the steady state, operating point and disturbances enforce $|V_{eq}| > |V_{DC}|$.

In the ideal sliding mode, at infinite switching frequency, state trajectories are directed toward the sliding surface and move exactly along the discontinuity surface. Practical power converters cannot switch at infinite frequency, so a typical implementation of (19.96) (Fig. 19.31a) with neglected $\dot{v}_{o_r}$) features a comparator with hysterisis 2ε, switching occurring at $|S(e_{v_o}, t)| > \varepsilon$ with frequency depending on the slopes of i_L. This hysterisis causes phase plane trajectory oscillations of width 2ε around the discontinuity surface $S(e_{v_o}, t) = 0$, but the V_{eq} voltage is still correctly generated, since the resulting duty cycle is a continuous variable (except for error limitations in the hardware or software, which can be corrected using the approach pointed out by (19.82)).

The design of the compensator and modulator is integrated with the same theoretical approach, since the signal $S(e_{v_o}, t)$ applied to a comparator generates the pulses for the power semiconductors drives. If short-circuit-proof operation is built into the power semiconductor drives, there is the possibility to measure only the capacitor current $(i_L - i_o)$.

Short-Circuit Protection and Fixed Frequency Operation of the Power Operational Amplifier

If we note that all the terms to the left of i_L in (19.96) represent the value of i_{L_r}, a simple way to provide short-circuit protection is to bound the sum of all these terms (Fig. 19.31a) with $i_{L_{r\max}} = 100$ A). Alternatively, the output current controllers of Fig. 19.28 can be used, comparing (19.91) to (19.96), to obtain $i_{L_r} = S(e_{v_o}, t)/k_p + i_L$. Therefore, the block diagram of Fig. 19.31a provides the i_{L_r} output (for $k_p = 1$) to be the input of the current controllers (Figs. 19.28 and 19.31a). As seen, the controllers of Figs. 19.28b and 19.30a also ensure fixed-frequency operation.

For comparison purposes a proportional integral (PI) controller, with antiwindup (Fig. 19.31b) for output voltage control, was designed, supposing current mode control of the half bridge (modeled considering a small delay T_d, $i_{L_r} = g_m v_{i_L}/(1 + sT_d)$, a pure resistive load R_o,

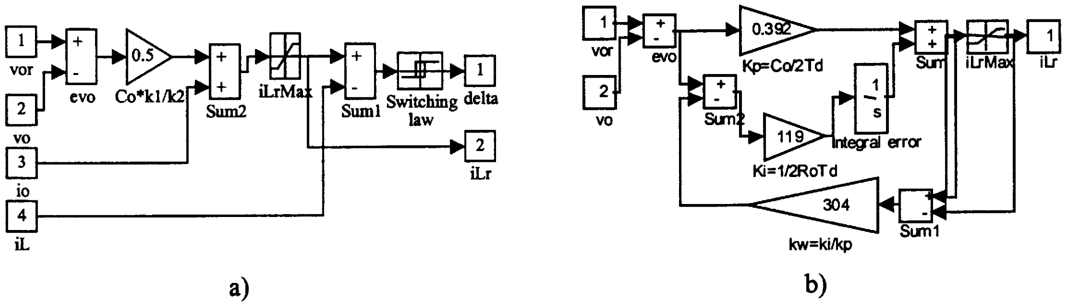
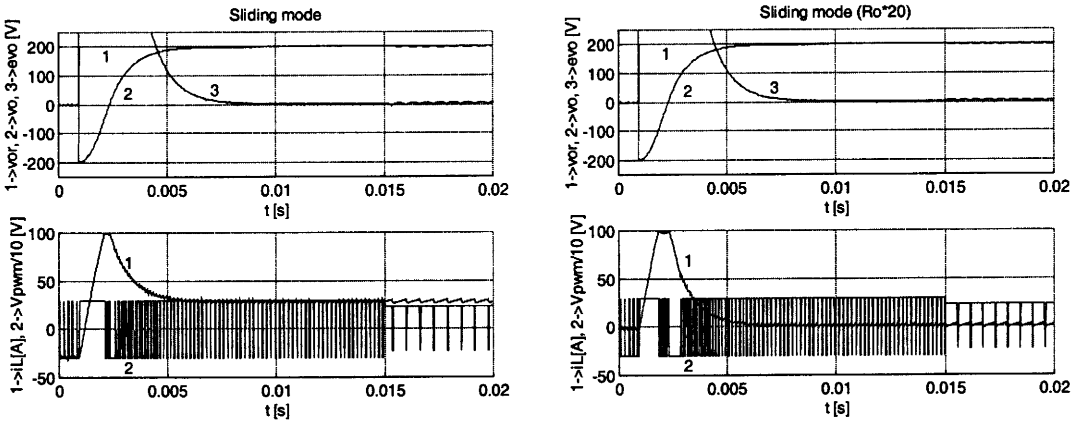


FIGURE 19.31 (a) Implementation of short-circuit-proof, sliding-mode output voltage controller (variable frequency); (b) implementation of antiwindup PI current mode (fixed-frequency) controller.



a) Variable frequency sliding mode (nominal load) **b) Variable frequency sliding mode (R_o×20)**

FIGURE 19.32 Performance of the power operational amplifier; response to a v_{o_r} step from −200 V to 200 V at $t = 0.001$ s and to a V_{DC} step from 300 V to 230 V at $t = 0.015$ s.

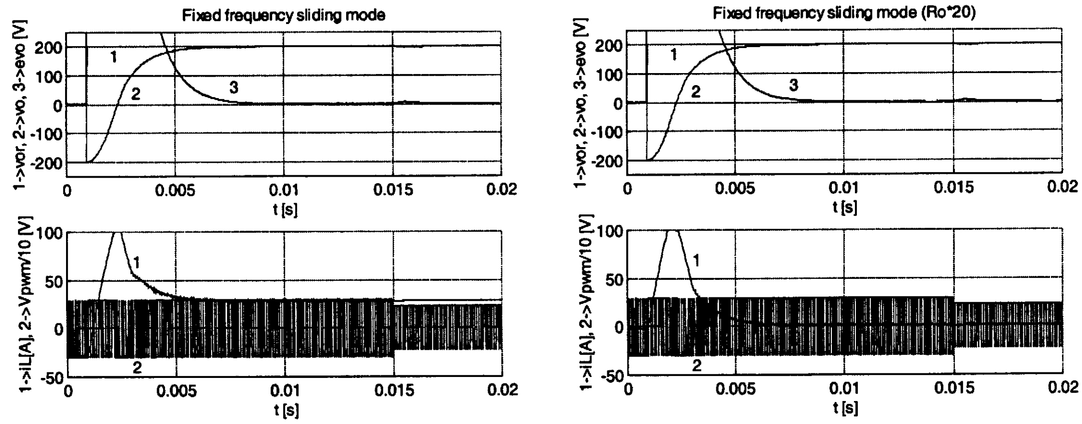
and using the approach outlined in Examples 19.6 and 19.8 ($k_v = 1$, $g_m = 1$, $\zeta^2 = 0.5$, $T_d = 600$ μs)). The obtained PI (19.37) parameters are

$$\begin{aligned} T_z &= R_o C_o \\ T_p &= 4\zeta^2 g_m k_v R_o T_d \end{aligned} \tag{19.100}$$

Both variable-frequency (Fig. 19.32) and constant frequency (Fig. 19.33) sliding-mode output voltage controllers present excellent performance and robustness with nominal loads. With loads much higher than the nominal value (Figs. 19.32b and Fig. 19.33b), the performance and robustness are also excellent. The sliding-mode constant-frequency PWM controller presents the additional advantage of injecting lower ripple in the load.

As expected, the PI regulator presents lower performance (Fig. 19.34). The response speed is lower and the insensitivity to power supply and load variations (Fig. 19.34b) is not as high as with sliding mode. Nevertheless, the PI performances are acceptable, since its design was carried considering a slow and fast manifold sliding mode approach: the fixed-frequency sliding-mode current controller (19.93) for the fast manifold (the i_L current dynamics) and the antiwindup PI for the slow manifold (the v_o voltage dynamics, usually much slower than the current dynamics).

EXAMPLE 19.12. CONSTANT-FREQUENCY SLIDING-MODE CONTROL OF p PULSE PARALLEL RECTIFIERS. This example presents a new paradigm to the control of thyristor rectifiers. Since p pulse rectifiers are variable-structure systems, sliding-mode control is applied here to 12 pulse rectifiers, still useful for very high power applications [12]. The design determines the variables to be measured and the controlled rectifier presents robustness and much shorter response times, even with parameter uncertainty, perturbations, noise, and nonmodeled dynamics. These



a) Fixed frequency sliding mode (nominal load) **b) Fixed frequency sliding mode (R_o×20)**

FIGURE 19.33 Performance of the power operational amplifier; response to a v_{o_r} step from −200 V to 200 V at $t = 0.001$ s and to a V_{DC} step from 300 V to 230 V at $t = 0.015$ s.

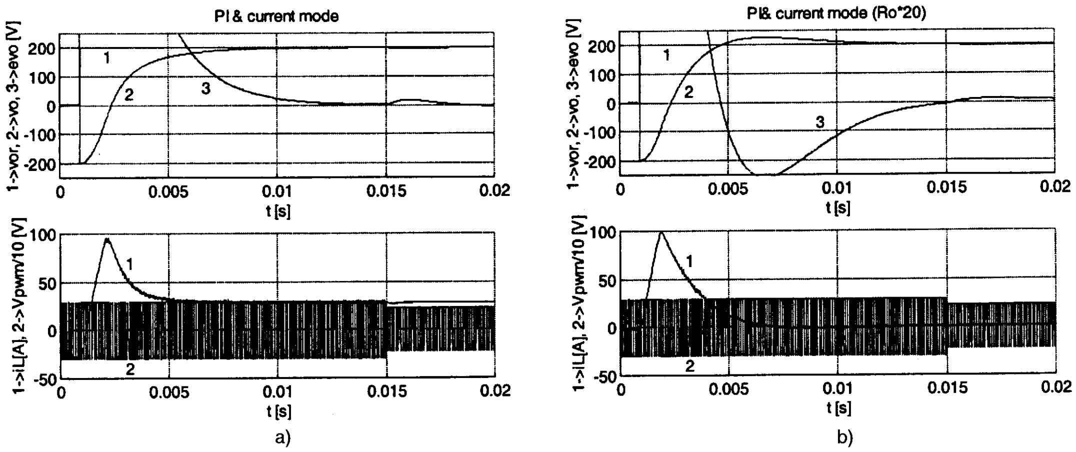


FIGURE 19.34 Performance of the PI controlled power operational amplifier; response to a v_{o_r} step from -200 V to 200 V at $t = 0.001$ s and to a V_{DC} step from 300 V to 230 V at $t = 0.015$ s.

performances are not feasible using linear controllers, obtained here for comparison purposes.

Modeling the 12-Pulse Parallel Rectifier

The 12-pulse rectifier (Fig. 19.35a) is built with four three-phase half-wave rectifiers, connected in parallel with current-sharing inductances l and l' merged with capacitors C', C_2, to obtain a second-order LC filter. This allows low output-voltage ripple and continuous mode of operation (laboratory model with $l = 44$ mH; $l' = 13$ mH; $C' = C_2 = 10$ mF; star-delta connected ac sources with $E_{RMS} \approx 65$ V and power rating 2.2 kW, load approximately resistive $R_o \approx 3$ to 5 Ω).

To control the output voltage v_{c_2}, given the complexity of the whole system, the best approach is to derive a low-order model. By averaging the four half-wave rectifiers, neglecting the rectifier dynamics and mutual couplings, the equivalent circuit of Fig. 19.35b is obtained $(l_1 = l_2 = l_3 = l_4 = l;\ \ l_5 = l_6 = l';\ \ C_{11} = C_{12} = C')$. Since the rectifiers are identical, the equivalent 12-pulse rectifier model of Fig. 19.35c is derived, simplifying the resulting parallel associations ($L_1 = l/4$; $L_2 = l'/2$; $C_1 = 2C'$).

Considering the load current i_o as an external perturbation and v_i the control input, the state-space model of the equivalent circuit Fig. 19.3.5c is:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{c_1} \\ v_{c_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1/L_1 & 0 \\ 0 & 0 & 1/L_2 & -1/L_2 \\ 1/C_1 & -1/C_1 & 0 & 0 \\ 0 & 1/C_2 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{c_1} \\ v_{c_2} \end{bmatrix} + \begin{bmatrix} 1/L_1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -1/C_2 \end{bmatrix}\begin{bmatrix} v_i \\ i_o \end{bmatrix} \tag{19.101}$$

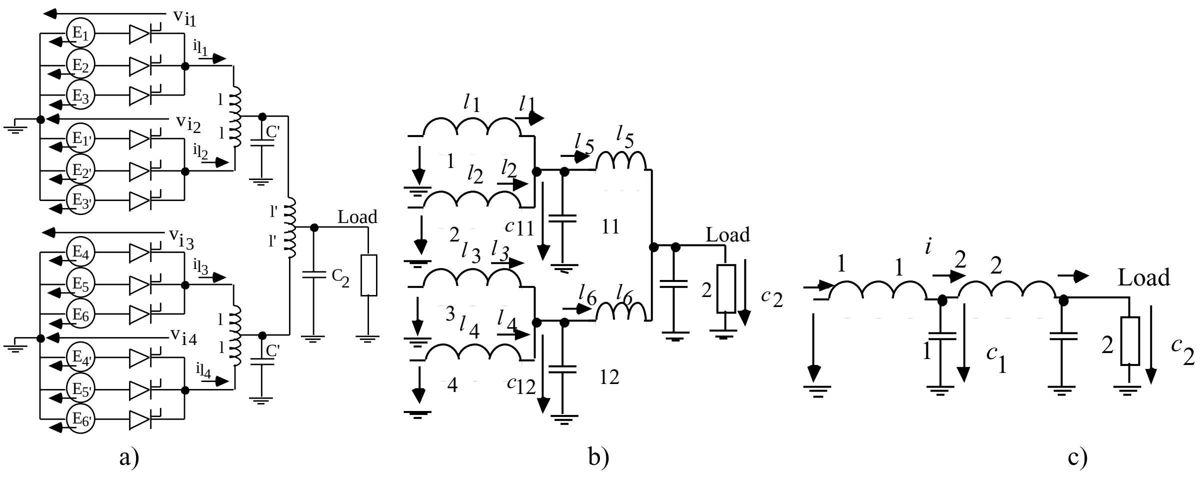


FIGURE 19.35 Twelve-pulse rectifier with interphase reactors and intermediate capacitors; (b) rectifier model neglecting the half-wave rectifier dynamics; (c) low-order averaged equivalent circuit for the 12-pulse rectifier with the resulting output double LC filter.

Sliding-Mode Control of the 12-Pulse Parallel Rectifier

Since the output voltage v_{c_2} of the system must follow the reference $v_{c_{2r}}$, the system equations in the phase canonical (or controllability) form must be written, using the error $e_{v_{c_2}} = v_{c_{2r}} - v_{c_2}$ and its time derivatives as new state error variables, as done in Example 19.11.

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} e_{v_{c_2}} \\ e_\theta \\ e_\gamma \\ e_\beta \end{bmatrix} = \begin{bmatrix} e_\theta \\ e_\gamma \\ e_\beta \\ -\left(\frac{1}{C_1L_1}+\frac{1}{C_1L_2}+\frac{1}{C_2L_2}\right)e_\gamma - \frac{e_{v_{c_2}}}{C_1L_1C_2L_2} \\ \quad -\left(\frac{1}{C_1L_1C_2}+\frac{1}{C_1C_2L_2}\right)\frac{\mathrm{d}i_o}{\mathrm{d}t} - \frac{1}{C_2}\frac{\mathrm{d}^3 i_o}{\mathrm{d}t^3} - \frac{v_i}{C_1L_1C_2L_2} \end{bmatrix} \tag{19.102}$$

The sliding surface $S(e_{x_i}, t)$, designed to reduce the system order, is a linear combination of all the phase canonical state variables. Considering (19.102), (19.101), and the errors $e_{v_{c_2}}$, e_θ, e_γ, and e_β, the sliding surface can be expressed as a combination of the rectifier currents, voltages, and their time derivatives:

$$\begin{aligned} S(e_{x_i}, t) &= e_{v_{c_2}} + k_\theta e_\theta + k_\gamma e_\gamma + k_\beta e_\beta \\ &= v_{c_{2r}} + k_\theta\theta_r + k_\gamma\gamma_r + k_\beta\beta_r \\ &\quad - \left(1 - \frac{k_\gamma}{C_2L_2}\right)v_{c_2} - \frac{k_\gamma}{C_2L_2}v_{c_1} \\ &\quad + \left(\frac{k_\theta}{C_2} - \frac{k_\beta}{C_2^2L_2}\right)i_o + \frac{k_\gamma}{C_2}\frac{\mathrm{d}i_o}{\mathrm{d}t} \\ &\quad + \frac{k_\beta}{C_2}\frac{\mathrm{d}^2 i_o}{\mathrm{d}t^2} - \frac{k_\beta}{C_1C_2L_2}i_{L_1} \\ &\quad - \left(\frac{k_\theta}{C_2} - \frac{k_\beta}{C_1C_2L_2} - \frac{k_\beta}{C_2^2L_2}\right)i_{L_2} \\ &= 0 \end{aligned} \tag{19.103}$$

Equation (19.103) shows the variables to be measured (v_{c_2}, v_{c_1}, i_o, i_{L_1}, and i_{L_2}). Therefore, it can be concluded that the output current of each three-phase half-wave rectifier must be measured.

The existence of the sliding mode implies $S(e_{x_i}, t) = 0$ and $\dot{S}(e_{x_i}, t) = 0$. Given the state models (19.101) (19.102), and from $\dot{S}(e_{x_i}, t) = 0$, the available voltage of the power supply v_i must exceed the equivalent average dc input voltage V_{eq} (19.104), which should be applied at the filter input, in order that the system state slides along the sliding surface (19.103).

$$\begin{aligned} V_{eq} = &\frac{C_1L_1C_2L_2}{k_\beta}(\theta_r + k_\theta\gamma_r + k_\gamma\beta_r + k_\beta\dot{\beta}_r) \\ &+ v_{c_2} - \frac{C_1L_1C_2L_2}{k_\beta}(\theta + k_\gamma\beta) \\ &+ \left(C_2L_2 + C_2L_1 + C_1L_1 - C_1L_1C_2L_2\frac{k_\theta}{k_\beta}\right)\gamma \\ &+ (L_1 + L_2)\frac{\mathrm{d}i_0}{\mathrm{d}t} + C_1L_1L_2\frac{\mathrm{d}^3 i_o}{\mathrm{d}t^3} \end{aligned} \tag{19.104}$$

This means that the power supply RMS voltage values should be chosen high enough to account for the maximum effects of the perturbations. This is almost the same criterion adopted when calculating the RMS voltage values needed with linear controllers. However, as the V_{eq} voltage contains the derivatives of the reference voltage, the system will not be able to stay in sliding mode with a step as the reference.

The switching law would be derived, considering that, from (19.102), $b_e(\mathbf{e}) > 0$. Therefore, from (19.81), if $S(e_{x_i}, t) > +\varepsilon$, then $v_i(t) = V_{eq_{\max}}$, else if $S(e_{x_i}, t) < -\varepsilon$, then $v_i(t) = -V_{eq_{\max}}$. However, because of the lack of gate turn-off capability of the rectifier thyristors, power rectifiers cannot generate the high-frequency switching voltage $v_i(t)$, since the statistical mean delay time is $T/2p$ and reaches $T/2$ when switching from $+V_{eq_{\max}}$ to $-V_{eq_{\max}}$. To control mains switched rectifiers, the described constant frequency sliding mode operation method is used, in which the sliding surface $S(e_{x_i}, t)$, instead of being compared to zero, is compared to an auxiliary constant frequency function $r(t)$ (Fig. 19.6b) synchronized with the mains frequency. The new switching law is:

$$\left.\begin{array}{l} \text{If } k_pS(e_{x_i}, t) > r(t) + \imath \Rightarrow \text{Trigger the next thyristor} \\ \text{If } k_pS(e_{x_t}, t) < r(t) - \imath \Rightarrow \text{Do not trigger any thyristor} \end{array}\right\} \Rightarrow v_i(t) \tag{19.105}$$

Since now $S(e_{x_i}, t)$ is not near zero, but around some value of $r(t)$, a steady-state error $e_{v_{c2av}}$ appears ($\min[r(t)]/k_p < e_{v_{c2av}} < \max[r(t)]/k_p$), as seen in Example 19.11. Increasing the value of k_p (toward the ideal saturation control) does not overcome this drawback, since oscillations would appear even for moderate k_p gains, because of the rectifier dynamics. Instead, the sliding surface (19.106), based on (19.83), should be used. It contains an integral term, which, given the canonical controllability form and the Routh–Hurwitz property, is the only nonzero term in steady state, enabling the complete elimination of the steady-state error.

$$S_i(e_{x_i}, t) = \int e_{v_{c_2}} \mathrm{d}t + k_{1_v} e_{v_{c_2}} + k_{1_\theta} e_\theta + k_{1\gamma} e_\gamma + k_{1\beta} e_\beta \tag{19.106}$$

To determine the constants of (19.106) a pole placement technique is selected, according to a fourth-order Bessel polynomial ($(B_E(s))_m$, $m = 4$, from (19.72c)), in order to obtain the smallest possible response time with almost no overshoot. For a delay characteristic as flat as possible, the delay t_r is taken inversely proportional to a frequency f_{ci} just below the lowest cutoff frequency ($f_{ci} < 8.44$ Hz) of the double LC filter. For this fourth-order filter, the delay is $t_r = 2.8/(2\pi f_{ci})$. By choosing $f_{ci} = 7$ Hz ($t_r \approx 64$ ms), and dividing all the Bessel polynomial terms by st_r, the characteristic polynomial (19.107) is obtained:

$$S_i(e_{x_i}, s) = \frac{1}{st_r} + 1 + \frac{45}{105} st_r + \frac{10}{105} s^2 t_r^2 + \frac{1}{105} s^3 t_r^3 \tag{19.107}$$

This polynomial must be applied to (19.106) to obtain the four sliding functions needed to derive the thyristor trigger pulses of the four three phase half wave rectifiers. These sliding functions will enable the control of the output current (i_{l_1}, i_{l_2}, i_{l_3} and i_{l_4}) of each half-wave rectifier, improving the current sharing among them (Fig. 19.35b). Supposing equal current share, the relation between the i_{L_i} current and the output currents of each three-phase rectifier is $i_{L_1} = 4i_{l_1} = 4i_{l_2} = 4i_{l_3} = 4i_{l_4}$. Therefore, for the nth half wave three phase rectifier, since for $n = 1$ and $n = 2$, $v_{c_1} = v_{c_{11}}$ and $i_{L_2} = 2i_{l_5}$ and for $n = 3$ and $n = 4$, $v_{c_1} = v_{c_{12}}$ and $i_{L_2} = 2i_{l_6}$, the four sliding surfaces are ($k_{1_v} = 1$):

$$\begin{aligned} S_i(e_{x_i}, t)_n = \Bigg[& k_{1_v} v_{c_{2r}} + \frac{45t_r}{105}\theta_r + \frac{10t_r^2}{105}\gamma_r + \frac{t_r^3}{105}\beta_r \\ & + \frac{1}{t_r}\int v_{c_{2r}} - v_{c_2} \mathrm{d}t - \left(\frac{k_{1_v}}{C_2 L_2} - \frac{10t_r^2}{105 C_2 L_2}\right) v_{c_2} \\ & - \frac{10t_r^2}{105 C_2 L_2} v_{c_{1\substack{1\\2}}} + \left(\frac{45t_r}{105 C_2} - \frac{t_r^3}{105 C_2^2 L_2}\right) i_o \\ & + \left(\frac{10t_r^2}{105 C_2}\right)\frac{\mathrm{d}i_o}{\mathrm{d}t} + \left(\frac{t_r^3}{105 C_2}\right)\frac{\mathrm{d}^2 i_o}{\mathrm{d}t^2}\Bigg] \Bigg/ 4 \\ & - \left[\left(\frac{45t_r}{105 C_2} - \frac{t_r^3}{105 C_2^2 L_2} - \frac{t_r^3}{105 C_1 L_2 C_2}\right) i_{l_6^5}\right] \Bigg/ 2 \\ & - \left(\frac{t_r^3}{105 C_1 L_2 C_2}\right) i_{l_n} \end{aligned} \tag{19.108}$$

If an inexpensive analog controller is desired, the successive time derivatives of the reference voltage and output current of (19.108) can be neglected, since their calculation is noise prone. Nonzero errors on the first-, second- and third-order derivatives of the controlled variable will appear, worsening the response speed. However, the steady-state error is not affected.

To implement the four equations (19.108), the variables v_{c_2}, $v_{c_{11}}$, $v_{c_{12}}$, i_o, i_{l_5}, i_{l_6}, i_{l_1}, i_{l_2}, i_{l_3}, and i_{l_4} must be measured. Although this could be done easily, it is very convenient to further simplify the practical controller, keeping its complexity and cost at the level of linear controllers, while maintaining the advantages of sliding mode. Therefore, the voltages $v_{c_{11}}$ and $v_{c_{12}}$ are assumed almost constant over one period of the filter input current, and $v_{c_{11}} = v_{c_{12}} = v_{c_2}$, meaning that $i_{l_5} = l_{l_6} = i_o/2$. With these assumptions, valid as the values of C' and C_2 are designed to provide an output voltage with very low ripple, the new sliding-mode functions are

$$\begin{aligned} & S_i(e_{x_i}, t)_n \\ & \quad \approx \frac{\frac{1}{t_r}\int v_{c_{2r}} - v_{c_2}\mathrm{d}t + k_{1_v}(v_{c_{2r}} - v_{c_2}) + \frac{t_r^3}{105}\frac{1}{C_1 C_2 L_2} i_o}{4} \\ & \quad - \left(\frac{t_r^3}{105 C_1 L_2 C_2}\right) i_{l_n} \end{aligned} \tag{19.109}$$

These approximations disregard only the high-frequency content of $v_{c_{11}}$, $v_{c_{12}}$, i_{l_5}, and i_{l_6}, and do not affect the rectifier steady-state response, but the step response will be a little slower (150 ms, Fig. 19.39, instead of $t_r \approx 64$ ms), although still much faster than the obtained with linear controllers.

Regardless of all the approximations, the low switching frequency of the rectifier would not allow the elimination of the dynamic errors. As a benefit of these approximations, the sliding-mode controller (Fig. 19.36a) will need only an extra current sensor (or a current observer) and an extra operational amplifier in comparison with linear controllers, derived hereafter (which need four current sensors and six operational amplifiers). Compared to the total cost of the 12 pulse rectifier plus output filter, the control hardware cost is negligible in both cases, even for medium-power applications.

Average Current Mode Control of the 12-Pulse Rectifier

For comparison purposes a PI-based controller structure is designed (Fig. 19.36b), taking into account that small mismatches of the line voltages or in the trigger angles can completely destroy the current share of the four paralleled rectifiers, in spite of the current equalizing inductances (l and l'). Output voltage control sensing only the output voltage is, therefore, not feasible.

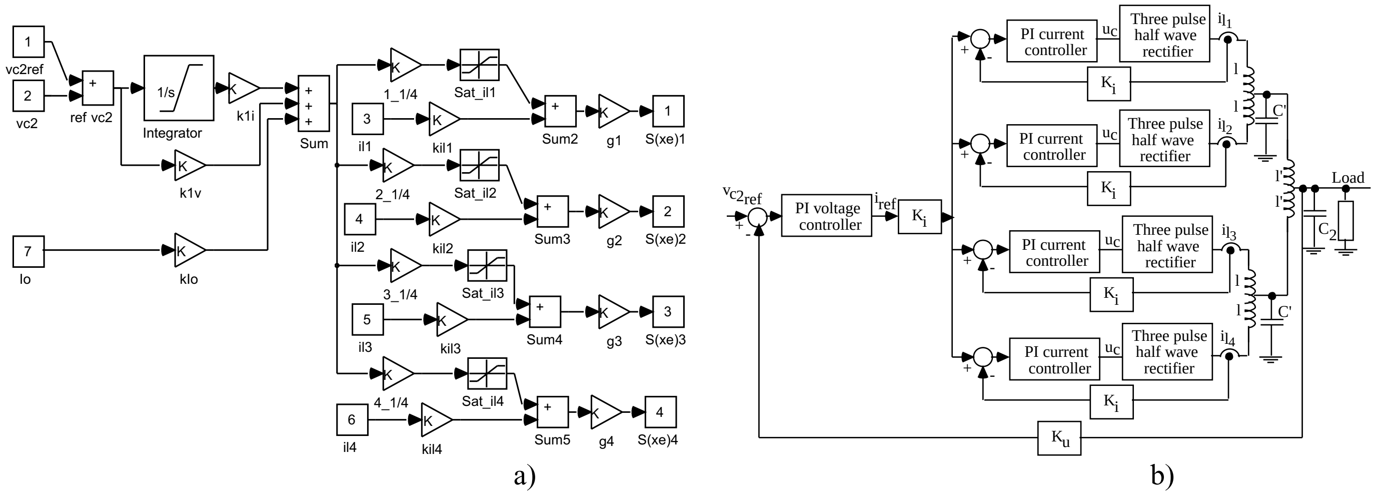


FIGURE 19.36 (a) Sliding-mode controller block diagram; (b) linear control hierarchy for the 12-pulse rectifier.

Instead, the slow and fast manifold approach is selected. For the fast manifold, four internal current control loops guarantee the same dc current level in each three-phase rectifier and limit the short-circuit currents. For the output slow dynamics, an external cascaded output voltage control loop (Fig. 19.36b), measuring the voltage applied to the load, is the minimum.

For a straightforward design, given the much slower dynamics of the capacitor voltages compared to the input current, the PI current controllers are calculated as shown in Example 19.6, considering the capacitor voltage constant during a switching period, and $r_t = 1\,\Omega$ the intrinsic resistance of the transformer windings, overlap, and inductor l. From (19.45), $T_z = l/r_t = 0.044$ s. From (19.48), with the common assumptions, $T_p = 0.0066$ s ($p = 3$). These values guarantee a small overshoot ($\approx 5\%$) and a current rise time of approximately $T/3$.

To design the external output voltage-control loop, each current-controlled rectifier can be considered a voltage-controlled current source $i_{L_i}(s)/4$, since each half-wave rectifier current response will be much faster than the filter output voltage response. Therefore, in the equivalent circuit of Fig. 19.35b, the current source $i_{L_1}(s)$ substitutes the input inductor, yielding the transfer function $v_{c_2}(s)/i_{L_1}(s)$:

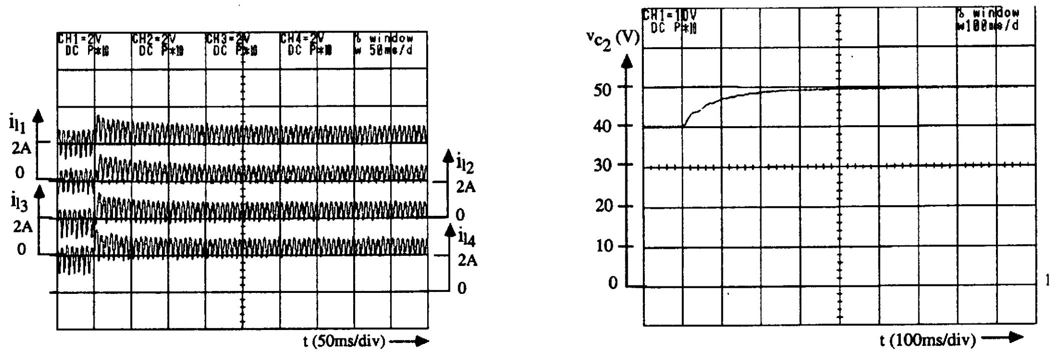
$$\frac{v_{c_2}(s)}{i_{L_1}(s)} = \frac{R_o}{C_2C_1L_2R_os^3 + C_1L_2s^2 + (C_2R_o + C_1R_o)s + 1} \tag{19.110}$$

Given the real pole ($p_1 = -6.7$) and two complex poles ($p_{2,3} = -6.65 \pm j140.9$) of (19.110), the PI voltage controller zero ($1/T_{zv} = p_1$) can be chosen with a value equal to the transfer function real pole. The integral gain T_{pv} can be determined using a root-locus analysis to determine the maximum gain, that still guarantees the stability of the closed loop controlled system. The critical gain for the PI was found to be $T_{zv}/T_{pv} \approx 0.4$, then $T_{pv} > 0.37$. The value $T_{pv} \approx 2$ was selected to obtain weak oscillations, together with almost no overshoot.

The dynamic and steady-state responses of the output currents of the four rectifiers (i_{l_1}, i_{l_2}, i_{l_3}, i_{l_4}) and the output voltage v_{c_2} were analyzed using a step input from 2 A to 2.5 A applied at $t = 1.1$ s, for the currents, and from 40 V to 50 V for the v_{c_2} voltage. The PI current controllers (Fig. 19.37) show good sharing of the total current, a slight overshoot ($\zeta = 0.7$) and response time 6.6 ms (T/p).

The open-loop voltage v_{c_2} presents a rise time of 0.38 s. The PI voltage controller (Fig. 19.38) shows a response time of 0.4 s no overshoot. The four three-phase half-wave rectifier output currents (i_{l_1}, i_{l_2}, i_{l_3}, and i_{l_4}) present nearly the same transient and steady-state values, with no very high current peaks. These results validate the assumptions made in the PI design.

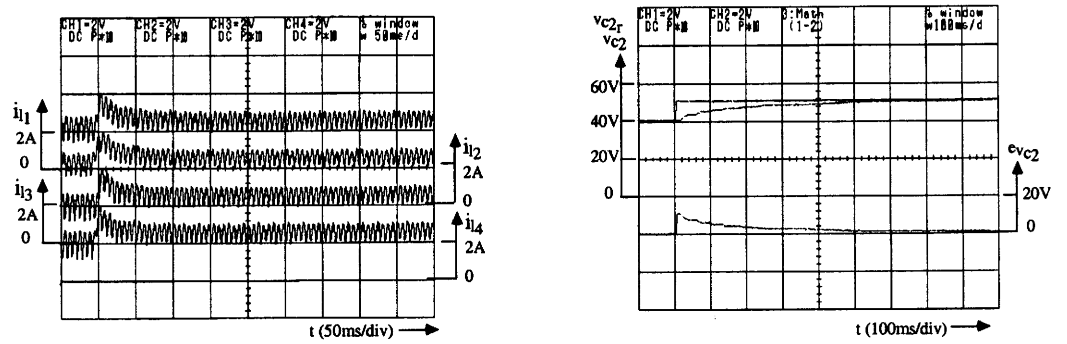
The closed-loop performance of the fixed-frequency sliding-mode controller (Fig. 19.39), shows that all the i_{l_1}, i_{l_2}, i_{l_3} and i_{l_4} currents are almost equal and have peak values only slightly higher than those obtained with the PI linear controllers. The output voltage presents a much faster response time (150 ms) than the PI linear controllers, negligible or no steady-state error, and no overshoot. From these waveforms it can be concluded that the sliding-mode controller provides a much more effective control of the rectifier, as the output voltage response time is much lower than the obtained with PI linear controllers, without significantly increasing the



a) i_{l1}, i_{l2}, i_{l3}, i_{l4} closed loop currents

b) open-loop output voltage v_{c_2}

FIGURE 19.37 PI current controller performance.



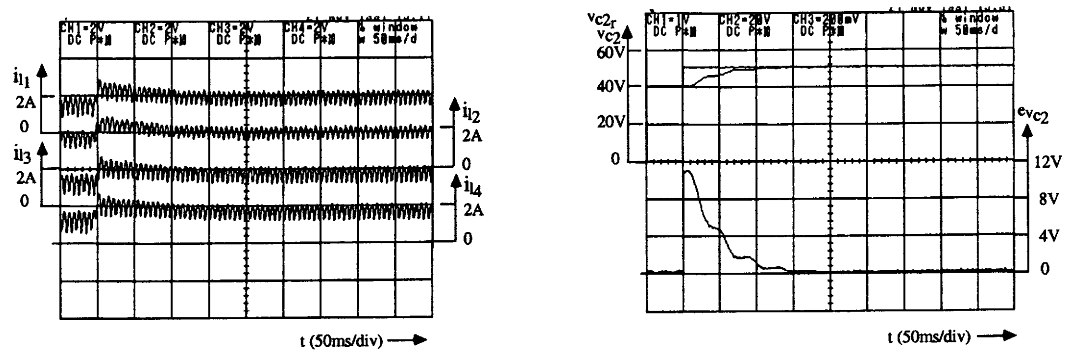
a) i_{l1}, i_{l2}, i_{l3}, i_{l4} closed loop currents

b) closed output voltage $v_{c_2}$and $e_{v_{c2}}$ output voltage error

FIGURE 19.38 PI voltage controller performance.

thyristor currents, overshoots, or costs. Furthermore, sliding mode is an elegant way to know the variables to be measured, and to design all the controller and the modulator electronics.

Example 19.13. Sliding-Mode Control of Pulse Width Modulation Audio Power Amplifiers. Linear audio power amplifiers can be astonishing, but have efficiencies as low as 15–20 with speech or music signals. To improve the efficiency of audio systems while preserving the quality, PWM switching power amplifiers, enabling the reduction of the power-supply cost, volume, and weight and compensating the efficiency loss of modern loudspeakers, are needed. Moreover, PWM amplifiers can provide a complete digital solution for audio power processing.



(a) (b)

FIGURE 19.39 Closed-loop constant-frequency sliding-mode controller performance.

For high-fidelity systems, PWM audio amplifiers must present flat passbands of at least 16 Hz–20 kHz (±0.05 dB), distortions less than 0.1 at the rated output power, fast dynamic response, and signal-to-noise ratios above 90 dB. This requires fast power semiconductors (usually MOSFET transistors), capable of switching at frequencies near 500 kHz and fast nonlinear control methods to provide the precise and timely control actions needed to accomplish the mentioned requirements and to eliminate the phase delays in the LC output filter and in the loudspeakers.

A low-cost PWM audio power amplifier, able to provide over 80 W to 8-Ω loads ($V_{dd} = 50$ V), can be obtained using a half-bridge power inverter (switching at $f_{PWM} \approx 450$ kHz), coupled to an output filter for high-frequency attenuation (Fig. 19.40). A low-sensitivity, doubly terminated passive ladder (double LC), low-pass filter using fourth-order Chebyshev approximation polynomials is selected, given its ability to meet, while minimizing the number of inductors, the following requirements: passband edge frequency 21 kHz, passband ripple 0.5 dB, stopband edge frequency 300 kHz, and 90 dB minimum attenuation in the stopband ($L_1 = 80$ µH $L_2 = 85$ µH; $C_1 = 1.7$ µF; $C_2 = 82$ nF; $R_2 = 8$ Ω; $r_1 = 0.47$ Ω).

Modeling the PWM Audio Amplifier

The two half-bridge switches must always be in complementary states, to avoid power supply internal short circuits. Their state can be represented by the time-dependent variable γ, which is $\gamma = 1$ when Q1 is on and Q2 is off, and is $\gamma = -1$ when Q1 is off and Q2 is on.

Neglecting switch delays, on state semiconductor voltage drops, auxiliary networks, and supposing small dead times, the half-bridge output voltage is $v_{PWM} = \gamma V_{dd}$. Considering the state variables and circuit components shown in Fig. 19.40, and modeling the loudspeaker load as a perturbation represented by the current i_o (ensuring robustness against the frequency dependent impedance of the speaker), the switched state-space model of the PWM audio amplifier is

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{L_1} \\ v_{c_1} \\ i_{L_2} \\ v_o \end{bmatrix} = \begin{bmatrix} -r_1/L_1 & -1/L_1 & 0 & 0 \\ 1/C_1 & 0 & -1/C_1 & 0 \\ 0 & -1/L_2 & 0 & -1/L_2 \\ 0 & 0 & 1/C_2 & 0 \end{bmatrix}\begin{bmatrix} i_{L_1} \\ v_{c_1} \\ i_{L_2} \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L_1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -1/C_2 \end{bmatrix}\begin{bmatrix} \gamma V_{dd} \\ i_o \end{bmatrix} \qquad (19.111)$$

This model will be used to define the output voltage v_o controller.

Sliding-Mode Control of the PWM Audio Amplifier

The filter output voltage v_o divided by the amplifier gain $(1/k_v)$ must follow a reference v_{o_r}. Defining the output error as $e_{v_o} = v_{o_r} - k_v v_o$, and also using its time derivatives $(e_\theta, e_\gamma, e_\beta)$ as a new state vector $\mathbf{e} = [e_{v_o}, e_\theta, e_\gamma, e_\beta]^{\mathrm{T}}$, the system equations, in the phase canonical (or controllability) form, can be written in the form

$$\frac{\mathrm{d}}{\mathrm{d}t}[e_{v_o}, e_\theta, e_\gamma, e_\beta]^{\mathrm{T}} = [e_\theta, e_\gamma, e_\beta, -f(e_{v_o}, e_\theta, e_\gamma, e_\beta) + p_e(t) - \gamma V_{dd}/C_1 L_1 C_2 L_2]^{\mathrm{T}} \qquad (19.112)$$

Sliding-mode control of the output voltage will enable a robust and reduced order dynamics, independent of semiconductors, power supply, and filter and load parameters. According to (19.75) and (19.112), the sliding surface is

$$\begin{aligned} &S(e_{v_o}, e_\theta, e_\gamma, e_\beta, t) \\ &= e_{v_o} + k_\theta e_\theta + k_\gamma e_\gamma + k_\beta e_\beta \\ &= v_{o_r} - k_v v_o + k_\theta \frac{\mathrm{d}(v_{o_r} - k_v v_o)}{\mathrm{d}t} \\ &\quad + k_\gamma \frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{\mathrm{d}(v_{o_r} - k_v v_o)}{\mathrm{d}t}\right) \\ &\quad + k_\beta \frac{\mathrm{d}}{\mathrm{d}t}\left[\frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{\mathrm{d}(v_{o_r} - k_v v_o)}{\mathrm{d}t}\right)\right] \\ &= 0 \end{aligned} \qquad (19.113)$$

In sliding mode, (19.113) confirms the amplifier gain $(v_o/v_{o_r} = 1/k_v)$. To obtain a stable system and the smallest possible response time t_r, a pole placement according to a third-order Bessel polynomial is used. Taking t_r inversely proportional to a frequency just below the lowest cut-off frequency (ω_1) of the double LC filter ($t_r \approx 2.8/\omega_1 \approx 2.8/(2\pi$ 21 kHz$) \approx 20$ µs) and

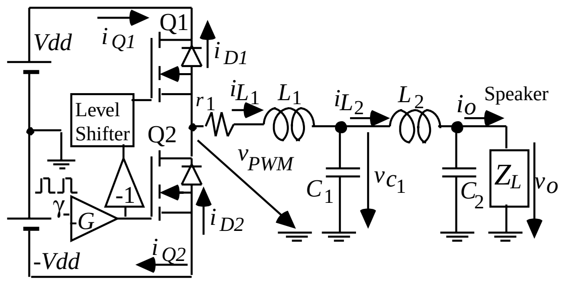


FIGURE 19.40 PWM audio amplifier with fourth-order Chebyshev low-pass output filter and loudspeaker load.

using (19.72c) with $m = 3$, the characteristic polynomial (19.114), verifying the Routh–Hurwitz criterion, is obtained

$$S(\mathbf{e}, s) = 1 + st_r + \frac{6}{15}(st_r)^2 + \frac{1}{15}(st_r)^3 \qquad (19.114)$$

From (19.91) the switching law for the control input at time t_k, $\gamma(t_k)$, must be

$$\gamma(t_k) = \operatorname{sgn}\{S(\mathbf{e}, t_k) + \varepsilon \operatorname{sgn}[S(\mathbf{e}, t_{k-1})]\} \qquad (19.115)$$

To ensure reaching and existence conditions, the power supply voltage V_{dd} must be greater than the maximum required mean value of the output voltage in a switching period $V_{dd} > \overline{(v_{\mathrm{PWMmax}})}$. The sliding-mode controller (Fig. 19.41) is obtained from (19.113), (19.114), and (19.115) with $k_\theta = t_r$, $k_\gamma = 6t_r^2/15$, $k_\beta = t_r^3/15$. The derivatives can be approximated by the block diagram of Fig. 19.41b, were h is the oversampling period.

Figure 19.42a shows the v_{PWM}, v_{o_r}, $v_o/10$, and the error $10 \times (v_{o_r} - v_o/10)$ waveforms for a 20-kHz sine input. The overall behavior is much better than the obtained with the sigma-delta controllers (Figs. 19.43 and 19.44) explained below for comparison purposes. There is no 0.5-dB loss or phase delay over the entire audio band; the Chebyshev filter behaves as a maximally flat filter, with higher stopband attenuation. Figure 19.42b shows v_{PWM}, v_{o_r}, and $10 \times (v_{o_r} - v_o/10)$ with a 1-kHz square input. There is almost no steady-state error and almost no overshoot on the speaker voltage v_o, attesting to the speed of response ($t \approx 20\ \mu\text{s}$ as designed, since, in contrast to Example 19.12, no derivatives were neglected). The stability, the system order reduction, and the sliding-mode controller usefulness for the PWM audio amplifier are also shown.

Sigma Delta Controlled PWM Audio Amplifier

Assume now the fourth-order Chebyshev low-pass filter, as an ideal filter removing the high-frequency content of the v_{PWM} voltage. Then, the v_{PWM} voltage can be

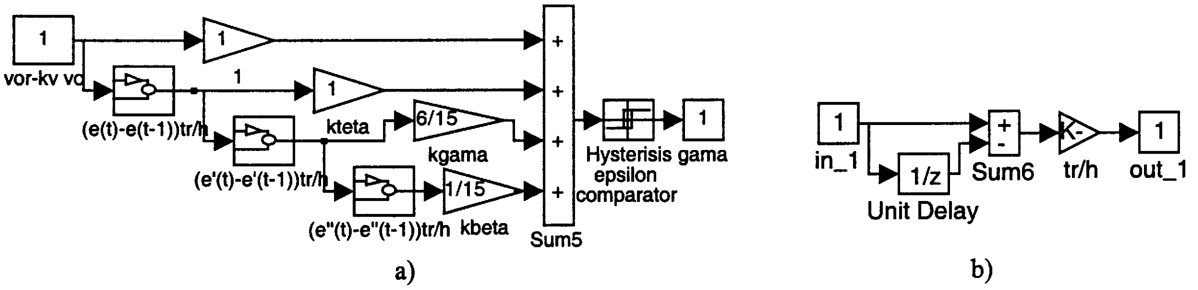


FIGURE 19.41 (a) Sliding-mode controller for the PWM audio amplifier; (b) implementation of the derivative blocks.

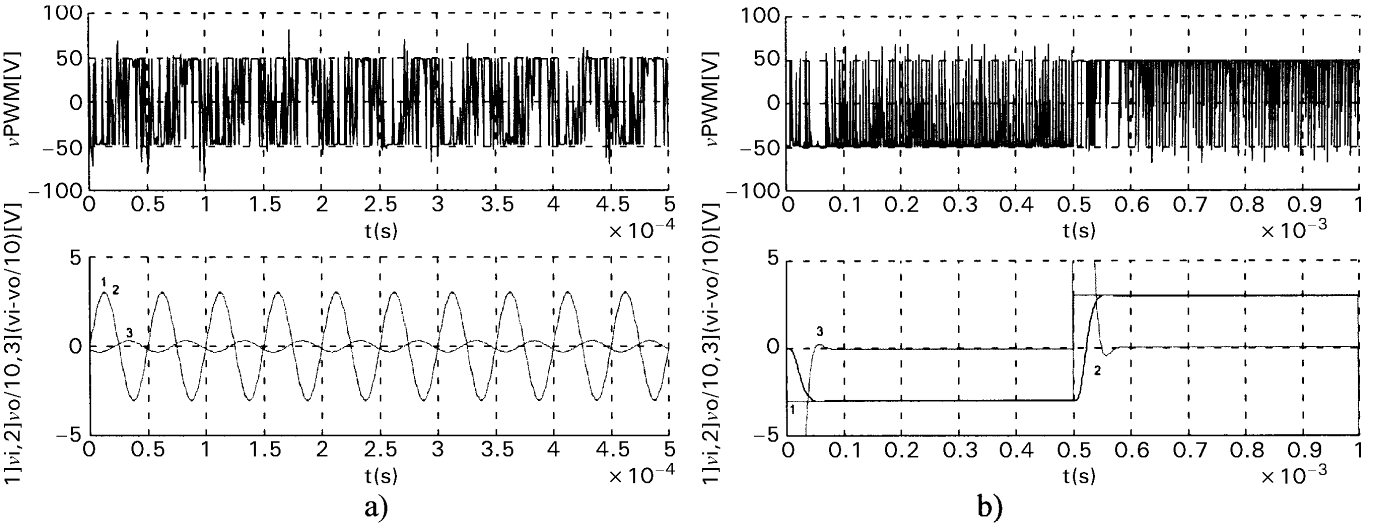


FIGURE 19.42 Sliding-mode controlled audio power amplifier performance (upper graphs show > v_{PWM}; lower graphs traces 1 show ($v_{o_r} \equiv v_i$), lower graphs traces 2 show > $v_o/10$, and lower graphs trace 3 show $10 \times (v_{o_r} - v_o/10)$), (a) response to a 20-kHz sine input, at 55 W output power; (b) response to 1 kHz square-wave input, at 100 W output power.

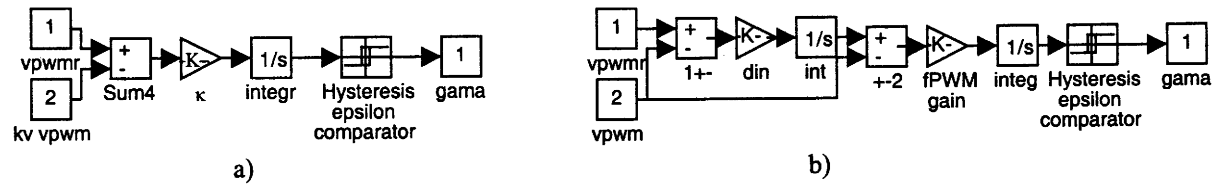


FIGURE 19.43 (a) First-order sigma-delta modulator; (b) second-order sigma-delta modulator.

considered the amplifier output. However, the discontinuous voltage $v_{PWM} = \gamma V_{dd}$ is not a state variable and cannot follow the almost continuous reference v_{PWM_r}. The new error variable $e_{vPWM} = v_{PWM_r} - k_v \gamma V_{dd}$ is always far from the zero value. Given this nonzero error, the approach outlined in Section 19.3.4 can be used. The switching law remains (19.115), but the new control law (19.116) is

$$S(e_{vPWM}, t) = \kappa \int (v_{PWM_r} - k_v \gamma V_{dd})\, \mathrm{d}t = 0 \qquad (19.116)$$

The κ parameter is calculated to impose the maximum switching frequency f_{PWM}. Since $\kappa \int_0^{1/2f_{PWM}} (v_{PWM_{r_{max}}} + k_v V_{dd}) \mathrm{d}t = 2\varepsilon$, we obtain

$$f_{PWM} = \kappa(v_{PWM_{r_{max}}} + k_v V_{dd})/4\varepsilon) \qquad (19.117)$$

Assuming that v_{PWM_r} is nearly constant over the switching period $1/f_{PWM}$, (19.116) confirms the amplifier gain, since $\overline{v_{PWM}} = v_{PWM_r}/k_v$.

Practical implementation of this control strategy can be done using an integrator with gain κ ($\kappa \approx 1800$), and a comparator with hysterisis ε($\varepsilon \approx 6$ mV), Fig. 19.43a. Such an arrangement is called a first-order sigma delta ($\Sigma\Delta$) modulator.

Figure 19.44a shows the v_{PWM}, v_{o_r}, and $v_o/10$ waveforms for a 20-kHz sine input. The overall behavior is as expected, because the practical filter and loudspeaker are not ideal, but notice the 0.5-dB loss and phase delay of the speaker voltage v_o, mainly due to the output filter and speaker inductance. In Fig. 19.44b, the v_{PWM}, v_{o_r}, $v_o/10$, and error $10 \times (v_{o_r} - v_o/10)$ for a 1-kHz square input are shown. Note the oscillations and steady-state error of the speaker voltage v_o, due to the filter dynamics and double termination.

A second-order sigma-delta modulator is a better compromise between circuit complexity and signal-to-quantization noise ratio. As the switching frequency of the two power MOSFET (Fig. 19.40) cannot be further increased, the second-order structure named "cascaded integrators with feedback" (Fig. 19.43b) was selected, and designed to eliminate the step response overshoot found in Fig. 19.44b.

Figure 19.45b, for 1-kHz square input, shows much less overshoot and oscillations than Fig. 19.44b. However, the v_{PWM}, v_{o_r}, and $v_o/10$ waveforms for a 20-kHz sine input presented in Fig. 19.45a show increased output voltage loss, compared to the first-order sigma-delta modulator, since the second-order modulator was designed to eliminate the v_o output voltage ringing (therefore reducing the amplifier band-

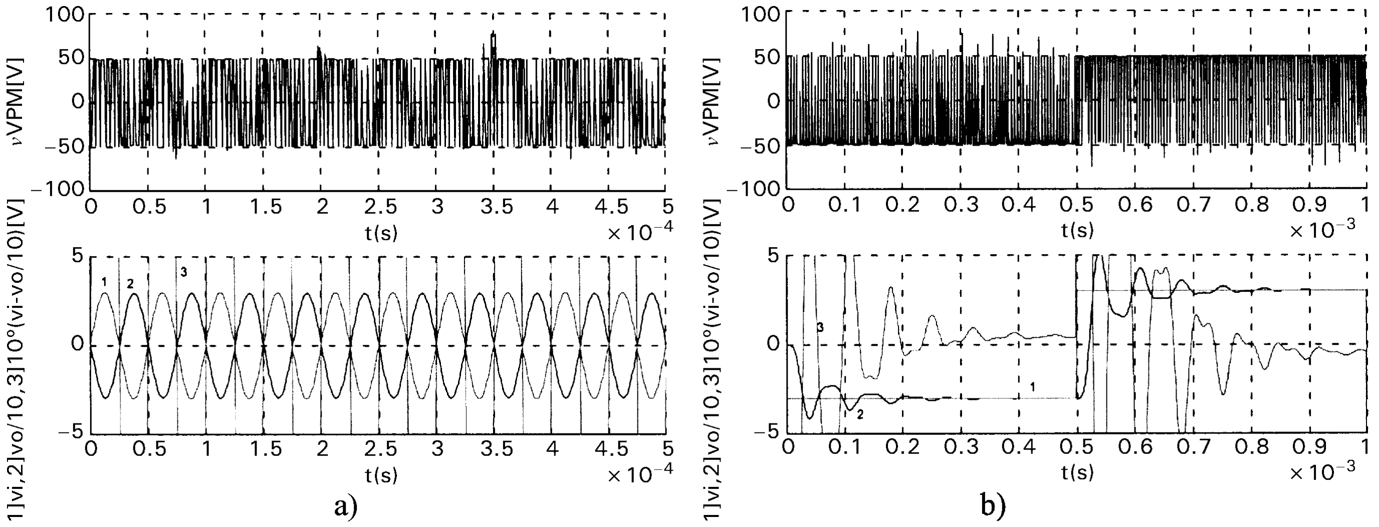


FIGURE 19.44 First-order sigma delta audio amplifier performance (upper graphs v_{PWM}; lower graphs trace 1, ($v_{o_r} \equiv v_i$); trace 2, $v_o/10$; and trace 3, $10 \times (v_{o_r} - v_o/10)$); (a) response to 20-kHz sine input, at 55 W output power; (b) response to 1 kHz square wave input, at 100 W output power.

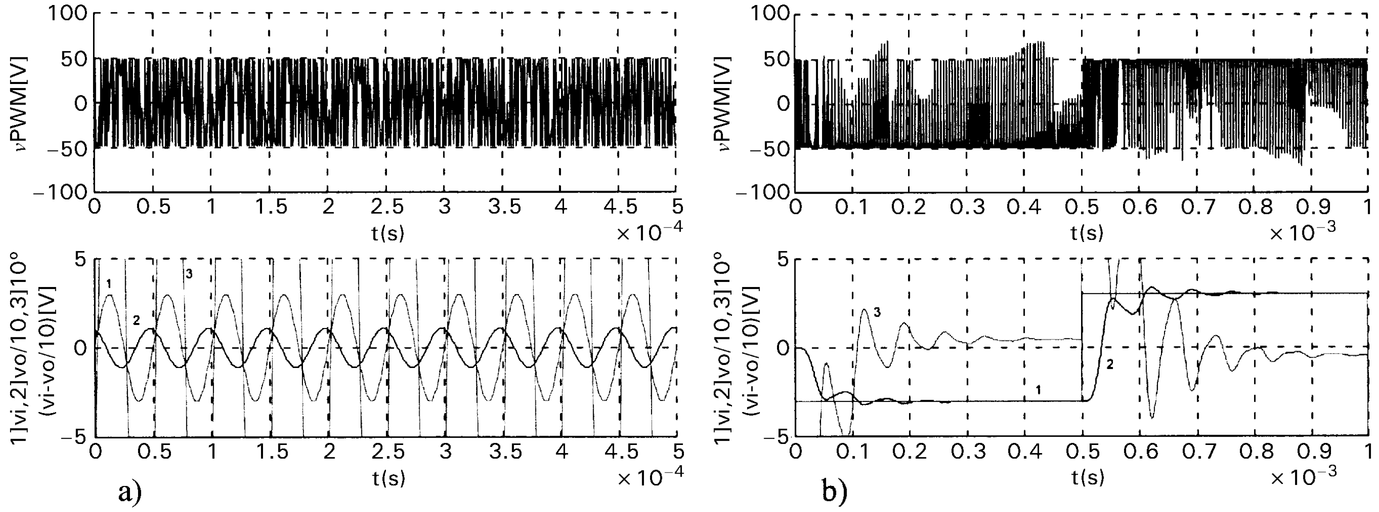


FIGURE 19.45 Second-order sigma delta audio amplifier performance (upper graphs v_{PWM}; lower graphs trace 1, ($v_{o_r} \equiv v_i$); lower graphs trace 2, $v_o/10$; and lower graphs trace 3, $10 \times (v_{o_r} - v_o/10)$); (a) response to a 20-kHz sine input, at 55 W output power; (b) response to 1-kHz square wave input, at 100 W output power.

width). The obtained performances with these and other sigma-delta structures are inferior to the sliding-mode performances (Fig. 19.43). Sliding mode brings definite advantages as the system order is reduced, flatter passbands are obtained, power supply rejection ratio is increased, and the nonlinear effects, together with the frequency-dependent phase delays, are cancelled out.

Example 19.14. Sliding-Mode Control of Near-Unity Power-Factor PWM Rectifiers. Boost-type voltage-sourced three-phase rectifiers (Fig. 19.46) are multiple-input, multiple-output (MIMO) systems capable of bidirectional power flow, near unity power factor operation, and almost sinusoidal input currents, and can behave as ac-dc power supplies or power factor compensators.

The fast power semiconductors used (usually MOSFETs or IGBTs), can switch at frequencies much higher than the mains frequency, enabling the voltage controller to provide an output voltage with fast dynamic response.

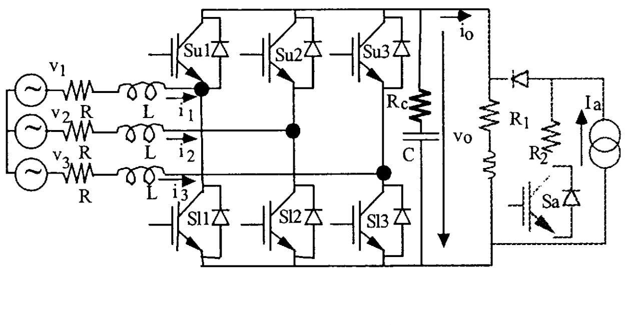


FIGURE 19.46 Voltage sourced PWM rectifier with IGBTs and test load.

Modeling the PWM Boost Rectifier

Neglecting switch delays and dead times, the states of the switches of the kth inverter leg (Fig. 19.46) can be represented by the time dependent nonlinear variables γ_k, defined as

$$\gamma_k = \begin{cases} 1 \rightarrow \text{if } \mathrm{Su}_k \text{ is on and } \mathrm{Sl}_k \text{ is off} \\ 0 \rightarrow \text{if } \mathrm{Su}_k \text{ is off and } \mathrm{Sl}_k \text{ is on} \end{cases} \tag{19.118}$$

Consider the displayed variables of the circuit (Fig. 19.46), where L is the value of the boost inductors, R their resistance, C the value of the output capacitor, and R_c its equivalent series resistance (ESR). Neglecting semiconductor voltage drops, leakage currents, and auxiliary networks, the application of Kirchhoff laws (taking the load current i_o as a time-dependent perturbation) yields the following switched state-space model of the boost rectifier:

$$\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_o \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & 0 & 0 & \frac{-2\gamma_1+\gamma_2+\gamma_3}{3L} \\ 0 & \frac{-R}{L} & 0 & \frac{-2\gamma_2+\gamma_3+\gamma_1}{3L} \\ 0 & 0 & \frac{-R}{L} & \frac{-2\gamma_3+\gamma_1+\gamma_2}{3L} \\ A_{41} & A_{42} & A_{43} & A_{44} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L} & 0 & 0 \\ \frac{\gamma_1 R_c}{L} & \frac{\gamma_2 R_c}{L} & \frac{\gamma_3 R_c}{L} & \frac{-1}{C} & -R_c \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_o \\ \frac{di_o}{dt} \end{bmatrix} \tag{19.119}$$

where

$$A_{41} = \gamma_1\left(\frac{1}{C} - \frac{RR_c}{L}\right); A_{42} = \gamma_2\left(\frac{1}{C} - \frac{RR_c}{L}\right);$$

$$A_{43} = \gamma_3\left(\frac{1}{C} - \frac{RR_c}{L}\right);$$

$$A_{44} = \frac{-2R_c(\gamma_1(\gamma_1 - \gamma_2) + \gamma_2(\gamma_2 - \gamma_3) + y_3(\gamma_3 - \gamma_1))}{3L}$$

Since the input voltage sources have no neutral connection, the preceding model can be simplified, eliminating one equation. Using the relationship (19.120) between the fixed frames x_{1-2-3} and $x_{\alpha-\beta}$, in (19.119), the state space model (19.121), in the $\alpha-\beta$ frame, is obtained

$$\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} \sqrt{2/3} & 0 \\ -\sqrt{1/6} & \sqrt{1/2} \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{19.120}$$

$$\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \\ v_o \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & 0 & \frac{-\gamma_\alpha}{L} \\ 0 & \frac{-R}{L} & \frac{-\gamma_\beta}{L} \\ A^\alpha_{31} & A^\alpha_{32} & A^\alpha_{33} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 \\ 0 & \frac{1}{L} & 0 & 0 \\ \frac{\gamma_\alpha R_c}{L} & \frac{\gamma_\beta R_c}{L} & \frac{-1}{C} & -R_c \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ i_o \\ \frac{di_o}{dt} \end{bmatrix} \tag{19.121}$$

where

$$A^\alpha_{31} = \gamma_\alpha\left(\frac{1}{D} - \frac{RR_c}{L}\right); A^\alpha_{32} = \gamma_\beta\left(\frac{1}{C} - \frac{RR_c}{L}\right);$$

$$A^\alpha_{33} = \frac{-R_c(\gamma^2_\alpha + \gamma^2_\beta)}{L}$$

Sliding-Mode Control of the PWM Rectifier

The model (19.121) is nonlinear and time variant. Applying the Park transformation (19.122), using a frequency ω rotating reference frame synchronized with the mains (with the q component of the supply voltages equal to zero), the nonlinear, time-invariant model (19.123) is written:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{19.122}$$

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ v_o \end{bmatrix} = \begin{bmatrix} \frac{-R}{L} & \omega & \frac{-\gamma_d}{L} \\ -\omega & \frac{-R}{L} & \frac{-\gamma_q}{L} \\ A^d_{31} & A^d_{32} & A^d_{33} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 \\ 0 & \frac{1}{L} & 0 & 0 \\ \frac{\gamma_d R_c}{L} & \frac{\gamma_q R_c}{L} & \frac{-1}{C} & -R_c \end{bmatrix} \begin{bmatrix} v_d \\ v_q \\ i_o \\ \frac{di_o}{dt} \end{bmatrix} \tag{19.123}$$

where

$$A^d_{31} = \gamma_d\left(\frac{1}{C} - \frac{RR_c}{L}\right); A^d_{32} = \gamma_q\left(\frac{1}{C} - \frac{RR_c}{L}\right);$$

$$A^d_{33} = \frac{-R_c(\gamma^2_d + \gamma^2_q)}{L}$$

This state-space model can be used to obtain the feedback controllers for the PWM boost rectifier. Considering the output voltage v_o and the i_q current as the controlled outputs and γ_d, γ_q the control inputs (MIMO system), the input–output linearization of (19.123), gives the state-space equations in the controllability canonical form (19.124):

$$\begin{aligned} \frac{di_q}{dt} &= -\omega i_d - \frac{R}{L} i_q - \frac{\gamma_q}{L} v_o + \frac{1}{L} v_q \\ \frac{dv_o}{dt} &= \theta \\ \frac{d\theta}{dt} &= -\frac{R + R_c(\gamma^2_d + \gamma^2_q)}{L}\theta - \frac{\gamma^2_d + \gamma^2_q}{LC} v_o \\ &\quad + \frac{\gamma_d v_d + \gamma_q v_q}{LC} - \frac{Ri_o}{LC} - \left(\frac{1}{C} + \frac{RR_c}{L}\right)\frac{di_o}{dt} \\ &\quad + \omega\left(\frac{1}{C} - \frac{RR_c}{L}\right)\left(\gamma_d i_q - \gamma_q i_d\right) - R_c \frac{d^2 i_o}{dt^2} \end{aligned} \tag{19.124}$$

where

$$\theta = \left(\frac{1}{C} - \frac{RR_c}{L}\right)(\gamma_d i_d + \gamma_q i_q) - \frac{R_c(\gamma_d^2 + \gamma_q^2)}{L} v_o + \frac{R_c}{L}(\gamma_d v_d + \gamma_q v_q) - \frac{i_o}{C} - R_c \frac{di_o}{dt}$$

Using the rectifier overall power balance (from Tellegen's theorem, the converter is conservative, e.g. the power delivered to the load or dissipated in the converter parasitic elements equals the input power), and neglecting the switching and output capacitor losses, $v_d i_d + v_q i_q = v_o i_o + Ri_d^2$. Supposing unity power factor ($i_{q_r} \approx 0$), and the output v_o in steady state, $\gamma_d i_d + \gamma_q i_q \approx i_o$, $v_d = \sqrt{3} V_{RMS}$, $v_q = 0$, $\gamma_q \approx v_q / v_o$, $\gamma_d \approx (v_d - Ri_d)/v_o$. Then, from (19.124) and (19.75), the following two sliding surfaces can be derived:

$$S_q(e_{i_q}, t) = k_{e_{iq}}(i_{qr} - i_q) = 0 \tag{19.125}$$

$$S_d(e_{v_o}, e_\theta, t); \approx \left[\beta^{-1}(v_{o_r} - v_o) + \frac{dv_{o_r}}{\mathrm{d}t} + \frac{1}{C} i_o + R_c \frac{di_o}{\mathrm{d}t}\right] \times \frac{LC}{L - CRR_c} \frac{v_o}{\sqrt{3} V_{RMS} - Ri_d} - i_d = i_{d_r} - i_d = 0 \tag{19.126}$$

where β^{-1} is the time constant of the desired first-order response of output voltage v_o ($\beta \gg T > 0$). For the synthesis of the closed-loop control system, notice that the terms of (19.126) inside the square brackets can be assumed as the i_d reference current i_{d_r}. Furthermore, from (19.125) and (19.126) it is seen that current control loops for i_d and i_q are needed. Considering (19.122) and (19.120), the two sliding surfaces can be written

$$S_\alpha(e_{i_\alpha}, t) = i_{\alpha_r} - i_\alpha = 0 \tag{19.127a}$$

$$S_\beta(e_{i_\beta}, t) = i_{\beta_r} - i_\beta = 0 \tag{19.127b}$$

The switching laws relating the sliding surfaces (19.127) with the switching variables γ_k are

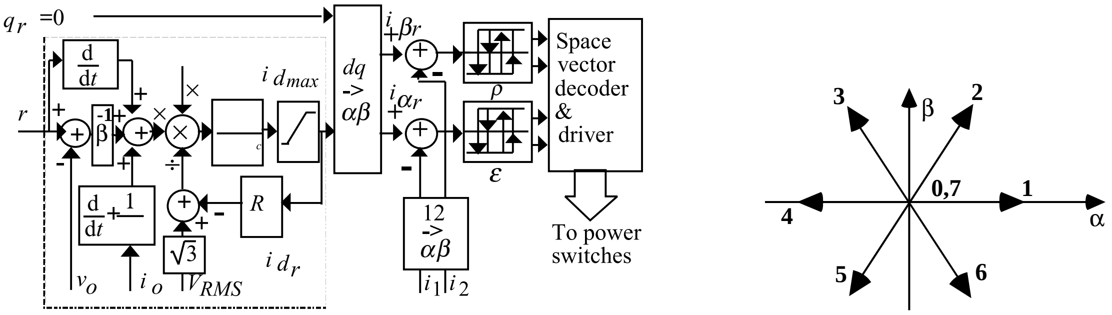
$$\begin{cases} \text{If } S_{\alpha,\beta}(e_{i_{\alpha,\beta}}, t) > \varepsilon \text{ then } i_{\alpha,\beta_r} > i_{\alpha,\beta} \text{ hence choose } \gamma_k \\ \quad \text{to increase the } i_{\alpha,\beta} \text{ current} \\ \text{If } S_{\alpha,\beta}(e_{i_{\alpha,\beta}}, t) < -\varepsilon \text{ then } i_{\alpha,\beta_r} < i_{\alpha,\beta} \text{ hence choose } \gamma_k \\ \quad \text{to decrease the } i_{\alpha,\beta} \text{ current} \end{cases} \tag{19.128}$$

The practical implementation of this switching strategy could be accomplished using three independent two-level hysteresis comparators. However, this might introduce limit cycles as only two line currents are independent. Therefore, the control laws (19.127) can be implemented using the block diagram of Fig. 19.47a, with d, q–α, β (from (19.122)) and $1, 2$–α, β (from (19.120)) transformations and two three-level hysteretic comparators with equivalent hysterisis ε and ρ to limit the maximum switching frequency. A limiter is included to bound the i_d reference current to $i_{d\max}$, keeping the input line currents within a safe value. This helps to eliminate the nonminimum-phase behavior (outside sliding mode) when large transients are present, while providing short-circuit-proof operation.

α–β Space Vector Current Modulator

Depending on the values of γ_k, the bridge rectifier leg output voltages can assume only eight possible distinct states represented as voltage vectors in the α–β reference frame (Fig. 19.47b), for sources with isolated neutral.

With only two independent currents, two three-level hysterisis comparators, for the current errors, must be used in order to accurately select all eight available voltage vectors. Each three-level comparator can be obtained by summing the outputs of two comparators with two levels each. One of these two comparators ($\delta_{L\alpha}$, $\delta_{L\beta}$) has a wide hysterisis width and the other ($\delta_{N\alpha}$, $\delta_{N\beta}$) has a narrower hysterisis width. The hysterisis bands are represented by ε and ρ. Table 19.2 represents all possible output combinations of the resulting four two-level



a) b)

FIGURE 19.47 (a) Sliding-mode PWM controller–modulator for the unity power factor three-phase PWM rectifier; (b) α–β space vector representation of the PWM bridge rectifier leg voltages.

TABLE 19.2 Two-level and three-level comparator results, showing corresponding vector choice, corresponding γ_K and vector $\alpha\beta$ component voltages. Vectors are mapped in Fig. 19.47b

$\delta_{L\alpha}$	$\delta_{N\alpha}$	$\delta_{L\beta}$	$\delta_{N\beta}$	δ_α	δ_β	**Vector**	γ_1	γ_2	γ_3	v_α	v_β
−0.5	−0.5	−0.5	−0.5	−1	−1	**2**	1	1	0	$v_o/\sqrt{6}$	$v_o/\sqrt{2}$
0.5	−0.5	−0.5	−0.5	0	−1	**2**	1	1	0	$v_o/\sqrt{6}$	$v_o/\sqrt{2}$
0.5	0.5	−0.5	−0.5	1	−1	**3**	0	1	0	$-v_o/\sqrt{6}$	$v_o/\sqrt{2}$
−0.5	0.5	−0.5	−0.5	0	−1	**3**	0	1	0	$-v_o/\sqrt{6}$	$v_o/\sqrt{2}$
−0.5	0.5	0.5	−0.5	0	0	**0 or 7**	0 or 1	0 or 1	0 or 1	0	0
0.5	0.5	0.5	−0.5	1	0	**4**	0	1	1	$-\sqrt{2/3}\,v_o$	0
0.5	−0.5	0.5	−0.5	0	0	**0 or 7**	0 or 1	0 or 1	0 or 1	0	0
−0.5	−0.5	0.5	−0.5	−1	0	**1**	1	0	0	$\sqrt{2/3}\,v_o$	0
−0.5	−0.5	0.5	0.5	−1	1	**6**	1	0	1	$v_o/\sqrt{6}$	$-v_o/\sqrt{2}$
0.5	−0.5	0.5	0.5	0	1	**6**	1	0	1	$v_o/\sqrt{6}$	$-v_o/\sqrt{2}$
0.5	0.5	0.5	0.5	1	1	**5**	0	0	1	$-v_o/\sqrt{6}$	$-v_o/\sqrt{2}$
−0.5	0.5	0.5	0.5	0	1	**5**	0	0	1	$-v_o/\sqrt{6}$	$-v_o/\sqrt{2}$
−0.5	0.5	−0.5	0.5	0	0	**0 or 7**	0 or 1	0 or 1	0 or 1	0	0
0.5	0.5	−0.5	0.5	1	0	**4**	0	1	1	$-\sqrt{2/3}\,v_o$	0
0.5	−0.5	−0.5	0.5	0	0	**0 or 7**	0 or 1	0 or 1	0 or 1	0	0
−0.5	−0.5	−0.5	0.5	−1	0	**1**	1	0	0	$\sqrt{2/3}\,v_o$	0

comparators, their sums giving the two three-level comparators (δ_α, δ_β), plus the voltage vector needed to accomplish the current tracking strategy $(i_{\alpha,\beta r} - i_{\alpha,\beta}) = 0$ (ensuring $(i_{\alpha,\beta_T} - i_{\alpha,\beta}) \times d(i_{\alpha,\beta_T} - i_{\alpha,\beta})/\mathrm{d}t < 0$), plus the γ_k variables and the α–β voltage components.

From the analysis of the PWM boost rectifier it is concluded that, if, for example, the voltage vector 2 is applied ($\gamma_1 = 1$, $\gamma_2 = 1$, $\gamma_3 = 0$), in boost operation, the currents i_α and i_β will both decrease. Oppositely, if the voltage vector 5 ($\gamma_1 = 0$, $\gamma_2 = 0$, $\gamma_3 = 1$) is applied, the currents i_α and i_β will both increase. Therefore, vector 2 should be selected when both i_α and i_β currents are above their respective references, that is for $\delta_\alpha = -1$, $\delta\beta = -1$, whereas vector 5 must be chosen when both i_α and i_β currents are under their respective references, or for $\delta_\alpha = 1$, $\delta_\beta = 1$. Nearly all the outputs of Table 19.2 can be filled using this kind of reasoning.

The cases where $\delta_\alpha = 0$, $\delta_\beta = -1$, the vector is selected upon the value of the i_α current error (if $\delta_{L\alpha} > 0$ and $\delta_{N\alpha} < 0$ then vector 2, if $\delta_{L\alpha} < 0$ and $\delta_{N\alpha} < 0$ then vector 3). When $\delta_\alpha = 0$, $\delta_\beta = 1$, if $\delta_{L\alpha} > 0$ and $\delta_{N\alpha} < 0$ then vector 6, else if $\delta_{L\alpha} < 0$ and $\delta_{N\alpha} > 0$ then vector 5. The vectors 0 and 7 are selected in order to minimize the switching frequency (if two of the three upper switches are on, then vector 7, otherwise vector 0). The space vector decoder can be stored in a look-up table (or in an EPROM) whose inputs are the four two level comparator outputs and the logic result of the operations needed to select between vectors 0 and 7.

PI Output Voltage Control of the Current-Mode PWM Rectifier

Using the α–β current mode hysteresis modulators to enforce the i_d and i_q currents to follow their reference values, i_{d_r}, i_{q_r} (the values of L and C are such that the i_d and i_q currents usually exhibit a very fast dynamics compared to the slow dynamics of v_o), a first-order model (19.129) of the rectifier output voltage can be obtained from (19.124).

$$\begin{aligned}\frac{dv_o}{dt} = {} & \left(\frac{1}{C} - \frac{RR_c}{L}\right)(\gamma_d i_{d_r} + \gamma_q i_{q_r}) \\ & - \frac{R_c(\gamma_d^2 + \gamma_q^2)}{L} v_o + \frac{R_c}{L}(\gamma_d v_d + \gamma_q v_q) \\ & - \frac{i_o}{C} - R_c \frac{\mathrm{d}i_l}{\mathrm{d}t}\end{aligned} \tag{19.129}$$

Assuming now a pure resistor load $R_1 = v_o/i_o$, and a mean delay T_d between the i_d current and the reference i_{d_r}, continuous transfer functions result for the i_d current ($i_d = i_{d_r}(1 + sT_d)^{-1}$) and for the v_o voltage ($v_o = k_A i_d/(1 + sk_B)$ with k_A and k_B obtained from (19.129). Therefore, using the same approach as Examples 19.6, 19.8, and 19.11, a linear PI regulator, with gains K_p and K_i (19.130), sampling the error between the output voltage reference v_{o_r} and the output v_o, can be designed to provide a voltage proportional (k_I) to the reference current i_{d_r} ($i_{d_r} = (K_p + K_i/s)k_I(v_{o_r} - v_o)$).

$$\begin{aligned} K_p &= \frac{R_1 + R_c}{4\zeta^2 T_d R_1 K_1 \gamma_d \left(\dfrac{1}{C} - \dfrac{RR_c}{L}\right)} \\ K_i &= \frac{\dfrac{R_c(\gamma_d^2 + \gamma_q^2)}{L} + \dfrac{1}{R_1 C}}{4\zeta^2 T_d K_I \gamma_d \left(\dfrac{1}{C} - \dfrac{RR_c}{L}\right)} \end{aligned} \tag{19.130}$$

These PI regulator parameters depend on the load resistance R_1, on the rectifier parameters (C, R_c, L, R), on the rectifier operating point γ_d, on the mean delay T_d, and on the required damping factor ζ. Therefore, the expected response can only be obtained with nominal load and input voltages, the line current dynamics depending on the K_p and K_i gains.

Results (Fig. 19.48) obtained with the values $V_{RMS} \approx 70$ V, $L \approx 1.1$ mH, $R \approx 0.1\ \Omega$, $C \approx 2000\ \mu$F with equivalent series resistance ESR $\approx 0.1\ \Omega$ ($R_c \approx 0.1\ \Omega$), $R_1 \approx 25\ \Omega$, $R_2 \approx 12\ \Omega$, $\beta = 0.0012$, $K_p = 1.2$, $K_i = 100$, $k_I = 1$, show that the α–β space vector current modulator ensures the current tracking needed (Fig. 19.48). The v_o step response reveals a faster sliding-mode controller and the correct design of the current mode/PI controller parameters. The robustness property of the sliding-mode controlled output v_o, compared to the current mode/PI, is shown in Fig. 19.49.

Example 19.15. Sliding-Mode Controllers for Multilevel Inverters. Multilevel inverters (Fig. 19.50) are the converters of choice for high-voltage, high-power dc–ac or ac–ac (with dc link) applications, as the active semiconductors (usually gate turn-off thyristors (GTO), or IGBT transistors) of n-level power conversion systems, must withstand only a fraction (normally $U_{cc}/(n-1)$) of the total supply voltage U_{cc}. Moreover, the output voltage of multilevel converters, being staircase-like waveforms with n steps, features lower harmonic distortion compared to the two-level waveforms with the same switching frequency.

The advantages of multilevel converters are paid into the price of the capacitor supply voltage dividers (Fig. 19.51) and voltage equalization circuits, or into the cost of extra power supply arrangements (Fig. 19.51c). This example shows how to extend the two-level switching law (19.81) to n-level converters, and how to equalize the voltage of the capacitive dividers.

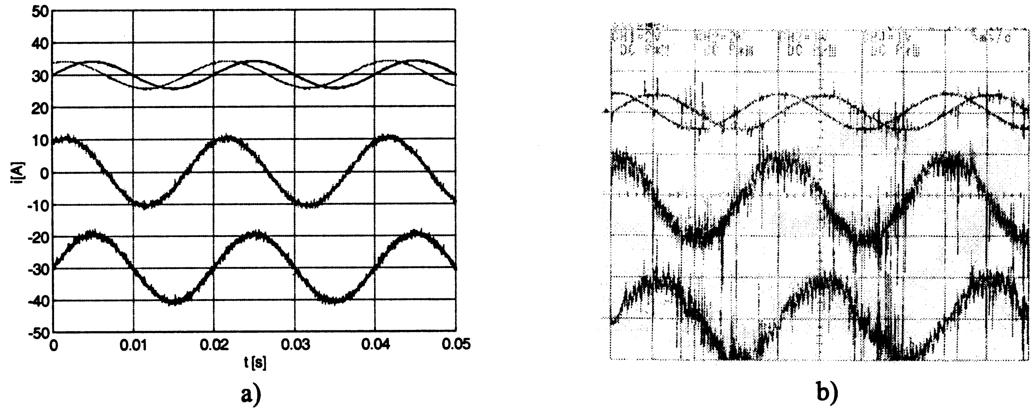
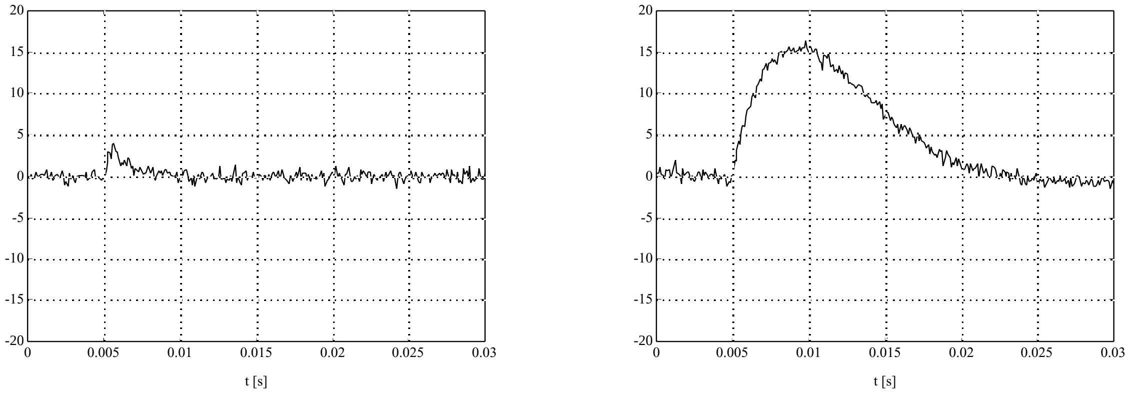


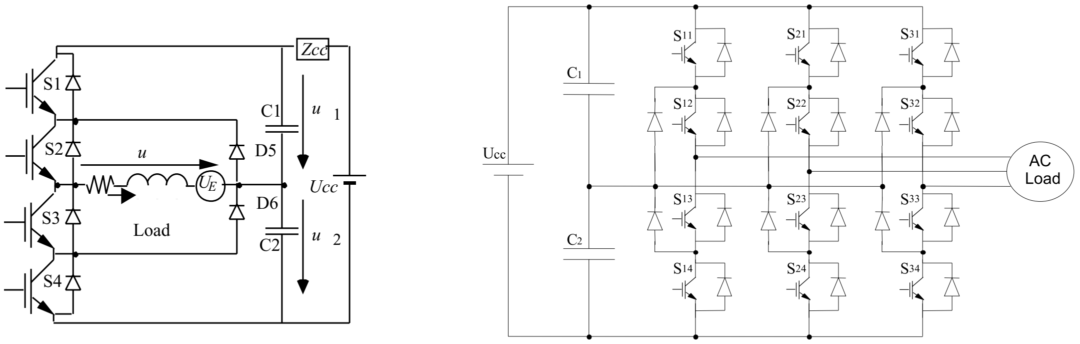
FIGURE 19.48 α–β space vector current modulator operation at near unity power factor; (a) simulation result ($i_{1r}+30$; $i_{2r}+30$; $2 \times i_2 - 30$; (b) experimental result ($1 \rightarrow i_{1r}$, $2 \rightarrow i_{2r}$ (10 A/div); $3 \rightarrow i_1$, $4 \rightarrow i_2$ (5 A/div)).



a) - ${}_r$[V] with sliding mode control

b) - ${}_r$[V] with current mode/PI control

FIGURE 19.49 Transition from rectifier to inverter operation (i_o from 8 A to −8 A) obtained by switching off IGBT Sa and using $I_a = 16$ A (Fig. 19.46).



a) b)

FIGURE 19.50 (a) Single phase, neutral-clamped, three-level inverter with IGBTs; (b) three-phase, neutral-clamped, three-level inverter.

Considering single-phase three level inverters (Fig. 19.50a), open-loop control of the output voltage can be made using three-level SWPWM. The two-level modulator, seen in Example 19.9, can be easily extended (Fig. 19.52a) to generate the γ_{III} command (Fig. 19.52b) to three-level inverter legs, from the two-level γ_{II} signal, using the following relation:

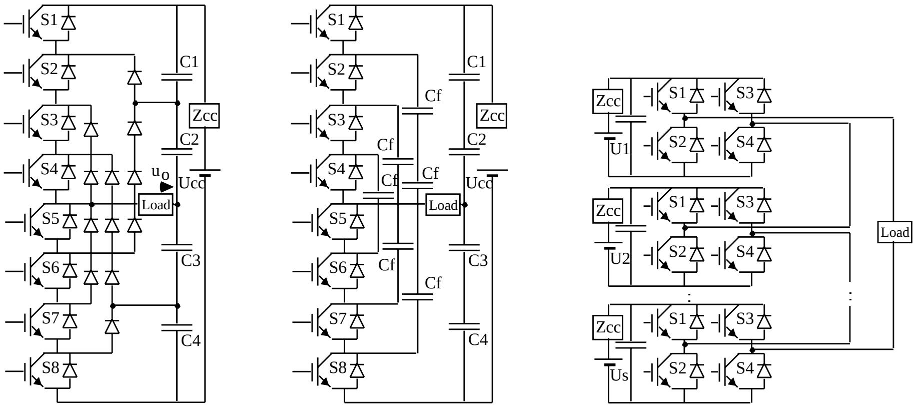
$$\gamma_{\mathrm{III}} = \gamma_{\mathrm{II}(m_i, \sin(\omega t) - \mathrm{sgn}(m_i \sin(\omega t))/2 - r(t)/2)} - 1/2 + \mathrm{sgn}(m_i \sin(\omega t))/2 \qquad (19.131)$$

The required three-level SWPWM modulators for the output voltage synthesis seldom take into account the semiconductors and the capacitor voltage divider nonideal characteristics. Consequently, the capacitor voltage divider tends to drift, one capacitor being overcharged, the other discharged, and an asymmetry appears in the currents of the power supply. A steady-state error in the output voltage can also be present. Sliding-mode control can provide the optimum switching timing between all the converter levels, together with robustness to supply voltage disturbances, semiconductor nonidealities, and load parameters.

Sliding-Mode Switching Law

For a variable-structure system where the control input $u_i(t)$ can present n levels, consider the n values of the integer variable γ, being $-(n-1)/2 \leq \gamma \leq (n-1)/2$ and $u_i(t) = \gamma U_{cc}/(n-1)$, dependent on the topology and on the conducting semiconductors. To ensure the sliding-mode manifold invariance condition (19.76) and the reaching mode behavior, the switching strategy $\gamma(t_{k+1})$ for the time instant t_{k+1}, considering the value of $\gamma(t_k)$ must be

$$\gamma(t_{k+1}) = \begin{cases} \gamma(t_k) + 1 & \text{if } S(e_{x_i}, t) > \varepsilon \wedge \dot{S}(e_{x_i}, t) > \\ & \varepsilon \wedge \gamma(t_k) < (n-1)/2 \\ \gamma(t_k) - 1 & \text{if } S(e_{x_i}, t) < -\varepsilon \wedge \dot{S}(e_{x_i}, t) < \\ & -\varepsilon \wedge \gamma(t_k) > -(n-1)/2 \end{cases} \qquad (19.132)$$



a) b) c)

FIGURE 19.51 (a) Five-level ($n = 5$) diode clamped inverter with IGBTs; (b) five-level ($n = 5$) flying capacitor converter; (c) multilevel converter based on cascaded full bridge inverters.

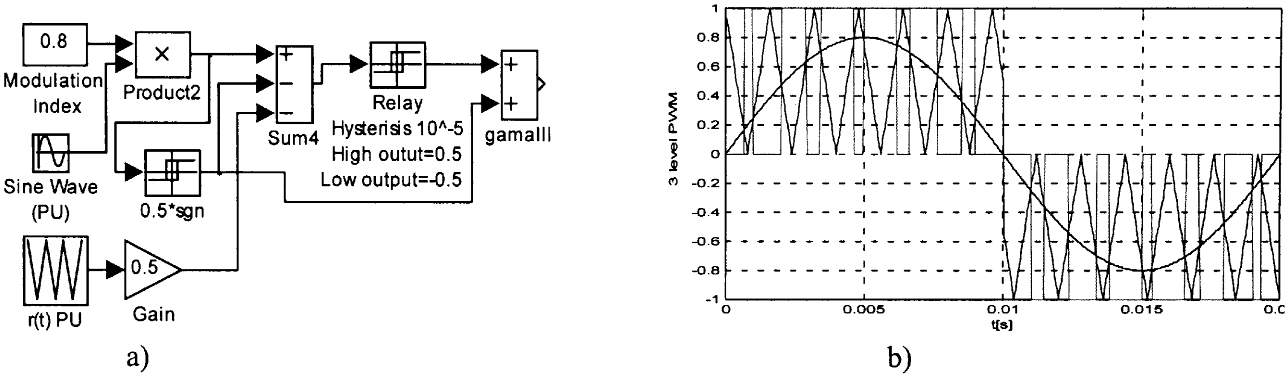

0.8
Modulation Index
Product2
Sine Wave (PU)
0.5*sgn
r(t) PU
0.5
Gain
Sum4
Relay
Hysterisis 10^-5
High outut=0.5
Low output=-0.5
gamaIII
a)
3 level PWM
t[s]
0
0.005
0.01
0.015
1
0.8
0.6
0.4
0.2
-0.2
-0.4
-0.6
-0.8
-1
b)

FIGURE 19.52 (a) Three-level SWPWM modulator schematic; (b) main three-level SWPWM signals.

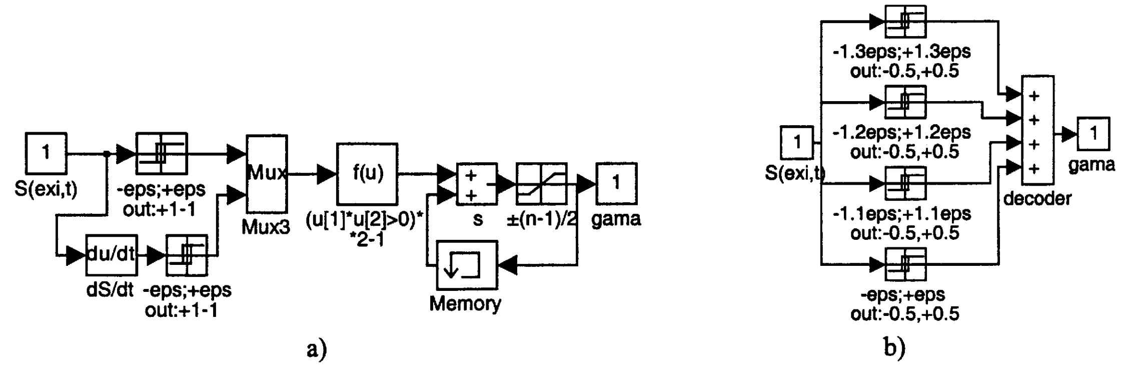

1
S(exi,t)
-eps;+eps
out:+1-1
Mux
Mux3
f(u)
(u[1]*u[2]>0)*
*2-1
s
±(n-1)/2
1
gama
du/dt
dS/dt
-eps;+eps
out:+1-1
Memory
a)
-1.3eps;+1.3eps
out:-0.5,+0.5
-1.2eps;+1.2eps
out:-0.5,+0.5
-1.1eps;+1.1eps
out:-0.5,+0.5
-eps;+eps
out:-0.5,+0.5
1
S(exi,t)
decoder
1
gama
b)

FIGURE 19.53 (a) Multilevel sliding-mode PWM modulator with n-level hysteresis comparator of quantization interval ϵ; (b) a four hysterisis comparator implementation of a five-level switching law.

This switching law can be implemented as depicted in Fig. 19.53.

Control of the Output Voltage in Single-Phase Multilevel Converters

To control the inverter output voltage, in a closed loop, in diode-clamped multilevel inverters with n levels and supply voltage U_{cc}, a control law similar to (19.116), $S(e_{u_o}, t) = \kappa \int (u_{o_r} - k_v \gamma(t_k) U_{cc}/(n-1))\mathrm{d}t = 0$, is suitable.

Figure 19.54a shows the waveforms of a five-level sliding-mode controlled inverter, namely the input sinus voltage, the generated output staircase wave, and the sliding-surface instantaneous error. This error is always within a band centered around the zero value and presents zero mean value, which is not the case of

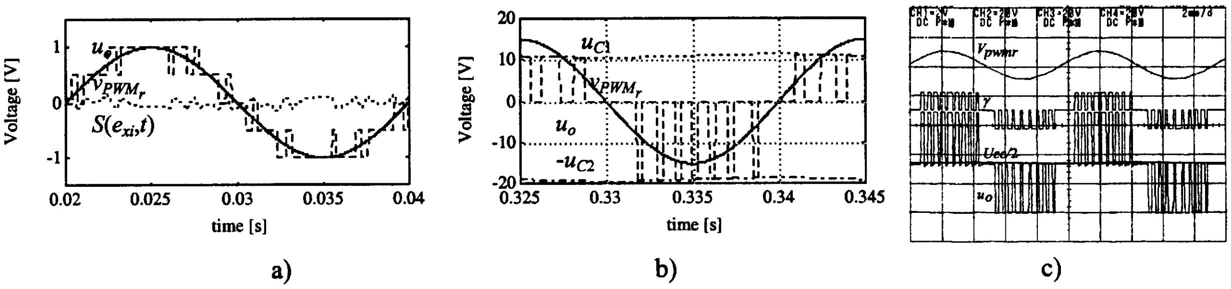
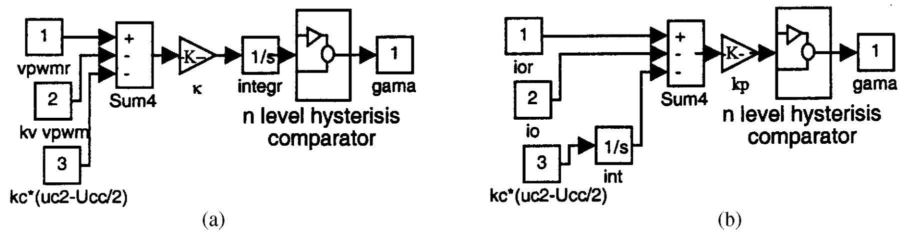
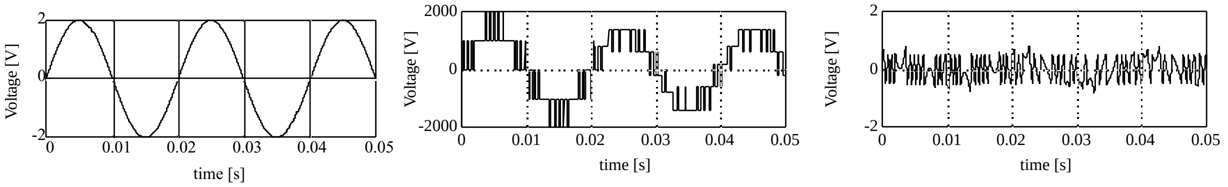


FIGURE 19.54 (a) Scaled waveforms of a five-level sliding-mode controlled single-phase converter, showing the input sinus voltage v_{PWM_r}, the generated output staircase wave u_o, and the value of the sliding surface $S(e_{xi}, t)$; (b) scaled waveforms of a three-level neutral-point clamped inverter showing the capacitor voltage unbalance (shown as two near flat lines touching the tips of the PWM pulses); (c) experimental results from a laboratory prototype of a three-level single-phase power inverter with the capacitor voltage equalization described.


1
vpwmr
2
kv vpwm
3
kc*(uc2-Ucc/2)
+
-
-
Sum4
K-
K
1/s
integr
n level hysterisis comparator
1
gama
1
ior
2
io
3
kc*(uc2-Ucc/2)
1/s
int
Sum4
kp
n level hysterisis comparator
1
gama

(a) (b)

FIGURE 19.55 (a) Multilevel sliding-mode output voltage controller and PWM modulator with capacitor voltage equalization; (b) Sliding-mode output current controller with capacitor voltage equalization.



a) b) c)

FIGURE 19.56 Simulated performance of a five-level power inverter, with a U_{cc} voltage dip (from 2 kV to 1.5 kV). Response to a sinusoidal wave of frequency 50 Hz. (a) v_{PWM_r} input; (b) PWM output voltage u_o; (c) the integral of the error voltage, which is maintained close to zero.

sigma-delta modulators followed by n-level quantizers, where the error presents an offset mean value in each half period.

Experimental multilevel converters always show capacitor voltage imbalances (Fig. 19.54b) due to small differences between semiconductor voltage drops and circuitry offsets. To obtain capacitor voltage equalization, the voltage error $(v_{c_2} - U_{cc}/2)$ is fed back to the controller (Fig. 19.55a) to counteract the circuitry offsets. Experimental results (Fig. 19.54c) clearly show the effectiveness of the correction made. The small steady-state error between the voltages of the two capacitors still present could be eliminated using an integral regulator (Fig. 19.55b).

Figure 19.56 confirms the robustness of the sliding-mode controller to power supply disturbances.

Output Current Control in Single-Phase Multilevel Converters

Considering an inductive load with current i_L, the control law (19.91) and switching law (19.132), should be used for single-phase multilevel inverters. Results obtained using the capacitor voltage equalization principle just described are shown in Fig. 19.57.

Example 19.16. Sliding-Mode Controllers for Three-Phase Multilevel Inverters. Three-phase n-level inverters (Fig. 19.58) are suitable for high-voltage, high-power dc-ac applications, such as modern high-speed railway traction drives, as the controlled turn-off semiconductors must block only a fraction (normally $U_{dc}/(n-1)$) of the total supply voltage U_{dc}.

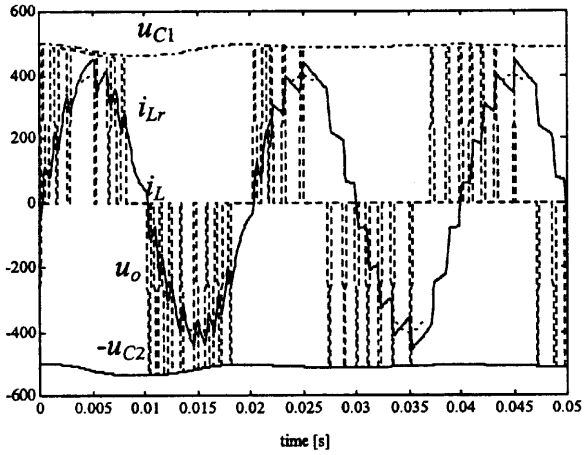


FIGURE 19.57 Operation of a three-level neutral-point clamped inverter as a sinusoidal current source: Scaled waveforms of the output current sine wave reference i_{L_r}, the output current i_L, showing ripple, together with the PWM-generated voltage u_o, with nearly equal pulse heights, corresponding to the equalized DC capacitor voltages u_{C1} and u_{C2}.

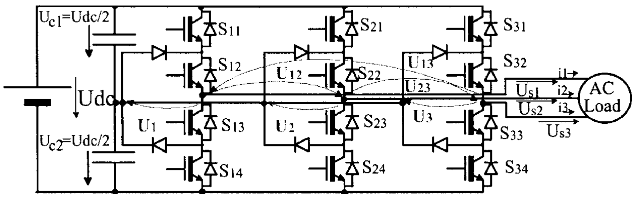

Uc1=Udc/2
Udc
Uc2=Udc/2
S11
S12
S13
S14
S21
S22
S23
S24
S31
S32
S33
S34
U1
U2
U3
U12
U13
U23
Us1
Us2
Us3
i1
i2
i3
AC Load

FIGURE 19.58 Three-phase, neutral-clamped three-level inverter with IGBTs.

This example presents a realtime modulator for the control of the three output voltages and capacitor voltage equalization, based on the use of sliding mode and space vectors represented in the $\alpha\beta$ frame. Capacitor voltage equalization is done with the proper selection of redundant space vectors.

Output Voltage Control in Multilevel Converters

For each leg of the three-phase multilevel converter, the switching strategy for the k leg ($k \in \{1, 2, 3\}$) must ensure complementary states to switches S_{k1} and S_{k3}. The same restriction must be observed for S_{k2}, S_{k4}. Neglecting switch delays, dead times, on-state semiconductor voltage drops, snubber networks, amd power-supply variations, supposing small dead times and equal capacitor voltages, and using the time-dependent switching variable $\gamma_k(t)$, the leg output voltage U_k (Fig. 19.58) will be $U_k = \gamma_k(t)U_{dc}/2$, with

$$\gamma_k(t) = \begin{cases} 1 & \text{if } \mathrm{S}_{k1} \wedge \mathrm{S}_{k2} \text{ are ON} \wedge \mathrm{S}_{k3} \wedge \mathrm{S}_{k4} \text{ are OFF} \\ 0 & \text{if } \mathrm{S}_{k2} \wedge \mathrm{S}_{k3} \text{ are ON} \wedge \mathrm{S}_{k1} \wedge \mathrm{S}_{k4} \text{ are OFF} \\ -1 & \text{if } \mathrm{S}_{k3} \wedge \mathrm{S}_{k4} \text{ are ON} \wedge \mathrm{S}_{k1} \wedge \mathrm{S}_{k2} \text{ are OFF} \end{cases} \tag{19.133}$$

The converter output voltages U_{Sk} of vector $\mathbf{U}_S$ can be expressed

$$\mathbf{U}_S = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} \gamma_1 \\ \gamma_2 \\ \gamma_3 \end{bmatrix} \frac{U_{dc}}{2} \tag{19.134}$$

The application of the Concordia transformation $U_{S1,2,3} = [\mathrm{C}]\ U_{S\alpha,\beta,o}$ (19.135) to (19.134) reduces the number of equations

$$\begin{bmatrix} U_{S_1} \\ U_{S_2} \\ U_{S_3} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & 0 & 1/\sqrt{2} \\ -1/2 & \sqrt{3}/2 & 1/\sqrt{2} \\ -1/2 & -\sqrt{3}/2 & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} U_{S_\alpha} \\ U_{S_\beta} \\ U_{s_o} \end{bmatrix} \tag{19.135}$$

The output voltage vector in the $\alpha\beta$ coordinates $\mathbf{U}_{S\alpha,\beta}$ is

$$\begin{aligned} \mathbf{U}_{S_{\alpha,\beta}} &= \begin{bmatrix} U_{s\alpha} \\ U_{s\beta} \end{bmatrix} \\ &= \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & 0\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \Gamma_1 \\ \Gamma_2 \\ \Gamma_3 \end{bmatrix} \frac{U_{dc}}{2} \\ &= \begin{bmatrix} \Gamma_\alpha \\ \Gamma_\beta \end{bmatrix} \frac{U_{dc}}{2} \end{aligned} \tag{19.136}$$

where

$$\Gamma_1 = \frac{2}{3}\gamma_1 - \frac{1}{3}\gamma_2 - \frac{1}{3}\gamma_3;\ \Gamma_2 = \frac{2}{3}\gamma_2 - \frac{1}{3}\gamma_3 - \frac{1}{3}\gamma_1;$$
$$\Gamma_3 = \frac{2}{3}\gamma_3 - \frac{1}{3}\gamma_1 - \frac{1}{3}\gamma_2 \tag{19.137}$$

The output voltage vector in the $\alpha\beta$ coordinates $\mathbf{U}_{S\alpha,\beta}$ is discontinuous. A suitable state variable for this output can be its average value $\bar{\mathbf{U}}_{S_{\alpha,\beta}}$ during one switching period:

$$\bar{\mathbf{U}}_{S_{\alpha,\beta}} = \frac{1}{T}\int_0^T \mathbf{U}_{S_{\alpha,\beta}} \mathrm{d}t = \frac{1}{T}\int_0^T \Gamma_{\alpha,\beta} \frac{U_{dc}}{2} \mathrm{d}t \tag{19.138}$$

The controllable canonical form is

$$\frac{\mathrm{d}}{\mathrm{d}t}\bar{\mathbf{U}}_{S_{\alpha,\beta}} = \frac{\mathbf{U}_{S_{\alpha,\beta}}}{T} = \frac{\Gamma_{\alpha,\beta}}{T}\frac{U_{dc}}{2} \tag{19.139}$$

Considering the control goal $\bar{\mathbf{U}}_{S_{\alpha,\beta}} = \bar{\mathbf{U}}_{S_{\alpha,\beta_{ref}}}$ and (19.75) the sliding surface is

$$\begin{aligned} \mathbf{S}(\mathbf{e}_{\alpha,\beta}, t) &= \sum_{o=1}^{j} \mathbf{k}_{\alpha,\beta_o}\mathbf{e}_{\alpha,\beta_o} = \mathbf{k}_{\alpha,\beta_1}\mathbf{e}_{\alpha,\beta_1} \\ &= \mathbf{k}_{\alpha,\beta_1}(\bar{\mathbf{U}}_{S_{\alpha,\beta ref}} - \bar{\mathbf{U}}_{S_{\alpha,\beta}}) \\ &= \frac{\mathbf{k}_{\alpha,\beta}}{T}\int_0^T (\mathbf{U}_{S_{\alpha,\beta ref}} - \mathbf{U}_{S_{\alpha,\beta}})\mathrm{d}t = 0 \end{aligned} \tag{19.140}$$

To ensure reaching mode behavior, and sliding mode stability (19.76), as the first derivative of (19.140), $\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta}, t)$, is

$$\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta}, t) = \frac{\mathbf{k}_{\alpha,\beta}}{T}(\mathbf{U}_{S_{\alpha,\beta ref}} - \mathbf{U}_{S_{\alpha,\beta}}) \tag{19.141}$$

the switching law is

$$\begin{aligned} \mathbf{S}(\mathbf{e}_{\alpha,\beta}, t) > 0 \Rightarrow \dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta}, t) < 0 \Rightarrow \mathbf{U}_{S_{\alpha,\beta}} > \mathbf{U}_{s_{\alpha,\beta ref}} \\ \mathbf{S}(\mathbf{e}_{\alpha,\beta}, t) < 0 \Rightarrow \dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta}, t) > 0 \Rightarrow \mathbf{U}_{S_{\alpha,\beta}} < \mathbf{U}_{s_{\alpha,\beta ref}} \end{aligned} \tag{19.142}$$

This switching strategy must select the proper values of $\mathbf{U}_{S_{\alpha,\beta}}$ from the available outputs. As each inverter leg (Fig. 19.58) can deliver one of three possible output voltages ($U_{dc}/2$; 0; $-U_{dc}/2$), all the 27 possible output voltage vectors listed in Table 19.3, can be represented in the $\alpha\beta$ frame of Fig. 19.59 (in per units, 1 p.u. = U_{dc}). There are nine different levels for the α space vector component and only five for the β component. However, considering any particular value of α (or β) component, there are at most five levels available in the remaining orthogonal component. From the load viewpoint, the 27 space vectors of Table 19.3 define only 19 distinct space positions (Fig. 19.59).

To select one of these 19 positions from the control law (19.140) and the switching law (19.142), two five-level hysteretic comparators (Fig. 19.53b) must be used ($5^2 = 25$). Their outputs are the integer variables λ_α and λ_β, denoted $\lambda_{\alpha,\beta}$ (λ_α, λ_β ($\lambda_\beta \in \{-2; -1; 0; 1; 2\}$) corresponding to the five selectable levels of Γ_α and Γ_β. Considering sliding-mode stability, $\lambda_{\alpha,\beta}$, at time step $j+1$, is given by (19.143), knowing their previous values at step j. This means that the output level is increased (decreased) if the error and its derivative are both positive (negative), provided the maximum (minimum) output level is not exceeded.

$$\begin{cases} (\lambda_{\alpha,\beta})_{j+1} = (\lambda_{\alpha,\beta})_j + 1 \text{ if } \mathbf{S}(\mathbf{e}_{\alpha,\beta}, t) > \varepsilon \\ \qquad \wedge \dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta}, t) > \varepsilon \wedge (\lambda_{\alpha,\beta})_j < 2 \\ (\lambda_{\alpha,\beta})_{j+1} = (\lambda_{\alpha,\beta})_j - 1 \text{ if } \mathbf{S}(\mathbf{e}_{\alpha,\beta}, t) < -\varepsilon \\ \qquad \wedge \dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta}, t) < -\varepsilon \wedge (\lambda_{\alpha,\beta})_j > -2 \end{cases} \tag{19.143}$$

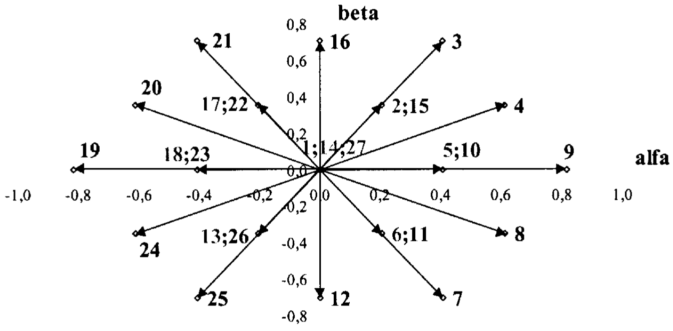


FIGURE 19.59 Output voltage vectors (1 to 27) of three-phase, neutral-clamped three-level inverters, in the $\alpha\beta$ frame.

The available space vectors must be chosen not only to reduce the mean output voltage errors, but also to guarantee transitions only between adjacent levels, to minimize the capacitor voltage unbalance, to minimize the switching frequency, to observe minimum on or off times if applicable, and to equally stress all the semiconductors.

Using (19.143) and the control laws $\mathbf{S}(\mathbf{e}_{\alpha,\beta}, t)$ (19.140), Tables 19.4 and 19.5 can be used to choose the correct voltage vector in order to ensure stability, current tracking, and capacitor voltage equalization. The vector with α, β components corresponding to the levels of the pair λ_β, λ_α is selected, provided that adjacent

TABLE 19.3 Vectors of the three-phase three-level converter, switching variables γ_k, switch states s_{kj} and the corresponding output voltages, line to neutral point, line to line, and $\alpha\beta$ components in per units

Vector	γ_1	γ_2	γ_3	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	S_{31}	S_{32}	S_{33}	S_{34}	U_1	U_2	U_3	U_{12}	U_{23}	U_{31}	$U_{s\alpha}/U_{dc}$	$U_{s\beta}/U_{dc}$
1	1	1	1	1	1	0	0	1	1	0	0	1	1	0	0	$U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	0	0	0	0,00	0,00
2	1	1	0	1	1	0	0	1	1	0	0	0	1	1	0	$U_{dc}/2$	$U_{dc}/2$	0	0	$U_{dc}/2$	$-U_{dc}/2$	0,20	0,35
3	1	1	−1	1	1	0	0	1	1	0	0	0	0	1	1	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	0	U_{dc}	$-U_{dc}$	0,41	0,71
4	1	0	−1	1	1	0	0	0	1	1	0	0	0	1	1	$U_{dc}/2$	0	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}$	0,61	0,35
5	1	0	0	1	1	0	0	0	1	1	0	0	1	1	0	$U_{dc}/2$	0	0	$U_{dc}/2$	0	$-U_{dc}/2$	0,41	0,00
6	1	0	1	1	1	0	0	0	1	1	0	1	1	0	0	$U_{dc}/2$	0	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	0	0,20	−0,35
7	1	−1	1	1	1	0	0	0	0	1	1	1	1	0	0	$U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	U_{dc}	$-U_{dc}$	0	0,41	−0,71
8	1	−1	0	1	1	0	0	0	0	1	1	0	1	1	0	$U_{dc}/2$	$-U_{dc}/2$	0	U_{dc}	$-U_{dc}/2$	$-U_{dc}/2$	0,61	−0,35
9	1	−1	−1	1	1	0	0	0	0	1	1	0	0	1	1	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	U_{dc}	0	$-U_{dc}$	0,82	0,00
10	0	−1	−1	0	1	1	0	0	0	1	1	0	0	1	1	0	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	0	$-U_{dc}/2$	0,41	0,00
11	0	−1	0	0	1	1	0	0	0	1	1	0	1	1	0	0	$-U_{dc}/2$	0	$U_{dc}/2$	$-U_{dc}/2$	0	0,20	−0,35
12	0	−1	1	0	1	1	0	0	0	1	1	1	1	0	0	0	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}$	$U_{dc}/2$	0,00	−0,71
13	0	0	1	0	1	1	0	0	1	1	0	1	1	0	0	0	0	$U_{dc}/2$	0	$-U_{dc}/2$	$U_{dc}/2$	−0,20	−0,35
14	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0,00	0,00
15	0	0	−1	0	1	1	0	0	1	1	0	0	0	1	1	0	0	$-U_{dc}/2$	0	$U_{dc}/2$	$-U_{dc}/2$	0,20	0,35
16	0	1	−1	0	1	1	0	1	1	0	0	0	0	1	1	0	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	U_{dc}	$-U_{dc}/2$	0,00	0,71
17	0	1	0	0	1	1	0	1	1	0	0	0	1	1	0	0	$U_{dc}/2$	0	$-U_{dc}/2$	$U_{dc}/2$	0	−0,20	0,35
18	0	1	1	0	1	1	0	1	1	0	0	1	1	0	0	0	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	0	$U_{dc}/2$	−0,41	0,00
19	−1	1	1	0	0	1	1	1	1	0	0	1	1	0	0	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}$	0	U_{dc}	−0,81	0,00
20	−1	1	0	0	0	1	1	1	1	0	0	0	1	1	0	$-U_{dc}/2$	$U_{dc}/2$	0	$-U_{dc}$	$U_{dc}/2$	$U_{dc}/2$	−0,61	0,35
21	−1	1	−1	0	0	1	1	1	1	0	0	0	0	1	1	$-U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}$	U_{dc}	0	−0,41	0,71
22	−1	0	−1	0	0	1	1	0	1	1	0	0	0	1	1	$-U_{dc}/2$	0	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	0	−0,20	0,35
23	−1	0	0	0	0	1	1	0	1	1	0	0	1	1	0	$-U_{dc}/2$	0	0	$-U_{dc}/2$	0	$U_{dc}/2$	−0,41	0,00
24	−1	0	1	0	0	1	1	0	1	1	0	1	1	0	0	$-U_{dc}/2$	0	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	U_{dc}	−0,61	−0,35
25	−1	−1	1	0	0	1	1	0	0	1	1	1	1	0	0	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	0	$-U_{dc}$	U_{dc}	−0,41	−0,71
26	−1	−1	0	0	0	1	1	0	0	1	1	0	1	1	0	$-U_{dc}/2$	$-U_{dc}/2$	0	0	$-U_{dc}/2$	$U_{dc}/2$	−0,20	−0,35
27	−1	−1	−1	0	0	1	1	0	0	1	1	0	0	1	1	$-U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	0	0	0	0,00	0,00

TABLE 19.4 Switching Table for Current Control and $u_{c1} > u_{c2}$ in the Inverter Mode, or $u_{c1} < u_{c2}$ in the Regenerative Mode ($(U_{C1} - U_{C2})(\Upsilon_1 i_1 + \Upsilon_2 i_2) > 0$), Showing Vector Selectioin upon the Variable λ_α, λ_β

$\lambda_\beta/\lambda_\alpha$	−2	−1	0	1	2
−2	25	25	12	7	7
−1	24	13	13;6	6	8
0	19	18	1;14;27	5	9
1	20	17	17;2	2	4
2	21	21	16	3	3

TABLE 19.5 Switching Table for Current Control and $u_{c1} < u_{c2}$ in the Inverter Mode, or $u_{c1} > u_{c2}$ in the Regenerative Mode ($(U_{C1} - U_{C2})(\Upsilon_1 i_1 + \Upsilon_2 i_2) < 0$), Showing Vector Selection upon the Variables λ_α, λ_β

$\lambda_\beta/\lambda_\alpha$	−2	−1	0	1	2
−2	25	25	12	7	7
−1	24	26	26;11	11	8
0	19	23	1;14;27	10	9
1	20	22	22;15	15	4
2	21	21	16	3	3

transitions on inverter legs are obtained. If there is no directly corresponding vector, then the nearest vector guaranteeing adjacent transitions is selected. If more than one vector is the nearest, one is selected to equalize the capacitor voltages. One of the three vectors (1, 14, 27) corresponding to the zero vector is selected to minimize the switching frequency.

The discrete values of $\lambda_{\alpha,\beta}$ allow 25 different combinations. As only 19 are distinct from the load viewpoint, the extra ones can be used to select vectors able to equalize the capacitor voltages. From circuit analysis it can be seen that vectors 2, 5, 6, 13, 17, 18 result in the discharge of capacitor C_1, if the inverter is operating in the inverter mode, or in the discharge of C_1 if the inverter is operating as a boost rectifier. Similar reasoning can be applied for vectors {10, 11, 15, 22, 23, 26} and capacitor C_2. Therefore, considering the vector $\Upsilon_{1,2} = [(\gamma_{1,2}/2)(\gamma_{1,2}+1) - (\gamma_3/2)(\gamma_3+1)]$, if $(U_{C1} - U_{C2}) \times (\Upsilon_1 i_1 + \Upsilon_2 i_2) > 0$, then according to $\lambda_{\alpha,\beta}$, choose one of the vectors {2, 5, 6, 13, 17, 18} (Table 19.4). If $(U_{C1} - U_{C2})(\Upsilon_1 i_1 + \Upsilon_2 i_2) < 0$, then according to $\lambda_{\alpha,\beta}$, choose one of the vectors {10, 11, 15, 22, 23, 26} (Table 19.5).

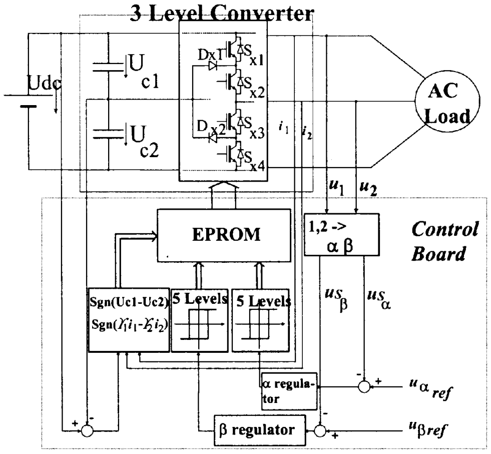


FIGURE 19.60 Block diagram of the multilevel converter and control board.

As an example, consider the case where $U_{C1} > U_{C2}$. Then the capacitor C_2 must be charged and Table 19.4 must be used if the multilevel inverter is operating in the inverter mode or Table 19.5 for the regenerative mode. Addicionally, when using Table 19.4, if $\lambda_\alpha = -1$ and $\lambda_\beta = -1$, then vector 13 should be used.

Experimental results shown in Fig. 19.61 were obtained with a low-power, low-voltage laboratory prototype (150 V, 3 kW) of a three-level inverter (Fig. 19.60), controlled by two four-level comparators, plus described capacitor voltage equalizing procedures and EPROM-based lookup Tables 19.3, 19.4 and 19.5. Transistors IGBT (MG25Q2YS40) were switched at frequencies near 4-kHz, with neutral clamp diodes 40HFL, $C_1 \approx C_2 \approx 20$ mF. The load was mainly inductive (3×10 mH, $2\,\Omega$).

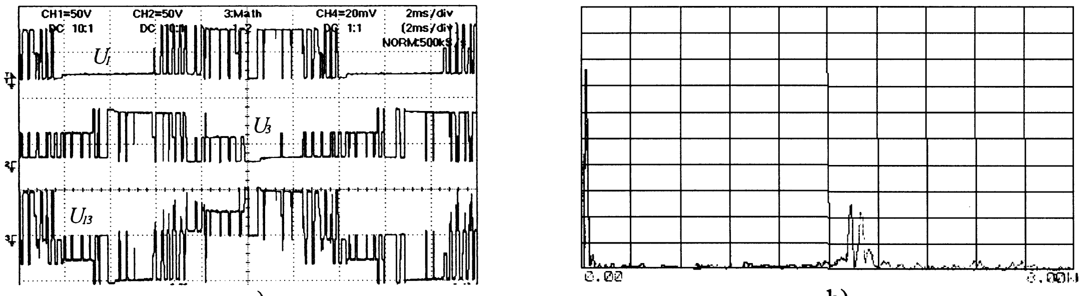
The inverter number of levels (three for the phase voltage and five for the line voltage), together with the adjacent transitions of inverter legs between levels, are shown in Fig. 19.61a) and, in detail, in Fig. 19.62a).

The performance of the capacitor voltage equalizing strategy is shown in Fig. 19.62b, where the reference current of phase 1 and the output current of phase 3, together with the power supply voltage ($U_{dc} \approx 100$ V) and the voltage of capacitor C_2 (U_{C2}), can be seen. It can be noted that the U_{C2} voltage is nearly half of the supply voltage. Therefore, the capacitor voltages are nearly equal. Furthermore, it can be stated that without this voltage equalization procedure, the three-level inverter operates only during a brief transient, during which one of the capacitor voltages vanishes to nearly zero volts and the other is overcharged to the supply voltage. Figure 19.61b shows the harmonic spectrum of the output voltages, where the harmonics due to the switching frequency (≈4.5 kHz) and the fundamental harmonic can be seen.

On-line Output Current Control in Multilevel Inverters

Considering a standard inductive balanced load (R, L) with electromotive force (u) and isolated neutral, the converter output currents i_k can be expressed

$$U_{Sk} = Ri_k + L\frac{di_k}{dt} + u_k \tag{19.144}$$



a) b)

FIGURE 19.61 (a) Experimental results showing phase and line voltages; (b) Harmonic spectrum of output voltages.

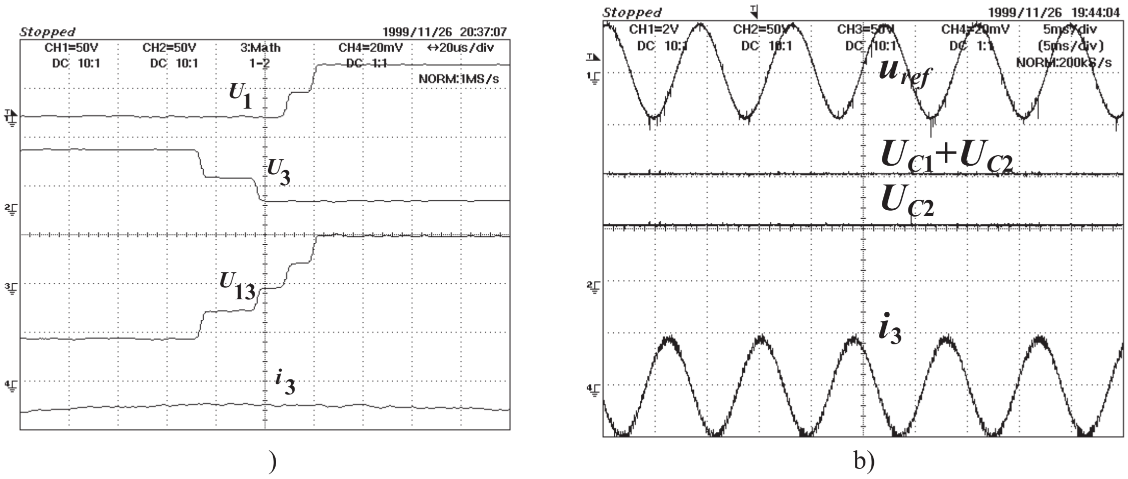
Now analysing the circuit of Fig. 19.58, the multilevel converter switched state-space model can be obtained:

$$\frac{d}{dt}\begin{bmatrix} i_1\\ i_2\\ i_3\end{bmatrix} = -\begin{bmatrix}\frac{R}{L}&0&0\\0&\frac{R}{L}&0\\0&0&\frac{R}{L}\end{bmatrix}\begin{bmatrix}i_1\\ i_2\\ i_3\end{bmatrix} - \begin{bmatrix}\frac{1}{L}&0&0\\0&\frac{1}{L}&0\\0&0&\frac{1}{L}\end{bmatrix}\begin{bmatrix}u_1\\ u_2\\ u_3\end{bmatrix} + \begin{bmatrix}\frac{\Gamma_1}{L}\\ \frac{\Gamma_2}{L}\\ \frac{\Gamma_3}{L}\end{bmatrix}\frac{U_{dc}}{2} \tag{19.145}$$

The application of the Concordia matrix (19.135) to (19.145), reduces the number of the new model (19.146) equations to two, since an isolated neutral is assumed

$$\frac{d}{dt}\begin{bmatrix} i_\alpha\\ i_\beta\end{bmatrix} = -\begin{bmatrix}\frac{R}{L}&0\\0&\frac{R}{L}\end{bmatrix}\begin{bmatrix}i_\alpha\\ i_\beta\end{bmatrix} - \begin{bmatrix}\frac{1}{L}&0\\0&\frac{1}{L}\end{bmatrix}\begin{bmatrix}u_\alpha\\ u_\beta\end{bmatrix} + \begin{bmatrix}\frac{1}{L}&0\\0&\frac{1}{L}\end{bmatrix}\begin{bmatrix}U_{S\alpha}\\ U_{S\beta}\end{bmatrix} \tag{19.146}$$

The model (19.146) of this multiple-input, multiple-output system (MIMO) with outputs i_α, i_β reveals the control inputs $U_{S\alpha}$, $U_{S\beta}$, dependent on the control variables $\gamma_k(t)$.



) b)

FIGURE 19.62 Experimental results showing (a) the transitions between adjacent voltage levels (50 V/div; time 20 μs/div); (b) performance of the capacitor voltage equalizing strategy; from top trace to bottom: 1, the voltage reference input; 2, the power supply voltage; 3, the midpoint capacitor voltage, which is maintained close to $U_{dc}/2$; 4, the output current of phase 3 (2 A/div; 50 V/div; 20 ms/div).

From (19.146) and (19.75), the two sliding surfaces $\mathbf{S}(\mathbf{e}_{\alpha\beta,t})$ are

$$\mathbf{S}(\mathbf{e}_{\alpha,\beta}, t) = \mathbf{k}_{\alpha,\beta}(\mathbf{i}_{\alpha,\beta_{ref}} - \mathbf{i}_{\alpha,\beta}) = \mathbf{k}_{\alpha,\beta}\mathbf{e}_{\alpha,\beta} = 0 \quad (19.147)$$

The first derivatives of (19.146), denoted $\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta}, t)$, are:

$$\begin{aligned}\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta}, t) &= \mathbf{k}_{\alpha,\beta}(\dot{\mathbf{i}}_{\alpha,\beta_{ref}} - \dot{\mathbf{i}}_{\alpha,\beta}) \\ &= \mathbf{k}_{\alpha,\beta}[\dot{\mathbf{i}}_{\alpha,\beta_{ref}} + \mathbf{R}\mathbf{L}^{-1}\mathbf{i}_{\alpha,\beta} + \mathbf{u}_{\alpha,\beta}\mathbf{L}^{-1} - \mathbf{U}_{S\alpha,\beta}\mathbf{L}^{-1}]\end{aligned} \quad (19.148)$$

Therefore, the switching law is

$$\begin{aligned}\mathbf{S}(\mathbf{e}_{\alpha,\beta}, t) > 0 &\Rightarrow \dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta}, t) < 0 \\ &\Rightarrow \mathbf{U}_{S\alpha,\beta} > \mathbf{L}\dot{\mathbf{i}}_{\alpha,\beta ref} + \mathbf{R}\mathbf{i}_{\alpha,\beta} + \mathbf{u}_{\alpha,\beta} \\ \mathbf{S}(\mathbf{e}_{\alpha,\beta}, t) < 0 &\Rightarrow \dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta}, t) > 0 \\ &\Rightarrow \mathbf{U}_{S\alpha,\beta} < \mathbf{L}\dot{\mathbf{i}}_{\alpha,\beta ref} + \mathbf{R}\mathbf{i}_{\alpha,\beta} + \mathbf{u}_{\alpha,\beta}\end{aligned} \quad (19.149)$$

These switching laws are implemented using the same $\alpha\beta$ vector modulator described above in this example.

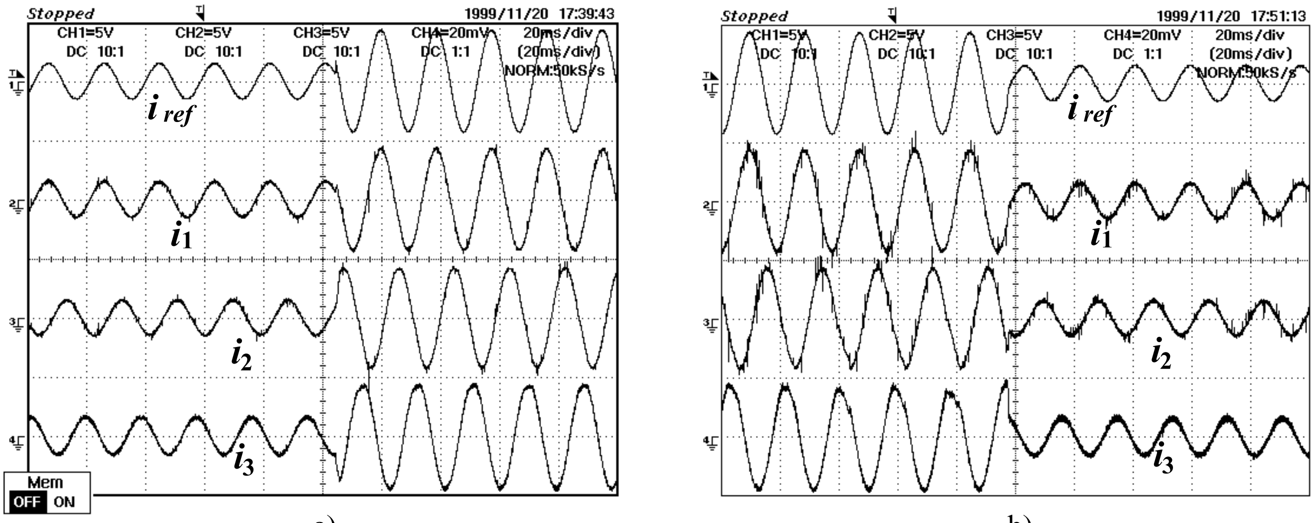
Figure 19.63a shows experimental results. The multilevel converter and proposed control behavior are obtained for step inputs (2 A to 4 A) in the amplitude of the sinus references with frequency near 52 Hz ($U_{dc} \approx 50$ V). Observe the tracking ability, the fast transient response, and the balanced three phase currents. Figure 19.63b shows almost the same test (step response from 4 A to 2 A at the same frequency), but now the power supply is set at 150 V and the inductive load was unbalanced (±30% of resistor value). The response remains virtually the same, with tracking ability, no current distortions due to dead times or semiconductor voltage drops. These results confirm experimentally that the designed controllers are robust concerning these nonidealities.

1 .4 uzzy Logic Control of Power Converters

1 .4.1 Introduction

Fuzzy logic control [17,18,19] is a heuristic approach that easily embeds the knowledge and key elements of human thinking in the design of nonlinear controllers. Qualitative and heuristic considerations, which cannot be handled by conventional control theory, can be used for control purposes in a systematic form by applying fuzzy control concepts [3]. Fuzzy logic control does not need an accurate mathematical model, can work with imprecise inputs, can handle nonlinearity, and can present disturbance insensitivity greater than most nonlinear controllers. Fuzzy logic controllers usually outperform other controllers in complex, nonlinear, or undefined systems for which a good practical knowledge exists.

Fuzzy logic controllers are based on fuzzy sets, i.e., classes of objects in which the transition from membership to nonmembership is smooth rather than abrupt. Therefore, boundaries of fuzzy sets can be vague and ambiguous, making them useful for approximation systems.



a) b)

FIGURE 19.63 Step response of the current control method; (a) step from 2 A to 4 A in the reference amplitude at 52 Hz. Traces show the reference current for phase 1 and the three output currents with 50 V power supply; (b) Step from 4 A to 2 A amplitude. Traces show the reference current for phase 1 and the three output currents with 150 V power supply (5 A/div; time scale 20 ms/div).

The first step in the fuzzy controller synthesis procedure is to define the input and output variables of the fuzzy controller. This is done accordingly with the expected function of the controller. There are not any general rules to select those variables, although typically the variables chosen are the states of the controlled system, their errors, error variation, and/or error accumulation. In power converters, the fuzzy controller input variables are commonly the output voltage or current error, and/or the variation or accumulation of this error. The output variables $u(k)$ of the fuzzy controller can define the converter duty cycle (Fig. 19.6), or a reference current to be applied in an inner current mode PI or sliding-mode controller.

The fuzzy controller rules are usually formulated in linguistic terms. Thus, the use of linguistic variables and fuzzy sets implies the fuzzification procedure, e.g. the mapping of the input variables into suitable linguistics values.

Rule evaluation or decision-making infers, using an inference engine, the fuzzy control action from the knowledge of the fuzzy rules and the linguistic variable definition.

The output of a fuzzy controller is a fuzzy set, and thus it is necessary to perform a defuzzification procedure, e.g. the conversion of the inferred fuzzy result to a nonfuzzy (crisp) control action, that better represents the fuzzy one. This last step obtains the crisp value for the controller output $u(k)$ (Fig. 19.64).

These steps can be implemented on-line or off-line. On-line implementation, useful if an adaptive controller is intended, performs realtime inference to obtain the controller output and needs a fast enough processor. Off-line implementation employs a lookup table built according to the set of all possible combinations of input variables. To obtain this lookup table, input values in a quantified range are converted (fuzzification) into fuzzy variables (linguistic). The fuzzy set output, obtained by the inference or decision-making engine according to linguistic control rules (designed by the expert knowledge), is then converted into numeric controller output values (defuzzification). The table contains the output for all the combinations of quantified input entries. Off-line process can actually reduce the controller actuation time since the only effort is limited to consulting the table at each iteration.

This section presents the main steps for the implementation of a fuzzy controller suitable for power converter control. A meaningful example is provided.

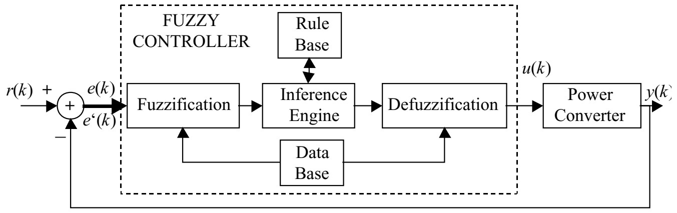


FIGURE 19.64 Structure of a fuzzy logic controller.

1 .4.2 Fuzzy Logic Controller Synthesis

Fuzzy logic controllers consider neither the parameters of the power converter or their fluctuations, nor the operating conditions, but only the experimental knowledge of the power converter dynamics. In this way, such a controller can be used with a wide diversity of power converters implying only small modifications. The necessary fuzzy rules are simply obtained considering roughly the knowledge of the power converter dynamic behavior.

1 .4.2.1 Fuzzification

Assume, as fuzzy controller input variables, an output voltage (or current) error, and the variation of this error. For the output, assume a signal $u(k)$, the reference input of the converter.

. . . . ***Quantization Levels*** Consider the reference $r(k)$ of the converter output kth sample, $y(k)$. The tracking error $e(k)$ is $e(k) = r(k) - y(k)$ and the output error change $\Delta_e(k)$, between the samples k and $k-1$, is determined by $\Delta_e(k) = e(k) - e(k-1)$.

These variables and the fuzzy controller output $u(k)$, usually ranging from −10 V to 10 V, can be quantified in m levels $\{-(m-1)/2, +(m-1)/2\}$. For off-line implementation, m sets a compromise between the finite length of a lookup table and the required precision.

. . . . ***Linguistic Variables and Fuzzy Sets*** The fuzzy sets for x_e, the linguistic variable corresponding to the error $e(k)$, for $x_{\Delta e}$, the linguistic variable corresponding to the error variation $\Delta_e(k)$, and for x_u the linguistic variable of the fuzzy controller output $u(k)$, are usually defined as positive big (**PB**), positive medium (**PM**), positive small (**PS**), zero (**ZE**), negative small (**NS**), negative medium (**NM**), and negative big (**NB**), instead of having numerical values.

In most cases, the use of these seven fuzzy sets is the best compromise between accuracy and computational task.

. . . . ***Membership Functions*** A fuzzy subset, for example $\mathbf{S_i}$($\mathbf{S_i}$ = (NB, NM, NS, ZE, PS, PM, or PB)) of a universe E, collection of $e(k)$ values denoted generically by $\{e\}$, is characterized by a membership function $\mu_{\mathrm{Si}}: E \to [0, 1]$, associating with each element e of universe E, a number $\mu_{\mathrm{Si}}(e)$ in the interval [0,1], which represents the grade of membership of e to E. Therefore, each variable is assigned a membership grade to each fuzzy set, based on a corresponding membership function (Fig. 19.65). Considering the m quantization levels, the membership function $\mu_{\mathrm{Si}}(e)$ of the element e in the universe of discourse E, may take one of the discrete values included in $\mu_{\mathrm{Si}}(e) \in \{0; 0.2; 0.4; 0.6; 0.8; 1; 0.8; 0.6; 0.4; 0.2; 0\}$. Membership functions are stored in the database (Fig. 19.64).

Considering $e(k) = 2$ and $\Delta e(k) = -3$, taking into account the staircase-like membership functions defined in Fig. 19.65,

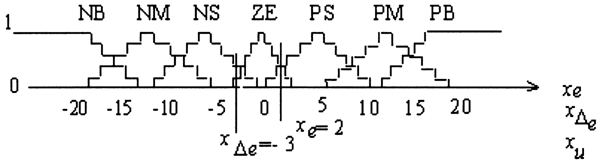


FIGURE 19.65 Membership functions in the universe of discourse.

it can be said that x_e is **PS** and also E, being equally **PS** and E. Also, $x_{\Delta e}$ is **NS** and E; being less E than **NS**.

. . . . ***Linguistic Control Rules*** The generic linguistic control rule has the following form:

> If $x_e(k)$ is membership of the set $\mathbf{S_i}$ = (NB, NM, NS, ZE, PS, PM, or PB) AND $x_{\Delta e}(k)$ is membership of the set $\mathbf{S}$ = (NB, NM, NS, ZE, PS, PM, or PB), THEN the output control variable is membership of the set $\mathbf{S_u}$ = (NB, NM, NS, ZE, PS, PM, or PB).

Usually, the rules are obtained considering the most common dynamic behavior of power converters, the second-order system with damped oscillating response (Fig. 19.66). Analyzing the error and its variation, together with the rough linguistic knowledge of the needed control input, an expert can obtain linguistic control rules such as the ones displayed in Table 19.6. For example, at point 6 of Fig. 19.66 the rule is "if $x_e(k)$ is NM AND $x_{\Delta e}(k)$ is ZE, THEN $x_u(k+1)$ should be NM."

Table 19.6, for example, states that:

if $x_e(k)$ is NB AND $x_{\Delta e}(k)$ is NB, THEN $x_u(k+1)$ must be NB, or
if $x_e(k)$ is PS AND $x_{\Delta e}(k)$ is NS, THEN $x_u(k+1)$ must be NS, or
if $x_e(k)$ is PS AND $x_{\Delta e}(k)$ is ZE, THEN $x_u(k+1)$ must be PS, or
if $x_e(k)$ is ZE AND $x_{\Delta e}(k)$ is NS, THEN $x_u(k+1)$ must be NS, or
if $x_e(k)$ is ZE AND $x_{\Delta e}(k)$ is ZE, THEN $x_u(k+1)$ must be ZE, or
if...

These rules (rule base) alone do not allow the definition of the control output, as several of them may apply at the same time.

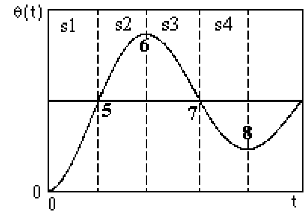


FIGURE 19.66 Reference dynamic model of power converters: second-order damped oscillating error response.

1 .4.2.2 Inference Engine

The result of a fuzzy control algorithm can be obtained using the control rules of Table 19.6, the membership functions, and an inference engine. In fact, any quantified value for $e(k)$ and $\Delta_e(k)$ is often included into two linguistic variables. With the membership functions used, and knowing that the controller considers $e(k)$ and $\Delta e(k)$, the control decision generically must be taken according to four linguistic control rules.

To obtain the corresponding fuzzy set, the min–max inference method can be used. The minimum operator describes the "AND" present in each of the four rules, that is, it calculates the minimum between the discrete value of the membership function $\mu_{\mathbf{Si}}(x_e(k))$ and the discrete value of the membership function $\mu_{\mathbf{S}}(x_{\Delta e}(k))$. The "THEN" statement links this minimum to the membership function of the output variable. The membership function of the output variable will therefore include trapezoids limited by the segment $\min(\mu_{\mathbf{Si}}(x_e(k)),\ \mu_{\mathbf{S}}(x_{\Delta e}(k)))$.

The OR operator linking the different rules is implemented by calculating the maximum of all the (usually four) rules. This mechanism to obtain the resulting membership function of the output variable is represented in Fig. 19.67.

1 .4.2.3 Defuzzification

As shown, the inference method provides a resulting membership function $\mu_{\mathbf{Sr}}(x_u(k))$, for the output fuzzy variable x_u (Fig. 19.67). Using a defuzzification process, this final membership function, obtained by combining all the membership functions, as a consequence of each rule, is then converted into a numerical value, called $u(k)$. The defuzzification strategy can

TABLE 19.6 Lingquistic control rules

$x_e(k)$ $x_{\Delta e}(k)$	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NM	NM	PS	PM
NM	NB	NB	NM	NS	NM	PM	PB
NS	NB	NB	NM	NS	NS	PM	PB
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NB	NM	PS	PS	PM	PB	PB
PM	NB	NM	PM	PS	PM	PB	PB
PB	NM	NS	PM	PM	PB	PB	PB

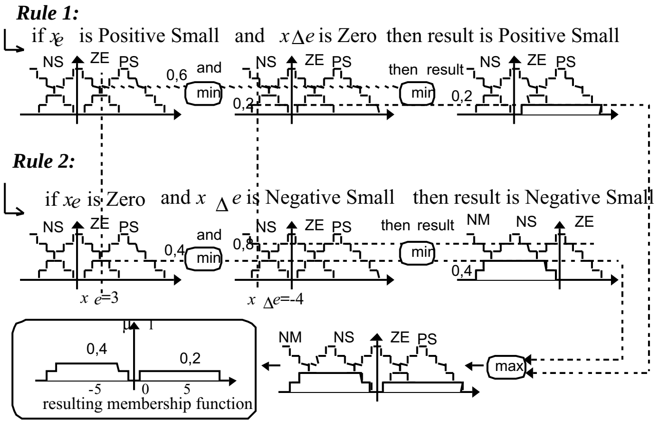

Rule 1:
if x_e is Positive Small and $x_{\Delta e}$ is Zero then result is Positive Small
NS ZE PS
0,6
and
min
NS ZE PS
0,2
then result
min
NS ZE PS
0,2
Rule 2:
if x_e is Zero and $x_{\Delta e}$ is Negative Small then result is Negative Small
NS ZE PS
0,4
and
min
0,8
NS ZE PS
then result
min
NM NS ZE
0,4
x_e=3
$x_{\Delta e}$=-4
μ 1
0,4
0,2
-5 0 5
resulting membership function
NM NS ZE PS
max

FIGURE 19.67 Application of the min-max operator to obtain the output membership function.

be the center of area (COA) method. This method generates one output value $u(k)$, which is the abscissa of the gravity center of the resulting membership function area, given by the following relation:

$$u(k) = \left(\sum_{i=1}^{m} \mu_{\mathbf{Sr}}(x_u(k))\; x_u(k) \right) \Big/ \sum_{i=1}^{m} \mu_{\mathbf{Sr}}(x_u(k)) \qquad (19.150)$$

This method provides good results for output control. Indeed, for a weak variation of $e(k)$ and $\Delta_e(k)$, the center of the area will move just a little, and so does the controller output value. By comparison, the alternative defuzzification method, the mean of maximum strategy (MOM), is advantageous for fast response, but it causes a greater steady-state error and overshoot (considering no perturbations).

1 .4.2.4 Lookup Table Construction

Using the rules given in Table 19.6, the min–max inference procedure, and COA defuzzification, all the controller output values for all quantified $e(k)$ and $\Delta_e(k)$ can be stored in an array to serve as the decision lookup table. This lookup table usually has a three-dimensional representation similar to Fig. 19.68. A microprocessor-based control algorithm just picks up output values from the lookup table.

EXAMPLE 19.17. FUZZY LOGIC CONTROL OF UNITY POWER FACTOR BUCK-BOOST RECTIFIERS. Consider the near unity power factor buck-boost rectifier of Fig. 19.69.

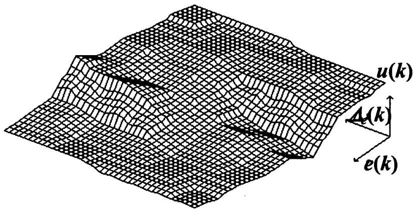


FIGURE 19.68 Three-dimensional view of the lookup table.

The switched state space model of this converter can be written

$$\begin{cases} \dfrac{di_s}{dt} = -\dfrac{R_f}{L_f} i_s - \dfrac{1}{L_f} v_{C_f} + \dfrac{1}{l_F} v_s \\ \dfrac{dv_{C_f}}{dt} = \dfrac{1}{C_f} i_s - \dfrac{\gamma_p}{C_f} i_{L_o} \\ \dfrac{di_{Lo}}{dt} = \dfrac{\gamma_p}{L_o} v_{C_f} - \dfrac{\gamma(1-|\gamma_p|)}{L_o} V_{C_o} \\ \dfrac{dV_{C_o}}{dt} = \dfrac{1-|\gamma_p|}{C_o} i_{L_o} - \dfrac{1}{R_o C_o} V_0 \end{cases} \qquad (19.151)$$

where

$$\gamma_p = \begin{cases} 1, & \text{(switch 1 and 4 are ON) and (switch 2 and 3 are OFF)} \\ 0, & \text{all the switches are OFF} \\ -1, & \text{(switch 2 and 3 are ON) and (switch 1 and 4 are OFF)} \end{cases}$$

and

$$\gamma = \begin{cases} 1, & i_{L_o} > 0 \\ 0, & i_{L_o} \leq 0 \end{cases}$$

For comparison purposes, a PI output voltage controller is designed considering that a current mode PWM modulator enforces the reference value for the i_s current (which usually exhibits a fast dynamics compared with the dynamics of V_{C_o}. A first-order model, similar to (19.129) is obtained. The PI gains are similar to (19.100) and load dependent ($K_p = C_o/(2T_d)$, $K_i = 1/(2T_d R_o)$).

A fuzzy controller is obtained considering the approach outlined, with seven membership functions for the output voltage error, five for its change, and three membership functions for the output. The linguistic control rules are obtained as the ones depicted in Table 19.6 and the lookup table is similar to Fig. 19.68. Performances obtained for the step response show a fuzzy controlled rectifier behavior close to the PI behavior. The advantages of the fuzzy controller emerge for perturbed loads or power supplies, where the low sensitivity of the fuzzy controller to system parameters is clearly seen (Fig. 19.70). Therefore, fuzzy controllers are advantageous for power converters with changing loads or supply voltage values and other external disturbances.

1 .5 Conclusions

Control techniques for power converters were reviewed. Linear controllers based on state-space averaged models or circuits

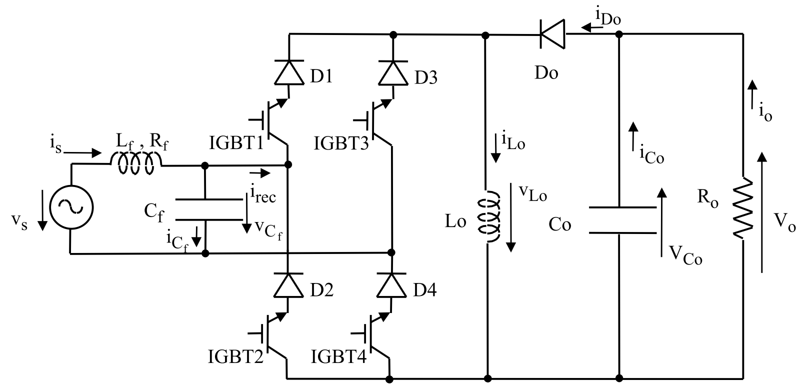
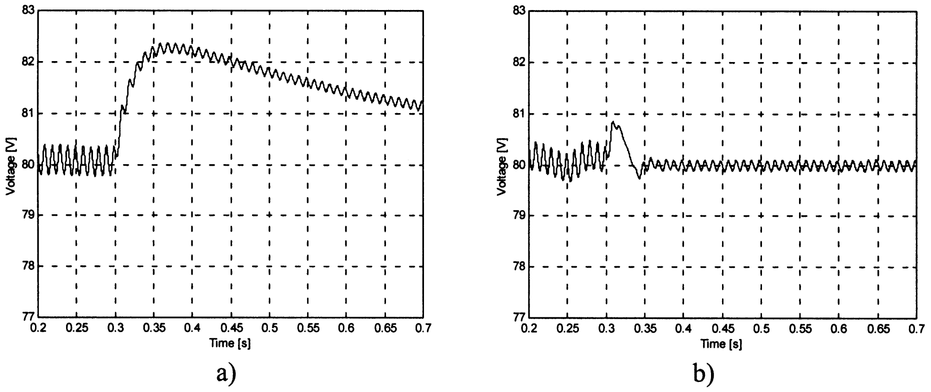


FIGURE 19.69 Unity power factor buck-boost rectifier with 4 IGBTs.

are well established and suitable for the application of linear systems control theory. Obtained linear controllers are useful, if the converter operating point is almost constant and disturbances are not relevant. For changing operating points and strong disturbances, linear controllers can be enhanced with nonlinear, antiwindup, soft-start, or saturation techniques. Current-mode control will also help to overcome the main drawbacks of linear controllers.

Sliding mode is a nonlinear approach well adapted for the variable structure of the power converters. The critical problem of obtaining the correct sliding surface was highlighted, and examples were given. The sliding-mode control law allows the implementation of the power converter controller, and the switching law gives the PWM modulator. The system variables to be measured and fed back are identified. The obtained reduced order dynamics is not dependent on system parameters or power supply (as long as it is high enough), presents no steady-state errors, and has a faster response speed (compared with linear controllers), as the system order is reduced and nonidealities are eliminated. Should the measure of the state variables be difficult, state observers may be used, with steady-state errors easily corrected. Sliding-mode controllers provide robustness against bounded disturbances and an elegant way to obtain the controller and modulator, using just the same theoretical approach. Fixed-frequency operation was addressed and solved, together with short-circuit-proof operation. Presented fixed-frequency techniques were applied to converters that can only operate with fixed frequency. Sliding-mode techniques were successfully applied to multiple-input multiple-output power converters and to multilevel converters, solving the capacitor voltage divider equalization. Sliding-mode control needs more information from the controlled system than do linear controllers, but is probably the most adequate tool to solve the control problem of power converters.

Fuzzy logic controller synthesis was briefly presented. Fuzzy logic controllers are based on human experience and intuition and do not depend on system parameters or operating points. Fuzzy logic controllers can be easily applied to various types of power converters having the same qualitative dynamics. Fuzzy logic controllers, like sliding-mode controllers, show robustness against load and power supply perturbations, semiconductor nonidealities (such as switch delays or uneven conduction voltage drops), and dead times. The controller implementation is simple, if based on the off-line concept. On-line implementation requires a fast microprocessor but



a) b)

FIGURE 19.70 Simulated result of the output voltage response to load disturbances ($R_o = 50\ \Omega$ to $R_o = 150\ \Omega$ at time 0.3 s); (a) PI control; b) fuzzy logic control.

can include adaptive techniques to optimize the rule base and/or the database.

Acknowledgments

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20

Power Supplies

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20.1 Introduction

Power supplies are used in most electrical equipment. Their applications cut across a wide spectrum of product types, ranging from consumer appliances to industrial utilities, from milliwatts to megawatts, from hand-held tools to satellite communications.

By definition, a power supply is a device that converts the output from an ac power line to a steady dc output or multiple outputs. The ac voltage is first rectified to provide a pulsating dc, and then filtered to produce a smooth voltage. Finally, the voltage is regulated to produce a constant output level despite variations in the ac line voltage or circuit loading. Figure 20.1 illustrates the process of rectification, filtering, and regulation in a dc power supply. The transformer, rectifier, and filtering circuits are discussed in other chapters. In this chapter, we will concentrate on the operation and characteristics of the regulator stage of a dc power supply.

In general, the regulator stage of a dc power supply consists of a feedback circuit, a stable reference voltage, and a control circuit to drive a pass element (a solid-state device such as transistor or MOSFET). The regulation is done by sensing variations appearing at the output of the dc power supply. A control signal is produced to drive the pass element to cancel any variation. As a result, the output of the dc power supply is maintained essentially constant. In a transistor regulator, the pass element is a transistor, which can be operated in its active region or as a switch, to regulate the output voltage. When the transistor operates at any point in its active region, the regulator is referred to as a *linear voltage regulator*. When the transistor operates only at cutoff and at saturation, the circuit is referred to as a *switching regulator*.

Linear voltage regulators can be further classified as either series or shunt types. In a series regulator, the pass transistor is connected in series with the load as shown in Fig. 20.2. Regulation is achieved by sensing a portion of the output voltage through the voltage divider network R_1 and R_2, and comparing this voltage with the reference voltage V_{REF} to produce a resulting error signal that is used to control the conduction of the pass transistor. This way, the voltage drop across the pass transistor is varied and the output voltage delivered to the load circuit is maintained essentially constant.

In the shunt regulator shown in Fig. 20.3, the pass transistor is connected in parallel with the load, and a voltage-dropping resistor R_3 is connected in series with the load. Regulation is achieved by controlling the current conduction of the pass transistor such that the current through R_3 remains essentially constant. This way, the current through the pass transistor is varied and the voltage across the load remains constant.

As opposed to linear voltage regulators, switching regulators employ solid-state devices, which operate as switches, either completely *on* or completely *off*, to perform power conversion. Because the switching devices are not required to operate in their active regions, switching regulators enjoy a much lower power loss than those of linear voltage regulators. Figure 20.4

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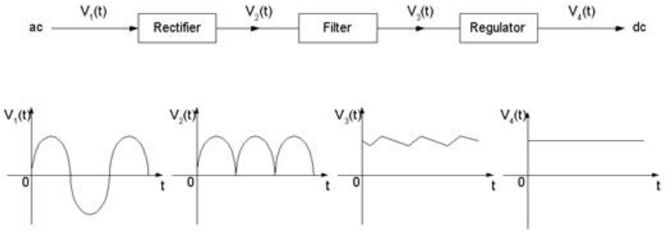


FIGURE 20.1 Block diagram of a dc power supply.

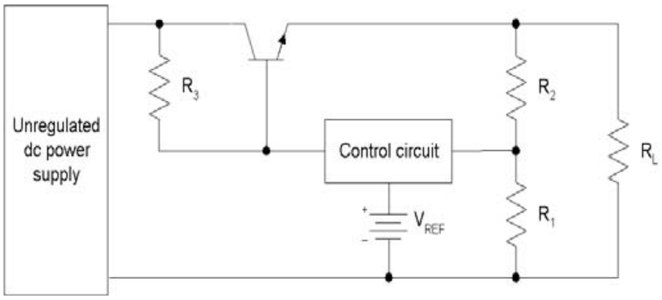


FIGURE 20.2 A linear series voltage regulator.

shows a switching regulator in a simplified form. The high-frequency switch converts the unregulated dc voltage from one level to another dc level at an adjustable duty cycle. The output of the dc supply is regulated by means of a feedback control that employs a pulse-width modulator (PWM) controller, where the control voltage is used to adjust the duty cycle of the switch.

Both linear and switching regulators are capable of performing the same function of converting an unregulated input into a regulated output. However, these two types of regulators have significant differences in properties and performances. In designing power supplies, the choice of using certain type of regulator in a particular design is significantly based on the cost and performance of the regulator itself. In order to use the more appropriate regulator type in the design, it is necessary to understand the requirements of the application and select the type of regulator that best satisfies those requirements. Advantages and disadvantages of linear regulators, as compared to switching regulators, are given below:

1. Linear regulators exhibit efficiency of 20 to 60%, whereas switching regulators have a much higher efficiency, typically 70 to 95%.
2. Linear regulators can only be used as a step-down regulator, whereas switching regulators can be used in both step-up and step-down operations.
3. Linear regulators require a mains-frequency transformer for off-the-line operation. Therefore, they are heavy and bulky. On the other hand, switching regulators use high-frequency transformers and can therefore be small in size.
4. Linear regulators generate little or no electrical noise at their outputs, whereas switching regulators may produce considerable noise if they are not properly designed.
5. Linear regulators are more suitable for applications of less than 20 W, whereas switching regulators are more suitable for large power applications.

In this chapter, we will examine the circuit operation, characteristics, and applications of linear and switching regulators. In Section 20.2, we will look at the basic circuits and properties of linear series voltage regulators. Some current-limiting techniques will be explained. In Section 20.3, linear shunt regulators will be covered. The important characteristics and uses of linear IC regulators will be discussed in Section 20.4. Finally, the operation and characteristics of switching regulators will be discussed in Section 20.5. Important design guidelines for switching regulators will also be given in this section.

2 .2 Linear Series Voltage Regulator

A Zener diode regulator can maintain a fairly constant voltage across a load resistor. It can be used to improve the voltage regulation and reduce the ripple in a power supply. However, the regulation is poor and the efficiency is low because of the nonzero resistance in the Zener diode. To improve the regulation and efficiency of the regulator, we have to limit the Zener

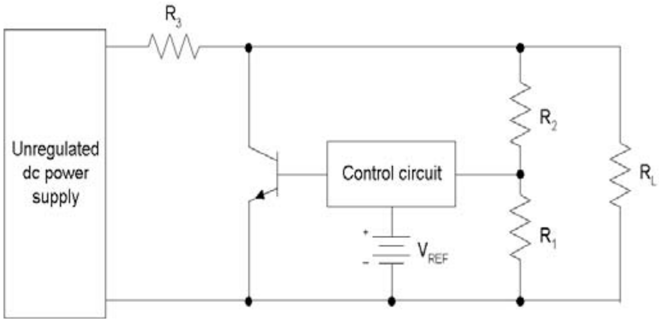


FIGURE 20.3 A linear shunt voltage regulator.

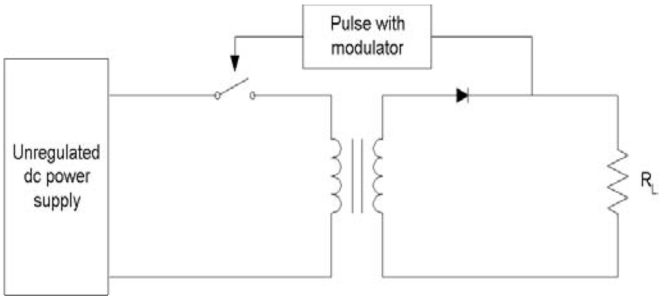


FIGURE 20.4 A simplified form of a switching regulator.

current to a smaller value. This can be accomplished by using an amplifier in series with the load as shown in Fig. 20.5. The effect of this amplifier is to limit the variations of current through the Zener diode. This circuit is known as a linear series voltage regulator because the transistor is in series with the load.

Because of the current-amplifying properties of the transistor, the current in the Zener diode is reduced by a factor of $(\beta + 1)$. Hence there is a little voltage drop across the diode resistance and the Zener diode approximates an ideal voltage source. The output voltage V_o of the regulator is

$$V_o = V_z + V_{BE} \tag{20.1}$$

The change in output voltage is

$$\begin{aligned} \Delta V_o &= \Delta V_z + \Delta V_{BE} \\ &= \Delta I_D r_d + \Delta I_L r_e \end{aligned} \tag{20.2}$$

where r_d is the dynamic resistance of the Zener diode and r_e is the output resistance of the transistor. Assume that V_i and V_z are constant. With $\Delta I_D \approx \Delta I_L/(\beta + 1)$, the change in output voltage is then

$$\Delta V_o \approx \Delta I_L r_e \tag{20.3}$$

If V_i is not constant, then the current I will change with the input voltage. When the change in output voltage is calculated, this current change must be absorbed by the Zener diode.

In designing linear series voltage regulators, it is imperative that the series transistor work within the rated SOA and be protected from excess heat dissipation because of current overloads. The emitter to collector voltage V_{CE} of Q_1 is given by

$$V_{CE} = V_i - V_o \tag{20.4}$$

Thus, with specified output voltage, the maximum allowable V_{CE} for a given Q_1 is determined by the maximum input voltage to the regulator. The power dissipated by Q_1 can be approximated by

$$P_{Q1} \approx (V_i - V_o)I_L \tag{20.5}$$

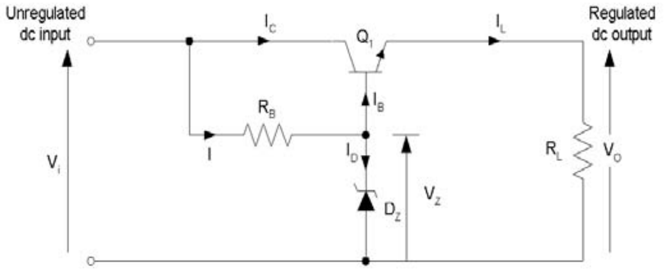


FIGURE 20.5 Basic circuit of a linear series regulator.

Consequently, the maximum allowable power dissipated in Q_1 is determined by the combination of the input voltage V_i and the load current I_L of the regulator. For a low output voltage and a high loading current regulator, the power dissipated in the series transistor is about 50% of the power delivered to the output.

In many high-current, high-voltage regulator circuits, it is necessary to use a Darlington-connected transistor pair so that the voltage, current, and power ratings of the series element are not exceeded. The method is shown in Fig. 20.6. An additional desirable feature of this circuit is that the reference diode dissipation can be reduced greatly. The maximum base current I_{B1} is then $I_L/(h_{FE1} + 1)(h_{FE2} + 1)$. This current is usually of the order of less than 1 mA. Consequently, a low-power reference diode can be used.

2 .2.1 Regulating Control

The series regulators shown in Figs. 20.5 and 20.6 do not have feedback loops. Although they provide satisfactory performance for many applications, their output resistances and ripples cannot be reduced. Figure 20.7 shows an improved form of the series regulator, in which negative feedback is employed to improve the performance. In this circuit, transistors Q_3 and Q_4 form a single-ended differential amplifier, and the gain of this amplifier is established by R_6. Here D_Z is a stable Zener diode reference, biased by R_4. For higher accuracy, D_Z can be replaced by an IC reference such as the REF series from Burr-Brown. Resistors R_1 and R_2 form a voltage divider for output voltage sensing. Finally, transistors Q_1 and Q_2 form a Darlington pair output stage. The operation of the regulator can be explained as follows. When Q_1 and Q_2 are on, the output voltage increases, and hence the voltage V_A at the base of Q_3 also increases. During this time, Q_3 is off and Q_4 is on. When V_A reaches a level that is equal to the reference voltage V_{REF} at the base of Q_4, the base-emitter junction of Q_3 becomes forward-biased. Some Q_1 base current will divert into the collector of Q_3. If the output voltage V_o starts to rise above V_{REF}, Q_3 conduction increases to further decrease the conduction of Q_1 and Q_2, which will in turn maintain output

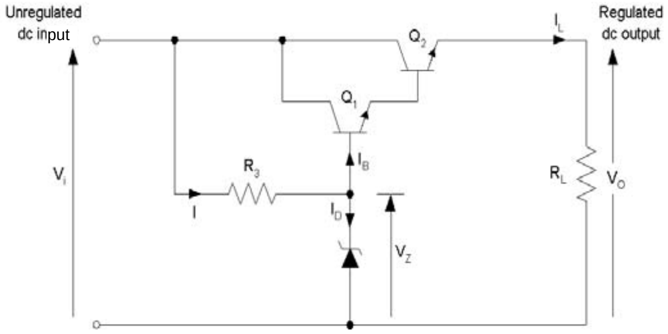


FIGURE 20.6 A linear series regulator with Darlington-connected amplifier.

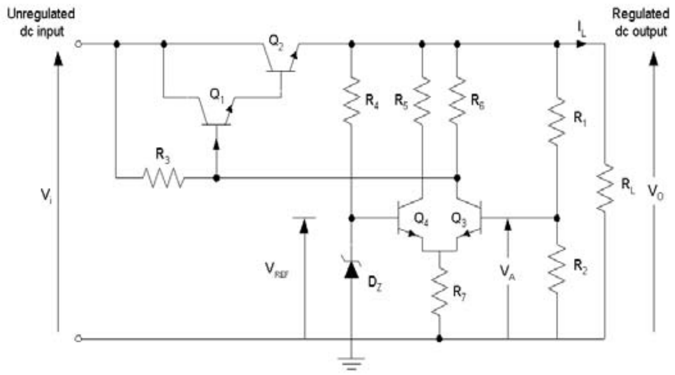


FIGURE 20.7 An improved form of discrete component series regulator.

voltage regulation. Figure 20.8 shows another improved series regulator that uses an operational amplifier (op-amp) to control the conduction of the pass transistor.

One of the problems in the design of linear series voltage regulators is the high-power dissipation in the pass transistors. If an excess load current is drawn, the pass transistor can be quickly damaged or destroyed. In fact, under short-circuit conditions, the voltage across Q_2 in Fig. 20.7 will be the input voltage V_i, and the current through Q_2 will be greater than the rated full-load output current. This current will cause Q_1 to exceed its rated SOA unless the current is reduced. In the next section, some current-limiting techniques will be presented to overcome this problem.

2 .2.2 Current Limiting and Overload Protection

In some series voltage regulators, overloading causes permanent damage to the pass transistors. The pass transistors must be kept from excessive power dissipation under current overloads or short-circuit conditions. A current-limiting mechanism must be used to keep the current through the transistors to a safe value as determined by the power rating of the transistors. The mechanism must be able to respond quickly to protect the transistor and yet permit the regulator to return to normal operation as soon as the overload condition is removed. One of the current-limiting techniques to prevent current overload, called the constant current-limiting method, is shown in Fig. 20.9a. Current-limiting is achieved by the combined action of the components shown inside the dashed line. The voltage developed across the current-limit resistor R_3 and the base-to-emitter voltage of current-limit transistor Q_3 is proportional to the circuit output current I_L. During current overload, I_L reaches a predetermined maximum value that is set by the value of R_3 to cause Q_3 to conduct. As Q_3 starts to conduct, Q_3 shunts a portion of the Q_1 base current. This action, in turn, decreases and limits I_L to a maximum value $I_{L(\max)}$. Since the base-to-emitter voltage V_{BE} of Q_3 cannot exceed 0.7 V, the voltage across R_3 is held at this value and $I_{L(\max)}$ is limited to

$$I_{L(\max)} = \frac{0.7\,\mathrm{V}}{R_3} \tag{20.6}$$

Consequently, the value of the short-circuit current is selected by adjusting the value of R_3. The voltage–current characteristic of this circuit is shown in Fig. 20.9b.

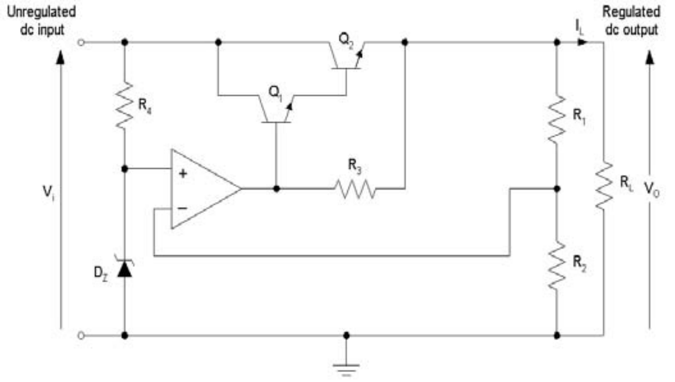
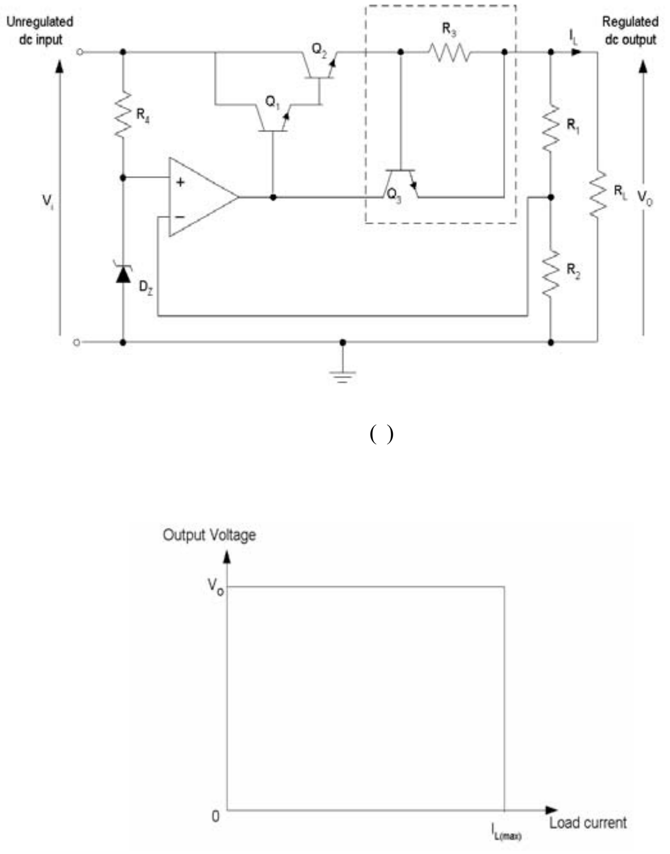


FIGURE 20.8 An improved form of op-amp series regulator.



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(b)

FIGURE 20.9 Series regulator with constant current limiting: (a) circuit, (b) voltage–current characteristic.

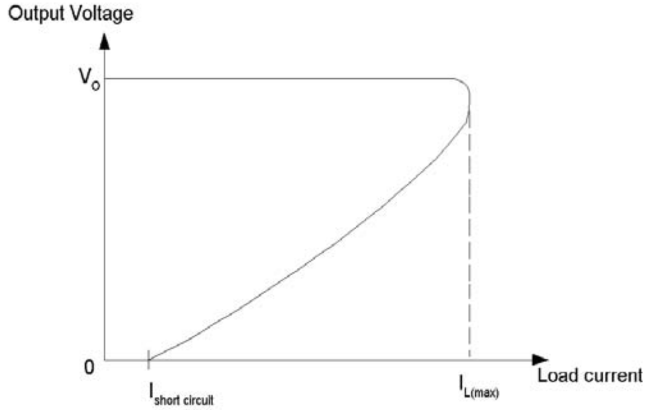


FIGURE 20.10 Voltage–current characteristic of foldback current-limit.

In many high-current regulators, foldback current-limiting is always used to protect against excessive current. This technique is similar to constant current-limiting, except that as the output voltage is reduced as a result of load impedance moving toward zero, the load current is also reduced. Therefore, a series voltage regulator that includes a foldback current-limiting circuit has the voltage–current characteristic shown in Fig. 20.10. The basic idea of foldback current-limiting, with reference to Fig. 20.11, can be explained as follows. The foldback current-limiting circuit (in dashed outline) is similar to the constant current-limiting circuit, with the exception of resistors R_5 and R_6. At low output current, the current-limit transistor Q_3 is cut off. A voltage proportional to the output current I_L is developed across the current-limit resistor R_3. This voltage is applied to the base of Q_3 through the divider network R_5 and R_6. At the point of transition into current limit, any further increase in I_L will increase the voltage across R_3 and hence across R_5, and Q_3 will be progressively turned on. As Q_3 conducts, it shunts a portion of the Q_1 base current. This action, in turn, causes the output voltage to fall. As the output voltage falls, the voltage across R_6 decreases and the current in R_6 also decreases, and more current is shunted into the base of Q_3. Hence, the current required in R_3 to maintain the conduction state of Q_3 is also decreased. Consequently, as the load resistance is reduced, the output voltage and current fall, and the current-limit point decreases toward a minimum when the output voltage is short-circuited. In summary, any regulator using foldback current-limiting can have peak load current up to $I_{L(\max)}$. But when the output becomes shorted, the current drops to a lower value to prevent overheating of the series transistors.

2 .3 Linear Shunt Voltage Regulator

The second type of linear voltage regulator is the shunt regulator. In the basic circuit shown in Fig. 20.12, the pass transistor Q_1 is connected in parallel with the load. A voltage-dropping resistor R_3 is in series with this parallel network. The operation of the circuit is similar to that of the series regulator, except that regulation is achieved by controlling the current through Q_1. The operation of the circuit can be explained as follows. When the output voltage tries to increase because of a change in load resistance, the voltage at the noninverting terminal of the operational amplifier also increases. This voltage is compared with a reference voltage and the resulting difference voltage causes Q_1 conduction to increase. With constant V_i and V_o, I_L will decrease and V_o will remain constant. The opposite action occurs when V_o tries to decrease. The voltage appearing at the base of Q_1 causes its conduction to decrease. This action offsets the attempted decrease in V_0 and maintains it at an almost constant level.

Analytically, the current flowing in R_3 is

$$I_{R3} = I_{Q1} + I_L \tag{20.7}$$

and

$$I_{R3} = \frac{V_i - V_o}{R_3} \tag{20.8}$$

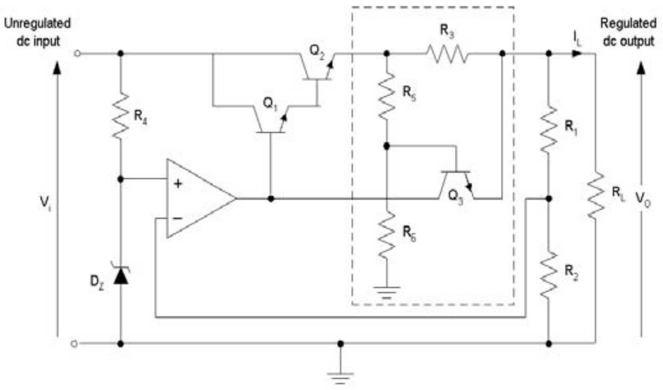


FIGURE 20.11 Series regulator with foldback current limiting.

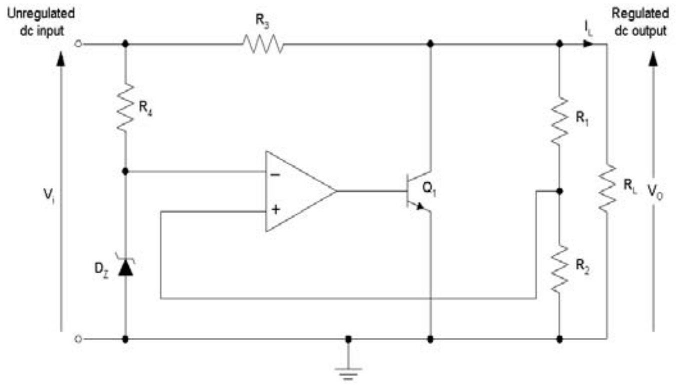


FIGURE 20.12 Basic circuit of a linear shunt regulator.

With I_L and V_o constant, a change in V_i will cause a change in I_{Q1}:

$$\Delta I_{Q1} = \frac{\Delta V_i}{R_3} \tag{20.9}$$

With V_i and V_o constant,

$$\Delta I_{Q1} = -\Delta I_L \tag{20.10}$$

Equation (20.10) shows that if I_{Q1} increases, I_L decreases, and vice versa. Although shunt regulators are not as efficient as series regulators for most applications, they have the advantage of greater simplicity. This topology offers inherent short-circuit protection. If the output is shorted, the load current is limited by the series resistor R_3 and is given by

$$I_{L(\max)} = \frac{V_i}{R_3} \tag{20.11}$$

The power dissipated by Q_1 can be approximated by

$$\begin{aligned} P_{Q1} &\approx V_o I_C \\ &= V_o(I_{R3} - I_L) \end{aligned} \tag{20.12}$$

For a low value of I_L, the power dissipated in Q_1 is large and the efficiency of the regulator may drop to 10% under this condition.

To improve the power handling of the shunt transistor, one or more transistors connected in the common-emitter configuration in parallel with the load can be employed, as shown in Fig. 20.13.

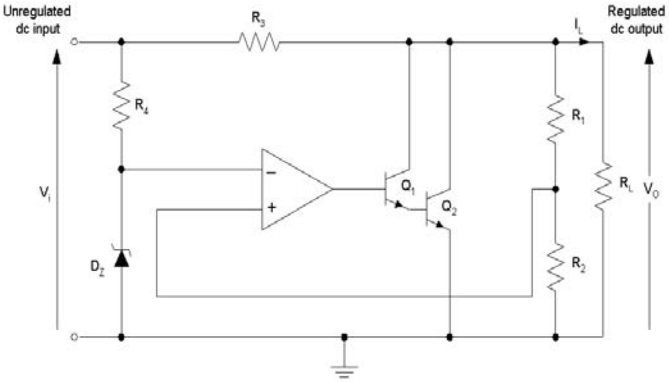


FIGURE 20.13 Linear shunt regulator with two transistors as shunt element.

2 .4 Integrated Circuit Voltage Regulators

The linear series and shunt voltage regulators presented in the previous sections have been developed by various solid-state device manufacturers and are available in integrated circuit (IC) form. Like discrete voltage regulators, linear IC voltage regulators maintain an output voltage at a constant value despite variations in load and input voltage.

In general, linear IC voltage regulators are three-terminal devices that provide regulation of a fixed positive voltage, a fixed negative voltage, or an adjustable set voltage. The basic connection of a three-terminal IC voltage regulator to a load is shown in Fig. 20.14. The IC regulator has an unregulated input voltage V_i applied to the input terminals, a regulated voltage V_o at the output, and a ground connected to the third terminal. Depending on the selected IC regulator, the circuit can be operated with load currents ranging from milliamperes to tens of amperes and output power from milliwatts to tens of watts. Note that the internal construction of IC voltage regulators may be somewhat more complex and different from that previously described for discrete voltage regulator circuits. However, the external operation is much the same. In this section, some typical linear IC regulators are presented and their applications are also given.

2 .4.1 Fixed Positive and Negative Linear Voltage Regulators

The 78XX series of regulators provide fixed regulated voltages from 5 to 24 V. The last two digits of the IC part number denote the output voltage of the device. For example, a 7824 IC regulator produces a +24 V regulated voltage at the output. The standard configuration of a 78XX fixed positive voltage regulator is shown in Fig. 20.15. The input capacitor C_1 acts as a line filter to prevent unwanted variations in the input line, and the output capacitor C_2 is used to filter the high-frequency noise that may appear at the output. In order to ensure proper operation, the input voltage of the regulator

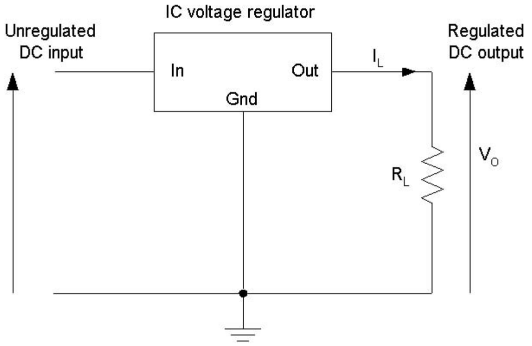


FIGURE 20.14 Basic connection of a three-terminal IC voltage regulator.

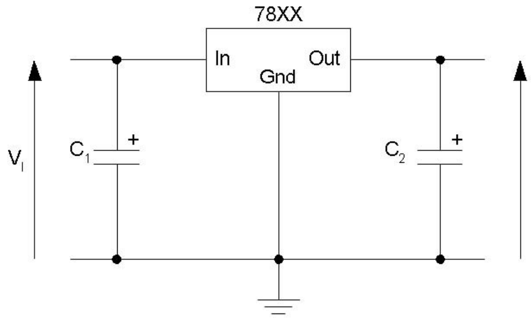


FIGURE 20.15 The 78XX series fixed positive voltage regulator.

must be at least 2 V above the output voltage. Table 20.1 shows the minimum and maximum input voltages of the 78XX series fixed positive voltage regulator.

The 79XX series voltage regulator is identical to the 78XX series except that it provides negative regulated voltages instead of positive ones. Figure 20.16 shows the standard configuration of a 79XX series voltage regulator. A list of 79XX series regulators is provided in Table 20.2. The regulation of the circuit can be maintained as long as the output voltage is at least 2 to 3 V greater than the input voltage.

2 .4.2 Adjustable Positive and Negative Linear Voltage Regulators

IC voltage regulators are also available in circuit configurations that allow the user to set the output voltage to a desired regulated value. The LM317 adjustable positive voltage regulator, for example, is capable of supplying an output current of more than 1.5 A over an output voltage range of 1.2 to 37 V. Figure 20.17 shows how the output voltage of an LM317 can be adjusted by using two external resistors R_1 and R_2. The capacitors C_1 and C_2 have the same function as those in the fixed linear voltage regulator.

TABLE 20.1 Minimum and maximum input voltages for 78XX series regulators

Type Number	Output Voltage $V_o(V)$	Minimum V_i (V)	Maximum V_i (V)
7805	+5	7	20
7806	+6	8	21
7808	+8	10.5	25
7809	+9	10.5	25
7812	+12	14.5	27
7815	+15	17.5	30
7818	+18	21	33
7824	+24	27	38

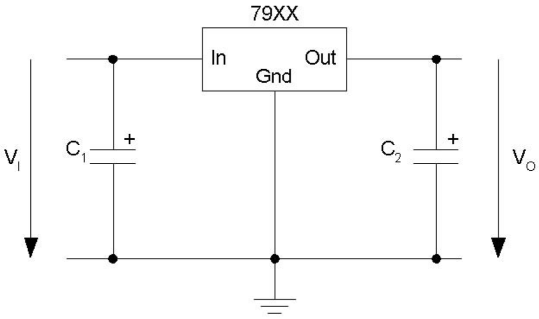


FIGURE 20.16 The 79XX series fixed negative voltage regulator.

TABLE 20.2 Minimum and maximum input voltages for 79XX series regulators

Type Number	Output Voltage (V) $V_o(V)$	Minimum V_i (V)	Maximum V_i (V)
7905	−5	−7	−20
7906	−6	−8	−21
7908	−8	−10.5	−25
7909	−9	−11.5	−25
7912	−12	−14.5	−27
7915	−15	−17.5	−30
7918	−18	−21	−33
7924	−24	−27	−38

As indicated in Fig. 20.17, the LM317 has a constant 1.25 V reference voltage, V_{REF}, across the output and the adjustment terminals. This constant reference voltage produces a constant current through R_1 regardless of the value of R_2. The output voltage V_o is given by

$$V_o = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{adj}R_2 \tag{20.13}$$

where I_{adj} is a constant current into the adjustment terminal and has a value of approximately 50 μA for the LM317. As can be seen from (20.13), with fixed R_1, V_o can be adjusted by varying R_2.

The LM337 adjustable voltage regulator is similar to the LM317 except that it provides negative regulated voltages instead of positive ones. Figure 20.18 shows the standard configuration of a LM337 voltage regulator. The output voltage can be adjusted from −1.2 to −37 V, depending on the external resistors R_1 and R_2.

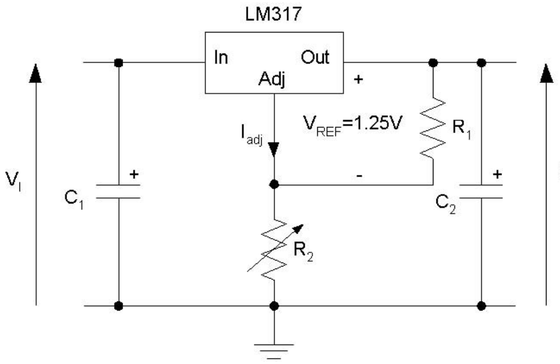


FIGURE 20.17 The LM317 adjustable positive voltage regulator.

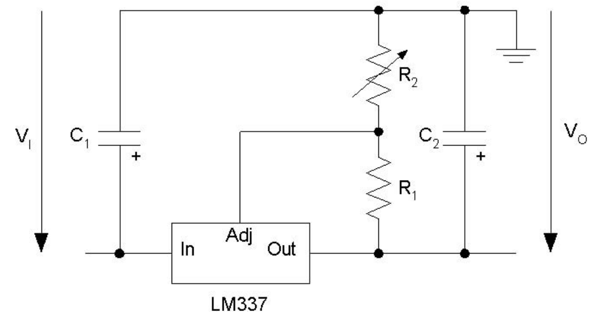


FIGURE 20.18 The LM337 adjustable negative voltage regulator.

2 .4.3 Applications of Linear IC Voltage Regulators

Most IC regulators are limited to an output current of 2.5 A. If the output current of an IC regulator exceeds its maximum allowable limit, its internal pass transistor will dissipate an amount of energy more than it can tolerate. As a result, the regulator will be shut down.

For applications that require more than the maximum allowable current limit of a regulator, an external pass transistor can be used to increase the output current. Figure 20.19 illustrates such a configuration. This circuit has the capability of producing higher current to the load, but still preserving the thermal shutdown and short-circuit protection of the IC regulator.

A constant current-limiting scheme, as discussed in Section 20.2.2, is implemented by using the transistor Q_2 and the resistor R_2 to protect the external pass transistor Q_1 from excessive current under current-overload or short-circuit conditions. The value of the external current-sensing resistor R_1 determines the value of current at which Q_1 begins to conduct. As long as the current is less than the value set by R_1, the transistor Q_1 is off, and the regulator operates normally as shown in Fig. 20.15. But when the load current I_L starts to increase, the voltage across R_1 also increases. This turns on the external transistor Q_1 and conducts the excess current. The value of R_1 is determined by

$$R_1 = \frac{0.7\,\mathrm{V}}{I_{\max}} \tag{20.14}$$

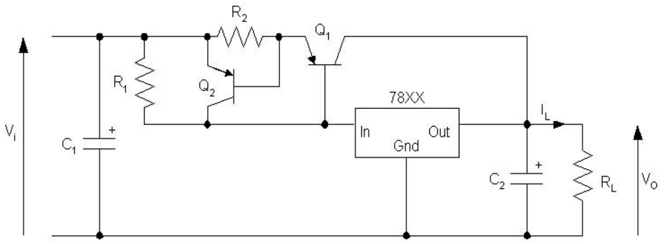


FIGURE 20.19 A 7800 series regulator with an external pass transistor.

where $I_{\max}$ is the maximum current that the voltage regulator can handle internally.

2 .5 Switching Regulators

The linear series and shunt regulators have control transistors that are operating in their linear active regions. Regulation is achieved by varying the conduction of the transistors to maintain the output voltage at a desirable level. The switching regulator is different in that the control transistor operates as a switch, either in the cutoff or the saturation region. Regulation is achieved by adjusting the *on* time of the control transistor. In this mode of operation, the control transistor does not dissipate as much power as that in the linear types. Therefore, switching voltage regulators have a much higher efficiency and can provide greater load currents at low voltage than linear regulators.

Unlike their linear counterparts, switching regulators can be implemented by many different topologies such as forward and flyback. In order to select an appropriate topology for an application, it is necessary to understand the merits and drawbacks of each topology and the requirements of the application. Basically, most topologies can work for various applications. Therefore, we have to determine from the factors such as cost, performances, and application that make one topology more desirable than the others. However, no matter which topology we decide to use, the basic building blocks of an off-the-line switching power supply are the same, as depicted in Fig. 20.1.

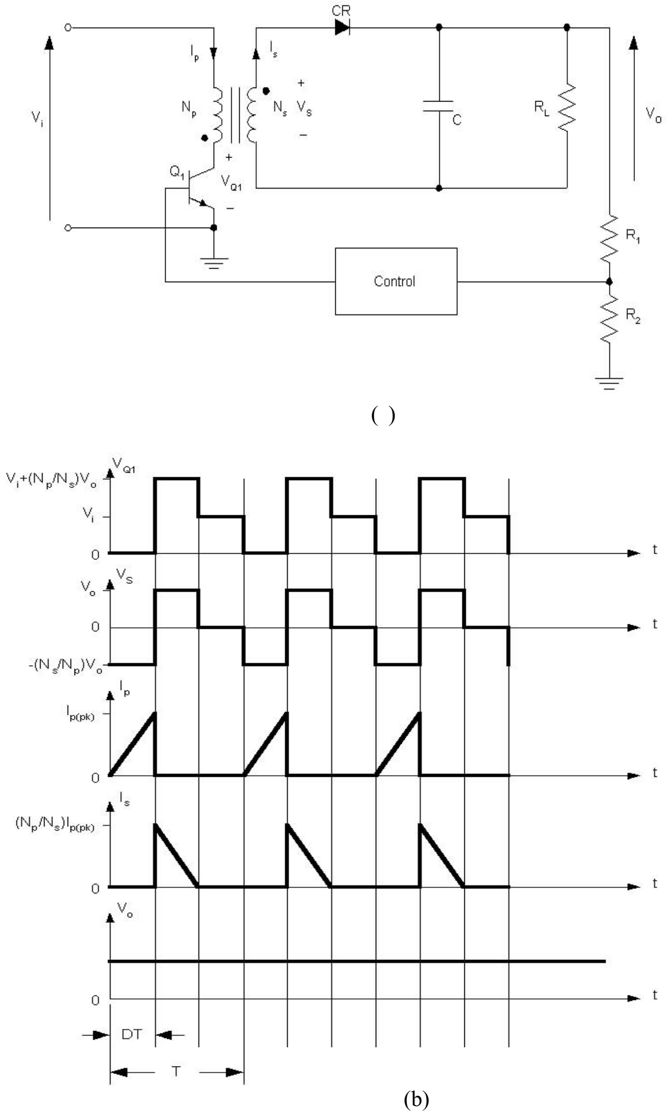
In this section, some popular switching regulator topologies, namely flyback, forward, half-bridge, and full-bridge topologies, are presented. Their basic operation is described, and the critical waveforms are shown and explained. The merits, drawbacks, and application areas of each topology are discussed. Finally, the control circuitry and pulse-width modulation (PWM) of the regulators are also discussed.

2 .5.1 Single-Ended Isolated Flyback Regulators

An isolated flyback regulator consists of four main circuit elements: a power switch, a rectifier diode, a transformer, and a filter capacitor. The power switch, which can be either a power transistor or a MOSFET, is used to control the flow of energy in the circuit. A transformer is placed between the input source and the power switch to provide DC isolation between the input and the output circuits. In addition to being an energy storage element, the transformer also performs a stepping up or down function for the regulator. The rectifier diode and filter capacitor form an energy transfer mechanism to supply energy to maintain the load voltage and current of the supply. Note that there are two distinct operating modes for flyback regulators: *continuous* and *discontinuous*. However, both modes have an identical circuit. It is only the transformer magnetizing current that determines the operating mode of the regulator. Figure 20.20a shows a simplified isolated flyback regulator. The associated steady-state waveforms, resulting from *discontinuous-mode* operation, is shown in Fig. 20.20b. As shown in the figure, the voltage regulation of the regulator is achieved by a control circuit, which controls the conduction period or duty cycle of the switch, to keep the output voltage at a constant level. For clarity, the schematics and operation of the control circuit will be discussed in a separate section.

2 .5.1.1 Discontinuous-Mode Flyback Regulators

Under steady-state conditions, the operation of the regulator can be explained as follows. When the power switch Q_1 is on, the primary current I_p starts to build up and stores energy in the primary winding. Because of the opposite-polarity arrangement between the input and output windings of the transformer, the rectifier diode *CR* is reverse biased. In this period of time, there is no energy transferred from the input to the load R_L. The output voltage is supported by the load current I_L, which is supplied from the output filter capacitor *C*. When Q_1 is turned off, the polarity of the windings reverses as a result of the fact that I_p cannot change instantaneously. This causes *CR* to turn on. Now *CR* is conducting, charging the output capacitor *C* and delivering current to R_L. This charging action ends at the point where all the magnetic energy stored in the secondary winding during the first half-cycle is emptied. At this point, *CR* will cease to conduct and R_L absorbs energy just from *C* until Q_1 is switched on again.



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(b)

FIGURE 20.20 A simplified isolated flyback regulator: (a) circuit, (b) associated waveforms.

During the Q_1 on time, the voltage across the primary winding of the transformer is V_i. The current in the primary winding I_p increases linearly and is given by

$$I_p = \frac{V_i t_{on}}{L_p} \tag{20.15}$$

where L_p is the primary magnetizing inductance. At the end of the on time, the primary current reaches a value equal to $I_{p(pk)}$ and is given by

$$I_{p(pk)} = \frac{V_i DT}{L_p} \tag{20.16}$$

where *D* is the duty cycle and *T* is the switching period. Now when Q_1 turns off, the magnetizing current in the transformer forces the reversal of polarities on the windings. At the instant of turn-off, the amplitude of the secondary current $I_{s(pk)}$ is

$$I_{s(pk)} = \left(\frac{N_p}{N_s}\right) I_{p(pk)} \tag{20.17}$$

This current decreases linearly at a rate of

$$\frac{dI_s}{dt} = \frac{V_o}{L_s} \tag{20.18}$$

where L_s is the secondary magnetizing inductance.

In the discontinuous-mode operation, $I_{s(pk)}$ will decrease linearly to zero before the start of the next cycle. Since the energy transfer from the source to the output takes place only in the first half-cycle, the power drawn from V_i is then

$$P_{in} = \frac{\frac{1}{2} L_p I_p^2}{T} \tag{20.19}$$

Substituting (20.15) into (20.19), we have

$$P_{in} = \frac{(V_i t_{on})^2}{2TL_p} \tag{20.20}$$

The output power P_o may be written as

$$\begin{aligned} P_o &= \eta P_{in} \\ &= \frac{\eta (V_i t_{on})^2}{2TL_p} = \frac{V_o^2}{R_L} \end{aligned} \tag{20.21}$$

where η is the efficiency of the regulator. Then, from (20.21), the output voltage V_o is related to the input voltage V_i by

$$V_o = V_i D \sqrt{\frac{\eta R_L T}{2L_p}} \tag{20.22}$$

Since the collector voltage V_{Q1} of Q_1 is maximum when V_i is maximum, the maximum collector voltage $V_{Q1(\max)}$, as shown in Fig. 20.20b, is given by

$$V_{Q1(\max)} = V_{i(\max)} + \left(\frac{N_p}{N_s}\right) V_o \tag{20.23}$$

The primary peak current $I_{p(pk)}$ can be found in terms of P_o by combining (20.16) and (20.21) and then eliminating L_p as

$$\begin{aligned} I_{p(pk)} &= \frac{2V_o^2}{\eta V_i D R_L} \\ &= \frac{2P_o}{\eta V_i D} \end{aligned} \tag{20.24}$$

The maximum collector current $I_{c(\max)}$ of the power switch Q_1 at turn-on is

$$\begin{aligned} I_{C(\max)} &= I_{p(pk)} \\ &= \frac{2P_o}{\mu V_i D} \end{aligned} \tag{20.25}$$

As can be seen from (20.21), V_o will maintain constant by keeping the product $V_i t_{on}$ constant. Since maximum on time $t_{on(\max)}$ occurs at minimum supply voltage $V_{i(\min)}$, the maximum allowable duty cycle for the discontinuous mode can be found from (20.22) as

$$D_{\max} = \frac{V_o}{V_{i(\min)}} \sqrt{\frac{2L_p}{\eta R_L T}} \tag{20.26}$$

and V_o at $D_{\max}$ is then

$$V_o = V_{i(\min)} D_{\max} \sqrt{\frac{\eta R_L T}{2L_p}} \tag{20.27}$$

2 .5.1.2 Continuous-Mode Flyback Regulators

In the continuous-mode operation, the power switch is turned on before all the magnetic energy stored in the secondary winding empties itself. The primary and secondary current waveforms have a characteristic appearance as shown in Fig. 20.21. This mode produces a higher power capability without increasing I_{pk}. During the on time, the primary current I_p rises linearly from its initial value $I_p(0)$ and is given by

$$I_p = I_p(0) + \frac{V_i t_{on}}{L_p} \tag{20.28}$$

At the end of the on time, the primary current reaches a value equal to $I_{p(pk)}$ and is given by

$$I_{p(pk)} = I_p(0) + \frac{V_i DT}{L_p} \tag{20.29}$$

In general, $I_p(0) \gg V_i DT/L_p$; thus, (20.29) can be written as

$$I_{p(pk)} \approx I_p(0) \tag{20.30}$$

The secondary current $I_{s(pk)}$ at the instant of turn-off is given by

$$\begin{aligned} I_{s(pk)} &= \left(\frac{N_p}{N_s}\right) I_{p(pk)} \\ &= \left(\frac{N_p}{N_s}\right)\left(I_p(0) + \frac{V_i DT}{L_p}\right) \\ &= \left(\frac{N_p}{N_s}\right) I_p(0) \end{aligned} \tag{20.31}$$

This current decreases linearly at a rate of

$$\frac{dI_s}{dt} = -\frac{V_o}{L_s} \tag{20.32}$$

The output power P_o is equal to V_o times the time average of the secondary current pulses and is given by

$$\begin{aligned} P_o &= V_o I_s \frac{T - t_{on}}{T} \\ &\approx V_o I_{s(pk)} \frac{T - t_{on}}{T} \end{aligned} \tag{20.33}$$

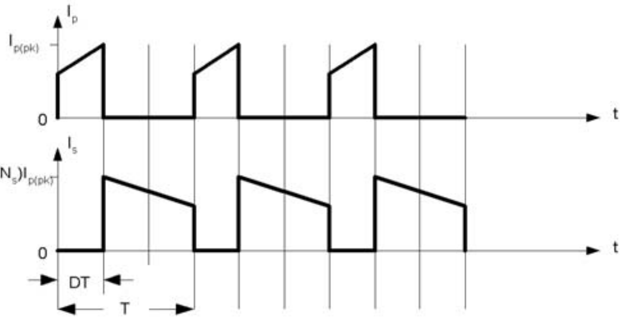

FIGURE 20.21 The primary and secondary winding currents of a flyback regulator operated in the continuous mode.

or

$$I_{s(pk)} = \frac{P_o}{V_o(1 - t_{on}/T)} \tag{20.34}$$

For an efficiency of η, the input power P_{in} is

$$\begin{aligned} P_{in} &= \frac{P_o}{\eta} \\ &= V_i I_p \frac{t_{on}}{T} \\ &\approx V_i I_{p(pk)} \frac{t_{on}}{T} \end{aligned} \tag{20.35}$$

or

$$I_{p(pk)} = \frac{P_o}{\eta V_i (t_{on}/T)} \tag{20.36}$$

Combining (20.31), (20.34), and (20.36) and solving for V_0, we have

$$V_o = \left(\frac{N_s}{N_p}\right) \frac{\eta V_i D}{1 - D} \tag{20.37}$$

The output voltage at $D_{\max}$ is then

$$V_o = \left(\frac{N_s}{N_p}\right) \frac{\eta V_{i(\min)} D_{\max}}{1 - D_{\max}} \tag{20.38}$$

The maximum collector current $I_{C(\max)}$ for the continuous mode is then given by

$$\begin{aligned} I_{C(\max)} &= I_{p(pk)} \\ &= \frac{P_o}{\eta V_i D_{\max}} \end{aligned} \tag{20.39}$$

The maximum collector voltage of Q_1 is the same as that in the discontinuous mode and is given by

$$V_{Q1(\max)} = V_{i(\max)} + \left(\frac{N_p}{N_s}\right) V_o \tag{20.40}$$

The maximum allowable duty cycle for the continuous mode can be found from (20.38) and is given by

$$D_{\max} = \frac{1}{1 + \left(\frac{N_s}{N_p}\right) \frac{\eta V_{i(\min)}}{V_o}} \tag{20.41}$$

At the transition from the discontinuous mode to continuous mode, the relationships in (20.27) and (20.38) must hold. Thus, equating these two equations, we have

$$V_{i(\min)} D_{\max} \sqrt{\frac{\eta R_L T}{2L_p}} = \frac{N_s}{N_p} \frac{D_{\max}}{1 - D_{\max}} \eta V_{i(\min)} \tag{20.42}$$

Solving this equation for L_p, we have

$$\begin{aligned} L_{p(\text{limit})} &= \frac{1}{2\eta} T R_L \left[(1 - D_{\max}) \frac{N_p}{N_s}\right]^2 \\ &= \frac{1}{2\eta} T \frac{V_o^2}{P_o} \left[(1 - D_{\max}) \frac{N_p}{N_s}\right]^2 \end{aligned} \tag{20.43}$$

Replacing V_o with (20.38) and solving for $I_{p(\text{limit})}$, we have

$$L_{p(\text{limit})} = \frac{1}{2} \eta T \frac{D_{\max}^2 V_{i(\min)}^2}{P_o} \tag{20.44}$$

Then, for a given $D_{\max}$, input, and output quantities, the inductance value $I_{p(\text{limit})}$ in (20.44) determines the mode of operation for the regulator. If $L_p < I_{p(\text{limit})}$, then the circuit is operated in the discontinuous mode. Otherwise, if $L_p > I_{p(\text{limit})}$, the circuit is operated in the continuous mode.

In designing flyback regulators, regardless of their operating modes, the power switch must be able to handle the peak collector voltage at turn-off and the peak collector currents at turn-on as shown in (20.23), (20.25), (20.39), and (20.40). The flyback transformer, because of its unidirectional use of the *B–H* curve, has to be designed so that it will not be driven into saturation. To avoid saturation, the transformer needs a relatively large core with an air gap in it.

Although the continuous and discontinuous modes have an identical circuit, their operating properties differ significantly. As opposed to the discontinuous mode, the continuous mode can provide higher power capability without increasing the peak current I_{pk}. It means that, for the same output power, the peak currents in the discontinuous mode are much higher than those operated in the continuous mode. As a result, a higher current rating and, therefore, a more expensive power transistor is needed. Moreover, the higher secondary peak currents in the discontinuous mode will have a larger transient spike at the instant of turn-off. However, despite all these problems, the discontinuous mode is still much more widely used than its continuous-mode counterpart. There are two main reasons. First, as mentioned earlier, the inherently smaller magnetizing inductance gives the discontinuous mode a quicker response and a lower transient output voltage spike to sudden changes in load current or input voltage. Second, the continuous mode has a right-half-plane zero in its transfer function, which makes the feedback control circuit more difficult to design.

The flyback configuration is mostly used in applications with output power below 100 W. It is widely used for high output voltages at relatively low power. The essential attractions of this configuration are its simplicity and low cost. Since no output filter inductor is required for the secondary, there is a significant saving in cost and space, especially for multiple output power supplies. Since there is no output filter inductor, the flyback exhibits high ripple currents in the transformer and at the output. Thus, for higher power applications, the flyback becomes an unsuitable choice. In practice, a small L_1C filter is added after the filter capacitor C in order to suppress high-frequency switching noise spikes.

As mentioned previously, the collector voltage of the power transistor must be able to sustain a voltage as defined in (20.23). In cases where the voltage is too high for the transistor to handle, the double-ended flyback regulator shown in Fig. 20.22 may be used. The regulator uses two transistors that are switched on or off simultaneously. The diodes CR_1 and CR_2 are used to restrict the maximum collector voltage to V_i. Therefore, the transistors with a lower voltage rating can be used in the circuit.

2 .5.2 Single-Ended Isolated Forward Regulators

Although the general appearance of an isolated forward regulator resembles that of its flyback counterpart, their operations are different. The key difference is that the dot on the secondary winding of the transformer is so arranged that the output diode is forward-biased when the voltage across the primary is positive, that is, when the transistor is *on*. Energy is thus not stored in the primary inductance as it was for the flyback. The transformer acts strictly as a transformer. An inductive energy storage element is required at the output for proper and efficiency energy transfer.

Unlike the flyback, the forward regulator is very suitable for working in the continuous mode. In the discontinuous mode, the forward regulator is more difficult to control because of a double pole at the output filter. Thus, it is not as much used as the continuous mode. In view of this, only the continuous mode will be discussed here.

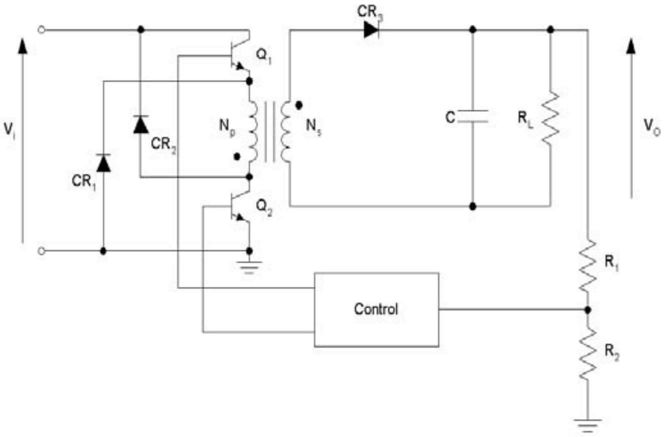

FIGURE 20.22 Double-ended flyback regulator.

Figure 20.23 shows a simplified isolated forward regulator and the associated steady-state waveforms for continuous-mode operation. Again, for clarity, the details of the control circuit are omitted from the figure. Under steady-state condition, the operation of the regulator can be explained as follows. When the power switch Q_1 turns on, the primary current I_p starts to build up and stores energy in the primary winding. Because of the same-polarity arrangement of the primary and secondary windings, this energy is forward-transferred to the secondary and onto the L_1C filter and the load R_L through the rectifier diode CR_2, which is forward biased. When Q_1 turns off, the polarity of the transformer winding voltage reverses. This causes CR_2 to turn off and CR_1 and CR_3 to turn on. Now CR_3 is conducting and delivering energy to R_L through the inductor L_1. During this period, the diode CR_1 and the tertiary winding provide a path for the magnetizing current returning to the input.

When the transistor Q_1 is turned on, the voltage across the primary winding is V_i. The secondary winding current is reflected into the primary, and the reaction current I_p, as shown in Fig. 20.24, is given by

$$I_p = \frac{N_s}{N_p} I_s \tag{20.45}$$

The magnetizing current in the primary has a magnitude of I_{mag} and is given by

$$I_{mag} = \frac{V_i t_{on}}{L_p} \tag{20.46}$$

The total primary current I'_p is then

$$\begin{aligned} I'_p &= I_p + I_{mag} \\ &= \frac{N_s}{N_p} I_s + \frac{V_i t_{on}}{L_p} \end{aligned} \tag{20.47}$$

The voltage developed across the secondary winding is

$$V_s = \frac{N_s}{N_p} V_i \tag{20.48}$$

Neglecting diode voltage drops and losses, the voltage across the output inductor is $V_s - V_o$.

The current in L_1 increases linearly at a rate of

$$I_{L1} = \frac{(V_s - V_o) t_{on}}{L_1} \tag{20.49}$$

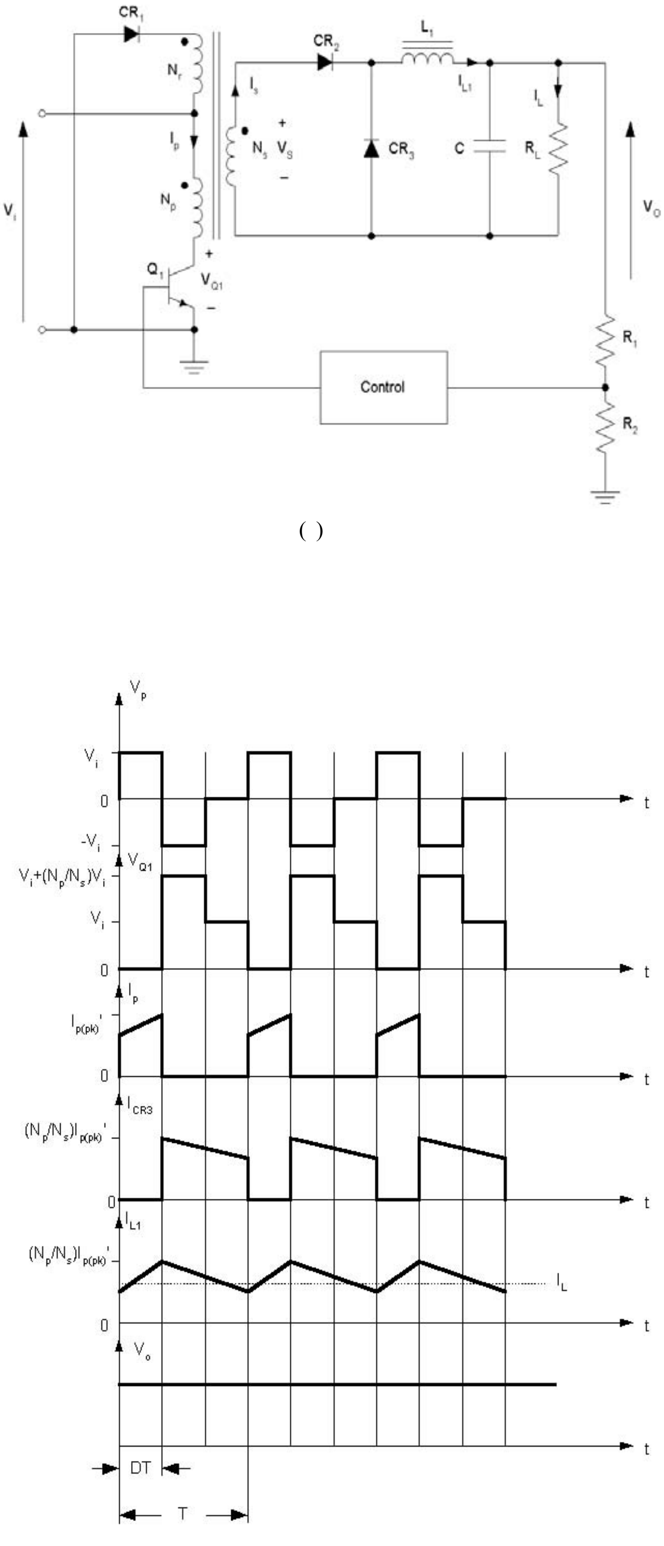

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FIGURE 20.23 A simplified isolated forward regulator: (a) circuit, (b) associated waveforms.

At the end of the on-time, the total primary current reaches a peak value equal to $I'_{p(pk)}$ and is given by

$$I'_{p(pk)} = I'_p(0) + \frac{V_i DT}{L_p} \tag{20.50}$$

The output inductor current I_{L1} is

$$I_{L1(pk)} = I_{L1}(0) + \frac{(V_s - V_o)DT}{L_1} \tag{20.51}$$

At the instant of turn-on, the amplitude of the secondary current has a value of $I_{s(pk)}$ and is given by

$$\begin{aligned} I_{s(pk)} &= \left(\frac{N_p}{N_s}\right) I'_{p(pk)} \\ &= \left(\frac{N_p}{N_s}\right)\left[I'_p(0) + \frac{V_i DT}{L_p}\right] \end{aligned} \tag{20.52}$$

During the off-time, the current I_{L1} in the output inductor is equal to the current I_{CR3} in the rectifier diode CR_3 and both decrease linearly at a rate of

$$\begin{aligned} \frac{dI_{L1}}{dt} &= \frac{dI_{CR3}}{dt} \\ &= -\frac{V_o}{L_1} \end{aligned} \tag{20.53}$$

The output voltage V_o can be found from the time integral of the secondary winding voltage over a time equal to DT of the switch Q_1. Thus, we have

$$\begin{aligned} V_o &= \frac{1}{T}\int_0^{DT} \frac{N_s}{N_p} V_i dt \\ &= \frac{N_s}{N_p} V_i D \end{aligned} \tag{20.54}$$

The maximum collector current $I_{C(\max)}$ at turn-on is equal to $I'_{p(pk)}$ and is given by

$$\begin{aligned} I_{C(\max)} &= I'_{p(pk)} \\ &= \left(\frac{N_s}{N_p}\right)\left[I'_p(0) + \frac{V_i DT}{L_p}\right] \end{aligned} \tag{20.55}$$

The maximum collector voltage $V_{Q1(\max)}$ at turn-off is equal to the maximum input voltage $V_{i(\max)}$ plus the maximum voltage $V_{t(\max)}$ across the tertiary winding and is given by

$$\begin{aligned} V_{Q1(\max)} &= V_{i(\max)} + V_{t(\max)} \\ &= V_{i(\max)}\left(1 + \frac{N_p}{N_t}\right) \end{aligned} \tag{20.56}$$

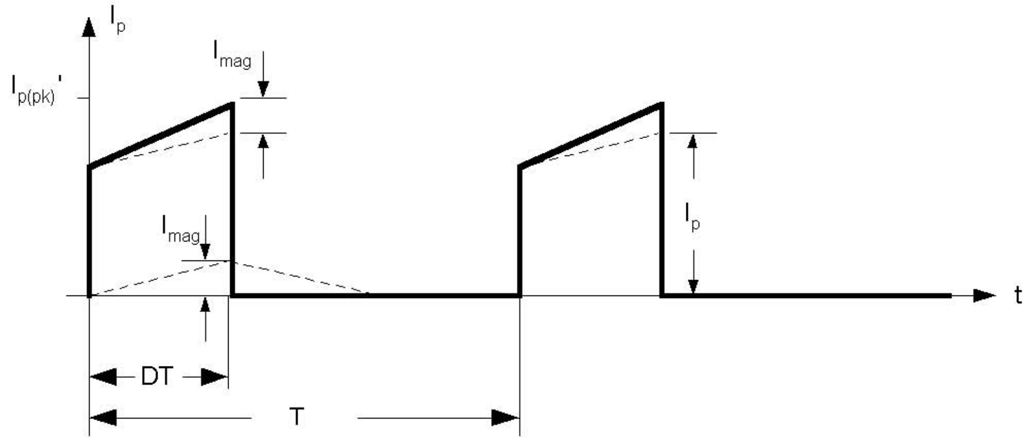

FIGURE 20.24 The current components in the primary winding.

The maximum duty cycle for the forward regulator operated in the continuous mode can be determined by equating the time integral of the input voltage when Q_1 is on and the clamping voltage V_r when Q_1 is off,

$$\int_0^{DT} V_i dt = \int_{DT}^{T} V_r dt \tag{20.57}$$

which leads to

$$V_i DT = V_r(1 - D)T \tag{20.58}$$

Grouping the D terms in (20.58) and replacing V_r/V_i with N_r/N_p, we have

$$D_{\max} = \frac{1}{1 + N_r/N_p} \tag{20.59}$$

Thus, the maximum duty cycle depends on the turn ratio between the demagnetizing winding and the primary one.

In designing forward regulators, the duty cycle must be kept below the maximum duty cycle $D_{\max}$ to avoid saturating the transformer. It should also be noted that the transformer magnetizing current must be reset to zero at the end of each cycle. Failure to do so will drive the transformer into saturation, which can cause damage to the transistor. There are many ways of implementing the resetting function. In the circuit shown in Figure 20.23(a), a tertiary winding is added to the transformer so that the magnetizing current will return to the input source V_i when the transistor turns off. The primary current always starts at the same value under steady-state conditions.

Unlike flyback regulators, forward regulators require a minimum load at the output. Otherwise, excess output voltage will be produced. One method commonly used to avoid this situation is to attach a small load resistance at the output terminals. Of course, with such an arrangement, a certain amount of power will be lost in the resistor.

Because forward regulators do not store energy in their transformers, for the same output power level the transformer can be made smaller than for the flyback type. The output current is reasonably constant owing to the action of the output inductor and the flywheel diode; as a result, the output filter capacitor can be made smaller and its ripple current rating can be much lower than that required for the flybacks.

The forward regulator is widely used with output power below 200 W, though it can be easily constructed with a much higher output power. The limitation comes from the capability of the power transistor to handle the voltage and current stresses if the output power were to increase. In this case, a configuration with more than one transistor can be used to share the burden. Figure 20.25 shows a double-ended forward regulator. Like the double-ended flyback counterpart, the circuit uses two transistors that are switched on and off simultaneously. The diodes are used to restrict the maximum collector voltage to V_i. Therefore, transistors with low voltage ratings can be used in the circuit.

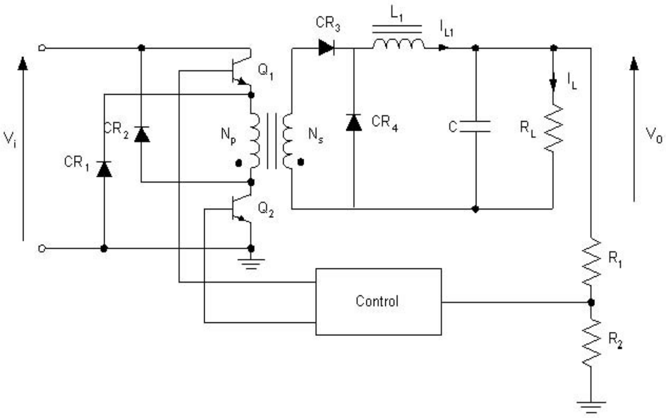

FIGURE 20.25 Double-ended forward regulator.

2 .5.3 alf-Bridge Regulators

The half-bridge regulator is another form of an isolated forward regulator. When the voltage on the power transistor in the single-ended forward regulator becomes too high, the half-bridge regulator is used to reduce the stress on the transistor. In a half-bridge regulator, the voltage stress imposed on the power transistors is subject to only the input voltage and is only half of that in a forward regulator. Thus, the output power of a half-bridge is double that of a forward regulator for the same semiconductor devices and magnetic core.

Figure 20.26 shows the basic configuration of a half-bridge regulator and the associated steady-state waveforms. As seen in Fig. 20.26a, the half-bridge regulator can be viewed as two back-to-back forward regulators, fed by the same input voltage, each delivering power to the load at each alternate half cycle. The capacitors C_1 and C_2 are placed between the input and ground terminals. As such, the voltage across the primary winding is always half the input voltage. The power switches Q_1 and Q_2 are switched on and off alternately to produce a square-wave ac at the input of the transformer. This square-wave is stepped either down or up by the isolation transformer and then rectified by the diodes CR_1 and CR_2. Subsequently, the rectified voltage is filtered to produce the output voltage V_o.

Under steady-state conditions, the operation of the regulator can be explained as follows. When Q_1 is on and Q_2 off, CR_1 conducts and CR_2 is reverse-biased. The primary voltage V_p is $V_i/2$. The primary current I_p starts to build up and stores energy in the primary winding. This energy is forward-transferred to the secondary and onto the L_1C filter and the load R_L, through the rectifier diode CR_1. During the time interval Δ, when both Q_1 and Q_2 are off, CR_1 and CR_2 are forced to conduct to carry the magnetizing current that resulted in the interval during which Q_1 is turned on. The inductor current I_{L1} in this interval is equal to the sum of the currents in CR_1 and CR_2. This interval terminates at half of the switching period T, when Q_2 is turned on. When Q_2 is on and Q_1 off, CR_1 is reverse-biased and CR_2 conducts. The primary voltage V_p is now $-V_i/2$. The circuit operates in a similar manner as during the first half-cycle.

With Q_1 on, the voltage across the secondary winding is

$$V_s = \frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) \tag{20.60}$$

Neglecting diode voltage drops and losses, the voltage across the output inductor is then given by

$$V_{L1} = \frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) - V_o \tag{20.61}$$

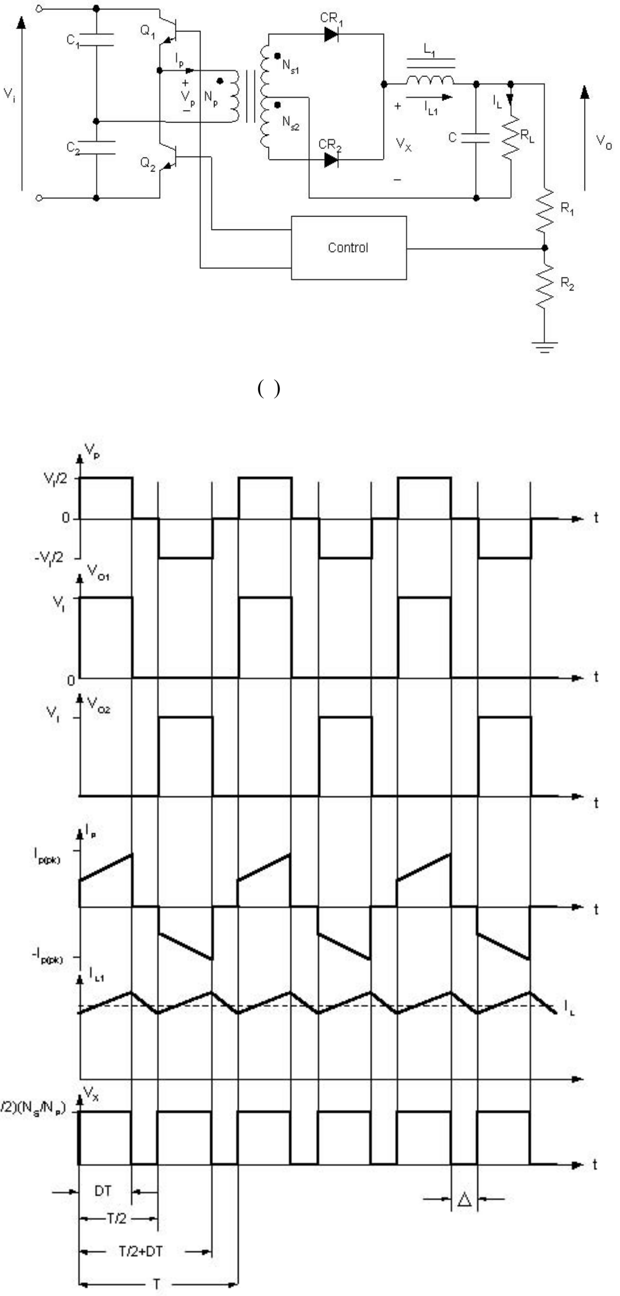

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FIGURE 20.26 A simplified half-bridge regulator: (a) circuit, (b) the associated waveforms.

In this interval, the inductor current I_{L1} increases linearly at a rate of

$$\begin{aligned}\frac{dI_{L1}}{dt} &= \frac{V_{L1}}{L_1}\\ &= \frac{1}{L_1}\left[\frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) - V_o\right]\end{aligned} \tag{20.62}$$

At the end of Q_1 on-time, I_{L1} reaches a value that is given by

$$I_{L1(pk)} = I_{L1}(0) + \frac{1}{L_1}\left[\frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) - V_o\right]DT \tag{20.63}$$

During the interval Δ, I_{L1} is equal to the sum of the rectifier diode currents. Assuming the two secondary windings are identical, I_{L1} is given by

$$I_{L1} = 2I_{CR1} = 2I_{CR2} \tag{20.64}$$

This current decreases linearly at a rate of

$$\frac{dI_{L1}}{dt} = -\frac{V_o}{L_1} \tag{20.65}$$

The next half-cycle repeats with Q_2 on and for the interval Δ.

The output voltage can be found from the time integral of the inductor voltage over a time equal to T. Thus, we have

$$V_o = 2 \times \frac{1}{T}\left\lfloor \int_o^{DT}\left(\frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) - V_o\right)dt + \int_{T/2}^{T/2+DT} - V_o dt\right\rfloor \tag{20.66}$$

Note that the multiplier of 2 appears in (20.66) because of the two alternate half-cycles. Solving (20.66) for V_o, we have

$$V_o = \frac{N_{s1}}{N_p} V_i D \tag{20.67}$$

The output power P_o is given by

$$\begin{aligned} P_o &= V_o I_L \\ &= \eta P_{in} \\ &= \eta \frac{V_i I_{p(avg)} D}{2} \end{aligned} \tag{20.68}$$

or

$$I_{p(avg)} = \frac{2P_o}{\eta V_i D} \tag{20.69}$$

where $I_{p(avg)}$ has the value of the primary current at the center of the rising or falling ramp. Assuming the reaction current I_p' reflected from the secondary is much greater than the magnetizing current, then the maximum collector currents for Q_1 and Q_2 are given by

$$\begin{aligned} I_{C(\max)} &= I_{p(avg)} \\ &= \frac{2P_o}{\eta V_i D_{\max}} \end{aligned} \tag{20.70}$$

As mentioned, the maximum collector voltages for Q_1 and Q_2 at turn-off are given by

$$V_{C(\max)} = V_{i(\max)} \tag{20.71}$$

In designing half-bridge regulators, the maximum duty cycle can never be greater than 50%. When both the transistors are switched on simultaneously, the input voltage is short-circuited to ground. The series capacitors C_1 and C_2 provide a dc bias to balance the volt-second integrals of the two switching intervals. Hence, any mismatch in devices would not easily saturate the core. However, if such a situation arises, a small coupling capacitor can be inserted in series with the primary winding. A dc bias voltage proportional to the volt-second imbalance is developed across the coupling capacitor. This balances the volt-second integrals of the two switching intervals.

One problem in using half-bridge regulators is related to the design of the drivers for the power switches. Specifically, the emitter of Q_1 is not at ground level, but is at a high ac level. The driver must therefore be referenced to this ac level. Typically, transformer-coupled drivers are used to drive both switches, thus solving the grounding problem and allowing the controller to be isolated from the drivers.

The half-bridge regulator is widely used for medium-power applications. Because of its core-balancing feature, the half-bridge becomes the predominant choice for output power ranging from 200 to 400 W. Since the half-bridge is more complex, for application below 200 W, the flyback or forward regulator is considered to be a better choice and more cost-effective. Above 400 W, the primary and switch currents of the half-bridge become very high. Thus, it becomes unsuitable.

2 .5.4 ull-Bridge Regulators

The full-bridge regulator is yet another form of isolated forward regulator. Its performance is improved over that of the half-bridge regulator because of the reduced peak collector current. The two series capacitors that appeared in half-bridge circuits are now replaced by another pair of transistors of the same type. In each switching interval, two of the switches are turned on and off simultaneously such that the full input voltage appears at the primary winding. The primary and the switch currents are only half that of the half-bridge for the same power level. Thus, the maximum output power of this topology is twice that of the half-bridge.

Figure 20.27 shows the basic configuration of a full-bridge regulator and the associated steady-state waveforms. Four power switches are required in the circuit. The power switches Q_1 and Q_4 turn simultaneously on and off in one of the half-cycles. Q_2 and Q_3 also turn simultaneously on and off in the other half-cycle, but with the opposite phase to Q_1 and Q_4. This produces a square-wave ac with a value of $\pm V_i$ at the primary winding of the transformer. Like the half-bridge, this

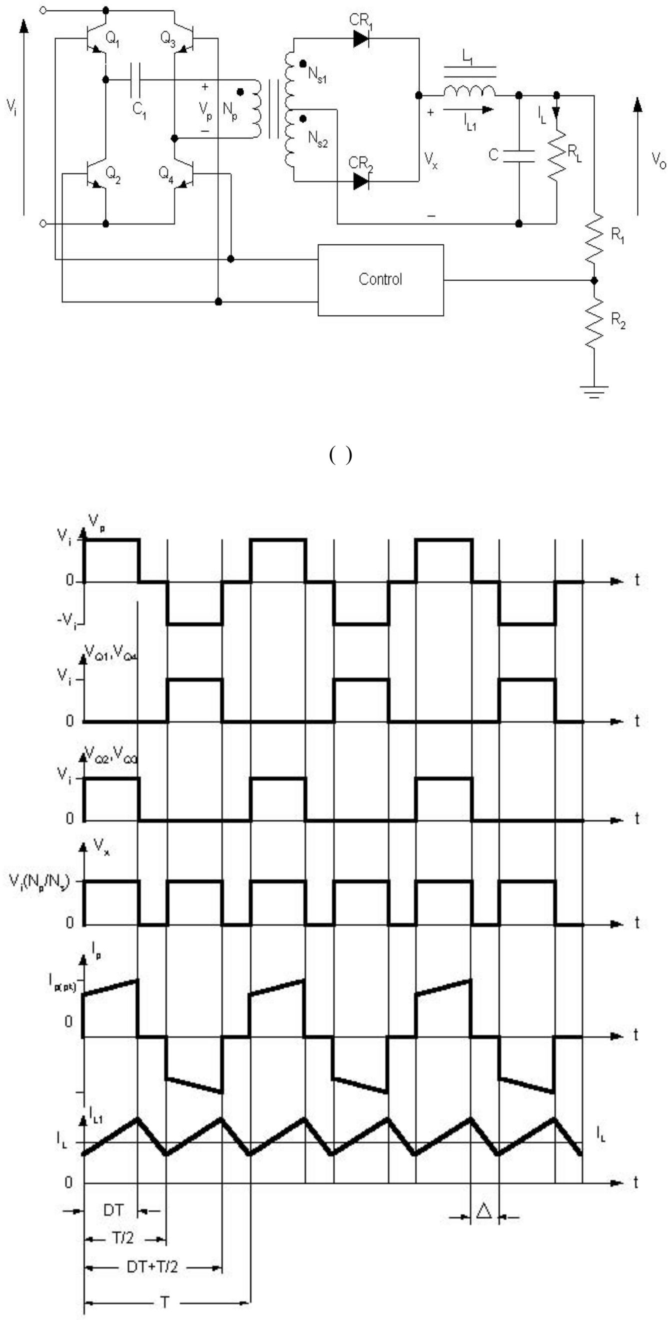

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FIGURE 20.27 A simplified full-bridge regulator: (a) circuit, (b) associated waveforms.

voltage is stepped down, rectified, and then filtered to produce a dc output voltage. The capacitor C_1 is used to balance the volt-second integrals of the two switching intervals and prevent the transformer from being driven into saturation.

Under steady-state conditions, the operation of the full bridge is similar to that of the half bridge. When Q_1 and Q_4 turn on, the voltage across the secondary winding is

$$V_s = \frac{N_s}{N_p} V_i \tag{20.72}$$

Neglecting diode voltage drops and losses, the voltage across the output inductor is then given by

$$V_{L1} = \frac{N_s}{M_p} V_i - V_o \tag{20.73}$$

In this interval, the inductor current I_{L1} increases linearly at a rate of

$$\begin{aligned} \frac{dI_{L1}}{dt} &= \frac{V_{L1}}{L_1} \\ &= \frac{1}{L_1}\left[\frac{N_s}{N_p} V_i - V_o\right] \end{aligned} \tag{20.74}$$

At the end of Q_1 and Q_4 on-time, I_{L1} reaches a value that is given by

$$I_{L1(pk)} = I_{L1}(0) + \frac{1}{L_1}\left[\frac{N_{s1}}{N_p} V_i - V_o\right] DT \tag{20.75}$$

During the interval Δ, I_{L1} decreases linearly at a rate of

$$\frac{dI_{L1}}{dt} = -\frac{V_o}{L_1} \tag{20.76}$$

The next half-cycle repeats with Q_2 and Q_3 on and the circuit operates in a similar manner as in the first half-cycle.

Again, as in the half-bridge, the output voltage can be found from the time integral of the inductor voltage over a time equal to t. Thus, we have

$$V_o = 2 \times \frac{1}{T}\left[\int_0^{DT}\left(\frac{N_{s1}}{N_p} V_i - V_o\right) dt + \int_{T/2}^{T/2+DT} - V_o dt\right] \tag{20.77}$$

Solving (20.77) for V_o, we have

$$V_o = \frac{N_s}{N_p} 2 V_i D \tag{20.78}$$

The output power P_o is given by

$$\begin{aligned} P_o &= \eta P_{in} \\ &= \eta V_i I_{p(avg)} D \end{aligned} \tag{20.79}$$

or

$$I_{p(avg)} = \frac{P_o}{\eta V_i D} \tag{20.80}$$

where $I_{p(avg)}$ has the same definition as in the half-bridge case.

Comparing (20.80) with (20.69), we see that the output power of a full bridge is twice that of a half-bridge with same input voltage and current. The maximum collector currents for Q_1, Q_2, Q_3, and Q_4 are given by

$$\begin{aligned} I_{C(\max)} &= I_{p(avg)} \\ &= \frac{P_o}{\eta V_i D_{\max}} \end{aligned} \tag{20.81}$$

If we compare (20.81) with (20.70), for the same output power, the maximum collector current is only half that of the half-bridge.

As mentioned, the maximum collector voltage for Q_1 and Q_2 at turn-off is given by

$$V_{C(\max)} = V_{i(\max)} \tag{20.82}$$

The design of the full bridge is similar to that of the half-bridge. The only difference is the use of four power switches instead of two in the full bridge. Therefore, additional drivers are required by adding two more secondary windings in the pulse transformer of the driving circuit.

For high-power applications ranging from several hundred to a thousand kilowatts, the full-bridge regulator is an inevitable choice. It has the most efficient use of magnetic core and semiconductor switches. The full bridge is complex and therefore expensive to build, and is only justified for high-power applications, typically over 500 W.

2 .5.5 Control Circuits and Pulse-Width Modulation

In previous subsections, we presented several popular voltage regulators that may be used in a switching-mode power supply. This section discusses the control circuits that regulate the output voltage of a switching regulator by constantly adjusting the conduction period t_{on} or duty cycle d of the power switch. Such adjustment is called *pulse-width modulation* (PWM).

The duty cycle is defined as the fraction of the period during which the switch is on, i.e.,

$$\begin{aligned} d &= \frac{t_{on}}{T} \\ &= \frac{t_{on}}{t_{on} + t_{off}} \end{aligned} \tag{20.83}$$

By adjusting either t_{on} or t_{off}, or both, d can be modulated. Thus, PWM-controlled regulators can operate at variable frequency as well as fixed frequency.

Among all types of PWM controllers, the fixed-frequency controller is by far the most popular choice. There are two main reasons for their popularity. First, low-cost fixed-frequency PWM IC controllers have been developed by various solid-state device manufacturers, and most of these IC controllers have all the features that are needed to build a PWM switching power supply using a minimum number of components. Second, because of their fixed-frequency nature, fixed-frequency controllers do not have the problem of unpredictable noise spectrum associated with variable frequency controllers. This makes EMI control much easier.

A PWM fixed-frequency controller consists of four main functional components: an adjustable clock for setting the switching frequency, an output voltage error amplifier for detecting deviation of the output from the nominal value, a sawtooth generator for providing a sawtooth signal that is synchronized to the clock, and a comparator that compares the output error signal with the sawtooth signal. The output of the comparator is the signal that drives the controlled switch. Figure 20.28 shows a simple PWM controlled forward regulator operating at fixed frequency. The duration of the on-time is determined by the time between the reset of the sawtooth generator and the intersection of the error voltage with the positive-going ramp signal.

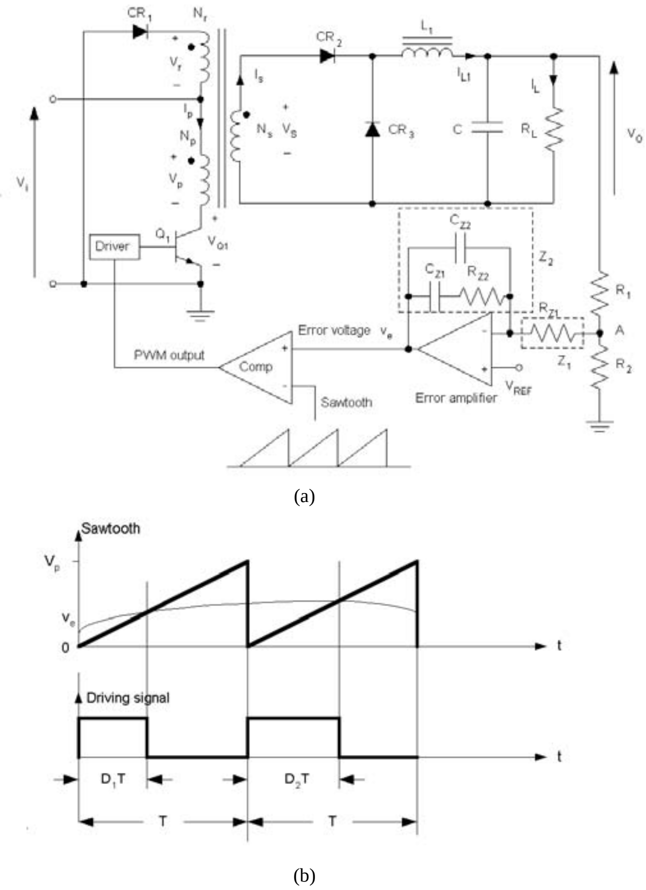


FIGURE 20.28 A simplified voltage-mode controlled forward regulator: (a) circuit, (b) the associated waveforms.

The error voltage v_e is given by

$$v_e = \left(1 + \frac{Z_2}{Z_1}\right) V_{REF} - \frac{Z_2}{Z_1} v_2 \tag{20.84}$$

From (20.84), the small-signal term can be separated from the dc operating point by

$$\Delta v_e = -\frac{Z_2}{Z_1} \Delta v_2 \tag{20.85}$$

The dc operating point is given by

$$V_e = \left(1 + \frac{Z_2}{Z_1}\right) V_{REF} - \frac{Z_2}{Z_1} V_2 \tag{20.86}$$

Inspecting the waveform of the sawtooth and the error voltage shows that the duty cycle is related to the error voltage by

$$d = \frac{v_e}{V_p} \tag{20.87}$$

where V_p is the peak voltage of the sawtooth.

Hence, the small-signal duty cycle is related to the small-signal error voltage by

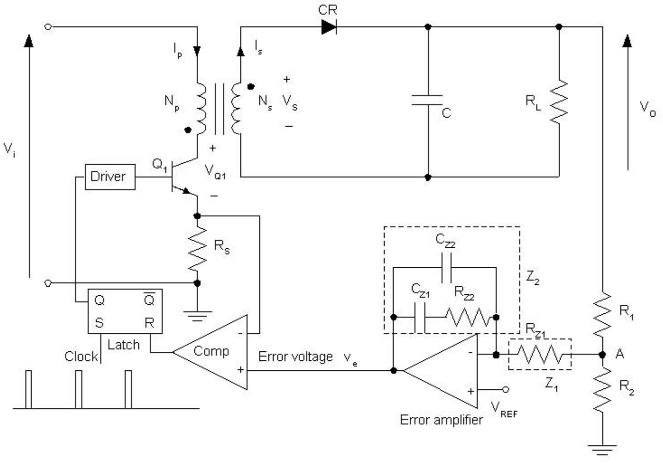
$$\Delta d = \frac{\Delta v_e}{V_p} \tag{20.88}$$

The operation of the PWM fixed-frequency controller can be explained as follows. When the output is lower than the nominal dc value, a high error voltage is produced. This means that Δv_e is positive. Hence, Δd is positive. The duty cycle is increased to cause a subsequent increase in output voltage. Such is a typical *voltage-mode control* operation. The feedback dynamics (stability and transient response) is determined by the operational amplifier circuit that consists of Z_1 and Z_2. Some of the popular voltage-mode control ICs are SG1524/25/26/27, TL494/5, and MC34060/63.

In addition to the voltage-mode control, a control scheme known as *current-mode control* makes use of the current information in a regulator to achieve output voltage regulation. In its simplest form, current-mode control consists of an inner loop that samples the inductance current value and turns the switches off as soon as the current reaches a certain value set by the outer voltage loop. In this way, the current-mode control achieves faster response than the voltage mode.

In current-mode control, no sawtooth generator is needed. In fact, the inductance current waveform is itself a sawtooth. The voltage analog of the current may be provided by a small resistance, or by a current transformer. Also, in practice, the switch current is used since only the positive-going portion of the inductance current waveform is required. Figure 20.29 shows a current-mode controlled flyback regulator.

In Fig. 20.29, the regulator operates at fixed frequency. Turn-on is synchronized with the clock pulse, and turn-off is determined by the instant at which the input current equals the error voltage.



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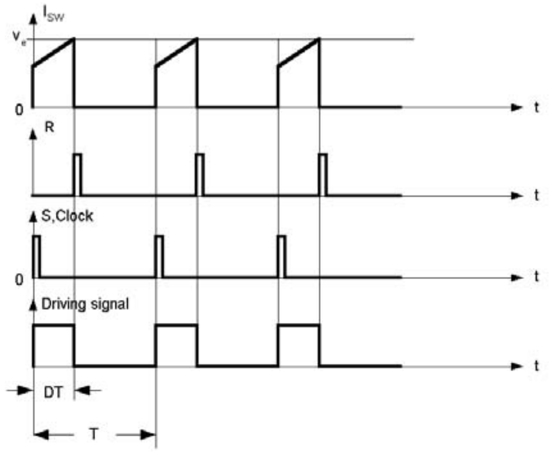

(b)

FIGURE 20.29 A simplified current-mode controlled flyback regulator: (a) circuit, (b) the associated waveforms.

Because of its inherent peak-current limiting capability, current-mode control can enhance reliability of power switches. The dynamic performance is improved because of the use of the additional current information. Moreover, current-mode control makes power factor correction possible. Some of the popular current-mode control ICs are UC3840/2, UC3825, MC34129, and MC34065.

It should be noted that current-mode control is particularly effective for the flyback and boost-type regulators that have an inherent right-half-plane zero. Current-mode control effectively reduces the system to first order by forcing the inductor current to be related to the output voltage, thus achieving faster response. In the case of the buck-type regulator, current-mode control presents no significant advantage because the current information can be derived from the output voltage, and hence faster response can still be achieved with a proper feedback network.

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21

Electronic Ballasts

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21.1 Introduction

Electronic ballasts, also called solid-state ballasts, are those power electronic converters used to supply discharge lamps. The modern age of electronic ballasts began with the introduction of power bipolar transistors with low storage time, allowing supply of fluorescent lamps at frequencies of several kilohertz and increasing lamp luminous efficacy by operating at these high frequencies. Later, electronic ballasts become very popular with the development of low-cost power MOSFETs, whose unique features make them very attractive for implementing solid-state ballasts. The main benefits of electronic ballasts are increased lamp and ballast overall efficiency, increased lamp life, reduction of ballast size and weight, and improvement in lighting quality. This chapter gives a general overview of the more important topics related to this type of power converters

21.1.1 Basic Notions

Discharge lamps generate electromagnetic radiation by means of an electric current passing through a gas or metal vapor. This radiation is discrete, as opposed to the continuous radiation emitted by an incandescent filament. Figure 21.1 shows the electromagnetic spectrum of an electric discharge, which consists of a number of separate spectral lines.

As can be seen in Fig. 21.1, only the electromagnetic radiation emitted within the visible region (380–780 nm) of the radiant energy spectrum is useful for lighting. The total power in watts emitted by an electric discharge can be obtained by integrating the spectral energy distribution. However, this is not a suitable parameter to measure the amount of light emitted by a discharge lamp.

The human eye responds differently to the different types of electromagnetic waves within the visible range. As illustrated in Fig. 21.2, there exist two response curves. First, the photopic curve, also called $V(\lambda)$, is the characteristic used to represent human eye behavior under normal illumination level conditions or daylight vision. Secondly, the scotopic curve $V'(\lambda)$ is the response of the human eye for situations with low illumination levels, also known as nocturnal vision. The reason for this different behavior is physiologic. The human eye consists of two types of photoreceptors: rods and cones. Rods are much more sensitive than cones at low lighting levels, but they are not sensitive to the different light colors. On the other hand, cones are responsible for normal color vision at higher lighting levels [5, 7]. Normally, only the photopic function is considered in lighting design and used to calibrate photometers.

Because the human eye responds in different ways to the different wavelengths or colors, the output power of a lamp measured in watts is no longer applicable to represent the amount of light generated. Thus, a unit is used that incorporates human eye response, which is called the *lumen*. The total light output of a lamp is then measured in lumens and is known as lamp luminous flux. The lamp luminous flux is obtained by integrating the radiant power as follows:

$$\Phi = K_m \int_{380\,\mathrm{nm}}^{780\,\mathrm{nm}} P(\lambda) V(\lambda) d\lambda \tag{21.1}$$

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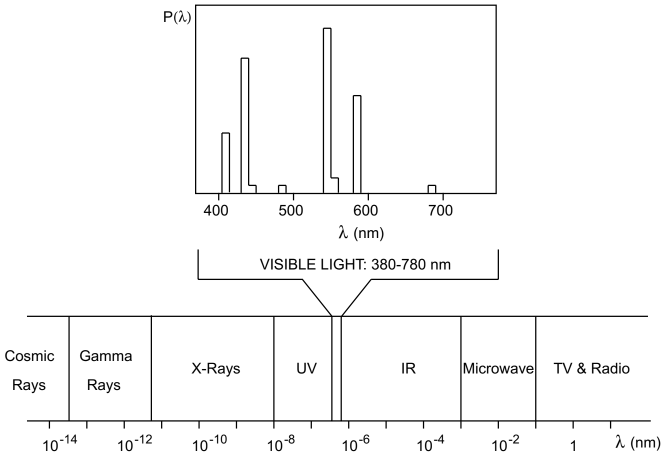


FIGURE 21.1 Spectral energy distribution of an arc discharge and radiant energy spectrum.

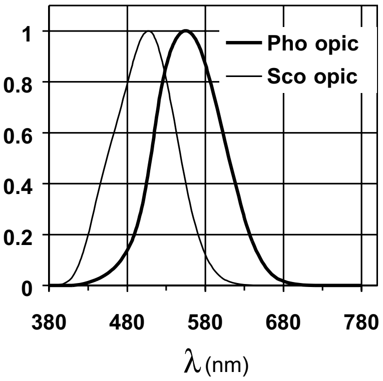


FIGURE 21.2 Spectral luminous efficiency functions for standard photopic and scotopic observers.

where K_m represents the maximal spectral luminous efficacy, which is equal to 683 lumens/watt (at $\lambda = 555\,\text{nm}$) for photopic vision and 1700 lumens/watt (at $\lambda = 507\,\text{nm}$) for scotopic vision. The standard photopic and scotopic functions were defined by the International Commission on Illumination (CIE) in 1924 and 1951, respectively [5].

The measurement of the lamp total luminous flux is very useful in determining whether the lamp is working properly or not. At the laboratory, the measurement of the lamp total luminous flux is performed by means of an integrating sphere and using the substitution method. The integrating sphere, also known as an Ulbricht photometer, is internally coated with a perfectly diffusing material. Thus, the sphere performs the integral in (21.1) and the illuminance on the internal surface is proportional to the total luminous flux. A photometer with a $V(\lambda)$ filter is placed so that the internal illuminance can be measured, and a baffle is placed to avoid direct illumination of the photometer probe by the lamp. The measurement is made in two steps, one with the lamp under test in place and the other with a standard lamp of known total luminous flux. From the two measurements, the total luminous flux of the lamp under test is deduced by a linear relationship. Figure 21.3 illustrates an integrating sphere photometer.

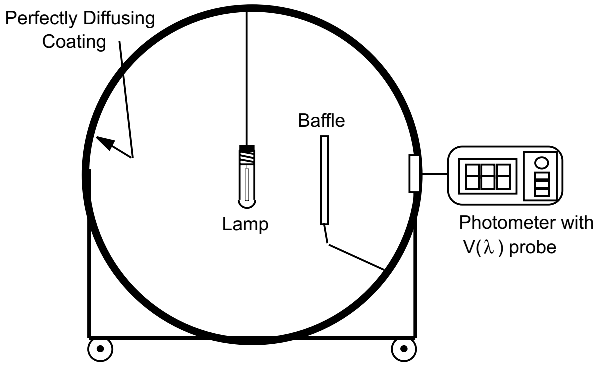


FIGURE 21.3 Integrating sphere used for measurement of the lamp total luminous flux.

An important parameter related to the supply of discharge lamps is the *luminous efficacy*. Luminous efficacy is defined as the rate of the lamp's total luminous flux to the total electric power consumed by the lamp, usually expressed in lumens per watt. The luminous efficacy of a discharge lamp can be increased by proper design of the electronic ballast, which also results in energy savings.

21.1.2 Discharge Lamps

Basically, discharge lamps consist of a discharge tube inside which the electric energy is transformed into electromagnetic radiation. The discharge tube is made of a transparent or translucent material with a sealed electrode placed in each end, as shown in Fig. 21.4. The discharge tube is filled with an inert gas and a metal vapor. The electrodes generate free electrons, which are accelerated by the electrical field existing in the discharge. These accelerated electrons collide with the gas atoms, having both elastic and inelastic collisions depending on the electron kinetic energy. The basic processes inside the discharge tube, illustrated in Fig. 21.4, are the following:

1. *Heat generation.* When the kinetic energy of the electron is low, an elastic collision takes place and only a small part of the electron energy is transferred to the gas atom. The result of this type of collision is an increase in the gas temperature. In this case, the electrical energy is consumed to produce heat dissipation. However, this is also an important process because the discharge has to set in its optimum operating temperature.
2. *Gas atom excitation.* Some electrons can have a high kinetic energy so that the energy transferred in the collision is used to send an electron of the gas atom to

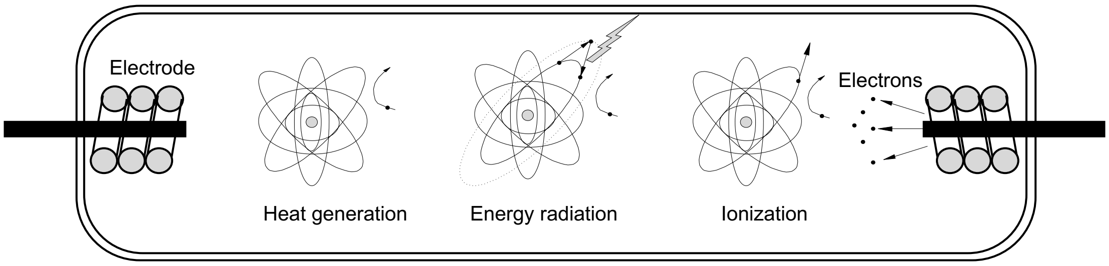


FIGURE 21.4 Basic processes inside the discharge volume.

a higher orbit. This situation is unstable and the electron trends to recover its original level, then emitting the absorbed energy in the form of electromagnetic radiation. This radiation is used to directly generate visible light. In other cases, ultraviolet radiation is first generated and then transformed into visible radiation by means of a phosphor coating on the inside wall of the discharge tube.

3. *Gas atom ionization.* In some cases electrons have gained such a high kinetic energy that during a collision with a gas atom an electron belonging to the gas atom is freed, resulting in a positively charged ion and a free electron. This freed electron can play the same roles as those generated by the electrodes. This process is especially important during both discharge ignition and normal operation, because ionized atoms and electrons are necessary to maintain the electric current through the lamp.

The number of free electrons in the discharge can increase rapidly because of continuing ionization, producing an unlimited current and finally a short-circuit. This is illustrated in Fig. 21.5, which shows how the voltage–current characteristic of a gas discharge exhibits a negative differential resistance. Therefore, to limit the discharge current the use of an auxiliary supply circuit is mandatory. This circuit is called a *ballast.*

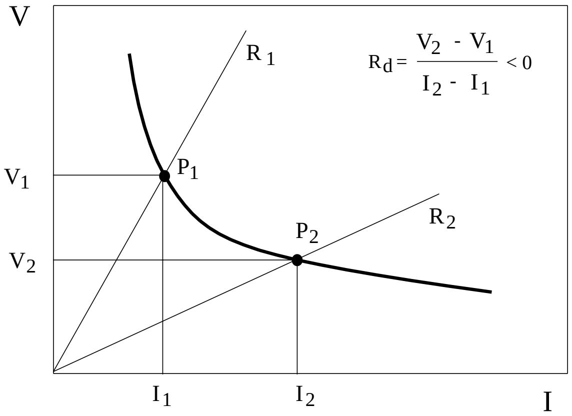


FIGURE 21.5 Voltage–current characteristic of an electric discharge.

Focusing on discharge lamps, the complete stabilization process consists of two main phases:

1. *Breakdown phase.* Most gases are very good insulators, and an electric discharge is only possible if a sufficient concentration of charged particles is present. Normally, a high voltage is used to provide electricity carriers and to initiate the discharge. The minimum voltage applied to initiate the discharge is called the *starting voltage.* The starting voltage mainly depends on the type of gas, gas pressure, and distance between electrodes. Figure 21.6a represents the starting voltage as a function of the product gas pressure multiplied by electrode distance, for different gases. These functions are known as Paschen curves.

   Usually, auxiliary inert gases are used to decrease the starting voltage. There exist some especially inert gas mixtures presenting a very low starting voltage, which are called *Penning mixtures.* These Penning mixtures are often used as initial starting gases. Figure 21.6a shows a typical Penning mixture consisting of neon with 0.1 argon.

2. *Warm-up phase.* Once the lamp is ignited, the collisions between free electrons and atoms generate heat and discharge temperature increases until normal operating conditions are reached. During this phase the heat is used to evaporate the metal atoms existing in the discharge tube, and the emitted electromagnetic radiation assumes the character of a metal vapor discharge instead of that of an inert gas discharge. From the electrical point of view, the discharge warm-up phase shows initially low discharge voltage and high discharge current. As long as more and more metal atoms are evaporated, the discharge voltage increases and the discharge current decreases. Finally, an equilibrium is reached at steady-state operation with the normal values of voltage and current. The time constant of the warm-up phase strongly depends on the lamp type. It varies from seconds for fluorescent lamps to minutes for high-intensity discharge lamps. Figure 21.6b illustrates some discharge waveforms during the warm-up phase.

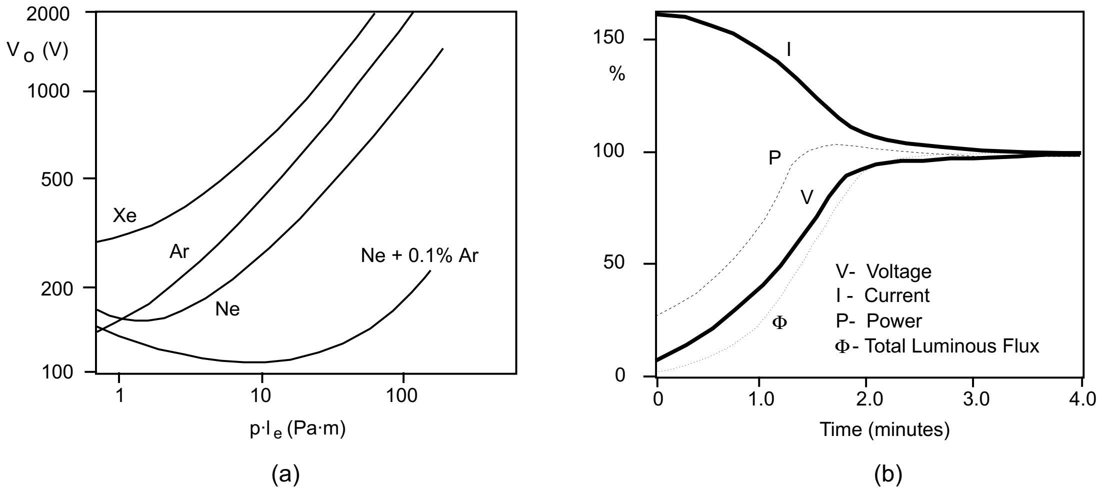


FIGURE 21.6 (a) Paschen curves for different inert gases; and (b) stabilization curve of a discharge lamp.

The basic elements used in lamps to generate radiation in the visible part of the spectrum are sodium and mercury. The former generates radiation directly within the visible part of the spectrum; the latter generates radiation mainly in the ultraviolet region, but this radiation can be easily transformed into visible radiation by means of a phosphor coating on the internal wall of the discharge volume. Besides the element used, a very important parameter related to the efficiency and richness of the emitted radiation is the discharge pressure. For sodium and mercury elements, there exist two pressure values around which the luminous efficacy of the discharge is higher. The first is obtained at quite low pressures, about 1 Pa, and the second at higher pressures, around 10^5 Pa (1 atm). This is why there exist two main types of discharge lamps:

1. *Low-pressure discharge lamps*. This type of lamp operates at pressures around 1 Pa and features low current density inside the discharge and low power per unit of discharge length. Therefore, these lamps normally present a quite large discharge volume with a low power rating. The most representative examples are low-pressure mercury lamps, also known as fluorescent lamps, and low-pressure sodium lamps.
2. *High-pressure discharge lamps*. The operating pressure in this type of lamp is raised to 10^5 Pa and higher in order to achieve a considerable increase in the luminous efficacy of the discharge. These lamps present a high current density in the discharge and a high power per discharge length ratio, thus showing much smaller discharge volumes. Examples are high-pressure sodium lamps, high-pressure mercury lamps, and metal halide lamps.

Finally, to characterize the light produced by a discharge lamp it is necessary to understand two important concepts: the *correlated color temperature* (CCT) and the *color rendering index* (CRI).

The correlated color temperature is defined as the temperature of the blackbody radiator whose perceived color most closely resembles that of the discharge lamp. The color of an incandescent body changes as its temperature rises from deep red to orange, yellow, and finally white. Thus, a cool white fluorescent lamp has a CCT around 3500 K and is perceived as a white source of light, whereas a high-pressure sodium lamp presents a CCT of about 2000 K and appears yellow.

The color rendering index of a light source is the effect that the source has on the color appearance of objects when compared to their appearance under a reference source of equal CCT. The measurement gives a value lower than 100, and a higher CRI means better color rendition. For example, daylight and incandescent lamps have CRIs equal to 100.

To conclude this introduction to discharge lamps, some comments regarding the most important types of discharge lamps will be given. Table 21.1 provides some additional data for the different discharge lamps for comparison.

1. *Fluorescent lamps*. These lamps belong to the category of low-pressure mercury-vapor discharge lamps. The discharge generates two main lines at 185 and 253.7 nm and other weak lines in the visible range of the spectrum. A fluorescent powder on the inside wall of the discharge tube converts the ultraviolet radiation into visible radiation, resulting in a broadband spectral distribution and good color rendition. In these lamps the optimum mercury vapor pressure (which gives the maximum luminous efficacy) is 0.8 Pa. For the tube diameters normally used, this pressure is reached at a wall temperature of about 40 °C, not much higher than typical ambient temperature. The heat generated inside the discharge is sufficient to attain the required operating temperature without the use of an outer

TABLE 21.1 Comparison of different discharge lamps

Lamp	Wattage (W)	Luminous Efficacy (Lumen·W^{-1})	Life (Hours)	CCT (K)	CRI
Fluorescent	4–100	62	20,000	4200	62
Compact fluorescent	7–30	60–80	10,000	2700–5000	82
Low-pressure sodium	50–150	110–180	15,000	1800	< 0
Mercury vapor	50–1000	40–70	24,000	4000–6000	15–50
Metal halide	40–15,000	80–125	10,000	4000	65
HPS	35–1000	65–140	24,000	2000	22
HPS (amalgam)	35–1000	45–85	10,000	2200	65

bulb. However, this structure causes a great variation of the lamp lumen output with the temperature, which is one important drawback of fluorescent lamps. One solution to this problem is the addition of amalgams to stabilize the light output. This is especially used in compact fluorescent lamps.

2. *Low-pressure sodium lamps.* These lamps are a most efficient source of light. The reason is the almost monochromatic radiation that they generate, with two main lines at 589 and 589.6 nm, very close to the maximum human eye sensitivity. Therefore, the color rendition of these lamps is very poor; however, contrasts are seen more clearly under this light. This is why these lamps are used in situations where the recognition of objects and contours is essential for safety, such as motorway bridges, tunnels, and intersections. The optimum pressure for the low-pressure sodium discharge is about 0.4 Pa, attained in normal discharge tubes at a temperature of 260 °C. An outer bulb is normally used to reach and maintain this temperature.
3. *High-pressure mercury vapor lamps.* The increase in the pressure of the mercury vapor produces a radiation richer in spectral lines, some of them in the visible part of the spectrum (405, 436, 546, and 577/579 nm). This leads to an increase in the luminous efficacy, reaching values of 40–60 lm W^{-1} at pressures of 10^5–10^7 Pa (1–100 atm). These lamps operate with unsaturated mercury vapor, which means that all the mercury in the discharge volume has evaporated and the number of mercury atoms per unit volume remains constant. Thus, the operation of this type of lamps is more independent of the temperature than that of most other discharge lamps. One drawback of these lamps is the lack of spectral lines in the long wavelengths (reds) of the spectrum, thus giving a low color rendering index. An increase of the color rendition can be obtained by adding metal-halide compounds into the discharge volume, in order to generate radiation all over the visible spectrum. These lamps are known as *metal halide lamps* [3].
4. *High-pressure sodium lamps.* This is a very popular source of light because of its high luminous efficacy and long life. The increase in the sodium vapor pressure produces a very wide spectrum, with good color rendition compared with the low-pressure sodium lamps. This also leads to a lower luminous efficacy that is still higher than those of other high-intensity discharge lamps. Some of these lamps also incorporate mercury in the form of sodium amalgam to increase the field strength of the discharge, thus decreasing the discharge current. A lower lamp current and a higher lamp voltage allow reduced size and cost of the ballast. However, the addition of sodium amalgam greatly reduces the life of the lamp.

21.1.3 Electromagnetic Ballasts

Electromagnetic ballasts are commonly used to stabilize the lamp at the required operating point by limiting the discharge current. The operating point of the lamp is given by the intersection of both lamp and ballast characteristics, as shown in Fig. 21.7. The ballast line is the characteristic that shows the variation of the lamp power versus lamp voltage for a constant line voltage; it can be measured during the warm-up phase of the lamp. The lamp line is the characteristic that gives the variation of the lamp power as a function of the lamp voltage for different line voltages and can be measured by varying the line voltage. Some lamps, such as high-pressure sodium, exhibit a great variation of lamp voltage with changes in the lamp wattage. Because of this behavior, trapezoids have been established that define maximum and minimum permissible lamp wattage versus lamp voltage for purposes of ballast design, as shown in Fig. 21.7.

Figure 21.8 shows basic electromagnetic ballast used to supply low- and high-pressure lamps at line frequencies (50–60 Hz). Figure 21.8a illustrates the typical circuit used to supply fluorescent lamps with preheating electrodes, which basically uses a series inductor to limit the current through the discharge. Initially the glow switch is closed and the short-circuit current flows through the circuit, heating the

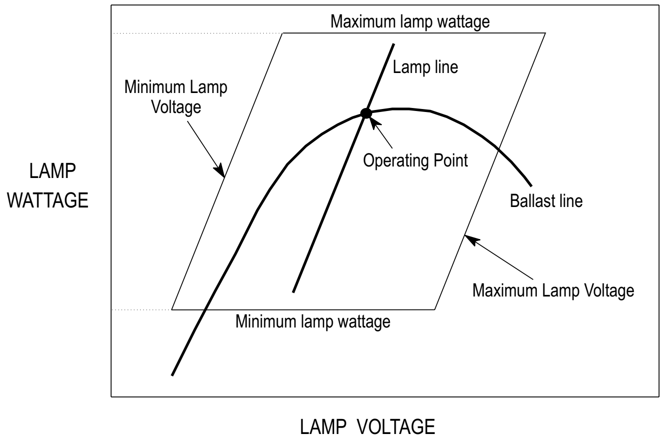


FIGURE 21.7 Lamp and ballast characteristics.

electrodes. A few fractions of a second later, the glow switch is opened and the energy stored in the ballast inductor causes a voltage spike between the lamp electrodes (about 800 V), which finally produces the discharge breakdown. Once the lamp is ignited, its voltage is lower than the line voltage, and the glow switch remains open during normal lamp operation. Typical glow switches are based on two bimetal strips inside a small tube filled with an inert gas. An external capacitor of about 10 nF is used to enhance the glow switch operation and also to reduce radio interference during lamp startup. Finally, in this type of inductive ballasts a capacitor placed across the line input is mandatory to achieve a reasonable value of the input power factor.

Starting voltages of high-pressure discharge lamps are normally higher than those of low-pressure discharge lamps and can go from 2500 V for a lamp at room temperature to 30–40 kV to reignite a hot lamp. Thus, the simple ignition system based on the glow switch is no longer applicable for these lamps. Figures 21.8b and 21.8c show two typical arrangements for supplying high-intensity discharge lamps. A series inductor is also used to limit the lamp current at steady-state operation, but autotransformers are used to attain higher voltage spikes for lamp ignition. For higher line voltages and short distances between starter and lamp, the inductor ballast can be used as ignition transformer as shown in Fig. 21.8b. In other cases, a separate igniting transformer is needed to provide higher voltage spikes and to avoid the effect of parasitic capacitance of connection cables (Fig. 21.8c).

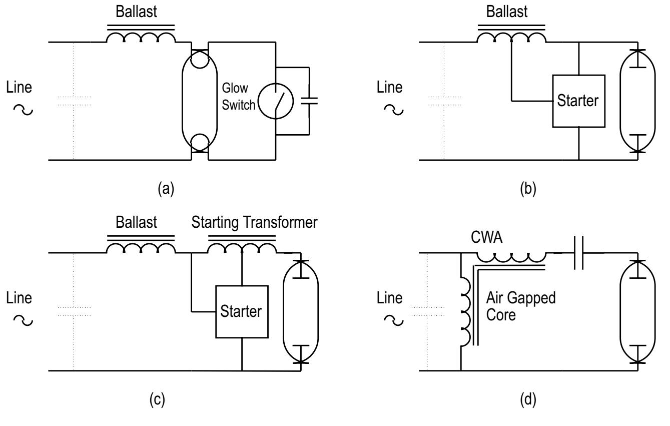


FIGURE 21.8 Typical electromagnetic ballast used to supply discharge lamps at low frequency.

The inductive ballast provides low lamp power regulation against line voltage variation, and therefore it is only recommended in those installations with low voltage fluctuations. When good lamp power regulation is necessary, the circuit shown in Fig. 21.8d is normally used. This circuit is commonly termed a constant wattage autotransformer (CWA) and incorporates a capacitor in series with the lamp to limit the discharge current. Compared with the normal inductive ballast, the CWA also exhibits a higher input power factor, lower line extinguishing voltage, and lower line starting currents.

The main advantage of electromagnetic ballasts is their simplicity, which in turn provides low cost and high reliability. However, since they operate at line frequencies, typically 50–60 Hz, they also feature high size and weight. Other important drawbacks of electromagnetic ballasts are the following:

- Low efficiency, especially for those ballasts featuring good lamp power regulation against line voltage variation.
- Low reliability for ignition and reignition. If the voltage spike is not located well within the line period, the ignition of the lamp can fail.
- Difficulty in controlling the lamp luminous flux (dimming).
- Lamp operating point changes due to the lamp aging process that reduce lamp life.
- Low input power factor and high harmonic distortion. Large capacitors are needed across the line input to increase power factor.
- Overcurrent risk due to ballast saturation caused by the rectifying effect of some discharge lamps, especially at the end of their life.
- *Flickering* and *stroboscopic effect* due to low-frequency supply. The energy radiated by the lamp is a function of the instantaneous input power. Therefore, when the lamp is supplied from an ac line, an instantaneous variation of the light output occurs, which is called *flicker*. For a line frequency of 60 Hz the resulting light frequency is 120 Hz. This variation is too fast for the human eye, but when rapidly moving objects are viewed under these lamps, the objects seem to move slowly or even are halted. This is called the *stroboscopic effect* and can be very dangerous in industrial environments. A flicker index is defined with values from 0 to 1.0 [1]. The higher the flicker index, the greater the possibility of a noticeable stroboscopic effect.

- Unsuitability for dc applications (emergency lighting, automobile lighting, etc.).

21.2 High-Frequency Supply of Discharge Lamps

21.2.1 General Block Diagram of Electronic Ballasts

Figure 21.9 shows the general block diagram of a typical electronic ballast. The main stages are the following:

- *EMI filter.* This filter is mandatory for commercial electronic ballasts. Usually it consists of two coupled inductors and a capacitor. The input filter is used to attenuate the electro magnetic interference (EMI) generated by the high-frequency stages of the ballasts. It also protects the ballast against possible line transients.
- *Ac–dc converter.* This stage is used to generate a dc voltage level from the ac line. Normally a full-bridge diode rectifier followed by a filter capacitor is used. However, this simple rectifier provides low input power factor and poor voltage regulation. In order to obtain a higher power factor and a regulated bus voltage, active converters can be used, as discussed later in this chapter.
- *Dc–ac inverter and high-frequency ballast.* These stages are used to supply the lamp at high frequency. The inverter generates a high-frequency waveform, and the ballast is used to limit the current through the discharge. Both inductors and capacitors can be used to perform this function, with the advantage of low size and weight because they operate at high frequencies.
- *Starting circuit.* In most electronic ballasts, especially those for low-pressure discharge lamps, the high-frequency ballast is used to both ignite the lamp and limit the lamp current at steady state. Therefore, no extra starting circuit is necessary. However, when supplying high-pressure discharge lamps, the starting voltages are much higher and separate ignition circuits are needed, especially if hot reignition is pursued.
- *Control and protection circuit.* This stage includes the main oscillator, error amplifiers to regulate lamp current or power, output overvoltage protection, timers to control the ignition times, overcurrent protection, lamp failure protection, etc. It can go from very simple circuits as those used in self-oscillating ballasts to very complicated ones, which sometimes include a microprocessor-based control circuit.

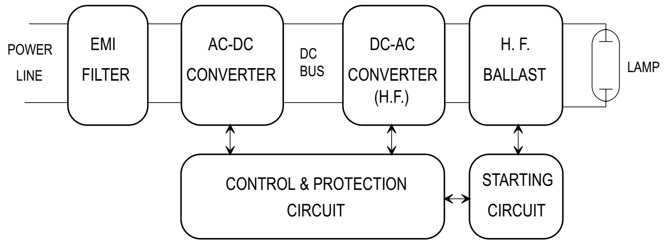


FIGURE 21.9 Block diagram of a typical electronic ballast.

There are several important topics when designing electronic ballasts:

- *Operating frequency.* The operating frequency should be high in order to take advantage of the lower size and weight of the reactive elements used to stabilize the discharge. Usually, the operating frequency should be higher than 20 kHz to avoid audible frequencies, which can produce annoying noises. On the other hand, a higher frequency produces higher switching losses, and a practical limit for the switching frequency is about 100 kHz when MOSFET switches are used. It is also important to avoid frequencies in the range 30–40 kHz, because these frequencies are normally used in IR remote controls and could generate some kind of interference.
- *Lamp current waveform.* In order to attain the maximum lamp life, it is important to drive the lamp with symmetrical alternating currents, thus making use of both lamp electrodes alternately. Also, an important parameter is the *lamp current crest factor* (CF), which is the ratio of the peak value to the rms value of the lamp current. In the case of electronic ballasts, the ratio of the peak value of the low-frequency modulated envelope to the rms value should be used. The higher the CF, the lower the lamp life. The ideal situation is to supply the lamp with a pure sinusoidal waveform. Usually, a CF lower than 1.7 is recommend to avoid early aging of the lamp [11].
- *Lamp starting procedure.* This is a very important issue when developing commercial electronic ballasts. The reason is that the life of the lamp depends greatly on how well lamp startup is performed, especially for hot-cathode fluorescent lamps. During the starting process, the electrodes must be warmed up to the emission temperature, about 800 °C, and no high voltage should be applied until their temperature is sufficiently high, thus avoiding sputtering damage. Once the electrodes reach the emission temperature, the starting voltage can be applied to ignite the lamp. For lamps with cold cathodes, the starting voltage must be applied rapidly to prevent harmful glow discharge and cathode sputtering. In any case, the starting voltage must be limited to the minimum value to ignite the lamp, since higher voltages could provide undesirable starting conditions that would reduce the life of the lamp.
- *Dimming.* This is an important feature that allows the ballast to control lamp power and thereby light output. Usually the switching frequency is used in solid-state ballasts as a control parameter to provide dimming capability. Variations in frequency affect high-frequency ballast impedances and allow changes in the discharge

current. For example, if an inductor is used as a high-frequency ballast, a frequency increase yields an increase in the ballast impedance, thus decreasing lamp current. Dimming should be carried out smoothly, avoiding abrupt changes in lamp power when passing from one level to another. In an eventual power cutoff, the lamp should be restarted at maximum lighting level and then slowly reduced to the required output level.

- *Acoustic resonance.* HID lamps exhibit unstable operation when they are supplied at high frequency. At a certain operating frequencies the arc fluctuates and becomes unstable, which can be observed as a high flicker due to important changes in the lamp power and thus in the lighting output. This can be explained by the dependence of the damping of acoustic waves on the plasma composition and pressure. More information about this topic can be found in [4]. The avoidance of acoustic resonance is mandatory to implement commercial electronic ballasts. This can be performed by selecting operating frequencies in a range free of acoustic resonances, typically below 1 kHz and over 100 kHz. Other methods are frequency modulation, square-wave operation, and sine-wave superposed with the third harmonic frequency [12,13].

21.2.2 Classification of Electronic Ballast Topologies

Typical topologies used to supply discharge lamps at high frequency can be classified into two main groups: nonresonant ballasts and resonant ballasts.

21.2.2.1 Nonresonant Ballasts

These topologies are usually obtained by removing the output diode of dc-to-dc converters, in order to supply alternating current to the lamp. Current mode control is normally employed to limit the discharge lamp current. The lamp is supplied with a square current waveform, which can exhibit a dc level in some cases. A small capacitor is used to initially ignite the lamp, but its effect at steady-state operation can be neglected.

Examples are shown in Fig. 21.10. Figures 21.10a and 21.10b illustrate a boost-based and a flyback-based ballast, respectively. Other topologies, which can supply symmetric alternating current through the lamp, are shown in Fig. 21.10c (symmetric boost) and 21.10d (push–pull).

These topologies present several drawbacks, such as high-voltage spikes across the switch, which make necessary the use of high-voltage transistors, and high switching losses due to hard switching, which gives low efficiency, especially for high powers. In addition, because the ideal situation is the lamp being supplied with a sine wave, these circuits produce early aging of the lamp. In conclusion, typical applications of these topologies are portable and emergency equipment, where lamp power is low and the number of ignitions during its life is not very high. Some applications of these circuits can be found in [14–17].

21.2.2.2 Resonant Ballasts

These ballasts use a resonant tank circuit to supply the lamp. The resonant tank filters the high-order harmonics, thus obtaining a sine current waveform through the lamp. Resonant ballasts can be classified into two categories: current-fed and voltage-fed.

. . . . *Current-Fed Resonant Ballasts*

These ballasts are supplied with a dc current source, usually obtained by means of a choke inductor in series with the input dc voltage source. The dc current is transformed into an alternating square current waveform by switching power transistors. Typical topologies of this type of ballasts are shown in Fig. 21.11.

The topology shown in Fig. 21.11a corresponds to a class E inverter. Inductor Le is used to obtain a dc input current with low current ripple. This current supplies the resonant tank through the power switch formed by Q1–D1. The resonant tank used in this topology can vary from one ballast to another; the circuit shown in Fig. 21.11a is one that is normally used. The main advantage of this topology is that zero-voltage switching (ZVS) can be attained in the power switch, thus reducing the switching losses and making possible operation at very high frequencies, which can reach several megahertz. This allows drastic reductions in the size and

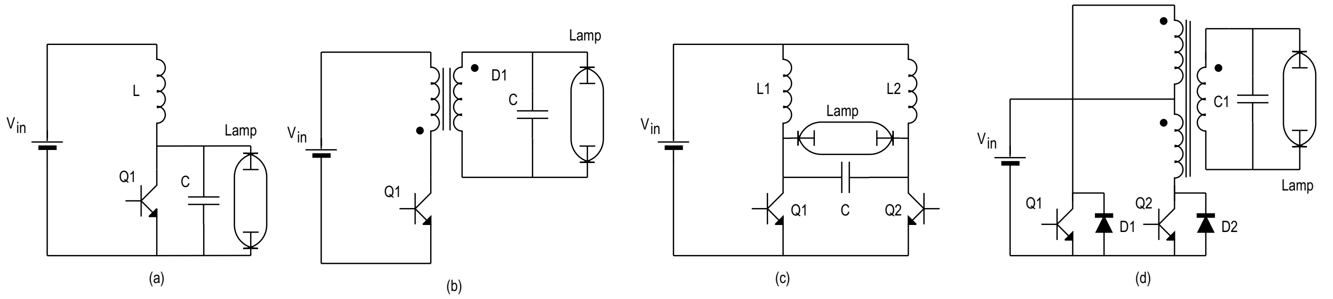
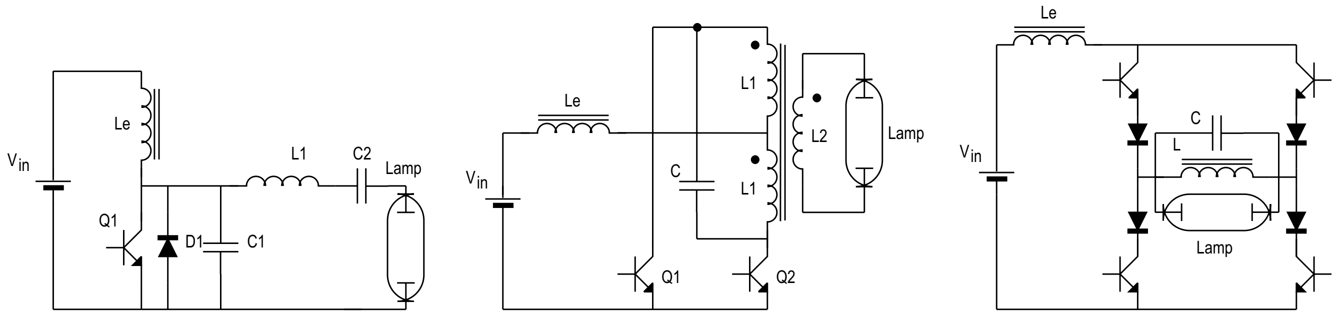


FIGURE 21.10 Nonresonant electronic ballasts.



(a) (b) (c)

FIGURE 21.11 Three typical current-fed resonant inverters: (a) class E inverter, (b) current-fed push–pull inverter, and (c) current-fed full-bridge inverter.

weight of the ballast. However, the adjustment of the circuit parameters to obtain optimum operation is quite difficult, especially for mass production. Another important drawback is the high voltage stress across the switch, which can reach values of three times the dc input voltage. For these reasons, the main applications of this circuit are battery supply ballasts with low input voltage and low lamp power, such as those used in emergency lighting and portable equipment. The typical power range of this ballast is 5 to 30 W. Applications of this circuit can be found in [18,19].

Another typical topology in this group is the current-fed push–pull inverter shown in Fig. 21.11b. In this circuit a dc input current is obtained by means of the choke inductor Le. Transistors are operated with a 50 duty cycle, thus providing a current square wave, which supplies the parallel resonant circuit formed by the mutual inductance of the transformer and capacitor C. This circuit presents the advantage of being relatively easy to implement in a self-oscillating configuration, avoiding the use of extra control circuits and reducing cost. Also, zero-voltage switching (ZVS) can be obtained in the power switches. However, the switches also present a high voltage stress, about three times the dc input voltage, which make this topology unsuitable for power-line applications. This circuit is also normally used in battery-operated applications in a self-oscillating arrangement. The typical power range is 4–100 W. Applications based on this circuit can be found in [20,21].

Finally, Fig. 21.11c shows a current-fed full-bridge resonant inverter, which can be used for higher power ratings. Also, this circuit allows control of the output power at constant frequency by switching the devices of the same leg simultaneously, generating a quasi-square current wave through the resonant tank [6].

. . . . Voltage-Fed Resonant Ballasts

This type of ballast is one of those used most by electronic ballast manufacturers at the present time, especially for applications supplied from ac mains. The circuit is fed from a dc voltage source, normally obtained by line-voltage rectifying. A square-wave voltage waveform is then obtained by switching the transistors with a 50 duty cycle, and used to feed a series resonant circuit. This resonant tank filters the high-order harmonics and supplies the lamp with a sine current waveform. One advantage of the voltage-fed series resonant circuit is that starting voltage can be easily obtained without using extra ignition capacitors by operating close to the resonant tank frequency. Figure 21.12 shows electrical diagrams of typical voltage-fed resonant ballasts.

The voltage-fed version of the push–pull inverter is illustrated in Fig. 21.12a. This inverter includes a transformer, which can be used to step the input voltage up or down in order to obtain an adequate rms value of the output square wave voltage. This provides greater design flexibility but also increases cost. One disadvantage is that voltage across transistors is twice the input voltage, which can be quite high for line applications. Therefore, this inverter is normally used for low-voltage applications. Another important drawback of this voltage-fed inverter is that any asymmetry in the two primary windings (different number of turns) or in the switching times of power transistors would provide an undesirable dc level in the transformer magnetic flux, which in turn could saturate the core or decrease efficiency because of the circulation of dc currents.

Figures 21.12b and 21.12c illustrates two possible arrangements for the voltage-fed half-bridge resonant inverter. The former is normally referred as the asymmetric half-bridge and uses one of the resonant tank capacitors (C1 in the figure) to block the dc voltage level of the square wave generated by the bridge. This means that capacitor C1 will exhibit a dc level equal to half the dc input voltage superimposed on its normal alternating voltage. A transformer can also be used in this inverter to step the input voltage up or down to the required level for each application. In this case the use of the series capacitor C1 prevents any dc current from circulating through the primary winding, thus avoiding transformer saturation. This topology is often used by ballast manufacturers to supply fluorescent lamps, especially in the self-oscillating version, which allows drastic reductions in cost. When supplying hot cathode fluorescent lamps, the parallel capacitor C2 is normally placed across two electrodes, as shown in Fig.

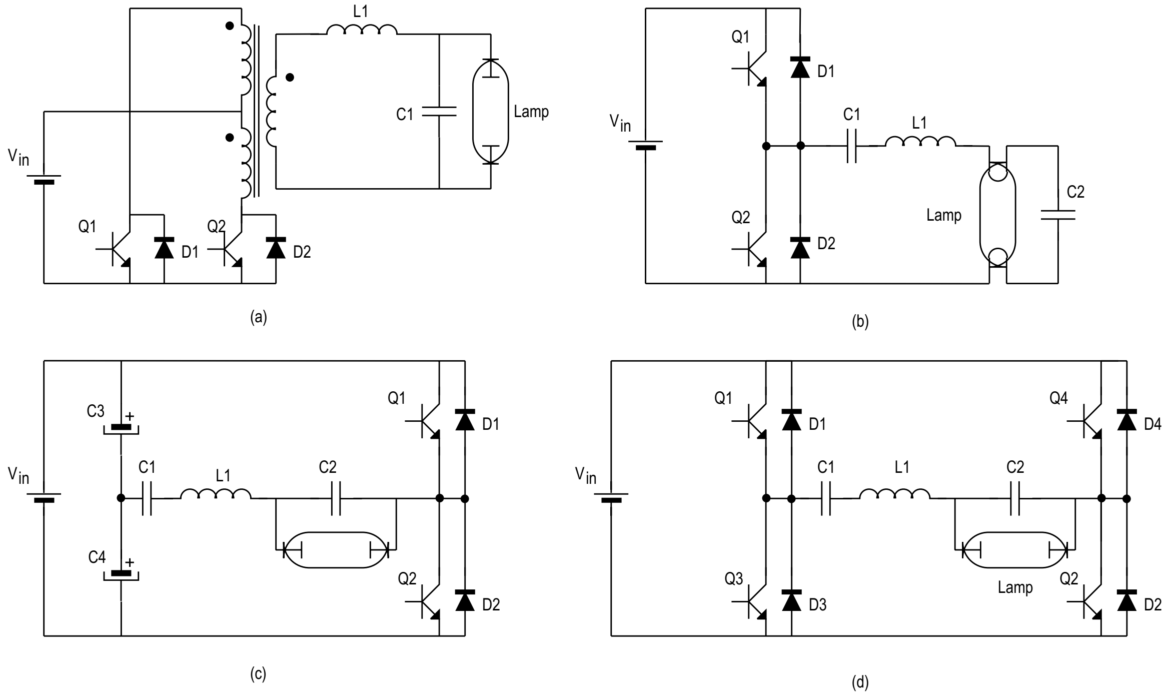


FIGURE 21.12 Typical voltage-fed resonant inverters: (a) push–pull; (b), (c) half bridge; and (d) full bridge.

21.12b, in order to provide a preheating current for the electrodes and achieve soft ignition. Figure 21.12c shows another version of the half-bridge topology, using two bulk capacitors to provide a floating voltage level equal to half the input voltage. In this case, capacitor C1 is no longer used to block a dc voltage, thus showing lower voltage stress.

Finally, for the high power range (> 200 W), the full-bridge topology shown in Fig. 21.12d is normally used. Transistors of each half-bridge are operated with a 50 duty cycle and their switching signals are phase shifted by 180°. Thus, when switches Q1 and Q2 are activated, direct voltage V_{in} is applied to the resonant tank, and when switches Q3 and Q4 are activated the reverse voltage $-V_{in}$ is obtained across the resonant circuit. One of the advantages of this circuit is that the switching signals of the two branches can be phase shifted by angles between 0 and 180°, thus controlling the rms voltage applied to the resonant tank in a range from 0 to V_{in}. This provides an additional parameter to control the output power at constant frequency, which is useful in implementing dimming ballasts.

21.3 Discharge Lamp Modeling

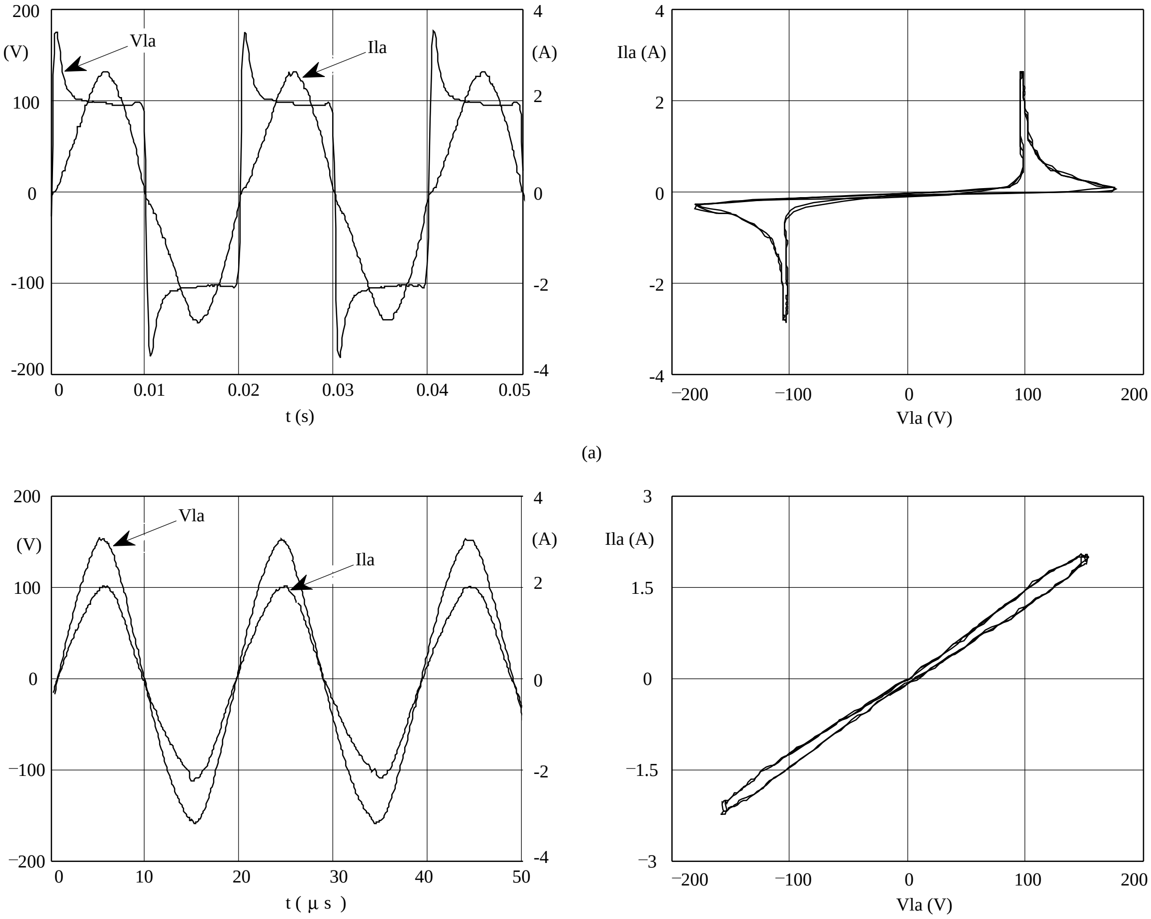
The low frequency of the mains is not the most adequate power source for supplying discharge lamps. At these low frequencies electrons and ionized atoms have enough time to recombine at each current reversal. For this reason, the discharge must be reignited twice within each line period. Figure 21.13a illustrates the current and voltage waveforms and the *I*–*V* characteristic of a 150-W HPS lamp operated with an inductive ballast at 50 Hz. As can be seen, the reignition voltage spike is nearly 50 higher than the normal discharge voltage, which is constant during the rest of the half-cycle.

When lamps are operated at higher frequencies (above 5 kHz), electrons and ions do not have enough time to recombine. Therefore, charge carrier density is sufficiently high at each current reversal and no extra power is needed to reignite the lamp. The result is an increase in the luminous flux compared to that at low frequencies, which is especially high for fluorescent lamps (10–15).

Figure 21.13b shows the lamp waveforms and *I*–*V* characteristic for the same 150-W HPS when supplied at 50 kHz. The reignition voltage spikes disappear and the lamp behavior is nearly resistive.

Figure 21.14 illustrates how the voltage waveforms change in a fluorescent lamp when increasing the supply frequency. As can be seen, at a frequency of 1 kHz the voltage is already nearly sinusoidal and the lamp exhibits a resistive behavior.

Therefore, a resistor can be used to model the lamp at high frequencies for ballast design purposes. However, most lamp manufacturers provide lamp data only for operation at low frequencies, where the lamp behaves as a square-wave voltage source. Table 21.2 shows the low-frequency electric data for different discharge lamps provided by the manufacturer and the measured values at high frequency for the same lamps. As



(a)

(b)

FIGURE 21.13 Waveforms and *I–V* characteristics of 150-W HPS lamp at (a) 50 Hz; and (b) 50 kHz.

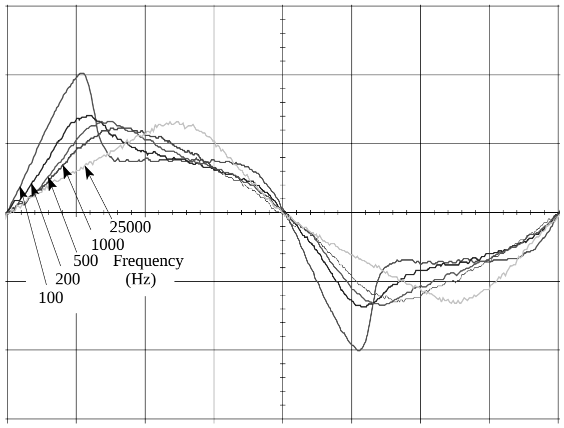


FIGURE 21.14 Voltage waveforms for a 36-W linear fluorescent lamp supplied through a resistive ballast at nominal power and different operating frequencies. Vertical scale: 100 V/div.

can be seen, a power factor close to unity is obtained at high frequency.

The equivalent lamp resistance at high frequencies can be easily estimated from the low-frequency data. Lamp power at any operating frequency can be expressed as follows:

$$P_{LA} = V_{LA} I_{LA} FP_{LA} \tag{21.2}$$

where V_{LA} and I_{LA} are the rms values of lamp voltage and current, and FP_{LA} is the lamp power factor.

At line frequencies the lamp power factor is low (typically 0.8) because of the high distortion in the lamp voltage waveform. However, at high frequencies the lamp power factor reaches nearly 1.0. Then, lamp voltage and current at high frequency $(V_{LA,hf},\ I_{LA,hf})$ can be estimated from the following equation:

$$I_{LA,hf} V_{LA,hf} = P_{LA} \tag{21.3}$$

TABLE 21.2 Electric data for different discharge lamps

	Manufacturer at 50 Hz				Measured at High Frequency			
Lamp[a]	*V*(Vrms)	*I*(Arms)	*P*(W)	PF	*V*(Vrms)	*I*(Arms)	*P*(W)	PF
Fluorescent (TLD-36W)	103	**0.44**	36	0.79	83.2	**0.46**	36	0.94
Compact fluorescent (PLC-26W)	105	**0.31**	26	0.80	82	**0.32**	26	0.99
Low-pressure sodium (SOX-55W)	109	0.59	55	0.86	75	0.76	56	0.98
Mercury vapor (HPLN-125W)	**125**	1.15	125	0.87	**132**	0.92	120	0.99
Metal halide (MHN-TD-150W)	**90**	1.80	150	0.93	**92**	1.63	146	0.97
High-pressure sodium (SON-T-150W)	**100**	1.80	150	0.83	**105**	1.42	148	0.99

[a] Lamps aged for 100 hours.

where P_{LA} is the nominal lamp power provided by the manufacturer.

As can be seen in Table 21.2, fluorescent lamps tend to maintain nearly the same rms current at low and high frequency, whereas high-pressure discharge lamps tends to maintain nearly the same rms voltage. Based on these assumptions, the equivalent lamp resistance at high frequency estimated from the low-frequency values is shown in Table 21.3.

Low-pressure sodium lamps seem not to maintain either constant voltage or constant current at high frequency, and they also exhibit an equivalent resistance that is quite dependent on the frequency. Therefore, their equivalent resistance can only be obtained by laboratory testing.

Note that the values given in Table 21.3 are only approximations of the real values, which should be obtained by measurement at the laboratory. They can be used as a starting point for the design of the electronic ballast, but final adjustments should be made in the laboratory.

Another important issue is that lamp equivalent resistance is strongly dependent on power delivered to the lamp, which is especially important for designing electronic ballasts with dimming features. The characteristic lamp resistance versus lamp power is different for each discharge lamp type and must be obtained by laboratory testing. One of the best possibilities for fitting the lamp resistance versus power characteristic is the hyperbolic approximation. For example, Mader and Horn propose in [8] the following simple approximation:

$$R_{LA}(P_{LA}) = \frac{V_0^2}{P_{LA} + P_0} \tag{21.4}$$

where R_{LA} is the equivalent lamp resistance, P_{LA} is the average lamp power, and V_0 and P_0 are two parameters that depend on each lamp. This characteristic has been plotted in Fig. 21.15 for a particular lamp with $V_0 = 100\,\text{V}$ and $P_0 = 1\,\text{W}$.

This model can be implemented very easily in circuit simulation programs, such as SPICE-based programs. Figure 21.16 shows the electric circuit and the description used to model the lamp behavior in a SPICE-based simulation program. The voltage-controlled voltage source EL is used to model the resistive behavior of the lamp. The voltage source VS is used to measure the lamp current so that the instantaneous and average lamp power can be calculated; for this reason its voltage value is equal to zero. GP is a voltage-controlled power source used to calculate the instantaneous lamp power, which is then filtered by RP and CP in order to obtain the averaged lamp power. Finally, the hyperbolic relationship between lamp resistance and power is implemented by means of the voltage-controlled voltage source EK. The time constant $\tau = \text{RP} \cdot \text{CP}$ is related to the ionization constant of the discharge.

Figure 21.17 illustrates some simulation results at low frequency when the lamp is supplied from a sinusoidal voltage source and stabilized with an inductive ballast.

The Mader–Horn model can also be used at high frequencies to give a resistive behavior for the lamp. The equivalent lamp resistance at high frequency will also exhibit a hyperbolic variation with the averaged lamp power and with a time constant given by τ. This model is then useful to simulate electronic ballasts with dimming features.

TABLE 21.3 Estimated electric data for discharge lamps at high frequency

Lamp	$V_{LA,hf}$	$I_{LA,hf}$	$R_{LA,hf}$
Fluorescent lamps	$P_{LA}/I_{LA,lf}$	$I_{LA,lf}$	$P_{LA}/I^2_{LA,lf}$
High-pressure lamps	$V_{LA,lf}$	$P_{LA}/V_{LA,lf}$	$V^2_{LA,lf}/P_{LA}$

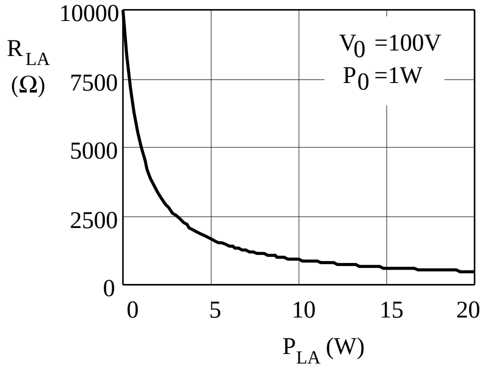
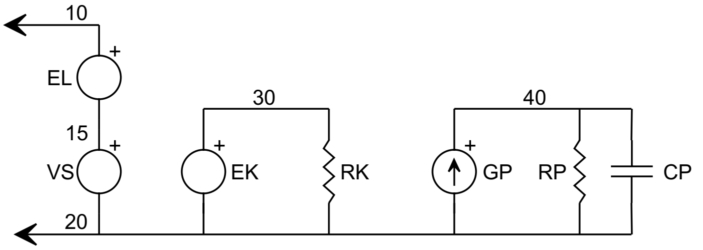


FIGURE 21.15 Lamp resistance versus lamp power characteristic.

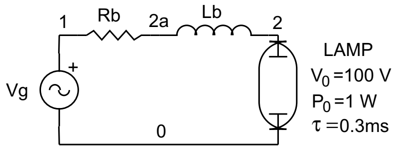


(a)

```
.subckt lamp 10 20
+ params: V =100 P =1 Tau=0.3m
E  10 15 Value={V(30,20)*I(VS)}
VS 15 20 0
EK 30 20 Value={V *V /(V(40,20)+P )}
 K 30 20 1
GP 20 40 Value={V(10,20)*I(VS)}
 P 40 20 1
 P 40 20 {Tau}
.ends
```

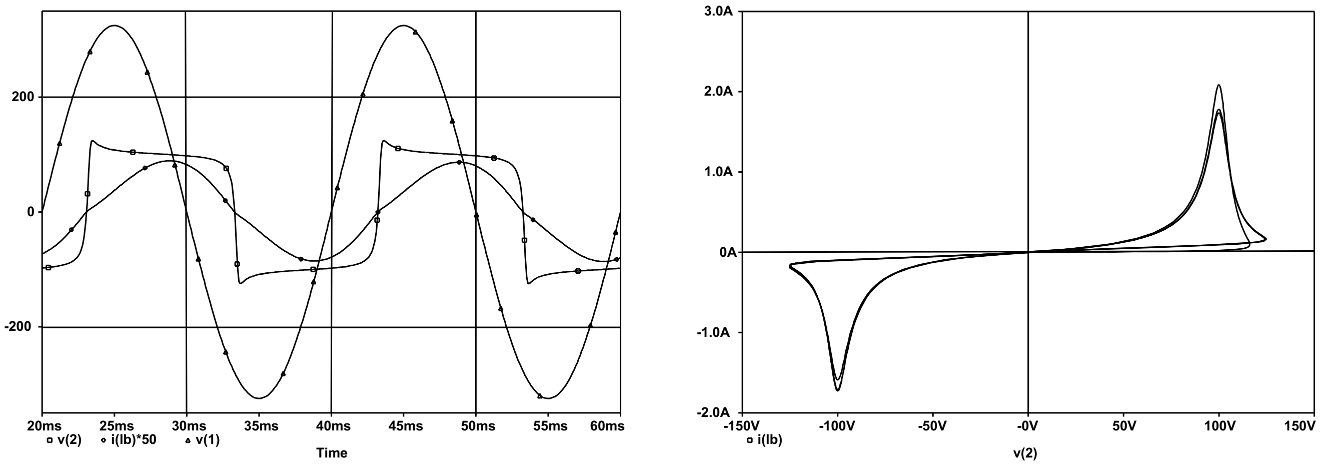
(b)

FIGURE 21.16 (a) Mader–Horn linear model for discharge lamps; and (b) SPICE description of the model.



```
Vg 1 0 SIN(0 325 50)
 b 1 2a 100
 b 2a 2 500mH
X A 2 0  AMP
.tran 0.1m 60m 0 0.1m
```

(a)



(b) (c)

FIGURE 21.17 (a) Example of simulation with an inductive ballast at low frequency; (b) Operating waveforms; and (c) Lamp *I–V* characteristic.

Discharge lamp modeling has become an important subject, because it is very useful in optimizing the electronic ballast performance. Some improvements on the Mader–Horn model and other interesting models can be found in the literature [8–10].

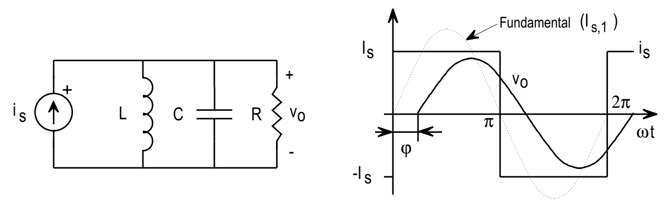
21.4 Resonant Inverters for Electronic Ballasts

Most modern domestic and industrial electronic ballasts use resonant inverters to supply discharge lamps. They can be implemented in two basic ways: current-fed resonant inverters and voltage-fed resonant inverters.

21.4.1 Current-Fed Resonant Inverters

One of the most popular topologies belonging to this category is the current-fed push–pull resonant inverter, previously shown in Fig. 21.11. For this reason, this inverter will be studied here to illustrate the operation of current-fed resonant ballasts.

The current-fed push–pull inverter uses an input choke to obtain a dc input current with low current ripple. This current is alternately conducted by the switches so that a parallel



(a) (b)

FIGURE 21.18 (a) Equivalent circuit of a parallel resonant inverter; and (b) Operating waveforms.

resonant tank can be supplied with a current square wave. Figure 21.18 shows the equivalent circuit and the operating waveforms of a current-fed resonant inverter.

The input current can be expressed as a Fourier series in the following way:

$$i_s(t) = \sum_{n=1,3,5\ldots} I_{S,n} \sin n\omega t = \sum_{n=1,3,5\ldots} \frac{4I_S}{n\pi} \sin n\omega t \tag{21.5}$$

$I_{S,n}$ is the peak value of each current harmonic, and I_S is the dc input current of the inverter. The output voltage for each current harmonic is obtained by multiplying the input current $I_{S,n}$ by the equivalent parallel impedance $Z_{E,n}$:

$$V_{o,n} = I_{S,n} Z_{E,n} = I_{S,n} \frac{1}{1/R + jn\omega C - j(1/n\omega L)} \tag{21.6}$$

Usually, normalized values are employed in order to provide more general results. Then, the output voltage can be expressed as follows:

$$V_{o,n} = I_{S,n} Z_B \frac{1}{1/Q + jn\Omega - j(1/n\Omega)} \tag{21.7}$$

where Z_B is the base impedance of the resonant tank, Q is the normalized load, Ω is the normalized frequency, and ω_0 is the natural frequency of the resonant circuit, given by:

$$Z_B = \sqrt{L/C}, \quad Q = R/Z_B, \quad \Omega = \omega/\omega_0 = \omega\sqrt{LC}, \quad \omega_0 = 1/\sqrt{LC} \tag{21.8}$$

From (21.7) the peak output voltage $V_{o,n}$ and phase angle φ_n can be obtained for each harmonic:

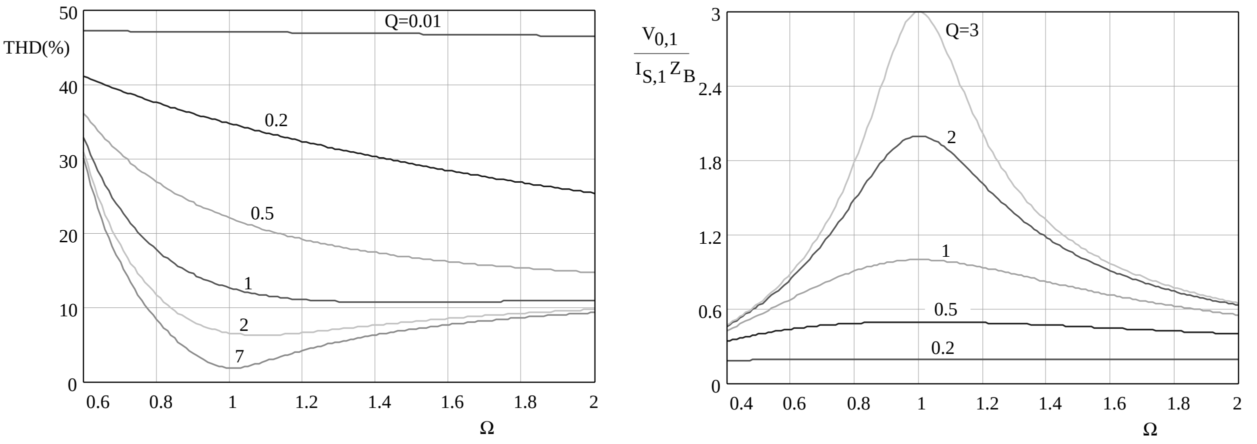
$$V_{o,n} = I_{S,n} Z_B \frac{1}{\sqrt{1/Q^2 + (n\Omega - 1/n\Omega)^2}} \tag{21.9}$$

$$\varphi_n = -\tan^{-1} Q(n\Omega - 1/n\Omega) \tag{21.10}$$

The total harmonic distortion (THD) of the output voltage can be calculated as follows:

$$\mathrm{THD}(\ ) = \frac{\sqrt{\sum_{n=3,5,7\ldots} V_{o,n}^2}}{V_{o,1}} \cdot 100 \tag{21.11}$$

Based on these equations, the analysis and design of the current-fed resonant inverter can be performed. Normally, the circuit operates close to the natural frequency ω_0, and the effect of the high-frequency harmonics can be neglected. To probe this, Fig. 21.19a illustrates the THD of the output voltage as a function of the normalized load and frequency, obtained by plotting (21.11). As can be seen, for values of Q greater than 1 and for operation close to the natural frequency ($\Omega = 1$), the THD is low, which means that the output voltage is nearly a sinusoidal waveform. However, for low values of Q the output voltage tends to be a square waveform, and the THD tends to a value of about 48 , corresponding to the THD of a square waveform. Figure 21.19b illustrates the normalized output voltage for the fundamental component.



(a) (b)

FIGURE 21.19 Characteristics of the parallel resonant inverter: (a) THD; and (b) fundamental output voltage.

As stated previously, when used as a lamp ballast the parallel resonant inverter operates at the natural frequency of the resonant tank to both ignite the lamp and limit the current in normal operation. If we neglect the effect of high-order harmonics, the rms output voltage is given by the fundamental component and can be obtained using $\Omega = 1$ in (21.9) as follows:

$$V_{o(rms)} \approx V_{o,1(rms)} = I_{S,1(rms)} Z_B Q = \frac{4 I_S R}{\pi\sqrt{2}} \tag{21.12}$$

In a current-fed resonant inverter, the dc input current I_S is supplied from a dc voltage source V_{in} with a series choke, as stated previously. Then, the dc input current can be obtained, assuming 100% efficiency, by equaling input and output power as follows:

$$P_{in} = V_{in} I_S = \frac{V_{o(rms)}^2}{R} \tag{21.13}$$

and then:

$$I_S = \frac{V_{o(rms)}^2}{V_{in} R} \tag{21.14}$$

Using (21.14) in (21.12) and solving for the output voltage:

$$V_{o(rms)} = \frac{\pi\sqrt{2}}{4} V_{in} = 1.1 V_{in} \tag{21.15}$$

As can be seen, in operation at the natural frequency, the rms output voltage is independent of the resonant tank load. The peak output voltage is equal to $\pi V_{in}/2$. This value is directly related to the peak voltage stress in the switches. For a full bridge topology such as that shown in Fig. 21.11c, this value is equal to the switch voltage stress. However, for the current-fed push–pull inverter the voltage stress is twice this value, that is, πV_{in}, because of the presence of the transformer. This gives a very high voltage stress for the switches in this topology, which is why the current-fed push–pull is mainly used to implement low-input-voltage ballasts.

On the other hand, the lamp starting voltage can vary from 5 to 10 times the lamp voltage in normal discharge mode. This makes it difficult to use the parallel resonant inverter at constant frequency to both ignite the lamp and supply it at steady state, since the output voltage is independent of the resonant tank load.

One solution to this problem is to ignite the lamp at the resonant tank natural frequency and then change the frequency to decrease the output voltage and output current to the normal running values of the lamp. This solution makes necessary the use of extra circuitry to control the frequency, normally in a closed loop to avoid lamp instabilities, which increase ballast cost.

Another solution, often used in low-cost ballasts, is to design the parallel resonant tank to ignite the lamp, and limit the lamp current in discharge mode by using an additional reactive element in series with the lamp. Normally a capacitor is used to limit the lamp current in order to minimize the cost of the ballast. This solution is used in combination with the self-oscillating technique, which ensures operation at a constant frequency equal to the natural frequency of the resonant tank. Figure 21.20a illustrates this circuit. Normally the effect of the series capacitor is neglected and the resonant tank is assumed to behave as a sinusoidal voltage source during both ignition and normal operation, as shown in Fig. 21.20b. The high lamp starting voltage is obtained by means of a step-up transformer, which is why typically a push–pull topology is used. If V_{in} is the dc input voltage and V_{ig} is the lamp ignition voltage, then the necessary transformer turn ratio is given by the following expression:

$$\frac{N_2}{N_1} = \frac{V_{ig}}{\pi V_{in}/2} \tag{21.16}$$

and the rms lamp current in discharge mode can be approximated as follows:

$$I_{LA} = \frac{1.1 (N_2/N_1) V_{in}}{\sqrt{R^2 + (1/2\pi f C_S)^2}} \tag{21.17}$$

R is the equivalent resistance of the lamp. From (21.17) the necessary value of the series capacitor C_S used to limit the lamp current to the nominal value I_{LA} can be easily obtained.

Finally, Figs. 21.21a and 21.21b illustrate a typical ballast based on a current-fed resonant inverter and its equivalent circuit, respectively.

21.4.2 Voltage-Fed Resonant Inverters

Some voltage-fed resonant inverters used to supply discharge lamps were previously shown in Fig. 21.12. Basically, they use two or more switches to generate a square voltage waveform. The different topologies are mainly given by the type of resonant tank used to filter this voltage waveform. There are three typical resonant tanks, whose equivalent circuits are

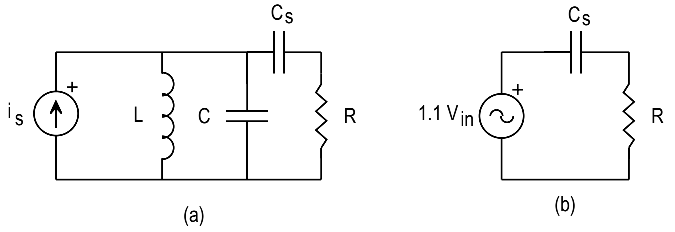


FIGURE 21.20 (a) Typical parallel resonant circuit used to supply discharge lamps; and (b) Equivalent circuit.

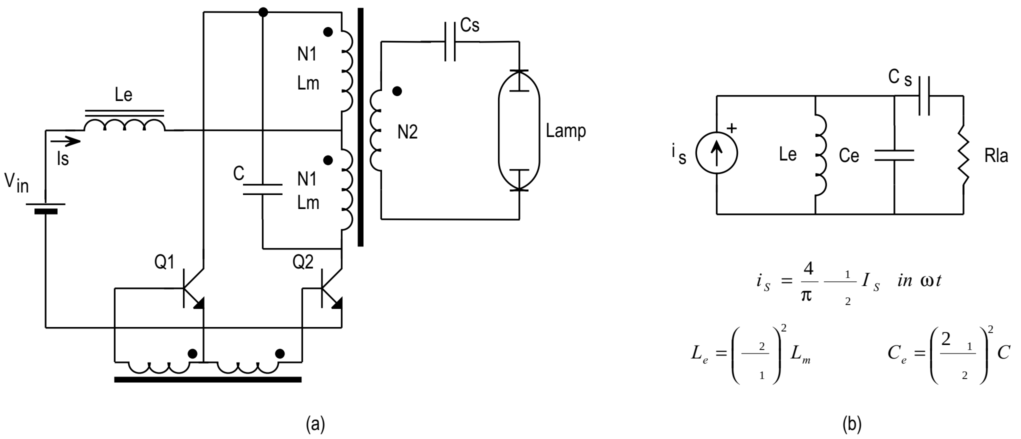

Cs
N1
Lm
Le
N2
Lamp
Is
Vin
C
N1
Lm
Q1
Q2
Cs
is
Le
Ce
Rla
$i_S = \frac{4}{\pi} \frac{1}{2} I_S$ in ωt
$L_e = \left(\frac{2}{1}\right)^2 L_m$
$C_e = \left(\frac{2}{\ \ }\frac{1}{2}\right)^2 C$
(a)
(b)

FIGURE 21.21 (a) Self-oscillating current-fed push–pull electronic ballast. (b) Equivalent circuit.

shown in Fig. 21.22. These circuits are the series-loaded resonant tank (Fig. 21.22a), the parallel-loaded resonant tank (Fig. 21.22b), and the series–parallel-loaded resonant tank (Fig. 21.22c). The typical operating waveforms are shown in Fig. 21.22d.

Similarly to the current-fed resonant inverter, the input voltage can be expressed as a Fourier series in the following way:

$$v_s(t) = \sum_{n=1,3,5\ldots} V_{S,n} \sin n\omega t = \sum_{n=1,3,5\ldots} \frac{4V_S}{n\pi} \sin n\omega t \quad (21.18)$$

$V_{S,n}$ is the peak value of each voltage harmonic, and V_S the dc input voltage of the inverter. The same methodology used to analyze the current-fed resonant inverter will be used here to study the behavior of the three basic voltage-fed resonant inverters.

21.4.2.1 Series-Loaded Resonant Circuit

The output voltage corresponding to the n-order harmonic is easily obtained as follows:

$$V_{o,n} = V_{S,n} \frac{1}{\sqrt{1 + \frac{1}{Q_S^2}\left(n\Omega - \frac{1}{n\Omega}\right)^2}} \quad (21.19)$$

where Q_S and Ω are the normalized load and switching frequency given by the following expressions:

$$Q_S = R/Z_B = R(L/C_S)^{-1/2}, \ \Omega = \omega/\omega_o = \omega\sqrt{LC_S} \quad (21.20)$$

Figure 21.23a shows the THD of the series-loaded circuit and Fig. 21.23b shows the fundamental output voltage, which is normally considered for design purposes.

In this circuit the input and output current are equal and can be calculated by dividing the output voltage by the load impedance. This current is also circulating through the inverter switches and therefore represents an important parameter for the design. Another important parameter is the phase angle of the input current, which defines the type of commutations in the inverter switches. For the fundamental harmonic, the phase angle of the current circulating through the resonant tank can be calculated as follows:

$$\varphi = -\tan^{-1}\frac{\Omega - 1/\Omega}{Q_S} \quad (21.21)$$

At the natural frequency (ω_0) the input voltage and current will be in phase, which means that no reactive energy is handled by the circuit and all the input energy is transferred to the load at steady-state operation. For frequencies higher than ω_0, the current is lagged and some reactive energy will be

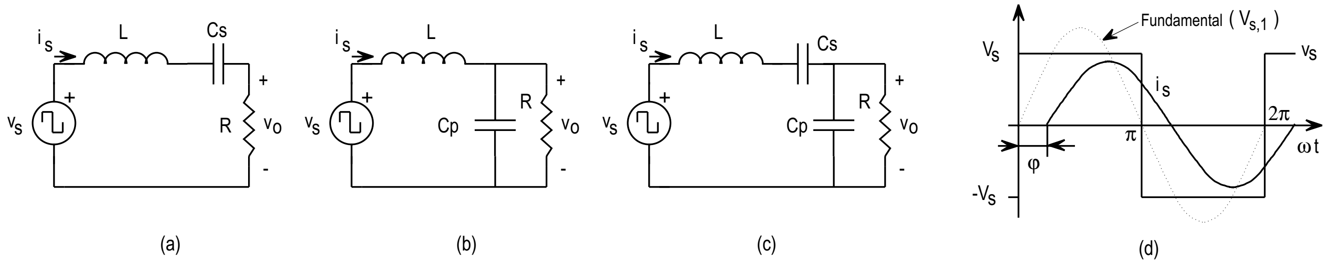
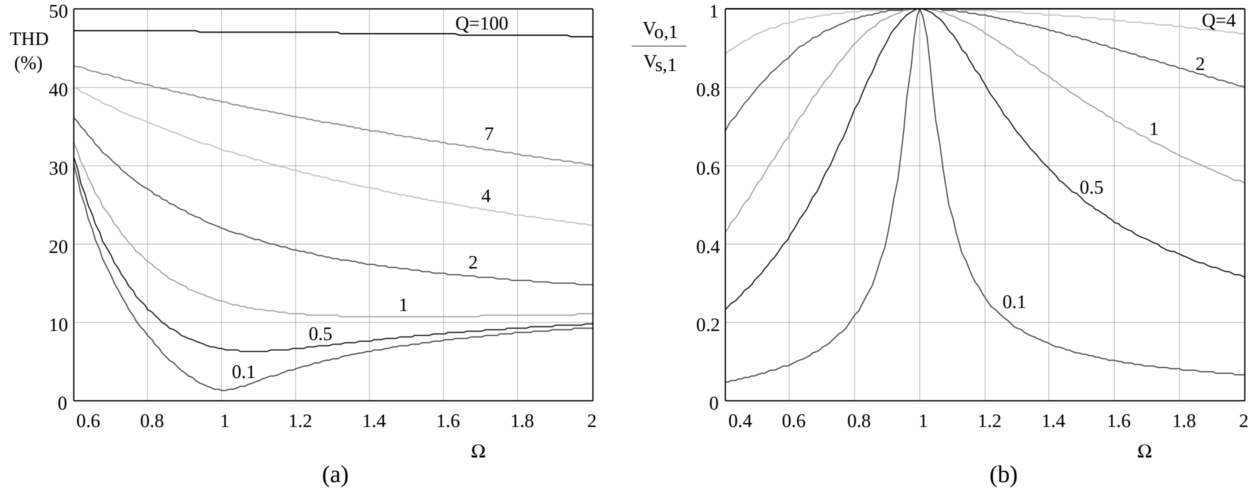


FIGURE 21.22 (a)–(c) Equivalent circuits of voltage-fed resonant inverters; and (d) typical operating waveforms.



(a) (b)

FIGURE 21.23 Characteristics of series-loaded resonant inverter: (a) THD; and (b) fundamental output voltage.

handled. In this case the inverter switches will present zero-voltage switching (ZVS) [22]. For frequencies lower than ω_0, the current is in advance and also some reactive energy will be handled. In this case the inverter switches will present zero-current switching (ZCS).

As can be seen in Fig. 21.23a, the THD is lower for the lower values of the normalized load and for frequencies close to the natural frequency of the resonant tank. For the higher values of Q_S the THD tends to the value corresponding to a square wave. The output voltage is always lower than the input voltage, and for frequencies around the natural frequency the circuit behaves as a voltage source, especially for high values of Q_S. This means that the lamp cannot be ignited and supplied in discharge mode while maintaining constant switching frequency. This behavior is similar to that encountered for the current-fed resonant inverter. The use of step-up transformers is mandatory to achieve lamp ignition, especially for low input voltages. In order to maintain a constant operating frequency, a series element will be necessary to limit the lamp current at normal discharge operation. A capacitor can also be used, as discussed in a previous section. In summary, this circuit is mainly used in high-input-voltage, low-current applications, and it is not often used to implement electronic ballasts.

21.4.2.2 Parallel-Loaded Resonant Circuit

In this circuit, the output voltage corresponding to the n-order harmonic is given by the following expression:

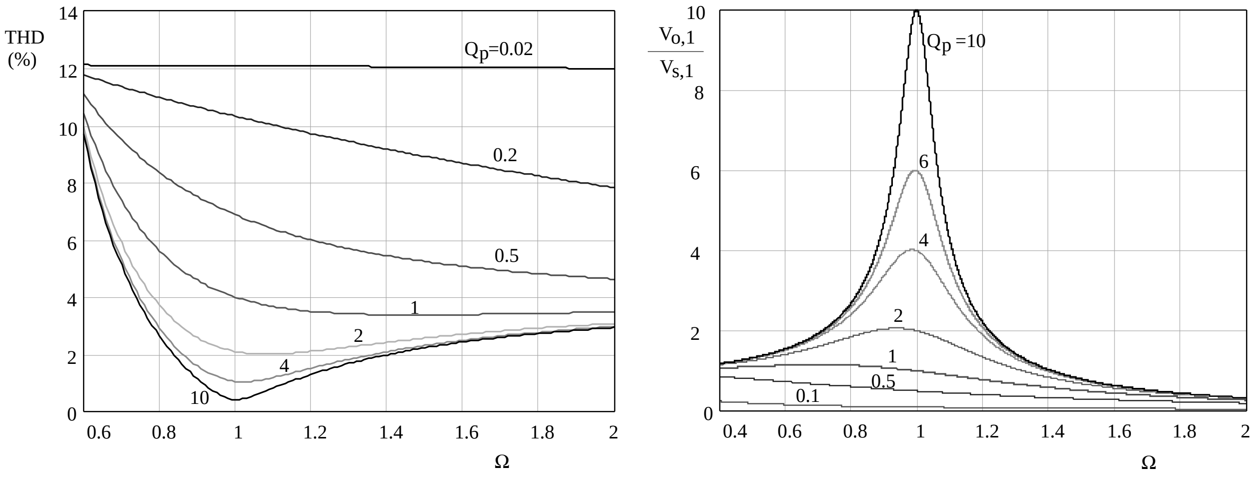
$$V_{o,n} = V_{S,n}\frac{1}{\sqrt{\dfrac{n^2\Omega^2}{Q_P^2}+(n^2\Omega^2-1)^2}} \tag{21.22}$$

where:

$$Q_P = R/Z_B = R(L/C_P)^{-1/2},\ \Omega = \omega/\omega_0 = \omega\sqrt{LC_P} \tag{21.23}$$

The THD and fundamental output voltage are shown in Fig. 21.24. This circuit presents characteristics that are much more useful in implementing electronic ballasts than the series-loaded resonant circuit. First, the THD of the output voltage around the natural frequency is in general much lower than that of the series circuit. For the lower values of Q_P, the THD tends to a value of 12 , which corresponds to the THD of a triangular wave. As a result, the lamp voltage and current waveforms will be very similar to a sine wave, which is the more adequate waveform to supply the lamp. Secondly, the frequency response of the output voltage (Fig. 21.24b) makes it possible to both ignite the lamp and limit the lamp current at steady state while maintaining constant operating frequency. During ignition the lamp behaves as a very high impedance, thus giving a high value of Q_P. Under these conditions the parallel circuit can generate a very high output voltage, provided that the operating frequency is close to the natural frequency. Once the lamp is ignited, the normalized load Q_P decreases and the circuit can limit the lamp current without changing the operating frequency. In fact, the parallel circuit operating close to the natural frequency behaves as a current source for the load, as will be shown later. This behavior is very adequate to supply discharge lamps because it ensures good discharge stability, keeping the lamp from being easily extinguished by transitory power fluctuations.

The maximum value of the voltage gain shown in Fig. 21.24 can be calculated to be equal to $Q_P/\sqrt{1-1/4Q_P^2}$, and it appears at a frequency $\Omega_m = \sqrt{1-1/2Q_P^2}$. This means that a maximum is only present if Q_P is greater than $1/\sqrt{2} \approx 0.71$. For the higher values of Q_P, the maximum gain can be



(a) (b)

FIGURE 21.24 Characteristics of parallel-loaded resonant inverter: (a) THD; and (b) fundamental output voltage.

approximated by Q_P and the frequency of the maximum gain can be approximated to the natural frequency ω_0.

The input current of the parallel resonant circuit is another important parameter to calculate the current handled by the inverter switches. Since the operating frequency is normally around resonance, only the fundamental component is considered. The value of this fundamental current and its phase angle can be obtained as follows:

$$I_{S,1} = \frac{V_{s,1}}{Z_B}\sqrt{\frac{1+Q_P^2\Omega^2}{\Omega^2+Q_P^2(\Omega^2-1)^2}} \tag{21.24}$$

$$\varphi = \tan^{-1}\frac{-1}{\Omega Q_P} - \tan^{-1} Q_P\left(\Omega-\frac{1}{\Omega}\right) \tag{21.25}$$

The condition for the input voltage being in phase with the input current can be obtained by equaling (21.25) to zero. This gives a value of the normalized frequency: $\Omega_{\varphi=0} = \sqrt{1-1/Q_P^2}$. For a frequency greater than that value, the input current will lag the input voltage and the inverter switches will present zero-voltage switching. For frequencies lower than that value, the current will be in advance and zero-current switching is obtained. The output voltage gain at that frequency is equal to Q_P.

Finally, it is very interesting to study the behavior of this circuit for frequencies close to the natural frequency ω_0 ($\Omega = 1$), since this is the normal region selected to operate for ballast applications. At this frequency, the output voltage gain is equal to Q_P and then the output current will be $V_{S,1}/Z_B$. This means that when operated at the natural frequency the parallel circuit behaves as a current source, whose value depends only on the input voltage. At the natural frequency the input current is equal to $V_{s,1}\sqrt{1+Q_P^2}/Z_B$ and the phase angle is equal to $\tan^{-1}(-1/Q_P)$. The behavior of the circuit is always inductive, with zero-voltage switching, and the phase angle decreases with increasing Q_P, which means that less reactive energy is handled by the circuit.

21.4.2.3 Series Parallel-Loaded Resonant Circuit

This circuit is also often used to implement electronic ballasts. The fundamental output voltage is given by the following expression:

$$V_{o,1} = V_{s,1}\frac{1}{\sqrt{\dfrac{1}{Q_{SP}^2}\left(\Omega-\dfrac{1-\alpha}{\Omega}\right)^2+\dfrac{1}{\alpha^2}(\Omega^2-1)^2}} \tag{21.26}$$

where:

$$\begin{gathered} Q_{SP} = R/Z_B = R(L/C_E)^{-1/2},\ \Omega = \omega/\omega_o = \omega\sqrt{LC_E}, \\ \alpha = C_E/C_P = 1 - C_E/C_S \end{gathered} \tag{21.27}$$

and $C_E = C_S C_P/(C_S + C_P)$ is the series equivalent of the two capacitors present in this resonant circuit.

The fundamental input current and its phase angle are the following:

$$I_{S,1} = \frac{V_{S,1}}{Z_B}\left[\frac{1+\dfrac{\Omega^2 Q_{SP}^2}{\alpha^2}}{\left(\Omega-\dfrac{1-\alpha}{\Omega}\right)^2+\dfrac{Q_{SP}^2}{\alpha^2}(\Omega^2-1)^2}\right]^{1/2} \tag{21.28}$$

$$\varphi = \begin{cases} \tan^{-1}\dfrac{-\alpha}{Q_{SP}\Omega} - \tan^{-1}\left(\dfrac{Q_{SP}}{\alpha}\dfrac{\Omega^2-1}{\Omega-\dfrac{1-\alpha}{\Omega}}\right) + 180^\circ \\ \qquad\qquad\qquad\qquad \text{if } \Omega < \Omega_c = \sqrt{1-\alpha} \\ \tan^{-1}\dfrac{-\alpha}{Q_{SP}\Omega} - \tan^{-1}\left(\dfrac{Q_{SP}}{\alpha}\dfrac{\Omega^2-1}{\Omega-\dfrac{1-\alpha}{\Omega}}\right) \\ \qquad\qquad\qquad\qquad \text{if } \Omega \ge \Omega_c = \sqrt{1-\alpha} \end{cases} \tag{21.29}$$

Figure 21.25 shows the characteristics corresponding to the THD of the output voltage and the fundamental output voltage for $\alpha = 0.5$. As can be seen, the THD is also very low around the natural frequency, especially for the higher values of the normalized load Q_{SP}. Regarding the output voltage, this circuit behaves as a parallel circuit around the natural frequency ω_0, with a maximum gain voltage of about Q_{SP}/α. Around the natural frequency of the series circuit given by L and C_S, $\omega_{0S} = \omega_0\sqrt{1-\alpha}$, the circuit behaves as a series-loaded circuit with a maximum voltage gain equal to unity.

The series–parallel circuit can also be used to both ignite and supply the lamp at constant frequency, since it also behaves as a current source at the natural frequency. Besides, this circuit allows limiting the ignition voltage by means of the factor α, thus avoiding sputtering damage of lamp electrodes. Also, the series capacitor can be used to block any dc component of the inverter square output voltage, such as that existing in the asymmetric half-bridge. In summary, the series–parallel circuit combines the best features of the series-loaded and the parallel-loaded circuits, and this is why it is often used to implement electronic ballasts.

When operated at frequency ω_0 the output voltage gain is equal to Q_{SP}/α, and then the circuit behaves as a current source equal to $V_{S,1}/\alpha Z_B$, which is independent of the load. As stated previously, this is very adequate for supplying discharge lamps. The input current phase angle at this frequency is equal to $\tan^{-1}(-\alpha/Q_{SP})$, and the input current always lags the input voltage, thus showing zero-voltage switching.

Finally, the condition to have input current in phase with the input voltage can be obtained by setting (21.29) equal to zero. This gives the following value:

$$Q_{SP,\varphi=0} = \frac{\alpha}{\Omega}\sqrt{\frac{\Omega^2-(1-\alpha)}{1-\Omega^2}} \tag{21.30}$$

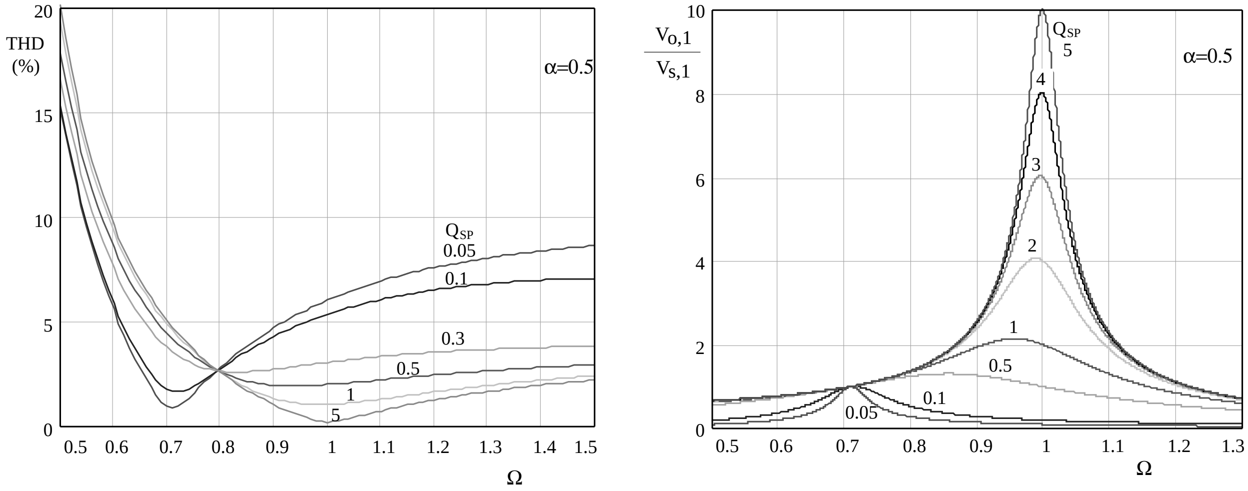
Equation (21.30) defines the borderline between zero-voltage switching and zero-current switching modes. The output voltage gain in this borderline can be obtained by using (21.30) in (21.26), and it is equal to $\alpha/\sqrt{\alpha(1-\Omega^2)}$.

21.4.3 Design Issues

The design methodology of a resonant inverter for discharge-lamp supply can be very different depending on the lamp type and characteristics, inverter topology, design goals, etc. Some guidelines focused especially on supplying fluorescent lamps with voltage-fed resonant inverters are presented in this section to illustrate the basic design methodology.

A typical starting process for a hot cathode fluorescent lamp is shown in Fig. 21.26. Initially, lamp electrodes are heated up to the emission temperature. During this phase, the inverter should ensure a voltage applied to the lamp that is not high enough to produce sputtering damage in lamp electrodes, thus avoiding premature aging of the lamp. Once electrodes reach the emission temperature, the lamp can be ignited by applying the necessary starting voltage. Following this procedure, soft starting is achieved and long lamp life is ensured.

The best method to perform this soft starting is to control the inverter switching frequency so that the lamp voltage and current are always under control. During the heating process the operating frequency is adjusted to a value over the natural frequency of the resonant tank. In this way, the heating current can be adjusted to the necessary value, maintaining a lamp voltage that is much lower than the starting voltage. Since normally MOSFET or bipolar transistors are used, operation over the natural frequency is preferable, because it provides ZVS and the slow parasitic diodes existing in these transistors can be used. After a short period of time, the switching frequency is reduced until the starting voltage is obtained; then the lamp is ignited. Normally, the final operating point at



(a) (b)

FIGURE 21.25 Characteristics of series–parallel-loaded resonant inverter: (a) THD; and (b) fundamental output voltage.

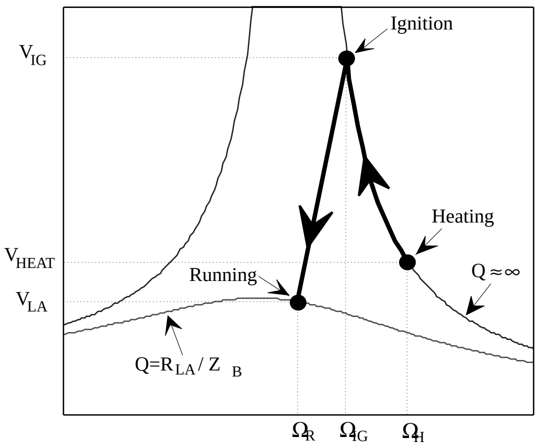


FIGURE 21.26 Typical starting process of discharge lamps.

steady-state operation is adjusted to be at a switching frequency equal to the natural frequency, so that very stable operation for the lamp is ensured.

Figure 21.27a shows a fluorescent lamp supplied using a series–parallel resonant tank. The input data for the design are normally the fundamental input voltage V_S, the switching frequency in normal discharge operation (running) f_S, the lamp voltage and current at high frequency V_{LA}, I_{LA}, the electrode heating current I_H, the maximum lamp voltage during heating process V_H, and the lamp starting voltage V_{IG}.

The equivalent circuit during the heating and ignition phase is shown in Fig. 21.27b. The current circulating in this circuit is the electrode heating current, which can be calculated by using $Q_{SP} = \infty$ in (21.28):

$$I_H = \frac{V_S / Z_B}{\Omega - 1/\Omega} \tag{21.31}$$

where the electrode resistance has been neglected for simplicity. For a given heating current I_H, the necessary switching frequency is obtained from (21.31) as follows:

$$\Omega_H = \frac{V_S}{2Z_B I_H} + \sqrt{1 + \left(\frac{V_S}{2Z_B I_H}\right)^2} \tag{21.32}$$

Regarding the heating voltage, it can be calculated from (21.26) using $Q_{SP} = \infty$, and the following value is obtained:

$$V_H = \frac{\alpha V_S}{\Omega_H^2 - 1} \tag{21.33}$$

The frequency at which the starting voltage is achieved can also be obtained using $Q_{SP} = \infty$ in (21.26), giving the following value:

$$\Omega_{IG} = \sqrt{1 + \alpha \frac{V_S}{V_{IG}}} \tag{21.34}$$

Once the lamp is ignited, the new operating circuit is shown in Fig. 21.27c. Normally the switching frequency is selected to be very close to the natural frequency, and the circuit characteristics can be obtained by setting $\Omega = 1$. Thus, as stated previously, the circuit behaves as a current source of the following value:

$$I_{LA} = \frac{V_S}{\alpha Z_B} \tag{21.35}$$

From this equation the impedance Z_B needed to provide a lamp current equal to I_{LA} is easily obtained:

$$Z_B = \frac{V_S}{\alpha I_{LA}} \tag{21.36}$$

Using Eqs. (21.31)–(21.36), the design procedure can be performed as follows:

Step 1: Steady-state operation. Choose a value for the factor α; normally a value of 0.8–0.9 will be adequate for most applications. From (21.36) calculate the value of Z_B for the resonant tank. Since the natural frequency is equal to the switching frequency, the reactive elements of the resonant tank can be calculated as follows:

$$L = \frac{Z_B}{2\pi f_S}, \quad C_P = \frac{1}{2\pi f_S \alpha Z_B}, \quad C_S = \frac{1}{2\pi f_S (1-\alpha) Z_B} \tag{21.37}$$

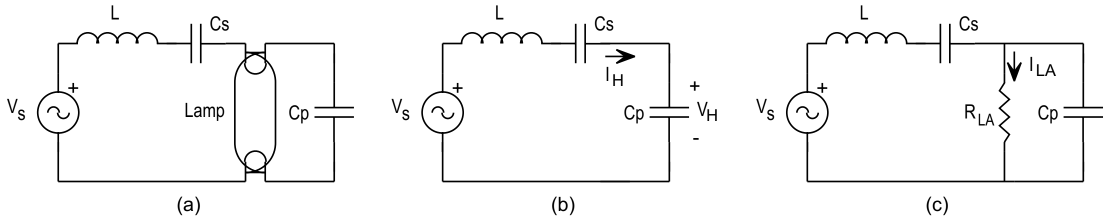


FIGURE 21.27 (a) Fluorescent lamp supplied with a series–parallel circuit; (b) equivalent circuit during heating and ignition; and (c) equivalent circuit during normal discharge mode.

Step 2: Heating phase. From (21.32) calculate the switching frequency for a given heating current I_H. Then, calculate the value of the heating voltage V_H from (21.33).

Step 3: Check if the heating voltage is lower than the maximum value allowed to avoid electrode sputtering. If the voltage is too high, choose a lower value of α and repeat steps 1 and 2. Also, the maximum heating frequency can be limited to avoid excessive frequency variation. The lower the value of α, the lower the frequency variation from heating to ignition, since the output voltage characteristics are narrower for the lower values of α.

The described procedure to achieve lamp soft ignition requires the use of a voltage-controlled oscillator to control the switching frequency. This can increase the cost of the ballast. A similar soft ignition can be achieved using the resonant circuit shown in Fig. 21.28. This circuit is often used in self-oscillating ballasts, where the switches are driven from the resonant current using a current transformer [23].

In the circuit shown in Fig. 21.28, the PTC is initially cold and capacitor C_{P1} is bypassed by the PTC. The resonant tank under these conditions is formed by L–C_S–C_{P2}, which can be designed to heat the lamp electrodes with a heating voltage low enough to avoid lamp cold ignition. Since the PTC is also heated by the circulating current, after a certain period of time it reaches the threshold temperature and trips. At this moment, the new resonant tank is formed by L, C_S, and the series equivalent of C_{P1} and C_{P2}. This circuit can be designed to generate the necessary ignition voltage and to supply the lamp in normal discharge mode. Once the lamp is ignited, the PTC maintains its high impedance since the dominant parallel capacitor in this phase is C_{P1} (usually $C_{P1} \ll C_{P2}$).

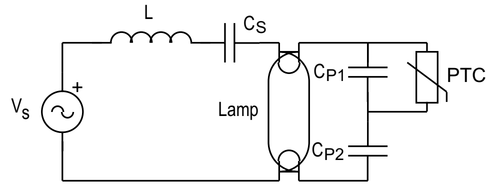


FIGURE 21.28 Resonant circuit using a PTC resistor.

21.5 High-Power-Factor Electronic Ballasts

As mentioned in a previous section, when electronic ballasts are supplied from the ac line an ac–dc stage is necessary to provide the dc input voltage of the resonant inverter (see Fig. 21.9). Since the introduction of harmonic regulations, such as IEC 1000-3-2, the use of a full-bridge diode rectifier followed by a filter capacitor is no longer applicable for this stage because of the high harmonic content of the input current. Therefore, the use of an ac–dc stage showing a high input power factor (PF) and a low total harmonic distortion (THD) of the input current is mandatory. The inclusion of this stage can greatly increase the cost of the complete ballast, and therefore the search for low-cost, high-power-factor electronic ballasts is an important field of research at present.

Figure 21.29a shows a first possibility to increase the input power factor of the ballast by removing the filter capacitor across the diode rectifier. However, since there are no low-frequency storage elements inside the resonant inverter, the output power instantaneously follows the input power, thus producing an annoying light flicker. Besides, the resulting lamp current crest factor is very high, which considerably decreases lamp life.

In order to avoid flicker and increase lamp current crest factor, continuous power must be delivered to the lamp. This can only be accomplished by using a PFC stage with a low-frequency storage element. This solution is shown in Fig. 21.29b, where capacitor C_0 is used as energy storage element. The main drawback of this solution is that the input power is handled by the two stages, which reduces the efficiency of the complete electronic ballast.

21.5.1 Harmonic Limiting Standards

The standards IEC 1000-3-2 and EN 61000-3-2 [24] are the most popular regulations regarding the harmonic pollution produced by electronic equipment connected to mains. These standards are a new version of the previous IEC 555-2 regulation and they are applicable to equipment with less than 16 A per phase and supplied from low-voltage lines of 220/380 V, 230/400 V, and 240/415 V at 50 or 60 Hz. Limits

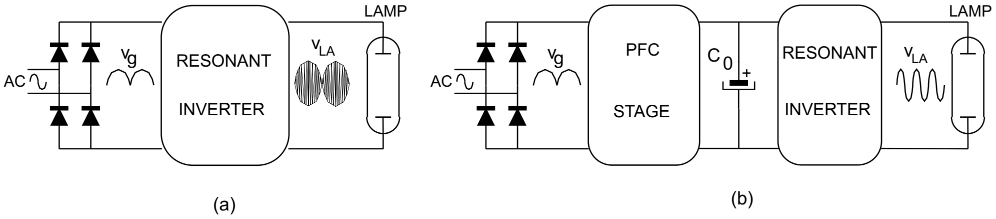


FIGURE 21.29 High-power-factor ballasts.

TABLE 21.4 IEC 1000-3-2: harmonic limits for class C equipment

Harmonic order n	Maximum Permissible Harmonic Current Expressed as a Percentage of the Input Current at the Fundamental Frequency
2	2
3	$30\lambda^a$
5	10
7	7
9	5
$11 \leq n \leq 39$ (odd harmonics only)	3

[a] λ is the circuit power factor.

for equipment supplied from voltages lower than 220 V have not yet been established.

This regulation divides electric equipment into several classes from class A to class D. Class C is especially for lighting equipment, including dimming devices; the harmonic limits for this class are shown in Table 21.4. As shown in the table, this regulation establishes a maximum amplitude for each input harmonic as a percentage of the fundamental harmonic component. The harmonic content established in Table 21.4 is quite restrictive, which means that the input current wave must be quite similar to a pure sine wave. For example, for a typical input power factor equal to 0.9 the total harmonic distortion calculated from Table 21.1 is only 32 .

21.5.2 Passive Solutions

A first possibility to increase the ballast power factor and to decrease the harmonic content of the input current is the use of passive solutions. Figure 21.30 shows two typical passive solutions, which can be used to improve the input power factor of electronic ballasts.

Figure 21.30a shows the most common passive solution based on a filter inductor *L*. Using a large inductance *L* a square input current can be obtained, with an input power factor of 0.9 and a THD of about 48 . A square input waveform does not satisfy the IEC 1000-3-2 requirements and thus is not a suitable solution. The addition of capacitor *C* across the ac terminals can increase the power factor to 0.95, but still the standard requirements are difficult to fulfill.

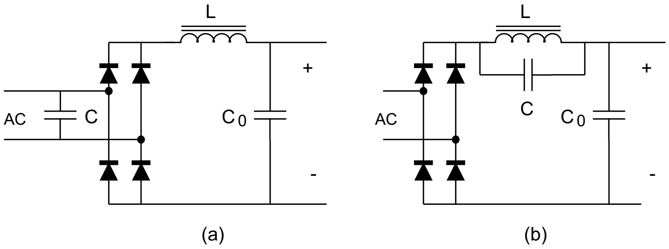


FIGURE 21.30 Passive circuits to improve input power factor: (a) LC filter; and (b) tuned LC filter.

A simple variation of this circuit is shown in Fig. 21.30b, where a parallel circuit tuned to the third harmonic of the line frequency is used to improve the shape of the line current. The input power factor obtained with this circuit can be close to unity.

A third possible solution, known as the valley-fill circuit, is shown in Fig. 21.31a. The typical filter capacitor following the diode rectifier is split into two different capacitors that are alternately charged using three extra diodes. The addition of a small series resistor improves the power factor in about two points, maintaining low cost for the circuit. An inductor in place of the resistor can also be used to improve the power factor, but with a higher cost penalty. Figure 21.31b shows the output voltage and input current of the valley-fill circuit. The main disadvantage of this circuit is the high ripple of the output voltage, which produces lamp power and luminous flux fluctuation and high lamp current crest factor.

Passive solutions are reliable, rugged, and cheap. However, the size and weight of these solutions are high and their design to fulfill the IEC 1000-3-2 requirements is usually difficult. Therefore, they are normally applied in the lower power range.

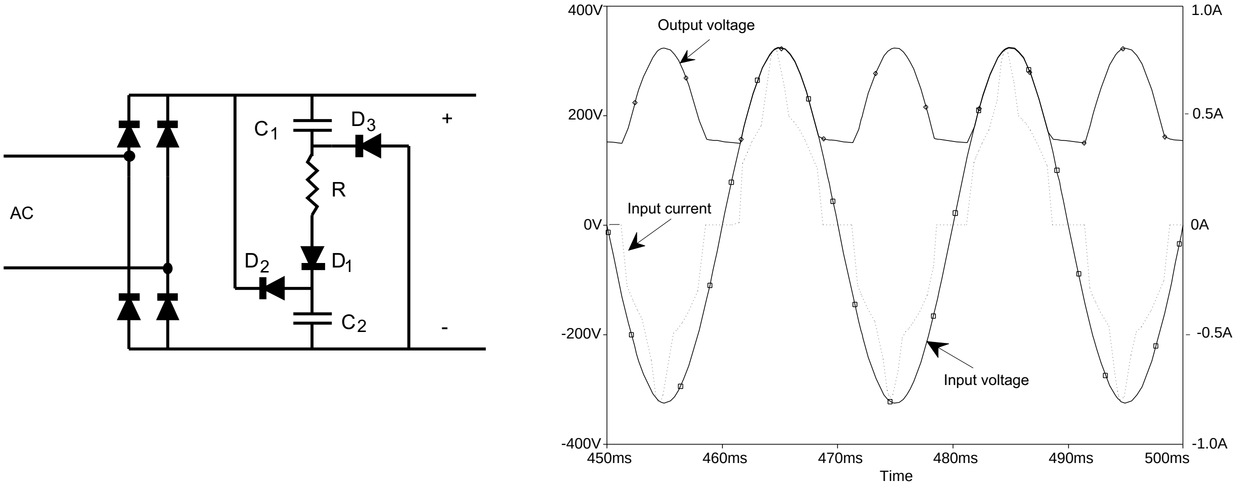
21.5.3 Active Solutions

Active circuits are the most popular solutions for implementing high-power-factor electronic ballasts. They use controlled switches to correct the input power factor and in some cases to include galvanic isolation via high-frequency transformers. Active circuits normally used in electronic ballasts operate at a switching frequency well above the line frequency and over the audible range.

Some typical active circuits used in electronic ballasts are shown in Fig. 21.32. Buck-boost and flyback converters, shown in Figs. 21.32a and 21.32b, respectively, can be operated in discontinuous conduction mode (DCM) with constant frequency and constant duty cycle in order to obtain an input power factor close to unity [25].

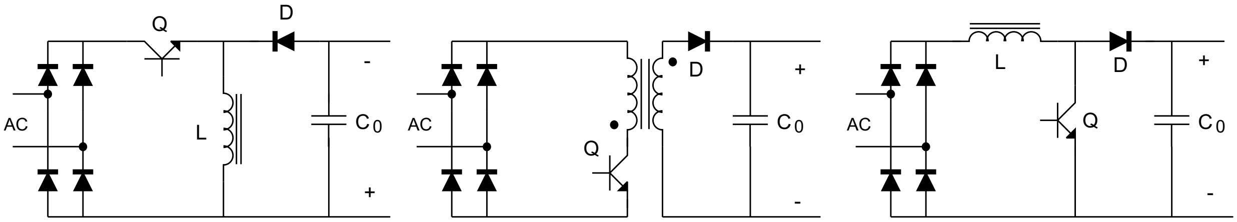
Figure 21.32c shows the boost converter, which is one of the most popular active circuits used to correct the input power factor of electronic ballasts [26–28]. If the boost converter is operated in DCM, an input power factor close to unity is obtained, provided that the output voltage is about twice the peak input voltage [26]. The main disadvantage of DCM operation, when compared to the CCM mode, is the high distortion of the input current (due to the discontinuous high-frequency current) and the higher current and voltage stresses in the switches. Therefore, DCM operation is only used for the lower power range.

For the medium power range, the operation of the boost converter at the DCM–CCM borderline is preferred. In this solution the on time of the controlled switch is maintained constant within the whole line period, and the switching frequency is adjusted to allow the input current to reach zero at the end of the switching period. The typical control



(a) (b)

FIGURE 21.31 Valley-fill circuit: (a) circuit diagram; and (b) waveforms.



(a) (b) (c)

FIGURE 21.32 Power factor correction circuits for ballasts: (a) buck-boost; (b) flyback; and (c) boost.

circuit used and the input current waveform are shown in Figs. 21.33a and 21.33b, respectively. The inductor current is sensed using a resistor in series with the switch, and the peak inductor current is programmed to follow a sine wave using a multiplier. A comparator is employed to detect the zero-crossing of the inductor current in order to activate the switch. Most IC manufacturers provide a commercial version of this circuit to be used for electronic ballast applications.

The boost circuit operating with borderline control provides a continuous input current, which is easier to filter. It also presents low switch turn-on losses and low recovery losses in the output diode. The main disadvantages are the variable switching frequency and the high output voltage, which must be higher than the peak line voltage.

For the higher power range, the boost converter can be operated in continuous conduction mode (CCM) to correct the input power factor. The input current in this scheme is continuous with very low distortion and easy to filter. The current stress in the switch is also lower, which means that more power can be handled, maintaining good efficiency. The normal efficiency obtained with a boost circuit operating either in the DCM–CCM borderline or in CCM can be as high as 95 .

21.6 Applications

Electronic ballasts are widely used in lighting applications such as portable lighting, emergency lighting, automotive applications, home lighting, and industrial lighting. They provide low volume and size, making it possible to reduce the luminaire size as well, with very interesting results for the new trends in lighting design.

21.6.1 Portable Lighting

In this application a battery is used as power source and then a low input voltage is available to supply the lamp. Examples are hand lanterns and back-lighting for laptop computers. Typical input voltages in these applications range from 1.5 to 48 V. Therefore, a step-up converter is necessary to supply the discharge lamp, and then electronic ballasts are the only

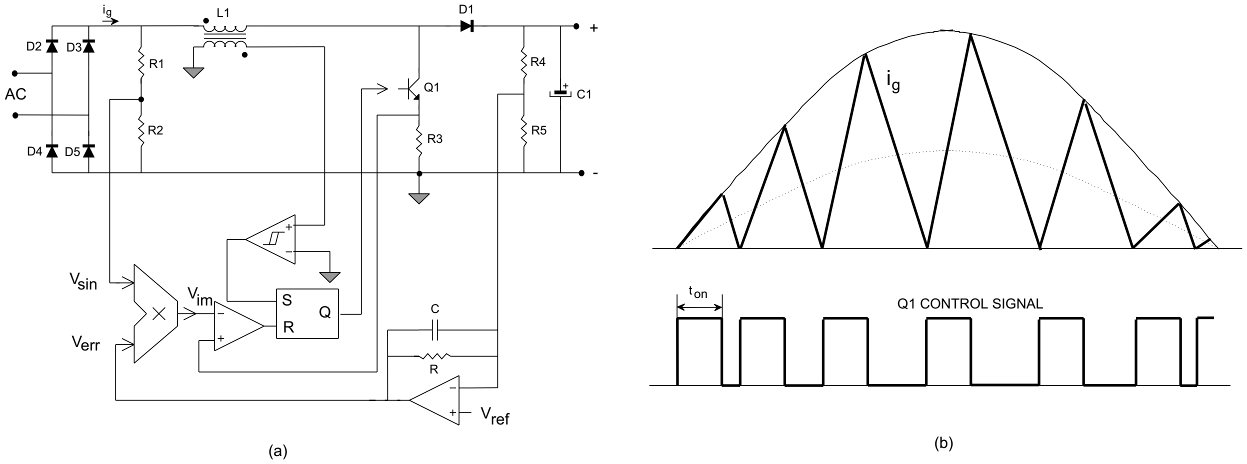


FIGURE 21.33 (a) Boost power factor corrector with borderline control; and (b) input current waveform.

suitable solution. Since the converter is supplied from a battery, the efficiency of the ballast should be as high as possible in order to optimize the use of the battery energy, thus increasing the operation time of the portable lighting. Typical topologies used are the class E inverter and the push–pull resonant inverter, providing efficiencies up to 95 .

21.6.2 Emergency Lighting

Emergency lighting is used to provide a minimum lighting level in case of a main supply cutoff. Batteries are employed to store energy from the mains and to supply the lamp in case of a main supply failure. A typical block diagram is shown in Fig. 21.34. An ac–dc converter is used as battery charger to store energy during normal line operation. A control circuit continuously measures the line voltage and activates the inverter in case of a main supply failure. Normally a minimum operating time of 1 hour is required for the system in emergency state; thus the use of high-efficiency electronic ballasts is mandatory to reduce battery size and cost. Typical topologies used include class E inverters, push–pull resonant inverters, and half-bridge resonant inverters. Fluorescent lamps are mainly used in emergency ballasts, but high-intensity discharge lamps, such as metal halide lamps or high-pressure sodium lamps, are also used in some special applications.

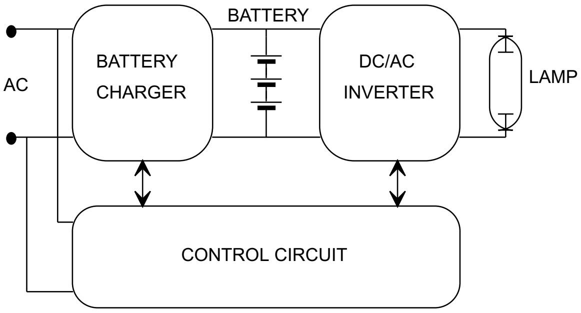


FIGURE 21.34 Block diagram of an emergency lighting system.

21.6.3 Automotive Lighting

Electronic ballasts are used in automotive applications such as automobiles, buses, trains, and aircraft. Normally a low-voltage dc bus is available to supply the lamps, and then these applications are similar to the portable and emergency lighting previously discussed. In modern aircraft a 120/208 V, 400 Hz, three-phase electrical system is also available and can be employed for lighting. Fluorescent lamps are typically used for automotive indoor lighting, whereas high-intensity discharge lamps are preferred in exterior lighting, for example, in automobile headlights.

21.6.4 ome and Industrial Lighting

Electronic ballasts, especially for fluorescent lamps, are also often used in home and industrial applications. The higher efficiency of fluorescent lamps supplied at high frequency provides significant energy savings when compared to incandescent lamps. A typical application is the use of compact fluorescent lamps with the electronic ballast inside the lamp base, which can directly substitute for an incandescent lamp, reducing the energy consumption by a factor of 4 or 5. A self-oscillating half-bridge inverter is typically used in these energy-saving lamps, since it allows reduced size and cost. The power of these lamps is normally below 25 W.

Other applications for higher power include more developed ballasts based on a power factor correction stage followed by a resonant inverter. Hot cathode fluorescent lamps are the most used in these electronic ballasts. Also, with the development of modern HID lamps such as metal halide lamps and very high pressure sodium lamps (both showing very good

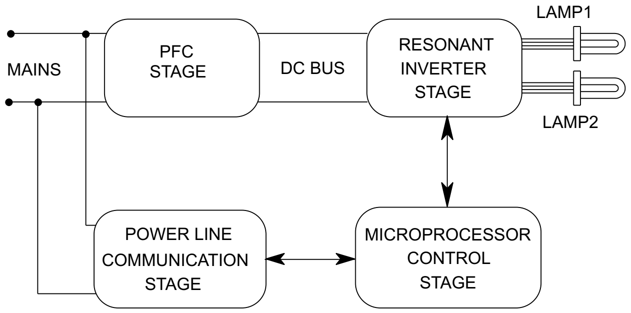


FIGURE 21.35 Block diagram of microprocessor-based lighting.

color rendition), the use of HID lamps is becoming more frequent in home, commercial, and industrial lighting.

21.6.5 Microprocessor-Based Lighting

The use of microprocessors in combination with electronic ballasts is very interesting from the point of view of energy savings [29–31]. The inclusion of microprocessor circuits allows incorporation of control strategies for dimming such as scheduling, task tuning, and daylighting [2]. Using these strategies, the energy savings achieved can be as great as 35–40 . Another advantage of using microprocessors is the possibility of detecting lamp failure or bad operation, thus increasing reliability and decreasing the maintenance cost of the installation. Most advanced electronic ballasts can include a communication stage to send and receive information regarding the state of the lighting to or from a central control unit. In some cases communications can be performed via power line, thus reducing installation costs. Figure 21.35 shows the block diagram of a microprocessor-based electronic ballast.

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22

Power Electronics in Capacitor Charging Applications

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22.1 Introduction

Conventional dc power supplies are designed to operate at a given output voltage into a constant or near-constant load. Pulse lasers, flashlamps, railguns, and other pulse power systems, however, require short but intense bursts of energy that may be derived from rapidly charging an energy storage capacitor. The rate at which the capacitor is discharged is called the repetition rate and may vary from 0.01 Hz for large capacitor banks to a few kilohertz for certain lasers. After the energy storage capacitor is discharged, it must be recharged to a specified voltage using a capacitor charging power supply (CCPS). The utilization of power electronics in capacitor charging applications is presented in this chapter.

Figure 22.1 shows the voltage across the energy storage capacitor connected to the output of a CCPS. As seen in this figure, the CCPS has three modes of operation. The first mode is the charging mode, in which the capacitor is charged from an initial voltage of zero to a specified final voltage. The duration of the charging mode is determined by the capacitance of the energy storage capacitor. The next mode of operation is the refresh mode, which can be considered a "standby mode." When the output voltage drops below a predetermined value, the CCPS should turn on and deliver the energy necessary to compensate for capacitor leakage. The duration of the refresh mode is determined by the load's repetition rate ($1/T$). The final mode of operation is the discharge mode, where the load is discharging the capacitor. The CCPS does not supply any energy to the load in this mode. The amount of time the CCPS remains in this mode is determined by how quickly the load can discharge the capacitor.

The instantaneous output power for a CCPS varies over a wide range in comparison to a conventional dc power supply, which supplies a constant or near-constant power to its load. This is shown in Fig. 22.2; the output power for the pulsed power load is drawn as linear for illustration purposes only. The charging mode is characterized by high peak power. At the beginning of this mode, the output power is zero (i.e., there is no voltage present but current is flowing). Thus, the load capacitor is equivalent to a short circuit. Additionally, at the end of the charging mode, the output power is again zero (i.e., there is an output voltage present but no current is flowing). Now the load capacitor is equivalent to an open circuit. The refresh mode is typically a low-power mode, because the current required to compensate for capacitor leakage is small. The CCPS does not supply any power during the discharge mode when the energy storage capacitor is being discharged by the pulsed load.

The average output power for a CCPS depends on the repetition rate of the load. It is a maximum when the energy storage capacitor is discharged at the end of the charging mode, which corresponds to operation without a refresh mode. Since the average output power is affected by the repetition rate of the load, the rating of a CCPS is often given in kJ/s instead of kW. The kJ/s rating indicates how fast a particular capacitor can be charged to a given voltage.

22.2 High-Voltage dc Power Supply with Charging Resistor

In this technique, the energy storage capacitor is charged by a high-voltage dc power supply through a charging resistor as

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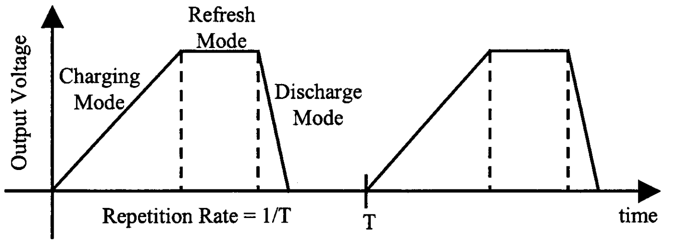

FIGURE 22.1 Three modes of operation of a capacitor charging power supply.

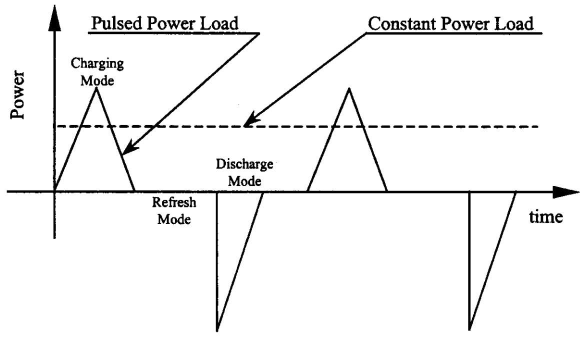

FIGURE 22.2 Power requirements for pulsed power and constant power loads.

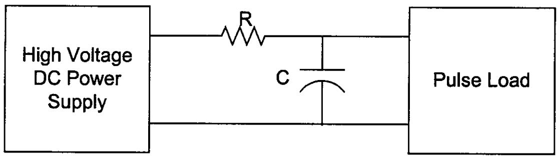

FIGURE 22.3 High-voltage dc power supply and charging resistor.

illustrated in Fig. 22.3. The charging mode ends when the capacitor voltage equals the output voltage of the power supply. The capacitor is continually refreshed by the power supply. During the discharge mode, the charging resistor isolates the power supply from the pulse load. The advantages of this technique are its simplicity, reliability, and low cost.

The major disadvantage of this technique is its poor efficiency. In the charging mode, the energy dissipated in the charging resistor is equal to the energy stored in the capacitor in the ideal case; therefore, the maximum efficiency is 50 . As a result, this technique is utilized only in applications where the charge rate is low, i.e., 200 J/s. Another disadvantage of this technique is related to the charge time, which is determined by the RC time constant. Some laser applications require that the output voltage be within 0.1 of a target voltage. For this technique, more than five time constants are required for the capacitor voltage to meet this voltage specification.

22.3 Resonance Charging

The basic resonance charging technique is illustrated in Fig. 22.4. An ac input voltage is stepped up with a transformer, rectified, and filtered with capacitor C_2 to produce a high dc voltage V_0. In this circuit, C_2 is much greater than C_1. Thyristor T_1 is gated and current flows through the inductor and diode D_1, transferring energy from C_2 to C_1. The voltage $v(t)$ and current $i(t)$ are described by the following equations assuming that $C_2 \gg C_1$. The charge time, t_c, for this circuit can be calculated by finding the time at which the current described by Eq. (22.2) reaches zero and is given below. The voltage $v(t)$ has a value of $2V_0$ at the end of the charging mode.

$$v(t) = V_0(1 - \cos\omega_0 t) \tag{22.1}$$

$$i(t) = V_0\sqrt{\frac{C_1}{L}}\sin\omega_0 t \tag{22.2}$$

$$\omega_0 = \frac{1}{\sqrt{LC_1}} \tag{22.3}$$

$$t_c = \pi\sqrt{LC_1} = \frac{\pi}{\omega_0} \tag{22.4}$$

Even though this technique is simple and efficient, it is not without its limitations. A high-voltage capacitor with a large capacitance value is needed for C_2, which increases the cost. A single thyristor is shown in Fig. 22.4. Multiple thyristors connected in series or a thyratron may be required, depending on the voltage level. The repetition rate of the pulse load should be such that C_1 is fully charged and $i(t)$ has reached zero before the load discharges to prevent latch-up of T_1. It is not possible for this circuit to operate in the refresh mode because of the switch characteristics. Therefore, $v(t)$ will drift as a result of capacitor leakage. The charge time is a function of the circuit parameters and will drift as they change with temperature or due to aging.

Since all of the energy stored in C_1 is transmitted from C_2 in a single pulse, it can be difficult to achieve a very small voltage regulation with the resonance charging technique. However, regulation can be improved with the addition of a dequeing circuit as shown in Fig. 22.5. The voltage $v(t)$ is monitored with a sensing network. Just before $v(t)$ reaches the desired level, thyristor T_2 is fired, which terminates the charging mode. The remaining energy stored in the inductor is dissipated in R. The addition of the dequeing circuit reduces circuit

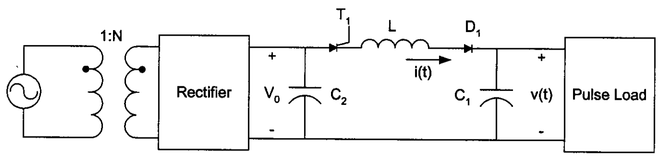

FIGURE 22.4 Resonance charging.

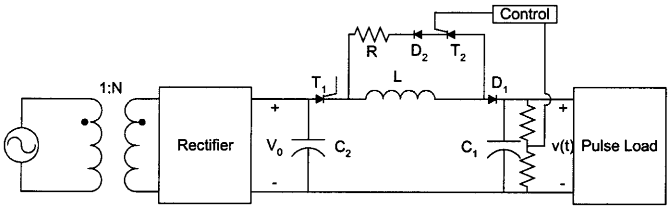

FIGURE 22.5 Resonance charging with dequeing.

efficiency and increases the circuit complexity and cost, but does not enable a refresh mode to compensate for capacitor leakage.

Boost charging, another variation on the resonance charging technique, is shown in Fig. 22.6 [1]. An extra switch is added to the circuit of Fig. 22.4 to improve the voltage gain. With switches S_1 and S_2 closed, the current $i(t)$ is given by

$$i(t) = \frac{V_0}{L} t \tag{22.5}$$

At some time $t = t_{\text{on}}$, S_2 is opened, and the current is now described by

$$i(t) = I_0 \cos \omega_0 t + V_0 \sqrt{\frac{C_1}{L}} \sin \omega_0 t \tag{22.6}$$

where

$$I_0 = \frac{V_0}{L} t_{\text{on}} \tag{22.7}$$

The voltage $v(t)$ is given by

$$v(t) = I_0 \sqrt{\frac{L}{C_1}} \sin \omega_0 t + V_0(1 - \cos \omega_0 t) \tag{22.8}$$

The time required for the current to reach zero and for the voltage $v(t)$ to reach its peak value can be calculated from

$$\tan(\omega_0 t_c) = -\frac{I_0 \sqrt{\frac{L}{C_1}}}{V_0} = -\omega_0 t_{\text{on}} \tag{22.9}$$

This is also the charge time, t_c, or the length of the charging mode. Note from Eq. (22.9) that the charge time depends on t_{on}, which is the on time of switch S_2. In addition, the peak capacitor voltage is a function of t_{on}. The peak capacitor voltage is limited to $2V_0$ without S_2; voltage gains as high as 20 are possible with the addition of S_2 [1].

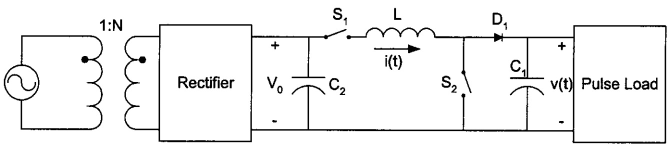

FIGURE 22.6 Boost charging.

The switching elements in Figs. 22.4 and 22.5 are realized with thyristors. Simple switches are shown for the boost charging technique in Fig. 22.6. Switch S_1 could be implemented with a thyristor. The boost capability provided by switch S_2 is best realized with a gate-controlled semiconductor device such as a GTO or an IGBT.

22.4 Switching Converters

The poor efficiency when charging a capacitor through a resistor from a high-voltage power supply limits its application to low charging rates. In the resonance charging concepts, the energy is transferred to the load capacitor in a single pulse, and it is not possible to compensate for capacitor leakage. Energy storage capacitors may be charged utilizing the same power electronic technology that has been applied in switching converters for constant power loads. Instead of charging the energy storage capacitor with a single pulse, switching converters can charge the capacitor with a series of pulses, or pulse train. The peak current is reduced when charging with a series of pulses, thus improving the efficiency of the charging process. In addition, soft-switching techniques may be employed in the switching converter to increase the efficiency. The regulation of the output voltage is also improved with the pulse train, because the energy is passed to the energy storage capacitor as small packets. Common control techniques such as pulse-width modulation can be used to control the size of the energy packet. This capability to control the size of the energy packet permits the CCPS to operate in the refresh mode and compensate for capacitor leakage. As a result, the CCPS may operate over a broad range of load repetition rates and still maintain the desired output voltage. During the refresh mode, energy lost as a result of capacitor leakage may be replaced in a burst fashion [2] or in a continuous fashion similar to trickle charging a battery [3]. In the switching converter, semiconductor switches may be operated on the low side of the transformer, permitting the use of MOSFETs or IGBTs in the CCPS. Since the CCPS begins the charging mode with a short circuit across its output, the switching converter must be capable of operating under this severe load condition. This may require the implementation of a current-limiting scheme in the converter control circuit.

One switching converter topology that may be employed in capacitor charging applications is the series resonant converter in Fig. 22.7. Note that the MOSFETs and resonant components L_r and C_r are connected on the low-voltage side of the transformer. Only the rectifier diodes and energy storage capacitor must have high voltage ratings. When the output rectifier is conducting, the energy storage capacitor C_1 is connected in series with the resonant capacitor C_r. For a

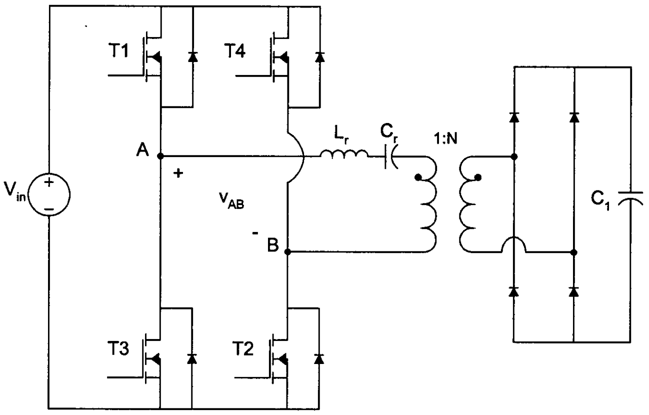

FIGURE 22.7 Series resonant converter.

transformer turns ratio of $1:N$, reflecting C_1 through the transformer yields a capacitance of N^2C_1. Since N is typically large, this reflected capacitance is much larger than C_r; thus, the resonant frequency, which is defined in Eq. (22.10), is not affected by C_1. For high-voltage, high-frequency operation, the leakage inductance of the transformer may be utilized as L_r

$$\omega_r = \frac{1}{\sqrt{L_r\left(\frac{NC_rC_1}{C_r+NC_1}\right)}} \tag{22.10}$$

One characteristic of this converter that makes it attractive for capacitor charging is the ability to operate under the short circuit conditions present at the beginning of the charging mode. The voltage across C_1 is zero at the beginning of this mode. The current flowing in the converter is limited by the input voltage and the impedance Z_0, which is defined in Eq. (22.11). The current may be limited to a safe maximum value; however, the charge time will be increased

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \tag{22.11}$$

Another method for current limiting is to vary the ratio of f_s, the switching frequency of the MOSFETs, and the resonant frequency, f_r, which is $\omega_r/2\pi$. This effectively controls the flow of energy from the source to C_1. The switching frequency may be held constant at some value such as $0.5f_r$. Alternatively, the ratio of f_s to f_r may be set to a low value at the beginning of the charging mode and increased toward 1 as the voltage across C_1 builds up. This limits the current when the voltage across C_1 is low and allows increased energy transfer as the voltage approaches the target voltage. The disadvantage of this approach is that all circuit components must be designed for variable-frequency operation.

The flyback converter [4, 5], shown in Fig. 22.8, also may be utilized for capacitor charging applications. When the MOSFET is turned on, current builds up in the primary winding, storing energy in the magnetic field. When it reaches a specified level, the MOSFET is turned off and energy is transferred from the magnetic field to C_1. This energy transfer is terminated when the MOSFET is turned on again.

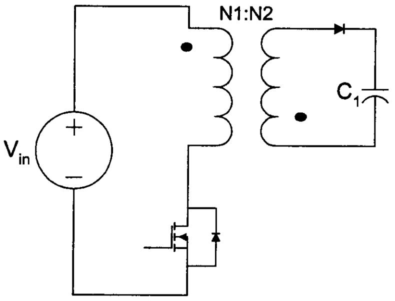

FIGURE 22.8 Flyback converter.

Sokal and Redl [4] have investigated different control schemes for charging capacitors using the flyback converter. Their recommendation is to charge C_1 with current pulses that are nearly flat-topped. This strategy results in higher average current for a given peak current. The capacitor is charged faster, because the charge delivered to it during a pulse is directly proportional to the average current. This desired pulse shape is achieved by turning on the MOSFET to terminate the transfer of energy to C_1 soon after the MOSFET is turned off. When the primary current reaches the desired level, the MOSFET is again turned off.

Another converter for capacitor charging applications is the Ward converter [6–8] shown in Fig. 22.9. When the MOSFET is on, energy is stored in the inductor and capacitor C_a transfers energy to the energy storage capacitor C_1 and capacitor C_b. The energy stored in the inductor is transferred to C_a when the MOSFET is off. The leakage inductance of the transformer and C_a resonate, producing a sinusoidal current that flows in the primary winding of the transformer and the MOSFET. When the primary current reaches zero and starts negative, the diode turns on, which allows the MOSFET to be turned off at zero current.

In some converter operating conditions, the voltage across C_a is very small because most of the energy has been transferred from C_a to C_1. The energy stored on C_a may be too small to ensure zero-current turn-off of the MOSFET. In this case, the energy stored on C_b helps to ensure that the

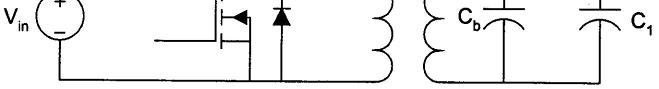

FIGURE 22.9 Ward converter.

amplitude of the current is large enough for zero-current turn-off of this device.

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23

Power Electronics for Renewable Energy Sources

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23.1 Introduction

The Kyoto agreement on global reduction of greenhouse gas emissions has prompted renewed interest in renewable energy systems worldwide. Many renewable energy technologies today are well developed, reliable, and cost competitive with the conventional fuel generators. The cost of renewable energy technologies is on a falling trend and is expected to fall further as demand and production increases. There are many renewable energy sources such as biomass, solar, wind, minihydro, and tidal power. However, solar and wind energy systems make use of advanced power electronics technologies and, therefore the focus in this chapter will be on solar photovoltaic and wind power.

One of the advantages offered by renewable energy sources is their potential to provide sustainable electricity in areas not served by the conventional power grid. The growing market for renewable energy technologies has resulted in a rapid growth in the need for power electronics. Most of the renewable energy technologies produce dc power, and hence power electronics and control equipment are required to convert the dc into ac power.

Inverters are used to convert dc to ac. There are two types of inverters: stand-alone and grid-connected. The two types have several similarities, but are different in terms of control functions. A stand-alone inverter is used in off-grid applications with battery storage. With backup diesel generators (such as PV–diesel hybrid power systems), the inverters may have additional control functions such as operating in parallel with diesel generators and bidirectional operation (battery charging and inverting). Grid-interactive inverters must follow the voltage and frequency characteristics of the utility-generated power presented on the distribution line. For both types of inverters, the conversion efficiency is a very important consideration. Details of stand-alone and grid-connected inverters for PV and wind applications are discussed in this chapter.

Section 23.2 covers stand-alone PV system applications such as battery charging and water pumping for remote areas. This section also discusses power electronic converters suitable for PV–diesel hybrid systems and grid-connected PV for rooftop and large-scale applications.

Among all the renewable energy options, wind-turbine technology is maturing very fast. A marked rise in installed wind power capacity has been noticed worldwide in the last decade. Per-unit generation cost of wind power is now quite comparable with conventional generation. Wind turbine generators are used in stand-alone battery charging applications, in combination with fossil fuel generators as a part of hybrid systems, and as grid-connected systems. As a result of advancements in blade design, generators, power electronics,

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and control systems, it has been possible to increase dramatically the availability of large-scale wind power. Many wind generators now incorporate speed control mechanisms such as blade pitch control or use converters/inverters to regulate power output from variable speed wind turbines. In Section 23.3, we discuss electrical and power conditioning aspects of wind energy conversion systems.

23.2 Power Electronics for Photovoltaic Power Systems

23.2.1 Basics of Photovoltaics

The density of power radiated from the sun (referred to as the "solar energy constant") at the outer atmosphere is 1.373 kW/m^2. Part of this energy is absorbed and scattered by the earth's atmosphere. The final incident sunlight on earth's surface has a peak density of 1 kW/m^2 at noon in the tropics. The technology of photovoltaics (PV) is essentially concerned with the conversion of this energy into usable electrical form. The basic element of a PV system is the solar cell. Solar cells can convert the energy of sunlight directly into electricity. Consumer appliances used to provide services such as lighting, water pumping, refrigeration, telecommunications, and television can be run from photovoltaic electricity. Solar cells rely on a quantum-mechanical process known as the "photovoltaic effect" to produce electricity. A typical solar cell consists of a $p-n$ junction formed in a semiconductor material similar to a diode. Figure 23.1 shows a schematic diagram of the cross section through a crystalline solar cell [1]. It consists of a 0.2–0.3 mm thick monocrystalline or polycrystalline silicon wafer having two layers with different electrical properties formed by "doping" it with other impurities (e.g., boron and phosphorus). An electric field is established at the junction between the negatively doped (using phosphorus atoms) and the positively doped (using boron atoms) silicon layers. If light is incident on the solar cell, the energy from the light (photons) creates free charge carriers, which are separated by the electrical field. An electrical voltage is generated at the external contacts, so that current can flow when a load is connected. The photocurrent (I_{ph}), which is internally generated in the solar cell, is proportional to the radiation intensity.

A simplified equivalent circuit of a solar cell consists of a current source in parallel with a diode as shown in Fig. 23.2a. A variable resistor is connected to the solar cell generator as a load. When the terminals are short-circuited, the output voltage and also the voltage across the diode are both zero. The entire photocurrent (I_{ph}) generated by the solar radiation then flows to the output. The solar cell current has its maximum (I_{sc}). If the load resistance is increased, which results in an increasing voltage across the $p-n$ junction of the diode, a portion of the current flows through the diode and the output current decreases by the same amount. When the load resistor is open-circuited, the output current is zero and the entire photocurrent flows through the diode. The relationship between current and voltage may be determined from the diode characteristic equation:

$$I = I_{\text{ph}} - I_0(e^{qV/kT} - l) = I_{\text{ph}} - I_{\text{d}} \tag{23.1}$$

where q is the electron charge, k is the Boltzmann constant, I_{ph} is photocurrent, I_0 is the reverse saturation current, I_d is diode current, and T is the solar cell operating temperature (K). The current versus voltage ($I-V$) of a solar cell is thus equivalent to an "inverted" diode characteristic curve shown in Fig. 23.2b.

A number of semiconductor materials are suitable for the manufacture of solar cells. The most common types using silicon semiconductor material (Si) are:

- Monocrystalline Si cells
- Polycrystalline Si cells
- Amorphous Si cells

A solar cell can be operated at any point along its characteristic current–voltage curve, as shown in Fig. 23.3. Two important points on this curve are the open circuit voltage (V_{oc}) and short-circuit current (I_{sc}). The open-circuit voltage is the maximum voltage at zero current, whereas the short-circuit current is the maximum current at zero voltage. For a silicon solar cell under standard test conditions, V_{oc} is typically 0.6–0.7 V, and I_{sc} is typically 20–40 mA for every square centimeter of the cell area. To a good approximation, I_{sc} is

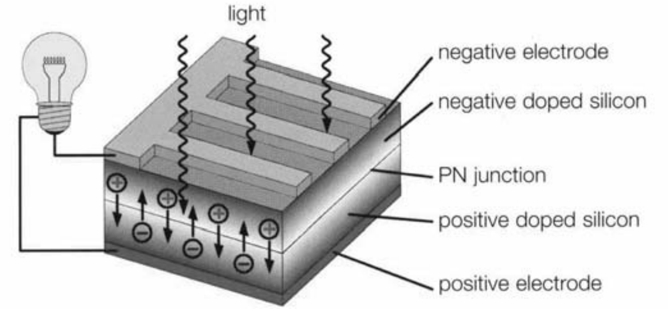


FIGURE 23.1 Principle of the operation of a solar cell [21].

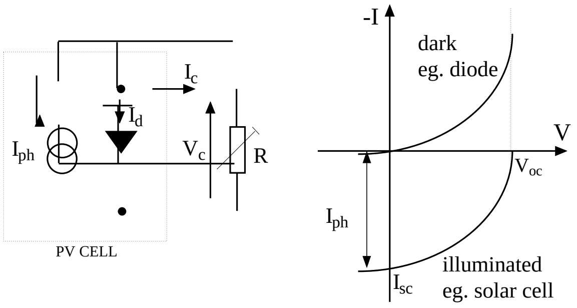


FIGURE 23.2 Simplified equivalent circuit for a solar cell.

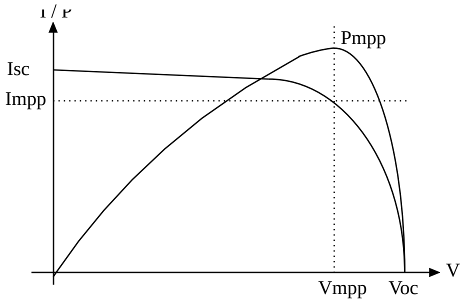


FIGURE 23.3 Current vs voltage ($I-V$) and current vs power ($I-P$) characteristics for a solar cell.

proportional to the illumination level, whereas V_{oc} is proportional to the logarithm of the illumination level.

A plot of power (P) against voltage (V) for this device (Fig. 23.3) shows that there is a unique point on the $I-V$ curve at which the solar cell will generate maximum power. This is known as the maximum power point (V_{mp}, I_{mp}). To maximize the power output, steps are usually taken during fabrication to maximize the three basic cell parameters: open-circuit voltage, short-circuit current, and fill factor (FF) a term describing how "square" the $I-V$ curve is, given by

$$\text{Fill factor} = (V_{mp} I_{mp})/(V_{OC} I_{Sc}) \tag{23.2}$$

For a silicon solar cell, FF is typically 0.6–0.8.

Because silicon solar cells typically produce only about 0.5 V, a number of cells are connected in series in a PV module. A panel is a collection of modules physically and electrically grouped together on a support structure. An array is a collection of panels (see Fig. 23.4).

The effect of temperature on the performance of a silicon solar module is illustrated in Fig. 23.5. Note that I_{sc} slightly increases linearly with temperature, but V_{oc} and the maximum power P_m decrease with temperature [1].

Figure 23.6 shows the variation of PV current and voltages at different insolation levels. From Figs. 23.5 and 23.6, it can be seen that the $I-V$ characteristics of solar cells at a given insolation and temperature consist of a constant-voltage segment and a constant-current segment [2]. The current is limited, as the cell is short-circuited. The maximum power condition occurs at the knee of the characteristic where the two segments meet.

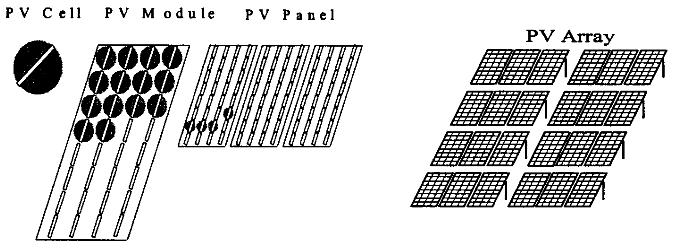


FIGURE 23.4 PV generator terms.

23.2.2 Types of PV Power Systems

Photovoltaic power systems can be classified as follows:

- Stand-alone
- Hybrid
- Grid connected

Stand-alone PV systems, shown in Fig. 23.7a, are used in remote areas with no access to a utility grid. Conventional power systems used in remote areas often based on manually controlled diesel generators operating continuously or for a few hours. Extended operation of diesel generators at low load levels significantly increases maintenance costs and reduces their useful life. Renewable energy sources such as PV can be added to remote area power systems using diesel and other fossil fuel powered generators to provide 24-hour power economically and efficiently. Such systems are called "hybrid energy systems." Figure 23.7b shows a schematic of a PV–diesel hybrid system. In grid-connected PV systems, as shown in Fig. 23.7c, PV panels are connected to a grid through inverters without battery storage. These systems can be classified as small systems, such as residential rooftop systems or large grid-connected systems. The grid interactive inverters must be synchronized with the grid in terms of voltage and frequency.

23.2.3 Stand-Alone PV Systems

The two main stand-alone PV applications are:

- Battery charging
- Solar water pumping

23.2.3.1 Battery Charging

. . . . ***Batteries or PV Systems*** A stand-alone photovoltaic energy system requires storage to meet the energy demand during periods of low solar irradiation and nighttime. Several types of batteries are available, such as lead-acid, nickel-cadmium, lithium, zinc bromide, zinc chloride, sodium–sulfur, nickel–hydrogen, redox and vanadium batteries. The provision of cost-effective electrical energy storage remains one of the major challenges for the development of improved PV power systems. Typically, lead-acid batteries are used to guarantee several hours to a few days of energy storage. Their reasonable cost and general availability has resulted in the widespread application of lead-acid batteries for remote area power supplies despite their limited lifetime compared to other system components. Lead acid batteries can be deep or shallow cycling, gelled batteries, batteries with captive or liquid electrolyte, sealed and nonsealed batteries, etc. [3]. Sealed batteries are valve regu-

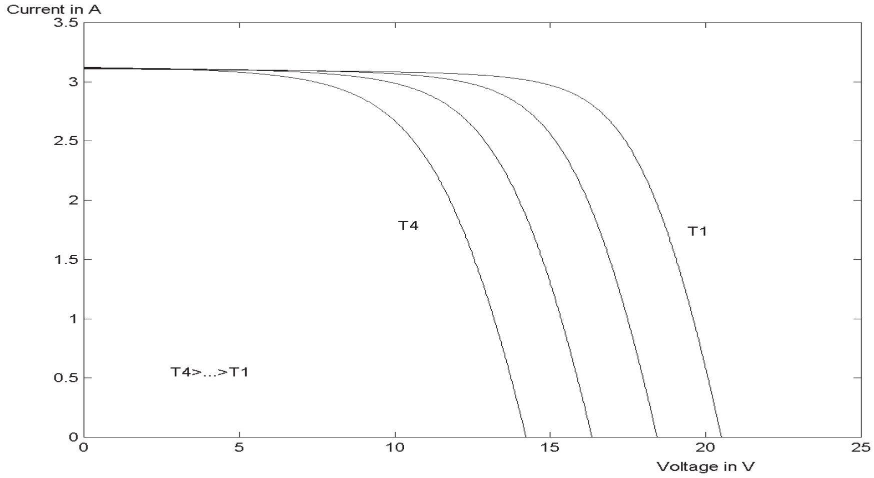


FIGURE 23.5 Effects of temperature on silicon solar cells.

lated to permit evolution of excess hydrogen gas (although catalytic converters are used to convert as much evolved hydrogen and oxygen back to water as possible). Sealed batteries need less maintenance.

The following factors are considered in the selection of batteries for PV applications [1]:

- Deep discharge (70–80 depth discharge)
- Low charging/discharging current
- Long-duration charge (slow) and discharge (long duty cycle)
- Irregular and varying charge/discharge
- Low self-discharge
- Long lifetime
- Less maintenance requirement
- High energy storage efficiency
- Low cost

Battery manufacturers specify the nominal number of complete charge and discharge cycles as a function of the depth-of-discharge (DOD), as shown in Fig. 23.8. Although this information can be used reliably to predict the lifetime of lead-acid batteries in conventional applications, such as uninterruptable power supplies or electric vehicles, it usually results in an overestimation of the useful life of the battery bank in renewable energy systems.

Two of the main factors that have been identified as limiting criteria for the cycle life of batteries in photovoltaic power systems are incomplete charging and prolonged operation at a low state-of-charge (SOC). The objective of improved battery control strategies is to extend the lifetime of lead-acid batteries to achieve the typical number of cycles shown in Fig. 23.8. If this is achieved, an optimum solution for the required storage capacity and the maximum depth-of-discharge of the battery can be found by referring to the manufacturer's information. Increasing the capacity will reduce the typical depth-of-discharge and therefore prolong the battery lifetime. Conversely, it may be more economic to replace a smaller battery bank more frequently.

. . . . ***PV Charge Controllers*** Blocking diodes in series with PV modules are used to prevent the batteries from being

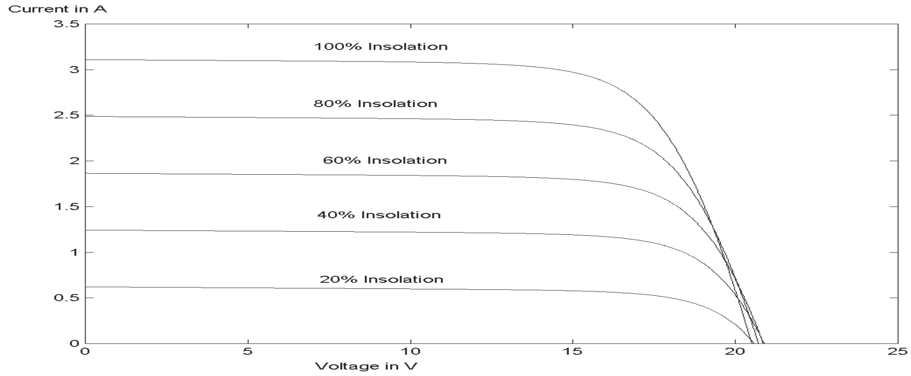


FIGURE 23.6 Typical current/voltage ($I-V$) characteristic curves for different insolation levels.

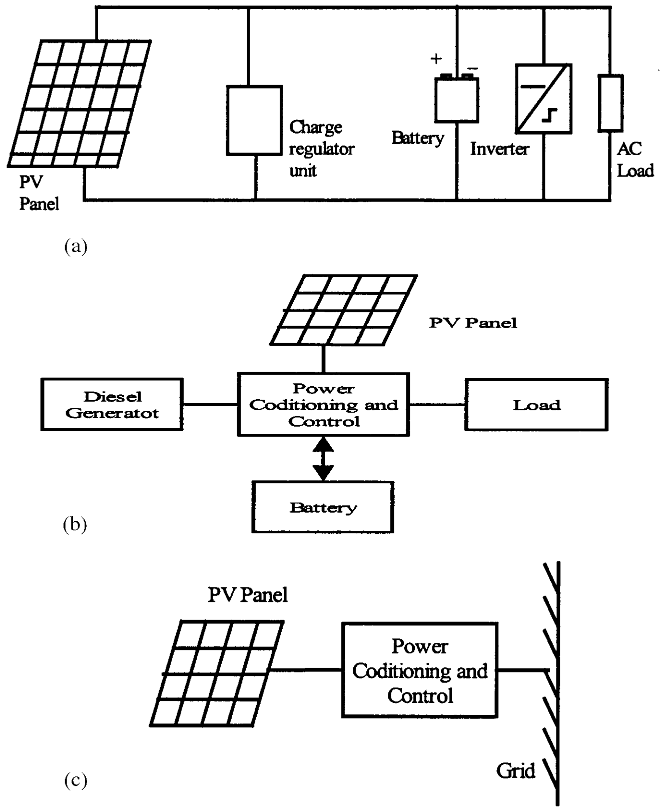

PV
Panel
Charge
regulator
unit
+
−
Battery
Inverter
AC
Load
(a)
PV Panel
Diesel
Generatot
Power
Coditioning and
Control
Load
Battery
(b)
PV Panel
Power
Coditioning and
Control
Grid
(c)

FIGURE 23.7 (a) Stand-alone PV system; (b) PV–diesel hybrid system; (c) grid-connected PV system.

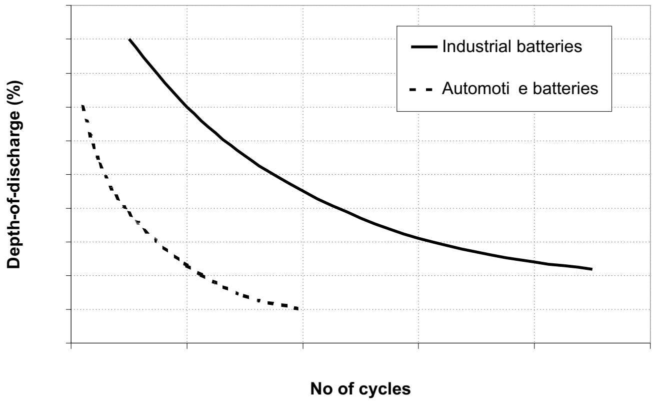


FIGURE 23.8 Nominal number of battery cycles vs depth-of-discharge.

discharged through the PV cells at night when there is no sun available to generate energy. These blocking diodes also protect the battery from short circuits. In a solar power system consisting of more than one string connected in parallel, if a short-circuit occurs in one of the strings, the blocking diode prevents the other PV strings from discharging through the short-circuited string.

The battery storage in a PV system should be properly controlled to avoid catastrophic operating conditions like overcharging or frequent deep discharging. Storage batteries account for most PV system failures and contribute significantly to both the initial and the eventual replacement costs. Charge controllers regulate the charge transfer and prevent the battery from being excessively charged and discharged. Three types of charge controllers are commonly used:

- Series charge regulators
- Shunt charge regulators
- Dc–dc Converters

23.2.3.1.2.1 Series Charge Regulators The basic circuit for the series regulators is given in Fig. 23.9. In the series charge controller, the switch S_1 disconnects the PV generator when a predefined battery voltage is achieved. When the voltage falls below the discharge limit, the load is disconnected from the battery to avoid deep discharge beyond the limit. The main problem associated with this type of controller is the losses associated with the switches. This extra power loss has to come from the PV power, and this can be quite significant. Bipolar transistors, MOSFETs, or relays are used as the switches.

23.2.3.1.2 Shunt Charge Regulators In this type, as illustrated in Fig. 23.10, when the battery is fully charged the PV generator is short-circuited using an electronic switch (S_1). Unlike series controllers, this method works more efficiently

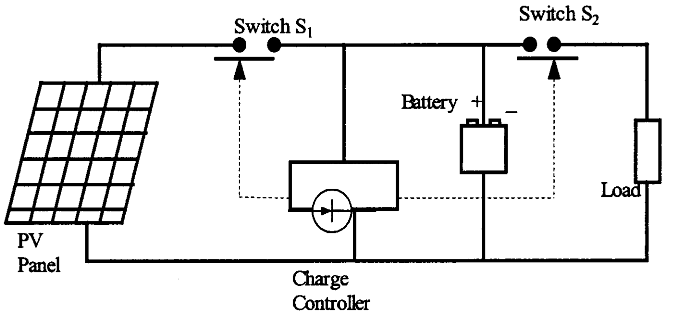

Switch S_1
Switch S_2
Battery +
−
Load
PV
Panel
Charge
Controller

FIGURE 23.9 Series charge regulator.

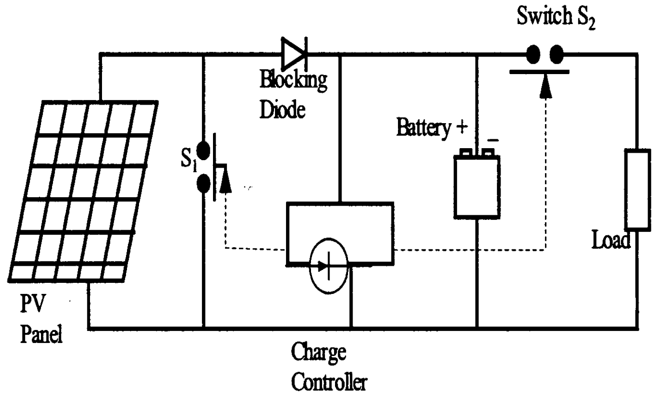

Switch S_2
Blocking
Diode
S_1
Battery +
−
Load
PV
Panel
Charge
Controller

FIGURE 23.10 Shunt charge regulator.

even when the battery is completely discharged, as the short-circuit switch need not be activated until the battery is fully discharged [1].

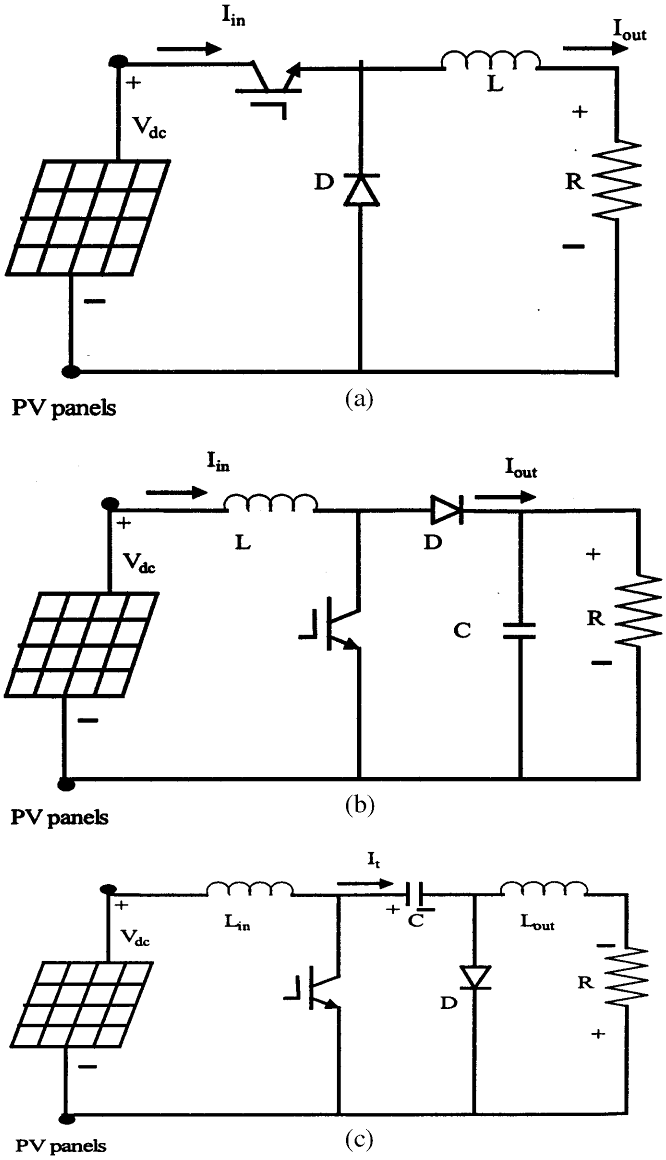
The blocking diode prevents short-circuiting of the battery. Shunt charge regulators are used for small PV applications (less than 20 A).

Deep-discharge protection is used to protect the battery against deep discharge. When the battery voltage reaches below the minimum set point for the deep-discharge limit, switch S_2 disconnects the load. Simple series and shunt regulators allow only relatively coarse adjustment of the current flow and seldom meet the exact requirements of PV systems.

23.2.3.1.2.3 Dc–dc Converter Type Charge Regulators Switch mode dc-to-dc converters are used to match the output of a PV generator to a variable load. There are various types of dc–dc converters:

- Buck (step-down) converter
- Boost (step-up) converter
- Buck-boost (step-down/up) converter

Figures 23.11a, 23.11b, and 23.11c show simplified diagrams of these three basic types of converters. The basic concepts are an electronic switch, an inductor to store energy, and a "flywheel" diode, which carries the current during that part of switching cycle when the switch is off. The dc–dc converters allow the charge current to be reduced continuously in such a way that the resulting battery voltage is maintained at a specified value.



(a)

(b)

(c)

FIGURE 23.11 (a) Buck converter; (b) boost converter; (c) Buck-boost converter.

. . . . ***Maximum-Power-Point-Tracking (MPPT)*** A controller that tracks the maximum-power-point locus of the PV array is known as an MPPT. In Fig. 23.12, the PV power output is plotted against the voltage for insolation levels from 200 W/m^2 to 1000 W/m^2. The points of maximum array power form a curve termed as the maximum power locus. Because of the high cost of solar cells, it is necessary to operate the PV array at its maximum power point. For overall optimal operation of the system, the load line must match the PV array's maximum-power-point locus.

Referring to Fig. 23.13, the load characteristics can be either curve OA or curve OB, depending on the nature of the load and its current and voltage requirements. If load OA is considered and the load is directly coupled to the solar array, the array will operate at point A1, delivering only power P1. The maximum array power available at the given insolation is P2. In order to use PV array power P2, a power conditioner coupled between the array and the load is needed.

There are two ways of operating PV modules at the maximum power point:

(a) *Open-loop control.* The open-loop method is based on the assumption that the maximum-power-point voltage V_{MPP} is a linear function of the open-circuit voltage V_{OC}. For example, $V_{MPP} = k\ V_{OC}$, where $k \approx 0.76$. This assumption is reasonably accurate even for large variations in the cell short-circuit current and temperature. This type of MPPT is probably the most common type. A variation to this method involves periodically open-circuiting the cell string and measuring the open-circuit voltage. The appropriate value of V_{MPP} can then be obtained with a simple voltage divider.

(b) *Closed-loop control.* The closed-loop control involves varying the input voltage around the optimum value by giving it a small increment or decrement alternately. The effect on the output power is then assessed and a further small correction is made to the input voltage. This type of control is called a hill-climbing control. The power output of the PV array is sampled

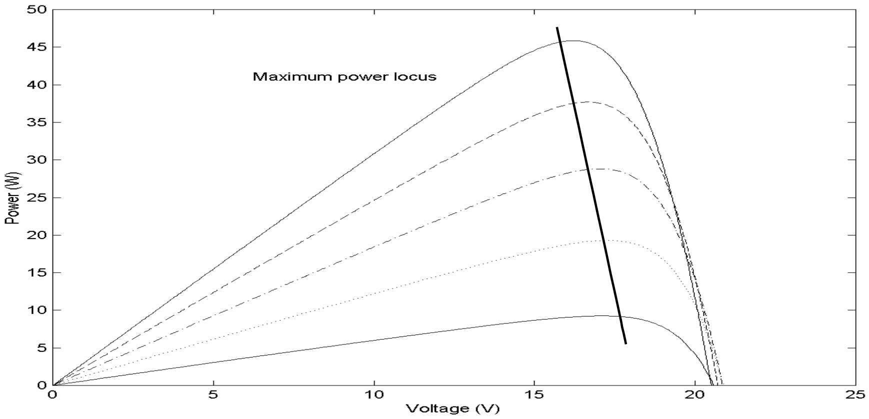


FIGURE 23.12 Typical power/voltage characteristics for increased insolation.

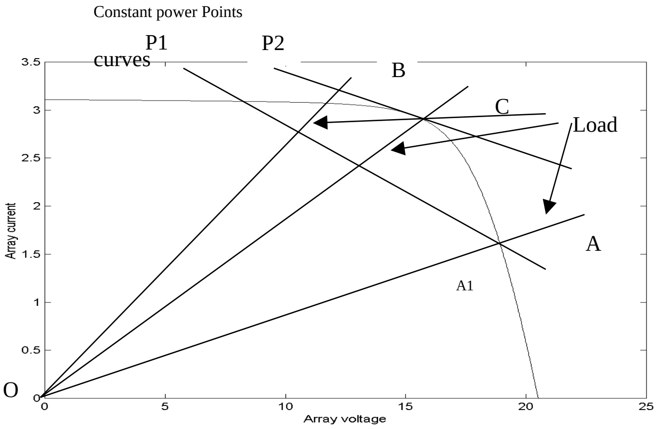


FIGURE 23.13 PV array and load characteristics.

at an every definite sampling period and compared with the previous value. In the event, when power is increased, the solar array voltage is stepped in the same direction as the previous sample time, but if the power is reduced, the array voltage is stepped in the opposite way, in order to try to operate the PV array at its optimum/maximum power point.

To operate the PV array at the maximum power point, perturb and adjust methods can be used in which the current drawn is sampled every few seconds and the resulting power output of the solar cells is monitored at regular intervals. When an increased current results in a higher power, it is further increased until the power output starts to decrease. But if the increased PV current results in a lesser amount of power than in the previous sample, then the current is reduced until the maximum power point is reached.

23.2.3.2 Inverters for Stand-Alone PV Systems

Inverters convert power from dc to ac, while rectifiers convert it from ac to dc. Many inverters are bi-directional, i.e., they are able to operate in both inverting and rectifying modes. In many stand-alone photovoltaic installations, alternating current is needed to operate 230 V (or 110 V), 50 Hz (or 60 Hz) appliances. Generally stand-alone inverters operate at 12, 24, 48, 96, 120, or 240 V dc, depending on the power level.

Ideally, an inverter for a stand-alone photovoltaic system should have the following features:

- Sinusoidal output voltage
- Voltage and frequency within the allowable limits
- Cable to handle large variation in input voltage
- Output voltage regulation
- High efficiency at light loads
- Less harmonic generation by the inverter to avoid damage to electronic appliances such as televisions, additional losses, and heating of appliances
- Ability to withstand overloading for a short term to take care of higher starting currents from pumps, refrigerators, etc.
- Adequate protection arrangement for over/undervoltage and frequency, short-circuit, etc.
- Surge capacity
- Low idling and no load losses
- Low battery voltage disconnect
- Low audio and RF noise

Several different semiconductor devices, such as MOSFETs (metal oxide semiconductor field-effect transistors) and IGBTs (insulated-gate bipolar transistors) are used in the power stage of inverters. Typically MOSFETs are used in units up to 5 kVA and 96 V dc. They have the advantage of low switching losses at higher frequencies. Because the on state voltage drop is 2 V dc, IGBTs are generally used only in systems above 96 V dc.

Voltage source inverters are usually used in stand-alone applications. They can be single-phase or three-phase. There are three switching techniques commonly used: square wave, quasi-square-wave, and pulse-width modulation. Square-wave or modified square-wave inverters can supply power tools, resistive heaters, or incandescent lights, which do not require a

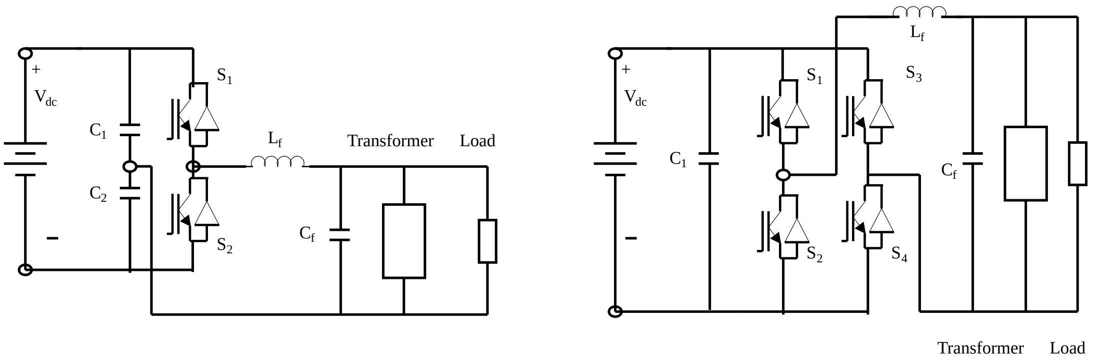


FIGURE 23.14 Single-phase inverter. (a) Half bridge; (b) full bridge.

high-quality sine wave for reliable and efficient operation. However, many household appliances require low-distortion sinusoidal waveforms. The use of true sine-wave inverters is recommended for remote area power systems. Pulse-width modulated (PWM) switching is generally used for obtaining sinusoidal output from the inverters.

A general layout of a single-phase system, both half-bridge and full bridge, is shown in Fig 23.14. In single-phase half bridge (Fig. 23.14a) with two switches, S_1 and S_2, the capacitors C_1 and C_2 are connected in series across the dc source. The junction between the capacitors is at the mid-potential. Voltage across each capacitor is $V_{dc}/2$. Switches S_1 and S_2 can be switched on/off periodically to produce ac voltage. A filter (L_f and C_f) is used to reduce high-switch-frequency components and to produce sinusoidal output from the inverter. The output of the inverter is connected to the load through a transformer. Figure 23.14b shows the similar arrangement for a full-bridge configuration with four switches. For the same input source voltage, the full-bridge output is twice as high, and the switches carry less current for the same load power.

The power circuit of a three phase, four-wire inverter is shown in Fig. 23.15. The output of the inverter is connected to load via a three-phase transformer (delta/star). The star point of the transformer secondary gives the neutral connection. Three-phase or single-phase can be connected to this system. Alternatively, a center-tap dc source can be used to supply the converter and the midpoint can be used as the neutral.

Figure 23.16 shows the inverter efficiency for a typical inverter used in remote-area power systems. It is important to consider that the system load is typically well below the nominal inverter capacity P_{nom}, which results in low conversion efficiencies at loads below 10 of the rated inverter output power. Optimum overall system operation is achieved if the total energy dissipated in the inverter is minimized. The high conversion efficiency at low power levels of recently developed inverters for grid-connected PV systems shows that there is a significant potential for further improvements in efficiency.

Bidirectional inverters convert dc power to ac power (inverter) or AC power to DC power (rectifying) and are becoming very popular in remote area power systems [4, 5]. The principle of a stand-alone single-phase bi-directional inverter used in a PV/Battery/Diesel hybrid system can be explained with reference to Fig. 23.17. A charge controller is used to interface the PV array and the battery. The inverter has a full-bridge configuration realized using four power electro-

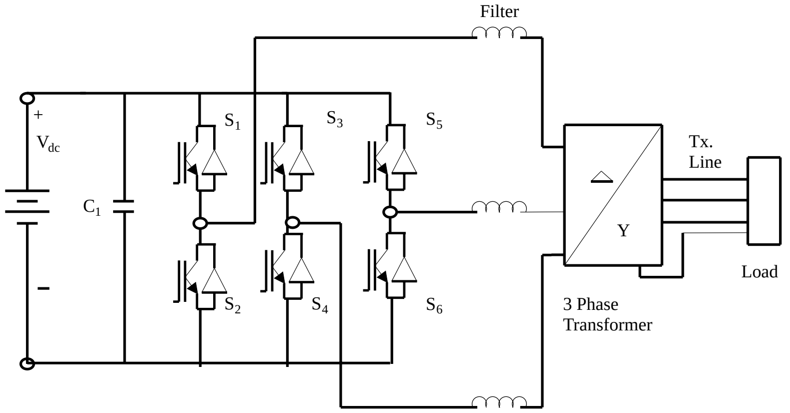


FIGURE 23.15. Stand-alone three-phase four-wire inverter.

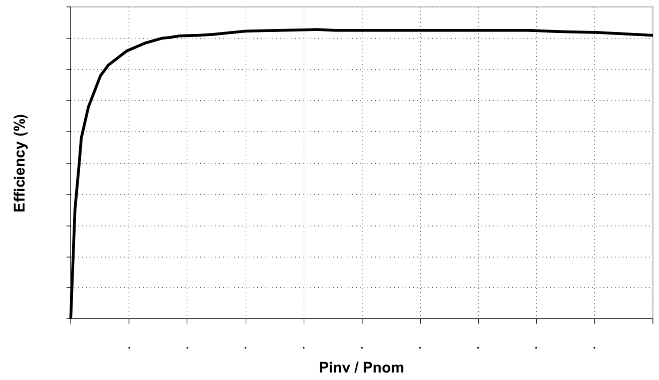


FIGURE 23.16 Typical inverter efficiency curve.

nic switches (MOSFET or IGBTs) S_1–S_4. In this scheme, the diagonally opposite switches (S_1, S_4) and (S_2, S_3) are switched using sinusoidally pulse-width modulated gate pulses. The inverter produces sinusoidal output voltage. The inductors X_1, X_2 and the ac output capacitor C_2 filter out the high-switch-frequency components from the output waveform. Most inverter topologies use a low-frequency (50 or 60 Hz) transformer to step up the inverter output voltage. In this scheme, the diesel generator and the converter are connected in parallel to supply the load. The voltage sources, diesel and inverter, are separated by the link inductor X_m. The bidirectional power flow between inverter and the diesel generator can be established. The power flow through the link inductor, X_m, is

$$S_m = V_m I_m \tag{23.3}$$

$$P_m = (V_m V_c \sin \delta)/X_m \tag{23.4}$$

$$Q_m = (V_m/X_m)(V_m - V_c \cos \delta) \tag{23.5}$$

$$\delta = \sin^{-1}[(X_m P_m)/(V_m V_c)] \tag{23.6}$$

where δ is the phase angle between the two voltages. From Eq. (4), it can be seen that the power supplied by the inverter from the batteries (inverter mode) or supplied to the batteries (charging mode) can be controlled by controlling the phase angle δ. The PWM pulses separately control the amplitude of the converter voltage, V_c, while the phase angle with respect to the diesel voltage is varied for power flow.

23.2.3.3 Solar Water Pumping

In many remote and rural areas, hand pumps or diesel driven pumps are used for water supply. Diesel pumps consume fossil fuel, affect the environment, need more maintenance, and are less reliable. Photovoltaic (PV)-powered water pumps have received considerable attention because of major developments in the field of solar-cell materials and power electronic systems technology.

. . . . Types of Pumps Two types of pumps are commonly used for water-pumping applications: Positive displacement and centrifugal. Both centrifugal and positive-displacement pumps can be further classified into those with motors that are surface mounted, and those that are submerged into the water (“submersible”).

Displacement pumps have water output directly proportional to the speed of the pump, but almost independent of head. These pumps are used for solar water pumping from deep wells or bores. They may be piston-type pumps or use a diaphragm driven by a cam or rotary screw, or use a progressive cavity system. The pumping rate of these pumps is directly related to the speed, and hence constant torque is desired.

Centrifugal pumps are used for low-head applications, especially if they are directly interfaced with the solar panels. Centrifugal pumps are designed for fixed-head applications, and the pressure difference generated increases in relation to the speed of the pump. These pumps are of the rotating-impeller type, which throws the water radially against a casing shaped so that the momentum of the water is converted into useful pressure for lifting [3]. The centrifugal pumps have relatively high efficiency, but it decreases at lower speeds, which can be a problem for a solar water-pumping system

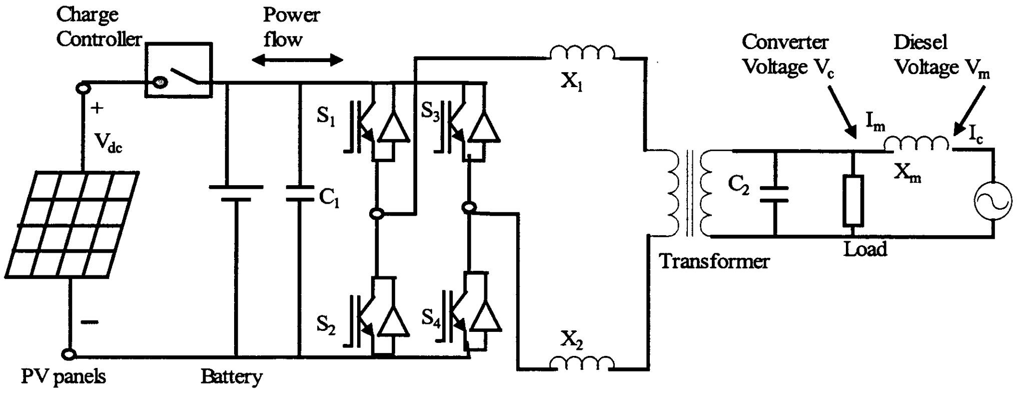


FIGURE 23.17 Bidirectional inverter system.

at times of low light levels. The single-stage centrifugal pump has just one impeller, whereas most borehole pumps are multistage types where the outlet from one impeller goes into the center of another and each one keeps increasing the pressure difference.

From Fig. 23.18a, it is quite obvious that the load line is located far away from the P_{max} line. It has been reported that the daily utilization efficiency for a dc motor drive is 87% for a centrifugal pump compared to 57% for a constant-torque characteristic load. Hence, centrifugal pumps are more compatible with PV arrays. The system operating point is determined by the intersection of the $I-V$ characteristic of the PV array and that of the motor, as shown in Fig. 23.18a. The torque-speed slope is normally large because of the armature resistance being small. At the instant of starting, the speed and the back emf are zero. Hence the motor starting current is approximately the short-circuit current of the PV array. Matching the load to the PV source through a maximum-power-point tracker increases the starting torque.

The matching of a dc motor depends on the type of load being used. For instance, a centrifugal pump is characterized by having the load torque proportional to the square of speed. The operating characteristics of the system (i.e., PV source, PM dc motor, and load) are at the intersection of the motor and load characteristics as shown in Fig. 23.18b (i.e., points *a*, *b*, *c*, *d*, *e*, and *f* for the centrifugal pump). From Fig. 23.18b, the system utilizing the centrifugal pump as its load tends to start at low solar irradiation (point *a*) level. However, for systems with an almost constant torque characteristic (Fig. 23.18b, line 1), the start is at almost 50% of one sun (full insolation), which results in a short period of operation.

. . . . Types of Motors There are various types of motors available for the PV water pumping applications: dc motors and ac motors. Dc motors are preferred where direct coupling to photovoltaic panels is desired, whereas ac motors are coupled to the solar panels through inverters. Ac motors in general are cheaper than dc motors and are more reliable, but

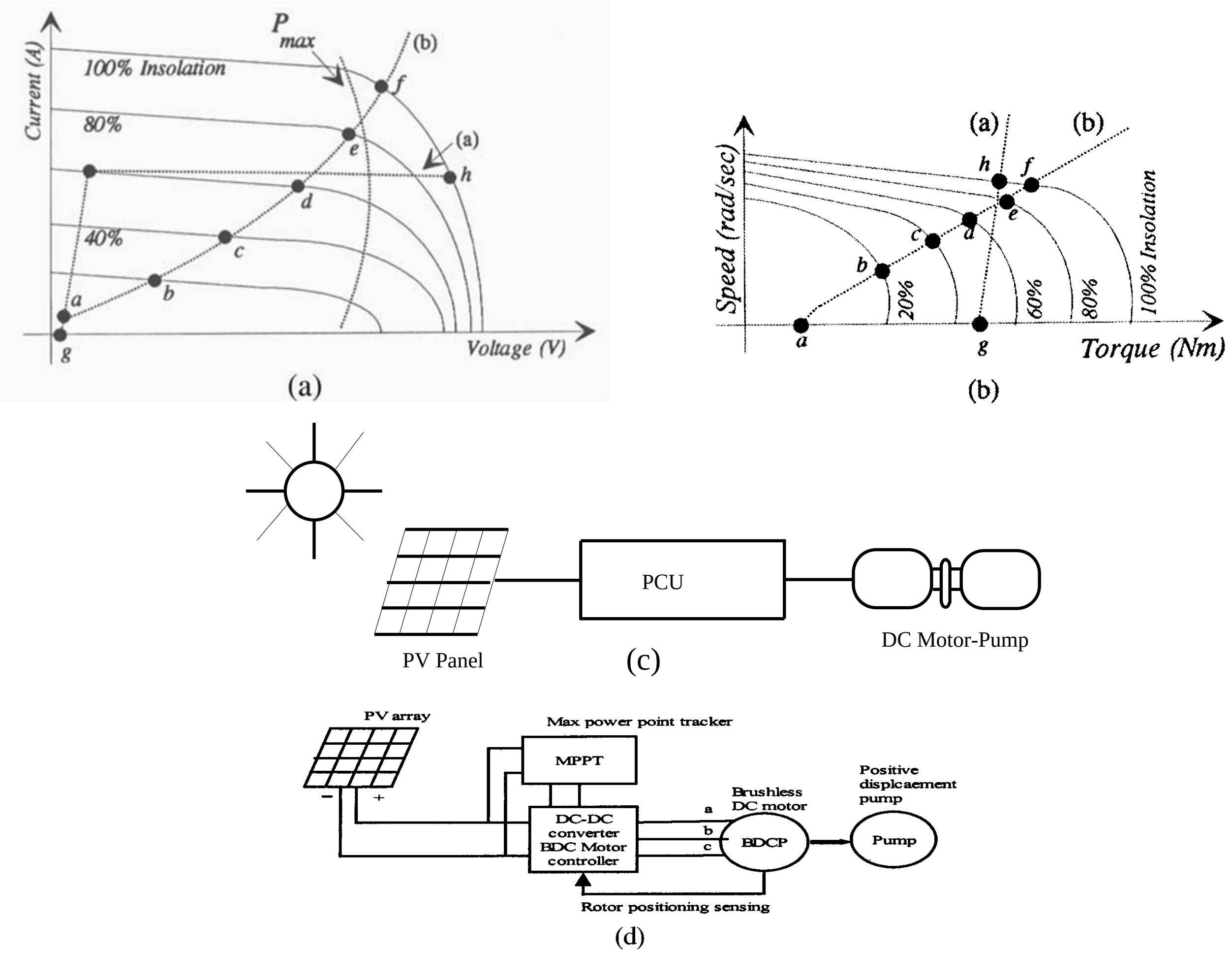

Current (A)
P max
(b)
100% Insolation
f
80%
e
(a)
h
d
40%
c
b
a
g
Voltage (V)
(a)
(a)
(b)
Speed (rad/sec)
h
f
e
c
d
b
20%
60%
80%
100% Insolation
a
g
Torque (Nm)
(b)
PCU
PV Panel
(c)
DC Motor-Pump
PV array
Max power point tracker
MPPT
−
+
DC-DC converter BDC Motor controller
a
b
c
Brushless DC motor
BDCP
Positive displcaement pump
Pump
Rotor positioning sensing
(d)

FIGURE 23.18 (a): $I-V$ characteristics of a PV array and two mechanical loads: (1) constant torque and (2) centrifugal pump. (b) Speed torque characteristics of a dc motor and two mechanical loads: (1) helical rotor, (2) centrifugal pump. (c) Block diagram for dc motor-driven pumping scheme. (d): Block diagram for brushless dc motor for PV application.

dc motors are more efficient. The dc motors used for solar pumping applications are permanent-magnet dc motors with or without brushes.

In dc motors with brushes, the brushes are used to deliver power to the commutator and need frequent replacement because of wear and tear. These motors are not suitable for submersible applications unless long transmission shafts are used. Brushless dc permanent-magnet motors have been developed for submersible applications.

The ac motors are of the induction motor type, which is cheaper than dc motors and available worldwide. However, they need inverters to change dc input from the PV to ac power. A comparison of the different types of motors used for PV water pumping is given in Table 23.1.

. . . . Power Conditioning Units for PV Water Pumping Most PV pump manufacturers include power conditioning units (PCUs), which are used for operating the PV panels close to their maximum power point over a range of load conditions and varying insolation levels, and also for power conversion. Dc or ac motor pump units can be used for PV water pumping. In its simplest from, a solar water pumping system comprises of PV array, PCU and DC water pump unit as shown in Figure 23.18(c).

In case of lower light levels, high currents can be generated through power conditioning to help in starting the motor-pump units, especially for reciprocating positive-displacement type pumps with constant torque characteristics requiring constant current throughout the operating region. In positive-displacement type pumps, the torque generated by the pumps depends on the pumping head, friction, pipe diameter, etc., and requires a certain level of current to produce the necessary torque. Some systems use electronic controllers to assist in starting and operating the motor under low solar radiation. This is particularly important when using positive-displacement pumps. The solar panels generate dc voltage and current. Solar water pumping systems usually have dc or ac pumps. For dc pumps, the PV output can be directly connected to the pump through maximum power point tracker, or a dc–dc converter can also be used for interfacing for controlled dc output from PV panels. To feed the ac motors, a suitable interface is required for the power conditioning. These PV inverters for the stand-alone applications are very expensive. The aim of power conditioning equipment is to supply the controlled voltage/current output from the converters/inverters to the motor-pump unit.

These power-conditioning units are also used for operating the PV panels close to their maximum efficiency for fluctuating solar conditions. The speed of the pump is governed by the available driving voltage. Current lower than the acceptable limit will stop the pumping. When the light level increases, the operating point will shift from the maximum-power point,

TABLE 23.1 Comparison of the different types of motors used for PV water pumping

Types of Motor	Advantages	Disadvantages	Main Features
Brushed dc	• Simple and efficient for PV applications	• Brushes need to be replaced periodically (typical replacement interval is 2000 to 4000 h or 2 years)	• Requires maximum power point tracker for optimum performance
	• No complex control circuit is required, as the motor starts without high current surge; these motors will run slowly but do not overheat with reduced voltage	• Available only in small motor sizes	• Available only in small motor sizes
			• Increasing current (by paralleling PV modules) increases the torque; increasing voltage (by series PV modules) increases the speed
Brushless dc	• Efficient • Less maintenance is required	• Electronic computation adds to extra cost, complexity, and increased risk of failure/malfunction	• Growing trend among PV pump manufacturers to use brushless dc motors, primarily for centrifugal-type submersible pumps
		• In most cases, oil cooled, cannot be submerged as deeply as water-cooled ac units	
Ac induction motors	• No brushes to replace • Can use existing ac motor/pump technology, which is cheaper and easily available worldwide; these motors can handle larger pumping requirements	• Needs an inverter to convert DC output from PV to AC, adding cost and complexity • Less efficient than dc motor-pump units • Prone to overheating if current is not adequate to start the motor or if the voltage is too low	• Available for single or three supply • Inverters are designed to regulate frequency to maximize power to the motor in response to changing insolation levels

leading to a reduction in efficiency. For centrifugal pumps, there is an increase in current at increased speed, and the matching of $I-V$ characteristics is closer for a wide range of light intensity levels. For centrifugal pumps, the torque is proportional to the square of the speed, and the torque produced by the motors is proportional to the current. Because of the decrease in PV current output, the torque from the motor and consequently the speed of the pump are reduced, resulting in a decrease in back emf and the required voltage for the motor. A maximum-power-point tracker (MPPT) can be used for controlling the voltage/current outputs from the PV inverters to operate the PV close to the maximum operating point for smooth operation of motor-pump units. The dc–dc converter can be used to keep the PV-panel output voltage constant and to help in operating the solar arrays close to the maximum-power point. In the beginning, a high starting current is required to produce a high starting torque. The PV panels cannot supply this high starting current without adequate power conditioning equipment such as a dc–dc converter or by using a starting capacitor. The dc–dc converter can generate the high starting currents by regulating the excess PV array voltage. The dc–dc converter can be a boost or buck converter.

Brushless dc motors (BDCM) and helical rotor pumps can also be used for PV water pumping [20]. BDCMs are a self-synchronous type of motor characterized by trapezoidal waveforms for back emf and air flux density. They can operate off a low-voltage dc supply that is switched through an inverter to create a rotating stator field. The current generation of BDCMs use rare earth magnets on the rotor to give high air-gap flux densities and are well suited to solar application. The block diagram of such an arrangement, shown in Fig. 23.18d, consists of PV panels, a dc–dc converter, an MPPT, and a brushless dc motor.

The PV inverters are used to convert the dc output of the solar arrays to an ac quantity so as to run the ac motor-driven pumps. These PV inverters can be of the variable-frequency type, which can be controlled to operate the motors over a wide range of loads. The PV inverters may involve impedance matching to match the electrical characteristics of the load and array. The motor–pump unit and PV panels operate at their maximum efficiencies [7]. The MPPT is also used in the power conditioning. To keep the voltage stable for the inverters, the dc–dc converter can be used. The inverter/converter has the capability of injecting high-switch-frequency components, which can lead to overheating and losses, care must be taken in doing this. The PV arrays are usually connected in series, parallel, or a combination of series and parallel configurations. The function of power electronic interface, as mentioned before, is to convert the dc power from the array to the required voltage and frequency to drive the ac motors. The motor–pump system load should be such that the array operates close to its maximum power point at all solar insolation levels. There are mainly three types solar powered water pumping systems, as shown in Fig. 23.19.

The first system shown in Fig 23.19a is an imported commercially available unit, which uses a specially wound low-voltage induction-motor-driven submersible pump. Such a low-voltage motor permits the PV array voltage to be converted to ac without using a step-up transformer. The second system, shown in Fig. 23.19b, makes use of a conventional "off-the-shelf" 415-V, 50-Hz, induction motor [6]. This scheme needs a step-up transformer to raise inverter output voltages to high voltage. The third scheme as shown in Fig. 23.19c comprises of a dc-to-dc converter, an inverter that switches at high frequency, and a mains-voltage motor-driven pump. To get the optimum discharge (Q) at a given insolation level, the efficiency of the dc–dc converter and the inverter should be high. So the purpose should be to optimize the output from the PV array, motor, and pump. The principle used here is to vary the duty cycle of a dc-to-dc converter so that the output voltage is maximum. The dc-to-dc converter is used to boost the solar array voltage to eliminate the need for a step-up transformer and to operate the array at the maximum power point. The three-phase inverter used in the interface is designed to operate in a variable-frequency mode over the range of 20 to 50-Hz, which is the practical limit for most 50-Hz induction motor applications. The block diagram for

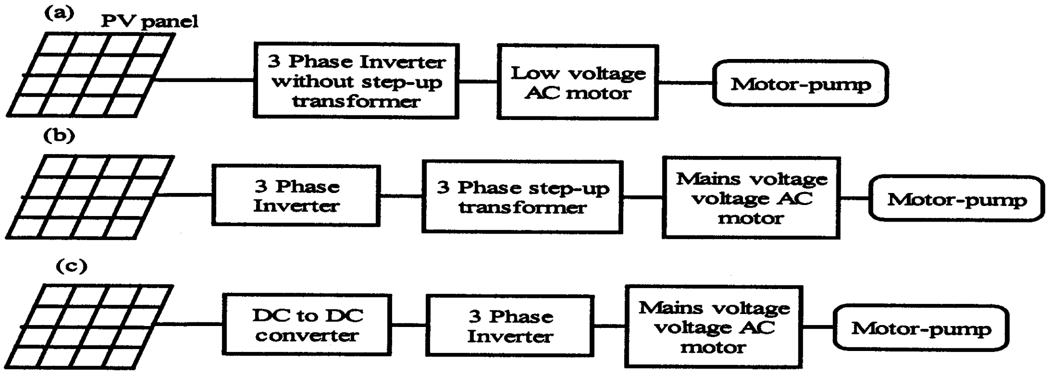

(a)
PV panel
3 Phase Inverter without step-up transformer
Low voltage AC motor
Motor-pump
(b)
3 Phase Inverter
3 Phase step-up transformer
Mains voltage voltage AC motor
Motor-pump
(c)
DC to DC converter
3 Phase Inverter
Mains voltage voltage AC motor
Motor-pump

FIGURE 23.19 Block diagrams for various ac motor-driven pumping schemes.

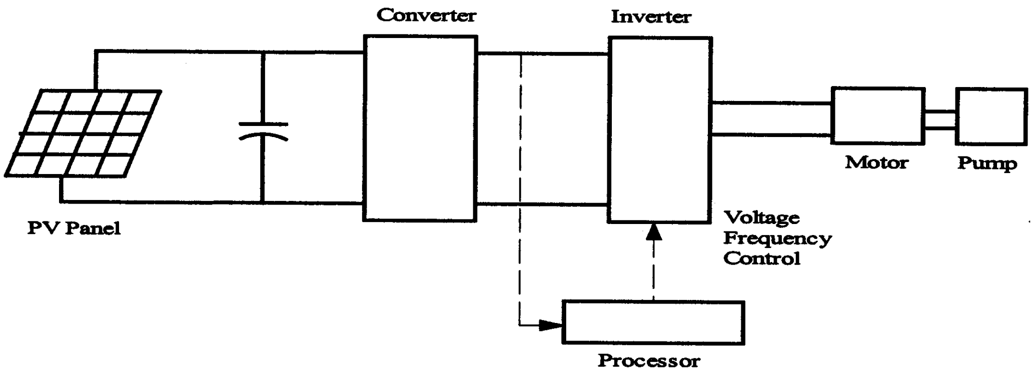


FIGURE 23.20 Block diagram for voltage/frequency control.

frequency control is given in Fig. 23.20. This inverter would be suitable for driving permanent-magnet motors by incorporating additional circuitry for position sensing of the motor's shaft. Also, the inverter could be modified, if required, to produce higher output frequencies for high-speed permanent-magnet motors. The inverter has a three-phase full-bridge configuration implemented by MOSFET power transistors.

23.2.4 PV Diesel Systems

Photovoltaic–diesel hybrid energy systems generate ac electricity by combining a photovoltaic array with an inverter, which can operate alternately or in parallel with a conventional engine-driven generator. They can be classified according to their configuration as follows [8]:

1. Series hybrid energy systems
2. Switched hybrid energy systems
3. Parallel hybrid energy systems

An overview of the three most common system topologies is presented by Bower [9]. In the following comparison, typical PV–diesel system configurations are described.

23.2.4.1 Series Configuration

Figure 23.21 shows a series PV–diesel hybrid energy system. To ensure reliable operation of series hybrid energy systems, both the diesel generator and the inverter have to be sized to meet peak loads. This results in a typical system operation where a large fraction of the generated energy is passed through the battery bank, resulting in increased cycling of the battery bank and reduced system efficiency. Ac power delivered to the load is converted from dc to regulated ac by an inverter or a motor generator unit. The power generated by the diesel generator is first rectified and subsequently converted back to ac before being supplied to the load, which leads to significant conversion losses.

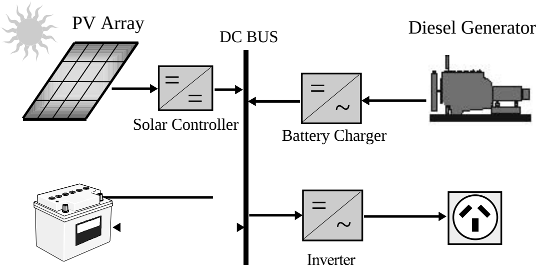


FIGURE 23.21 Series PV–diesel hybrid energy system.

The actual load demand determines the amount of electrical power delivered by the photovoltaic array, the battery bank, or the diesel generator. The solar controller prevents overcharging of the battery bank from the PV generator when the PV power exceeds the load demand and the batteries are fully charged. It may include maximum power point tracking to improve the utilization of the available photovoltaic energy, although the energy gain is marginal for a well-sized system. The system can be operated in manual or automatic mode, with the addition of appropriate battery voltage sensing and start/stop control of the engine-driven generator.

The advantages of such a system include the following:

- The engine-driven generator can be sized to be optimally loaded while supplying the load and charging the battery bank, until a battery state-of-charge (SOC) of 70–80% is reached.
- No switching of ac power between the different energy sources is required, which simplifies the electrical output interface.
- The power supplied to the load is not interrupted when the diesel generator is started.
- The inverter can generate a sine-wave, modified square wave, or square wave, depending on the application.

The disadvantages are:

- The inverter cannot operate in parallel with the engine-driven generator; therefore, the inverter must be sized to supply the peak load of the system.

- The battery bank is cycled frequently, which shortens its lifetime.
- The cycling profile requires a large battery bank to limit the depth-of-discharge.
- The overall system efficiency is low, since the diesel cannot supply power directly to the load;
- Inverter failure results in complete loss of power to the load, unless the load can be supplied directly from the diesel generator for emergency purposes.

23.2.4.2 Switched Configuration

Despite its operational limitations, the switched configuration as shown in Fig. 23.22 remains one of the most common installations today. It allows operation with either the engine-driven generator or the inverter as the ac source, yet no parallel operation of the main generation sources is possible. The diesel generator and the renewable energy source can charge the battery bank. The main advantage compared with the series system is that the load can be supplied directly by the engine-driven generator, which results in a higher overall conversion efficiency. Typically, the diesel generator power will exceed the load demand, with excess energy being used to recharge the battery bank. During periods of low electricity demand the diesel generator is switched off and the load is supplied from the PV array together with stored energy. Switched hybrid energy systems can be operated in manual mode, although the increased complexity of the system makes it highly desirable to include an automatic controller, which can be implemented with the addition of appropriate battery voltage sensing and start/stop control of the engine-driven generator.

The advantages of this system are:

- The inverter can generate a sine-wave, modified square wave, or square wave, depending on the particular application.
- The diesel generator can supply the load directly, therefore improving the system efficiency and reducing the fuel consumption.

The disadvantages are:

- Power to the load is interrupted momentarily when the ac power sources are transferred.
- The engine-driven alternator and inverter are typically designed to supply the peak load, which reduces their efficiency at part-load operation.

23.2.4.3 Parallel Configuration

The parallel configuration shown in Fig. 23.23 allows all energy sources to supply the load separately at low or medium load demand, as well as supplying peak loads from combined sources by synchronizing the inverter with the alternator output waveform. The bidirectional inverter can charge the battery bank (rectifier operation) when excess energy is available from the engine-driven generator, as well as act as a dc–ac converter (inverter operation). The bidirectional inverter may provide "peak shaving" as part of the control strategy when the engine-driven generator is overloaded.

Parallel hybrid energy systems are characterized by two significant improvements over the series and switched system configurations.

1. The inverter plus the diesel generator capacity rather than their individual component ratings limit the maximum load that can be supplied. Typically, this will lead to a doubling of the system capacity. The capability to synchronize the inverter with the diesel generator allows greater flexibility to optimize the operation of the system. Future systems should be sized with a reduced peak capacity of the diesel generator, which results in a higher fraction of directly used energy and hence higher system efficiencies.
2. By using the same power electronic devices for both inverter and rectifier operation, the number of system components is minimized. Additionally, wiring and system installation costs are reduced through the integration of all power conditioning devices in one central power unit. This highly integrated system concept has advantages over a more modular approach to system design, but it may prevent convenient system upgrades when the load demand increases.

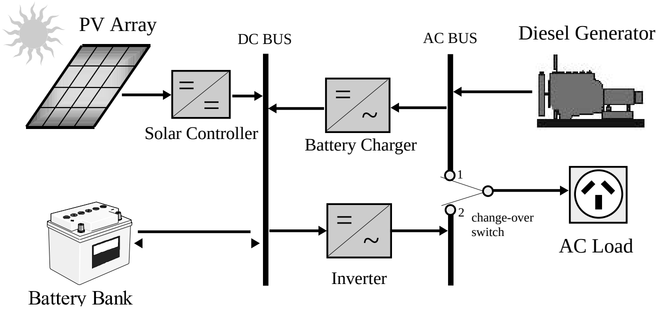


FIGURE 23.22 Switched PV-diesel hybrid energy system.

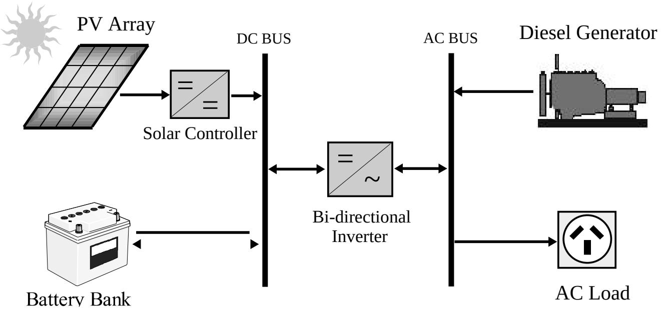


FIGURE 23.23 Parallel PV–diesel hybrid energy system.

The parallel configuration offers a number of potential advantages over other system configurations. These objectives can only be met if the interactive operation of the individual components is controlled by an "intelligent" hybrid energy management system. Although today's generation of parallel systems includes system controllers of varying complexity and sophistication, they do not optimize the performance of the complete system. Typically, both the diesel generator and the inverter are sized to supply anticipated peak loads. As a result, most parallel hybrid energy systems do not utilize their capability of parallel, synchronized operation of multiple power sources.

The advantages of this system include the following:

- The system load can be met in an optimal way.
- Diesel generator efficiency can be maximized.
- Diesel generator maintenance can be minimized.
- A reduction in the rated capacities of the diesel generator, battery bank, inverter, and renewable resources is feasible, while also meeting the peak loads.

The disadvantages are:

- Automatic control is essential for the reliable operation of the system.
- The inverter has to be a true sine-wave inverter with the ability to synchronize with a secondary ac source.
- System operation is less transparent to the untrained user of the system.

23.2.4.4 Control of PV Diesel Hybrid Systems

The design process of hybrid energy systems requires the selection of the most suitable combination of energy sources, power-conditioning devices, and energy-storage system, together with the implementation of an efficient energy-dispatch strategy. System simulation software is an essential tool to analyze and compare possible system combinations. The objective of the control strategy is to achieve optimal operational performance at the system level. Inefficient operation of the diesel generator and "dumping" of excess energy is common for many remote-area power supplies operating in the field. Component maintenance and replacement contributes significantly to the life-cycle cost of systems. These aspects of system operation are clearly related to the selected control strategy and have to be considered in the system design phase.

Advanced system control strategies seek to reduce the number of cycles and the depth-of-discharge for the battery bank, run the diesel generator in its most efficient operating range, maximize the utilisation of the renewable resource, and ensure high reliability of the system. Because of the varying nature of the load demand, the fluctuating power supplied by the photovoltaic generator, and the resulting variation of battery SOC, the hybrid energy system controller has to respond to continuously changing operating conditions. Figure 23.24 shows different operating modes for a PV single-diesel system using a typical diesel dispatch strategy.

Mode (I):	The base load, which is typically experienced at night and during the early morning hours, is supplied by energy stored in the batteries. Photovoltaic power is not available and the diesel generator is not started.
Mode (II):	PV power is supplemented by stored energy to meet the medium load demand.
Mode (III):	Excess energy is available from the PV generator, which is stored in the battery. The medium load demand is supplied from the PV generator.
Mode (IV):	The diesel generator is started and operated at its nominal power to meet the high evening load. Excess energy available from the diesel generator is used to recharge the batteries.
Mode (V):	The diesel generator power is insufficient to meet the peak load demand. Additional power is supplied from the batteries by synchronizing the inverter ac output voltage with the alternator waveform.
Mode (VI):	The diesel generator power exceeds the load demand, but it is kept operational until the batteries are recharged to a high state-of-charge level.

In principle, most efficient operation is achieved if the generated power is supplied directly to the load from all energy sources, which also reduces cycling of the battery bank. However, since diesel generator operation at light loads is inherently inefficient, it is common practice to operate the engine-driven generator at its nominal power rating and to recharge the batteries from the excess energy. The selection of the most efficient control strategy depends on fuel, maintenance and component-replacement cost, the system configuration, and environmental conditions, as well as constraints imposed on the operation of the hybrid energy system.

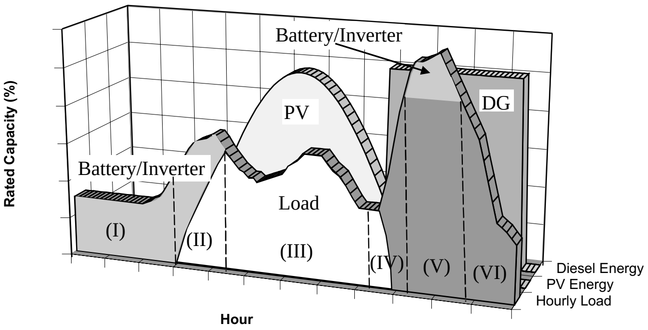


FIGURE 23.24 Operating modes for a PV single-diesel hybrid energy system.

23.2.5 Grid Connected PV Systems

Utility interactive inverters not only condition the power output of the photovoltaic arrays but ensure that the PV system output is fully synchronized with the utility power. These systems can be batteryless or with battery backup. Systems with battery storage (or a flywheel) provide additional power-supply reliability. The grid connection of photovoltaic systems is gathering momentum because of various rebate and incentive schemes. This system allows the consumer to feed its own load utilizing the available solar energy, and the surplus energy can be injected into the grid under the energy buy-back scheme to reduce the payback period. Grid-connected PV systems can become a part of the utility system. The contribution of solar power depends on the size of system and the load curve of the house. When the PV system is integrated with the utility grid, a two-way power flow is established. The utility grid will absorb excess PV power and will feed the house at night and at instants when the PV power is inadequate. The utility companies are encouraging this scheme in many parts of the world. The grid-connected system can be classified as follows:

- Rooftop application of grid-connected PV system
- Utility-scale large system

For small household PV applications, a roof-mounted PV array can be the best option. Solar cells provide an environmentally clean way of producing electricity, and rooftops have always been the ideal place to put them. With a PV array on the rooftop, the solar-generated power can supply residential load. The rooftop PV systems can help in reducing the peak summer load to the benefit of utility companies by feeding the household lighting, cooling, and other domestic loads. The battery storage can further improve the reliability of the system at times of low insolation level, at night or on cloudy days. But the battery storage has some inherent problems, such as maintenance and higher cost.

For roof-integrated applications, the solar arrays can be either mounted on the roof or directly integrated into the roof. If the roof integration does not allow for an air channel behind the PV modules for ventilation purposes, then it can increase the cell temperature during the operation, consequently leading to some energy losses. The disadvantage of the rooftop application is that the PV array orientation is dictated by the roof. In cases, where the roof orientation differs from the optimal orientation required for the cells, the efficiency of the entire system would be suboptimal.

Utility interest in PV has centered around the large grid-connected PV systems. In Germany, the United States, Spain, and several other parts of the world, some large PV-scale plants have been installed. The utilities are more inclined toward large-scale, centralized power supplies. The PV systems can be centralized or distributed systems.

Grid-connected PV systems must observe the islanding situation, when the utility supply fails. In case of islanding, the PV generators should be disconnected from mains. PV generators can continue to meet only the local load, if the PV output matches the load. If the grid is reconnected during islanding, transient overcurrents can flow through the PV system inverters, and protective equipment such as circuit breakers may be damaged. Islanding control can be achieved through inverters or via the distribution network. Inverter controls can be designed on the basis of detection of grid voltage or measurement of impedance, frequency variation, or increase in harmonics. Protection must be designed for islanding, short circuits, over/under voltages/currents, grounding and lightning etc.

The importance of the power generated by the PV system depends on the time of the day, especially when the utility is experiencing peak load. The PV plants are well suited to summer peaking, but it depends upon the climatic condition of the site. PV systems being investigated for use as peaking stations would be competitive for load management. The PV users can defer their load by adopting load management to get the maximum benefit out of the grid-connected PV plants and feeding more power into the grid at the time of peak load.

The assigned capacity credit is based on the statistical probability that the grid can meet peak demand [3]. The capacity factor during peaks is very similar to that of conventional plants, and similar capacity credit can be given for PV generation, except at times when the PV plants are generating very much less power, unless adequate storage is provided. With the installation of PV plants, the need for extra transmission lines and transformers can be delayed or avoided. The distributed PV plants can also contribute in providing reactive power support to the grid and reduce the burden on VAR compensators.

23.2.5.1 Inverters for Grid-Connected Applications

The power conditioner is the key link between the PV array and mains in the grid-connected PV system. It acts as an interface that converts dc current produced by the solar cells into utility-grade ac current. The PV system behavior relies heavily on the power-conditioning unit. The inverters must produce good-quality sine-wave output, must follow the frequency and voltage of the grid, and must extract maximum power from the solar cells with the help of a maximum-power-point tracker. The inverter input stage varies the input voltage until the maximum power point on the $I-V$ curve is found. The inverter must monitor all the phases of the grid, and inverter output must be controlled in terms of voltage and frequency variation. A typical grid-connected inverter may use a pulse-width modulation (PWM) scheme and operate in the range of 2 kHz up to 20 kHz.

23.2.5.2 Inverter Classifications

The inverters used for grid interfacing are broadly classified as voltage-source inverters (VSI) and current-source inverters (CSI); whereas the inverters based on the control schemes can be classified as current-controlled inverters (CCI) and voltage-controlled inverters (VCI). The source is not necessarily characterized by the energy source for the system. It is a characteristic of the topology of the inverter. It is possible to change from one source type to another source type by the addition of passive components. In the voltage-source inverter (VSI), the dc side is made to appear to the inverter as a voltage source. The voltage-source inverters have a capacitor in parallel across the input, whereas the current-source inverters have an inductor in series with the dc input. In the current-source inverter (CSI), the dc source appears as a current source to the inverter. Solar arrays are fairly good approximation to a current source. Most PV inverters are voltage source, even though the PV is a current source. Current-source inverters are generally used for large motor drives although there have been some PV inverters built using a current source topology. The voltage-source inverter is more popular, with the PWM voltage-source inverter (VSI) dominating the sine-wave inverter topologies.

Fig 23.25a shows a single-phase full bridge bidirectional voltage source inverter (VSI) with (a) voltage control and phase shift (δ) control. The active power transfer from the PV panels is accomplished by controlling the phase angle δ between the converter voltage and the grid voltage. The converter voltage follows the grid voltage. Figure 23.25b shows the same voltage source inverter operated as a current-controlled inverter (CSI). The objective of this scheme is to control active and reactive components of the current fed into the grid using pulse-width modulation techniques.

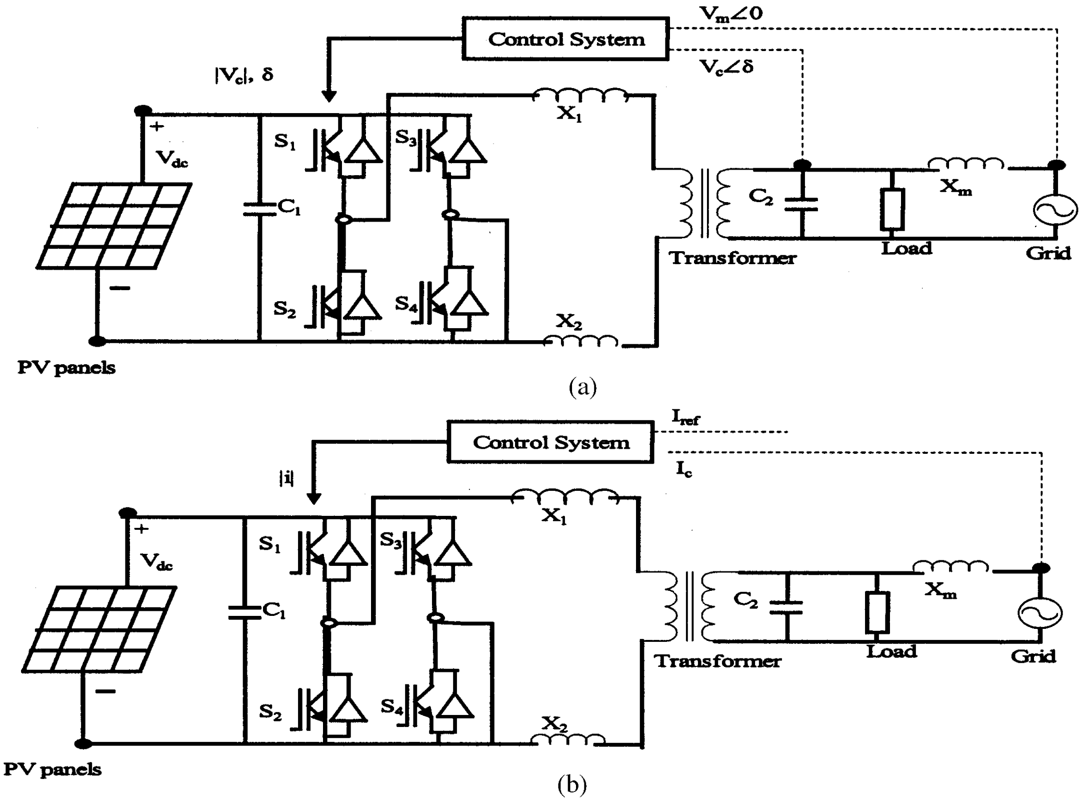
23.2.5.3 Inverter Types

Various types of inverters are in use for grid-connected PV applications, including the following:

- Line-commutated inverter
- Self-commutated inverter
- PV inverter with high-frequency transformer

. . . . ***Line-Commutated Inverter*** Line-commutated inverters are generally used for electric-motor applications. The power stage is equipped with thyristors. A maximum-power tracking control is required in the control algorithm for solar application. The basic diagram for a single-phase line-commutated inverter is shown in Fig. 23.26 [2].

The driver circuit has to be changed to shift the firing angle from rectifier operation ($0^\circ < \phi < 90^\circ$) to inverter operation ($90^\circ < \phi < 180^\circ$). Six-pulse or 12-pulse inverters are used for grid interfacing, but 12-pulse inverters produce fewer harmo-



(a)

(b)

FIGURE 23.25 (a) Grid-interactive VSI; (b) grid-interactive CSI.

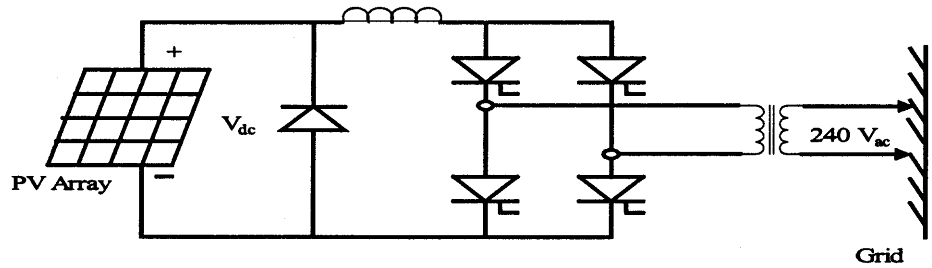


FIGURE 23.26 Line-commutated single-phase inverter.

nics. Thyristor-type inverters require a low-impedance grid interface connection for commutation purposes. If the maximum power available from the grid connection is less than twice the rated PV inverter power, then the line-commutated inverter should not be used [2]. The line-commutated inverters are cheaper but can lead to poor power quality. The harmonics injected into the grid can be large unless taken care of by employing adequate filters. These line-commutated inverters also have poor power factors that require additional control to improve them. Transformers can be used to provide electrical isolation. To suppress the harmonics generated by these inverters, tuned filters are employed and reactive power compensation is required to improve the lagging power factor.

. . . . Self-Commutated Inverter A switch-mode inverter using pulse-width modulated (PWM) switching control can be used for the grid connection of PV systems. The basic block diagram for this type of inverter is shown in Fig. 23.27.

The inverter bridges may consist of bipolar transistors, MOSFET transistors, IGBTs, or GTOs, depending on the type of application. GTOs are used for higher-power applications, whereas IGBTs can be switched at higher frequencies, i.e., 20 kHz, and are generally used for many grid-connected PV applications. Most present-day inverters are self-commutated sine-wave inverters.

Based on the switching control, voltage-source inverters can be further classified as follows:

- PWM (pulse width modulated) inverters
- Square-wave inverters
- Single-phase inverters with voltage cancellations
- Programmed harmonic elimination switching
- Current-controlled modulation

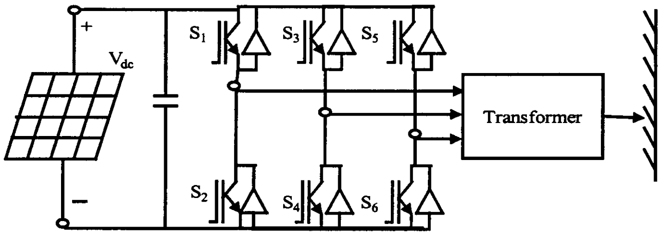


FIGURE 23.27 Self-commutated inverter with PWM switching.

. . . . PV Inverter with High-Frequency Transformer The 50-Hz transformer for a standard PV inverter with PWM switching scheme can be very heavy and costly. When using frequencies more than 20 kHz, a ferrite core transformer can be a better option [2]. A circuit diagram of a grid-connected PV system using high frequency transformer is shown in Fig. 23.28.

The capacitor on the input side of the high-frequency inverter acts as a filter. The high-frequency inverter with pulse-width modulation is used to produce a high-frequency ac across the primary winding of the high-frequency transformer. The secondary voltage of this transformer is rectified using a high-frequency rectifier. The dc voltage is interfaced with a thyristor inverter through a low-pass inductor filter and hence connected to the grid. The line current is required to be sinusoidal and in phase with the line voltage. To achieve this, the line voltage (V_l) is measured to establish the reference waveform for the line current I_L^*. This reference current I_L^*

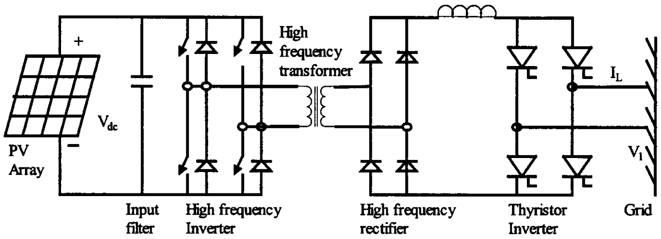


FIGURE 23.28 PV inverter with high-frequency transformer.

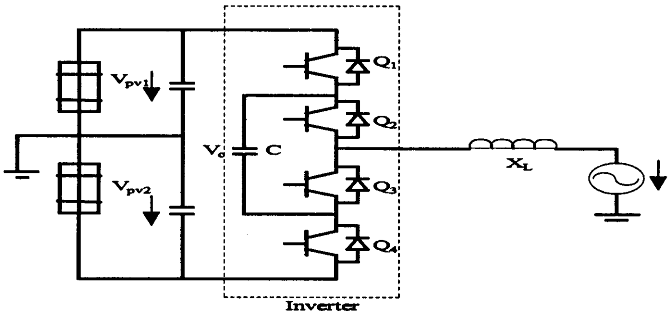


FIGURE 23.29 Half-bridge diode-clamped three-level inverter.

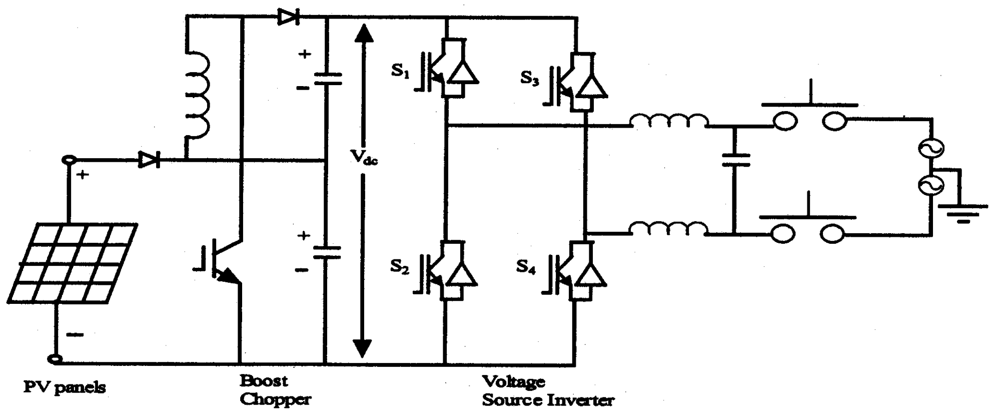


FIGURE 23.30 Noninsulated voltage source.

multiplied by the transformer ratio gives the reference current at the output of the high-frequency inverter. The inverter output can be controlled using current-controls technique [10]. These inverters can be used with low-frequency or high-frequency transformer isolation. The low-frequency (50/60 Hz) transformer of a standard inverter with pulse-width modulation is a very heavy and bulky component. For residential grid interactive rooftop inverters below 3-kW rating, high-frequency transformer isolation is often preferred.

. . . . ***Other PV Inverter opologies*** In this section, some of the inverter topologies discussed in various research papers are discussed.

Multilevel Converters Multilevel converters can be used with large PV systems where multiple PV panels can be configured to create voltage steps. These multilevel voltage source converters can synthesize the ac output terminal voltage from different levels of dc voltages and can produce staircase waveforms. This scheme involves less complexity and needs less filtering. One of the schemes (half-bridge diode-clamped three-level inverter [11]) is given in Fig. 23.29. There is no transformer in this topology. Multilevel converters can be beneficial for large systems in terms of cost and efficiency. Problems associated with shading and malfunction of PV units need to be addressed.

Noninsulated Voltage Source In this scheme [12], a string of low-voltage PN panels or one high-voltage unit can be coupled with the grid through a dc-to-dc converter and voltage-source inverter. This topology is shown in Fig. 23.30. A PWM switching scheme can be used to generate ac output. A filter has been used to reject the switching components.

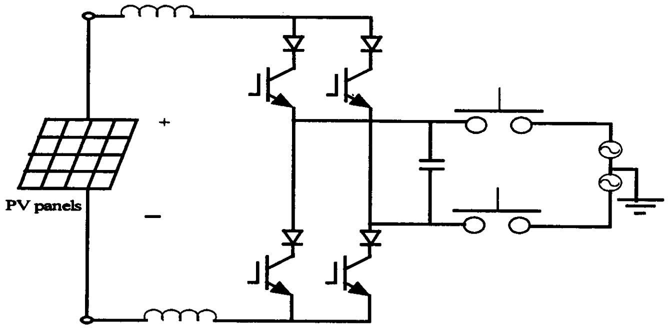


FIGURE 23.31 Noninsulated current source.

Non-insulated Current Source This type of configuration is shown in Fig. 23.31. Non-insulated current source inverters [12] can be used to interface the PV panels with the grid. This topology involves low cost and can provide better efficiency. Appropriate controllers can be used to reduce current harmonics.

Buck Converter with Half-bridge Transformer Link PV panels are connected to grid via a buck converter and half-bridge as shown in Fig. 23.32. In this, high-frequency PWM switching has been used at the low-voltage photovoltaic side to generate an attenuated rectified 100-Hz sine wave current waveform [13]. A half-wave bridge is utilized to convert this output to a 50-Hz signal suitable for grid interconnection. To step up the voltage, the transformer has also been connected before the grid connection point.

Flyback Converter This converter topology steps up the PV voltage to dc bus voltage. The PWM-operated converter has been used for grid connection of a PV system in Fig. 23.33. This scheme is less complex and has fewer switches. Flyback converters can be beneficial for remote areas because of their complex power-conditioning components.

Interface using Paralleled PV Panels A low-voltage ac bus scheme [14] can be a comparatively efficient and cheaper option. One of the schemes is shown in Fig. 23.34. A number of smaller PV units can be paralleled together and then

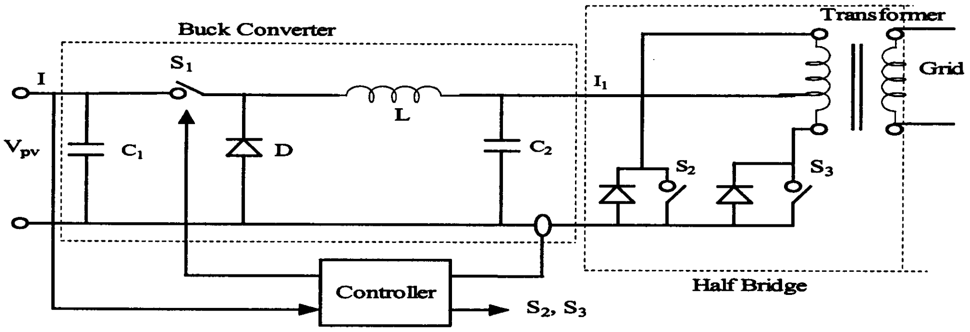


FIGURE 23.32 Buck converter with half-bridge transformer link.

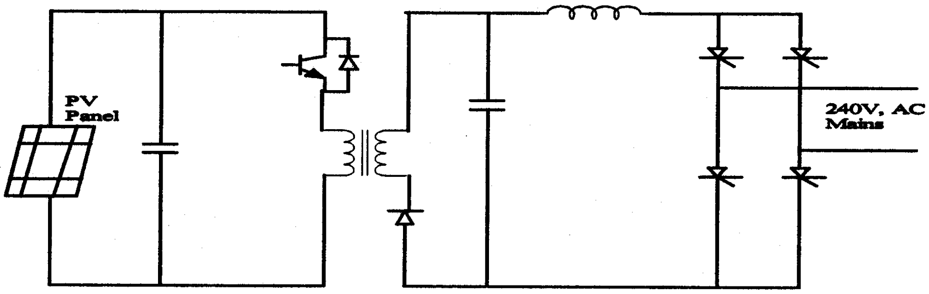


FIGURE 23.33 Flyback converter.

connected to a single low-frequency transformer. In this scheme, PV panels are connected in parallel rather than series to avoid problems associated with shading or malfunction of one of panels in series connection.

23.2.5.4 Power Control through PV Inverters

The system shown in Fig. 23.35a shows control of power flow onto the grid. This control can be analog or a microprocessor system. This control system generates the waveforms and regulates the waveform amplitude and phase to control the power flow between the inverter and the grid. The grid-interfaced PV inverters, voltage-controlled (VCI) or current-controlled (CCI), have the potential of bidirectional power flow. They not only can feed the local load, but also can export the excess active and reactive power to the utility grid. An appropriate controller is required in order to avoid any error in power export due to errors in synchronization, which can overload the inverter. A simple grid–inverter interface with a first-order filter and the phasor diagram [15] are shown in Figs. 23.35a and 23.35b.

In the case of voltage controllers, the power equation can be written as [10]:

$$S = P + jQ$$

$$\text{or } S = \frac{VV_{\text{pwm}}}{X_{\text{L}}}\sin\delta + j\left[\frac{VV_{\text{pwm}}}{X_{\text{L}}}\cos\delta - \frac{V^2}{X_{\text{L}}}\right]$$

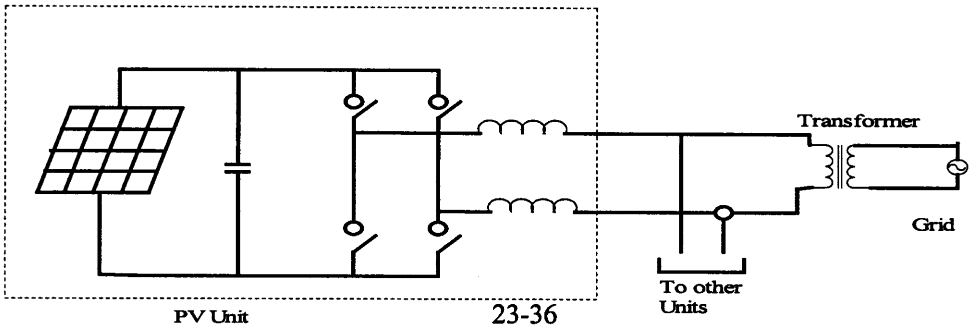


FIGURE 23.34 Converter using parallel PV units.

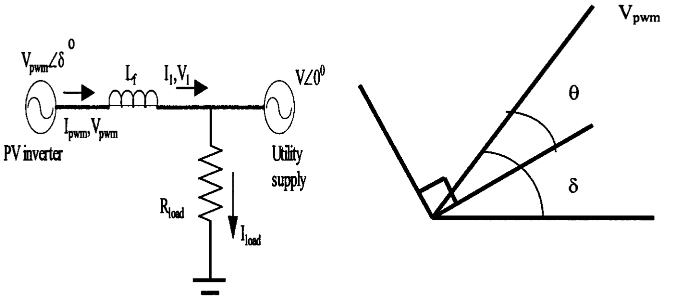


FIGURE 23.35 (a) Simple grid interface system; (b) phasor diagram of grid-integrated PV.

whereas for the current controllers [16]:

$$S = V_{\mathrm{pwm}} 1 \cos\theta + j[V_{\mathrm{pwm}} 1 \sin\theta] \qquad (23.7)$$

It has been observed that the inverter rated power export is achieved at $\delta = 5°$. When using a voltage controller for grid connected PV inverter, it has been observed that a slight error in the phase of synchronising waveform can grossly overload the inverter whereas a current controller is much less susceptible to voltage phase shifts [15]. For this reason, the current controllers are better suited for the control of power export from the PV inverters to the utility grid since they are less sensitive to errors in synchronizing sinusoidal voltage waveforms.

A prototype current-controlled-type power conditioning system has been developed by the first author and tested on a weak rural feeder line at Kalbarri in Western Australia [17]. The choice may be between additional conventional generating capacity at a centralized location or adding smaller distributed generating capacities using renewable energy sources such as PV. The latter option can have a number of advantages:

- The additional capacity is added wherever it is required without adding power-distribution infrastructure. This is a critical consideration where the power lines and transformers are already at or close to their maximum ratings.
- The power conditioning system can be designed to provide much more than just a source of real power, for minimal extra cost. A converter providing real power needs only a slight increase in ratings to handle significant amounts of reactive or even harmonic power. The same converter that converts dc photovoltaic power to ac power can simultaneously provides reactive power support to the weak utility grid.

The block diagram of the power conditioning system used in the Kalbarri project is shown in the Fig. 23.36. This CC-VSI operates with a relatively narrow switching frequency band near 10 kHz. The control diagram indicates the basic operation of the power conditioning system. The two outer control loops operate to independently control the real and reactive power flow from the PV inverter. The real power is controlled by an outer maximum-power-point tracking (MPPT) algorithm with an inner dc link voltage-control loop providing the real current magnitude request. I_{p}^{*} and hence the real power export through PV converter are controlled through the dc link-voltage regulation. The dc link voltage is maintained at a reference value by a PI control loop, which gives the real current reference magnitude as its output. At regular intervals, the dc link voltage is scanned over the entire voltage range to check that the algorithm is operating on the absolute MPP and is not stuck around a local MPP. During the night, the converter can still be used to regulate reactive power of the grid-connected system, although it cannot provide active power. During this time, the PI controller maintains a minimum dc link voltage to allow the power-conditioning system to continue to operate, providing the necessary reactive power.

The ac line voltage regulation is provided by a separate reactive power control, which provides the reactive current magnitude reference I_{Q}^{*}. The control system has a simple transfer function, which varies the reactive power command in response to ac voltage fluctuations. Common to the outer real and reactive power control loops is an inner higher bandwidth ZACE current control loop. I_{p}^{*} is in phase with

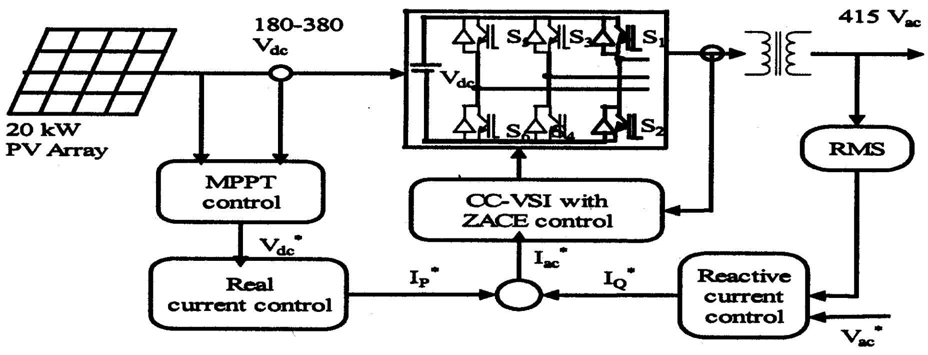


FIGURE 23.36 Block diagram of Kalbarri power-conditioning system.

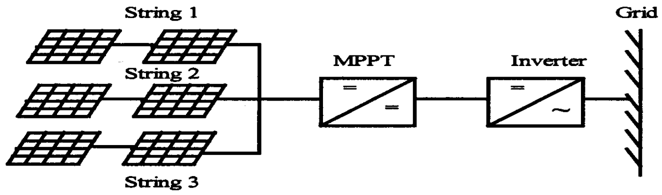


FIGURE 23.37 Central-plant inverter.

the line voltages, and I_Q^* is at 90° to the line voltages. These are added together to give one (per phase) sinusoidal converter current reference waveform (I_{ac}^*). The CC-VSI control consists of analog and digital circuitry that acts as a ZACE transconductance amplifier in converting I_{ac}^* into ac power currents [18].

23.2.5.5 System Configurations

The utility-compatible inverters are used for power conditioning and synchronization of PV output with the utility power. In general, four types of batteryless grid connected PV system configurations have been identified:

- Central-plant inverter
- Multiple-string dc–dc converter with single-output inverter
- Multiple-string inverter
- Module-integrated inverter

. . . . ***Central-Plant Inverter*** In the central-plant inverter, usually a large inverter is used to convert dc power output of PV arrays to ac power. In this system, the PV modules are serially strung to form a panel (or string), and several such panels are connected in parallel to a single dc bus. The block diagram of such a scheme is shown in Fig. 23.37.

. . . . ***Multiple-String dc/dc Converter*** In the multiple-string dc–dc converter, as shown in Fig. 23.38, each string will have a boost dc–dc converter with transformer isolation. There will be a common dc link, which feeds a transformerless inverter.

. . . . ***Multiple-String Inverter*** Figure 23.39 shows the block diagram of a multiple-string inverter system. In this scheme, several modules are connected in series on the dc side to form a string. The output from each string is converted to ac through a smaller individual inverter. Many such inverters are connected in parallel on the ac side. This arrangement is not badly affected by shading of the panels. It is also not seriously affected by inverter failure.

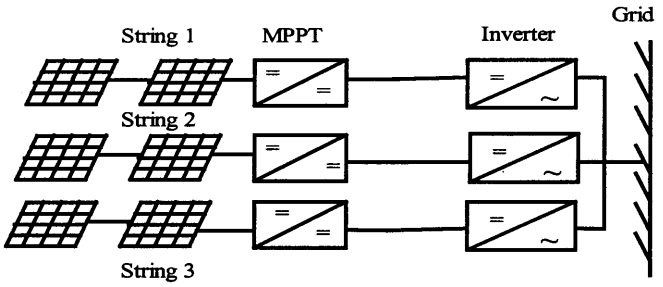


FIGURE 23.39 Multiple-string inverter.

. . . . ***Module-Integrated Inverter*** In the module-integrated inverter system (Fig. 23.40), each module (typically 50 W to 300 W) will have a small inverter. No cabling is required. It is expected that a high volume of small inverters will bring down the cost.

23.2.5.6 Grid-Compatible Inverter Characteristics

The characteristics of the grid-compatible inverters are:

- Response time
- Power factor
- Frequency control
- Harmonic output
- Synchronization
- Fault current contribution
- Dc current injection
- Protection

The response time of the inverters must be extremely fast and governed by the bandwidth of the control system. The absence of rotating mass and the use of semiconductor switches allow inverters to respond in a millisecond time frame. The power factor of the inverters is traditionally poor because of the displacement power factor and harmonics. But with the latest developments in inverter technology, it is possible to maintain a power factor close to unity. The converters/inverters have

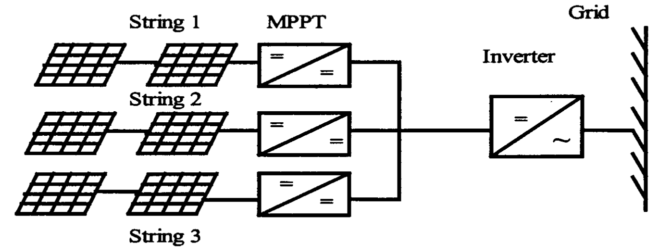


FIGURE 23.38 Multiple-string dc/dc converter.

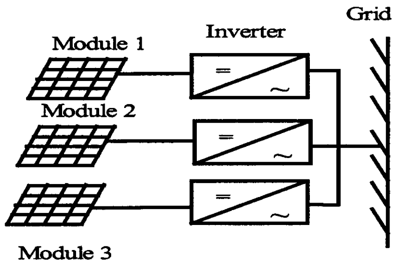


FIGURE 23.40 Module-integrated inverter.

the capability of creating large voltage fluctuations by drawing reactive power from the utility rather than supplying it [19]. With proper control, inverters can provide voltage support by importing/exporting reactive power to push/pull toward a desired set point. This function would be of more use to the utilities as it can assist in the regulation of the grid system at the domestic consumer level.

The frequency of the inverter output waveshape is locked to the grid. Frequency bias is where the inverter frequency is deliberately made to run at, say, 53 Hz. When the grid is present, this will be pulled down to the nominal 50 Hz. If the grid fails, it will drift upward toward 53 Hz and trip on overfrequency. This can help in preventing islanding.

Harmonic output from inverters has traditionally been very poor. Old thyristor-based inverters operated with slow switching speeds and could not be pulse-width modulated. This resulted in inverters known as six-pulse or 12-pulse inverters. The harmonics so produced from the inverters can be injected into the grid, resulting in losses, heating of appliances, tripping of protection equipment, and poor power quality, the number of pulses being the number of steps in a sine-wave cycle. With the present advances in power-electronics technology, inverter controls can be made very good. PWM inverters produce high-quality sine waves. The harmonic levels are very low and can be lower than those of common domestic appliances. If harmonics are present in the grid voltage waveform, harmonic currents can be induced in the inverter. These harmonic currents, particularly those generated by a voltage-controlled inverter, will in fact help in supporting the grid. These are good harmonic currents. This is the reason that the harmonic current output of inverters must be measured onto a clean grid source so that only the harmonics being produced by the inverters are measured.

Synchronization of inverters with the grid is performed automatically and typically uses zero-crossing detection on the voltage waveform. An inverter has no rotating mass and hence has no inertia. Synchronization does not involve the acceleration of a rotating machine. Consequently, the reference waveforms in the inverter can be jumped to any point required within a sampling period. If phase-locked loops are used, the jump could take up a few seconds. Phase-locked loops are used to increase the immunity to noise. This allows the synchronization to be based on several cycles of zero-crossing information. The response time for this type of locking will be slower.

PV panels produce a current that is proportional to the amount of light falling on them. The panels are normally rated to produce 1000 W/m^2 at 25°C. Under these conditions, the short circuit current possible from these panels is typically only 20 higher than the nominal current, whereas it is extremely variable for wind. If the solar radiation is low then the maximum current possible under short circuit is going to be less than the nominal full-load current. Consequently, PV systems cannot provide short-circuit capacity to the grid. If a battery is present, the fault current contribution is limited by the inverter. With battery storage, it is possible for the battery to provide the energy. However, inverters are typically limited to between 100 and 200 of nominal rating under current-limit conditions. The inverter needs to protect itself against short circuits because the power electronic components will typically be destroyed before a protection device such as a circuit breaker trip.

In case of inverter malfunction, inverters have the capability to inject the dc components into the grid. Most utilities have guidelines for this purpose. A transformer must be installed at the point of connection on the ac side to prevent dc from entering the utility network. The transformer can be omitted when a dc detection device is installed at the point of connection on the ac side in the inverter. The dc injection is essentially caused by the reference or power electronics device producing a positive half-cycle that is different from the negative half-cycle resulting into the dc component in the output. If the dc component can be measured, it can then be added into the feedback path to eliminate the dc quantity.

. . . . *Protection Requirements* A minimum requirement to facilitate the prevention of islanding is that the inverter energy system protection operates and isolates the inverter energy system from the grid if any of the following occurs:

- Overvoltage
- Undervoltage
- Overfrequency
- Underfrequency

These limits may be either factory-set or site-programmable. The protection voltage operating points may be set in a narrower band if required, e.g., 220 V to 260 V. In addition to the passive protection detailed above, and to prevent the situation where islanding may occur because multiple inverters provide a frequency reference for one another, inverters must have an accepted active method of islanding prevention following grid failure, e.g., frequency drift or impedance measurement. Inverter controls for islanding can be designed on the basis of detection of grid voltage, measurement of impedance, frequency variation, or increase in harmonics. This function must operate to force the inverter output outside the protection tolerances specified previously, thereby resulting in isolation of the inverter energy system from the grid. The maximum combined operation time of both passive and active protections should be 2 seconds after grid failure under all local load conditions. If frequency shift is used, it is recommended that the direction of shift be down. The inverter energy system must remain disconnected from the grid until the reconnection conditions are met. Some inverters produce high-voltage spikes, especially at light load, which can be dangerous for the electronic equipment. IEEE P929 gives some idea of the permitted voltage limits.

If the inverter energy system does not have the preceding frequency features, the inverter must incorporate an alternate antiislanding protection feature that is acceptable to the relevant electricity distributor. If the protection function above is to be incorporated in the inverter, it must be type tested for compliance with these requirements and accepted by the relevant electricity distributor. Otherwise, other forms of external protection relaying are required that have been type tested for compliance with these requirements and approved by the relevant electricity distributor. The inverter must have adequate protection against short-circuit, other faults, and overheating of inverter components.

23.3 Power Electronics for Wind Power Systems

In the rural United States, the first windmill to generate electricity was commissioned in 1890. Today, large wind generators are competing with utilities in supplying clean power economically. The average wind turbine size has been 300–600 kW until recently. New wind generators of 1–3 MW have been developed and are being installed worldwide, and prototypes of even higher capacity are under development. Improved wind turbine designs and plant utilization have resulted in significant reduction in wind energy generation cost from 35 cents per kWh in 1980 to less than 5 cents per kWh in 1999 in locations where wind regime is favorable. At this generation cost, wind energy has become one of the cheapest power sources. The main factors that have contributed to the wind power technology development are:

- High-strength fiber composites for manufacturing large, low-cost blades
- Variable-speed operation of wind generators to capture maximum energy
- Advances in power electronics and decreased associated cost
- Improved plant operation and efficiency
- Economy of scale due to availability of large wind generation plants
- Accumulated field experience improving the capacity factor
- Computer prototyping by accurate system modeling and simulation

Table 23.2 is for wind sites with average annual wind speed of 7 m/s at 30 m hub height. Since the 1980s, wind technology capital costs have been reduced by 80 % worldwide. Operation and maintenance costs have declined by 80 %, and the availability factor of grid-connected wind plants has increased to 95 %. At present, the capital cost of wind generator plants has dropped to about $600 per kW and the electricity generation cost has reduced to 6 cents per kWh. It is expected that the generation cost will fall below 4 cents per kWh. Keeping this in view, the wind generation is going to be highly competitive with the conventional power plants. In Europe, the United States, and Asia, wind power generation is increasing rapidly, and this trend is going to continue because of the economic viability of wind power.

TABLE 23.2 Wind power technology developments

	1980	1999	Future
Cost per kWh	0.35–0.40	0.05–0.07	0.04
Capital cost per kW	2000–3000	500–700	400
Operating life	5–7 years	20 years	30 years
Capacity factor (average)	15	25–30	30
Availability	50–65	95	95
Wind turbine unit size range	50–150 kW	300–1000 kW	500–2000 kW

The technical advancement in power electronics is playing an important part in the development of wind power technology. The contribution of power electronics to the control of fixed-speed/variable-speed wind turbines and interfacing to the grid is of extreme importance. Because of the fluctuating nature of wind speed, the power quality and reliability of the wind-based power system needs to be evaluated in detail. Appropriate control schemes require power conditioning.

23.3.1 Basics of Wind Power

The ability of a wind turbine to extract power from wind is a function of three main factors:

- Wind power availability
- Power curve of the machine
- Ability of the machine to respond to wind perturbations

The mechanical power produced by a wind turbine is given by

$$P_{\mathrm{m}} = 0.5\rho C_{\mathrm{p}} A U^3 \text{ (watts)}$$

Where tip speed ratio $\lambda = r\omega_A/U$, $\rho =$ air density (kg m^{-3}), $C_{\mathrm{p}} =$ power coefficient, $A =$ wind turbine rotor swept area (m^2), $U =$ wind speed (m/sec). The power from the wind is a cubic function of wind speed. The curve for power coefficient C_{p} and λ is required to infer the value of C_{p} for λ based on wind speed at that time.

The case of a variable-speed wind turbine with a pitch mechanism that alters the effective rotor dynamic efficiency can be easily considered if an appropriate expression for C_{p} as a function of the pitch angle is applied. The power curve of a typical wind turbine is given in Fig. 23.41 as a function of wind speed.

The $C_{\mathrm{p}}-\lambda$ curve for a 150-kW Windmaster machine is given in Fig. 23.42, which has been inferred from the power curve of the machine. The ratio of shaft power to the available power in

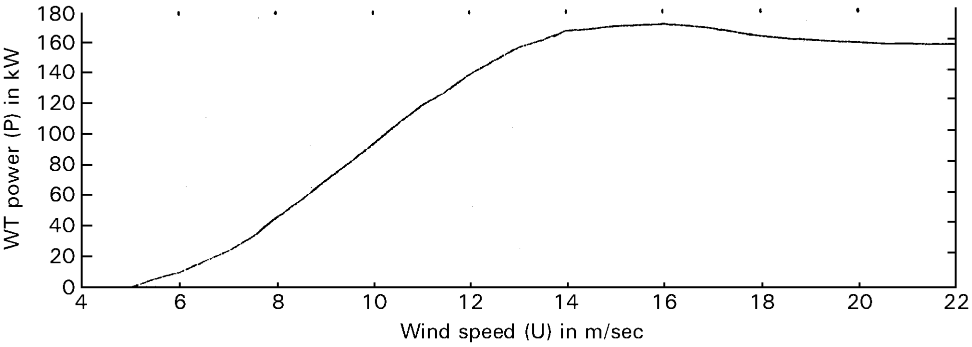


FIGURE 23.41 Power curve of wind turbine as a function of wind speed.

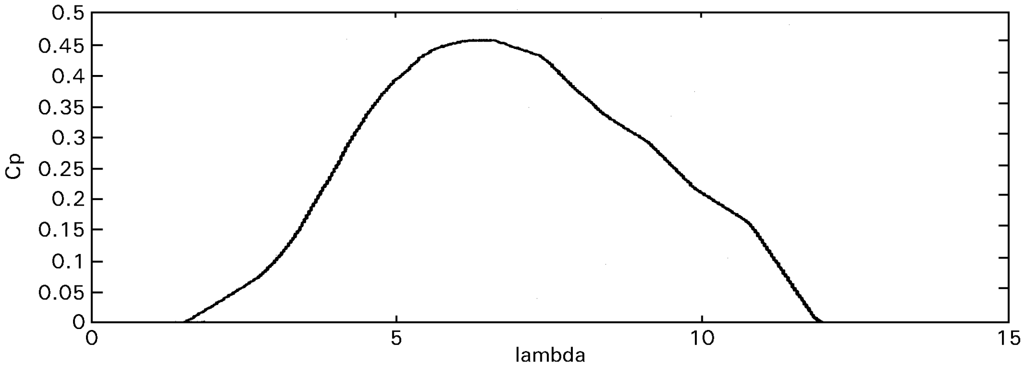


FIGURE 23.42 $C_p - \lambda$ curve of wind machine.

the wind is the efficiency of conversion, known as the power coefficient C_p:

$$C_p = \frac{P_m}{(1/2 \rho A U^3)}$$

The power coefficient is a function of the ratio β of turbine-blade tip speed to wind speed. A tip-speed ratio of 1 means the blade tips are moving at the same speed as the wind, and when β is 2 the tips are moving at twice the speed of the wind and so on [22]. Solidity (σ) is defined as the ratio of the sum of the width of all the blades to the circumference of the rotor. Hence,

$$\sigma = Nd/(2\pi R)$$

where N = number of blades, d = width of the blades.

The power from a wind turbine doubles as the area swept by the blades doubles. But doubling of the wind speed increases the power output eight times. Figure 23.43 gives a family of power curves for a wind turbine. If the loading of the turbine is controlled such that the operating point is along the maximum power locus at different wind speeds, then the wind energy system will be more efficient.

23.3.1.1 Types of ind Turbines

There are two types of wind turbines available:

- Horizontal-axis wind turbines (HAWTs)
- Vertical-axis wind turbines (VAWTs)

The horizontal-axis turbines are generally used. Horizontal-axis wind turbines are, by far, the most common design. A

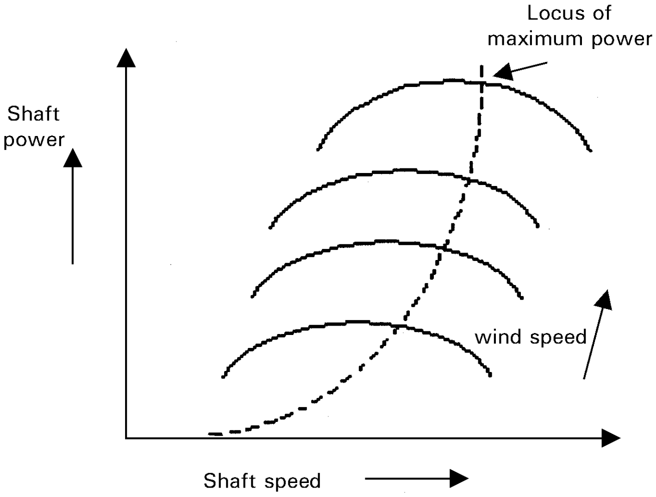


FIGURE 23.43 Shaft power vs shaft speed curves.

large number of designs are commercially available, ranging from 50 W to 1.8 MW. The number of blades ranges from one to many in the familiar agriculture windmill. The best compromise for electricity generation, where high rotational speed allows use of a smaller and cheaper electric generator, is two or three blades. The mechanical and aerodynamic balance is better for a three-bladed rotor. In small wind turbines, three blades are common. Multiblade wind turbines are used for water pumping on farms.

Vertical-axis wind turbines (VAWTs) have an axis of rotation that is vertical, and so, unlike the horizontal wind turbines, they can capture winds from any direction without the need to reposition the rotor when the wind direction changes. The vertical-axis wind turbines have also been used in some applications because they do not depend on the direction of the wind. It is relatively easier to extract power. But there are some disadvantages, such as no self-starting system, smaller power coefficient than obtained in the horizontal-axis wind turbines, strong discontinuation of rotations due to periodic changes in the lift force, and still-unsatisfactory regulation of power.

Based on the pitch control mechanisms, wind turbines can also be classified as fixed-pitch or variable-pitch wind turbines. Different manufacturers offer fixed-pitch and variable-pitch blades. Variable pitch is desirable on large machines because the aerodynamic loads on the blades can be reduced, and when used in fixed-speed operation they can extract more energy. But necessary mechanisms require maintenance, and for small machines, installed in remote areas, fixed pitch seems more desirable. In some machines, power output regulation involves yawing blades so that they no longer point into the wind. One such system designed in Western Australia has a tail that progressively tilts the blades in a vertical plane so that they present a small surface to the wind at high speeds.

23.3.1.2 Types of Wind Generators

The three most common electric generators used for isolated wind-power generation are:

- Dc generators
- Synchronous generators or permanent-magnet synchronous generators
- Asynchronous generators

The dc generator and field-wound alternators have maintenance problems associated with commutators and brush gear. Schemes based on permanent-magnet alternators and induction generators are receiving close attention because of qualities such as ruggedness, low cost, manufacturing simplicity, and low maintenance requirements. Despite many positive features over the conventional synchronous generators, the PMSG has not been used widely [23]. However, the advances in power electronics has made it possible to control the variable-voltage, variable-frequency output of PMSGs. The permanent-magnet machine is generally favored for developing new designs, because of its higher efficiency and the possibility of a somewhat smaller diameter. These PMSG machines are now being used with variable-speed wind machines [24].

In the large power system networks, generally the synchronous generators are used. The synchronous generators can supply both active and reactive power, and their reactive power flow can be controlled. The synchronous generators can operate at any power factor. For an induction generator driven by wind turbines, it is a well-known fact that it can deliver only active power and requires reactive power, although reactive power can be provided from an advanced static var compensator (ASVC).

Squirrel-cage induction generators are widely used with fixed-speed wind turbines. In some applications, wound-rotor induction generators have also been used with adequate control schemes for regulating speed by external rotor resistance. This allows the shape of the torque-slip curve to be controlled to improve the dynamics of the drive train. In the case of PMSG, the converter/inverter can be used to control the variable-voltage–variable-frequency signal of the wind generator at varying wind speed. The converter converts this varying signal to the dc signal, and the output of converter is converted to an ac signal of desired amplitude and frequency.

Induction generators are not locked to the frequency of the network. Cyclic torque fluctuations at the wind turbine can be absorbed by a very small change in the slip speed. In the case of the capacitor-excited induction generators, they obtain the magnetizing current from capacitors connected across their output terminals [25–27].

23.3.2 Types of Wind Power Systems

Wind power systems can be classified as:

- Stand-alone
- Hybrid
- Grid-connected

23.3.3 Stand-Alone Wind Energy Systems

Stand-alone wind energy systems are being used for the following purposes in remote-area power systems:

- Battery charging
- Household power supply

23.3.3.1 Battery Charging with Stand-Alone Wind Energy Systems

The basic elements of a stand-alone wind energy conversion system are:

- Wind generator
- Tower
- Charge control system

- Battery storage
- Distribution network

In a remote-area power supply, an inverter and a diesel generator are more reliable and sophisticated systems. Most small isolated wind energy systems use batteries as a storage device to level out mismatch between the availability of the wind and the load requirement. Batteries are a major cost component in an isolated power system.

23.3.3.2 Wind Turbine Charge Controller

The basic block diagram of a stand-alone wind generator and battery charging system is shown in Fig. 23.44. The function of the charge controller is to feed the power from the wind generator to the battery bank in a controlled manner. In the commonly used permanent-magnet generators, this is usually done by using controlled rectifiers [28]. The controller should be designed to limit the maximum current into the battery, reduce charging current for a high battery state of charge, and maintain a trickle charge during full-state-of-charge periods.

23.3.4 Wind Diesel Hybrid Systems

The details of hybrid systems have been covered in Section 23.2.4. Diesel systems without batteries in a remote area are characterized by poor efficiency and high maintenance and fuel costs. The diesel generators must be operated above a certain minimum load level to reduce cylinder wear and tear due to incomplete combustion. It is a common practice to install dump loads to dissipate extra energy. More efficient systems can be devised by combining the diesel generator with a battery inverter subsystem and incorporating renewable energy sources, such as wind/solar where appropriate. An integrated hybrid energy system incorporating a diesel generator, wind generator, battery or flywheel storage, and inverter will be cost-effective at many sites with an average daily energy demand exceeding 25 kWh [29]. These hybrid energy systems can serve as a minigrid as a part of distributed generation rather than extending the grid to the remote rural areas. The heart of the hybrid system is a high-quality sine-wave inverter, which can also be operated in reverse as a battery charger. The system can cope with loads ranging from zero (inverter-only operation) to approximately three times greater capacity (inverter and diesel operating in parallel).

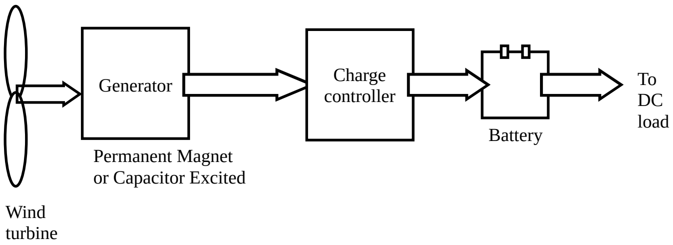


FIGURE 23.44 Block diagram for wind turbine charge controller.

A decentralized form of generation can be beneficial in a remote-area power supply. Because of the high cost of PV systems and the problems associated with storing electricity over longer periods (such as maintenance difficulties and costs), wind turbines can be a viable alternative in hybrid systems. Systems with battery storage, however, provide better reliability. Wind power penetration can be high enough to make a significant impact on the operation of diesel generators.

High wind penetration also poses significant technical problems for the system designer in terms of control and transient stability [30]. In earlier stages of wind–diesel systems, they were installed without assessment of system behavior, because of the lack of design tools/software. With the continual research in this area, there is now software available to assist in this process. Wind–diesel technology has now matured because of research and development in this area. Now there is a need to utilize this knowledge in designing cost-effective and reliable hybrid systems [30]. In Western Australia, dynamic modeling of a wind diesel hybrid system has been developed in Curtin/MUERI, supported by the Australian Cooperative Research Centre for Renewable Energy (ACRE) program 23.5.21.

23.3.5 Grid-Connected Wind Energy Systems

Wind turbines connected to the grid (weak or strong) are discussed here. Wind–diesel systems have received attention in many remote parts of the world. Remote-area power supplies are characterized by low inertia, low damping, and poor reactive power support. Such weak power systems are more susceptible to sudden changes in network operating conditions [31]. In this weak-grid situation, the significant power fluctuations in the grid would lead to reduced quality of supply to users. This may manifest itself as voltage and frequency variations or spikes in the power supply. These weak grid systems need appropriate storage and control systems to smooth out these fluctuations without sacrificing the peak power tracking capability. These systems can have two storage elements. The first is the inertia of rotating mechanical parts, which includes blades, gearbox, and the rotor of the generators. Instead of wind-speed fluctuation causing a large and immediate change in the electrical output of the generator, as in a fixed-speed machine, the fluctuation will cause a change in shaft speed and not create a significant change in generator output. The second energy storage element is the small battery storage between the dc–dc converter and the inverter. The energy in a gust could be stored temporarily in the battery bank and released during a lull in the wind speed, thus reducing the size of fluctuations.

The addition of inverter control would further reduce the fluctuations and increase the total output power. Thus the total output of the wind energy system can be stabilized or smoothed to track the average wind speed and may not show every gust. The system controller should track the peak power to keep the output of the wind energy system constant. It should monitor the stator output and adjust the inverter to smooth the total output. The amount of smoothing would depend on the state of charge of the battery. The nominal total output would be adjusted to keep the battery bank state of charge at a reasonable level. In this way, the total wind energy system will track the long-term variations in the wind speed without having fluctuations caused by the wind. The storage capacity of the battery bank need only be several minutes to smooth out the gusts in the wind, which can be easily handled by the weak grid. In cases where the weak grid is powered by diesel generators, the conventional wind turbine can cause the diesel engines to operate at low capacity. In case of strong wind applications, the fluctuations in the output of the wind energy generator system can be readily absorbed by the grid. The main aim here is to extract the maximum energy from the wind. The basic block layout of such a system [32] is shown in Fig. 23.45.

The function of the dc–dc converter will be to adjust the torque on the machine and hence ensure by measurement of wind speed and shaft speed that the turbine blades are operating so as to extract optimum power. The purpose of the inverter is to feed the energy gathered by the rotor and dc–dc converter, in the process of peak power tracking, to the grid system. The interaction between the two sections would be tightly controlled so as to minimize or eliminate the need for a battery bank. The control must be fast enough that the inverter output power set point matches the output of the dc–dc converter. For a wound rotor induction machine operating over a two-to-one speed range, the maximum power extracted from the rotor is equal to the power rating of the stator. Thus, the rating of the generator from a traditional point of view is only half that of the wind turbine [32]. Since half the power comes from the stator and half from the rotor, the power electronics of the dc–dc converter and inverter need to handle only half the total wind-turbine output, and no battery would be required.

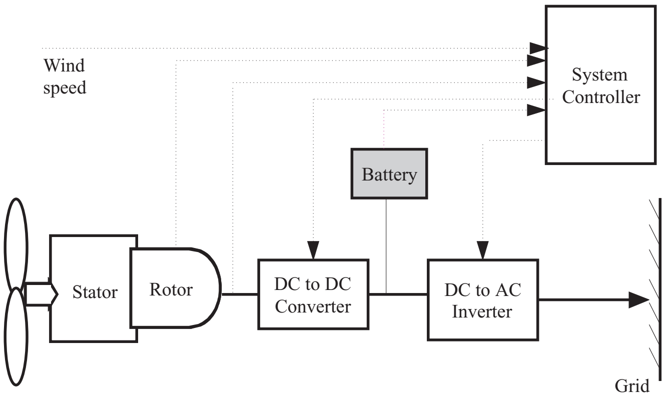


FIGURE 23.45 System block diagram of grid-connected wind energy system.

23.3.5.1 Soft Starters for Induction Generators

When an induction generator is connected to a load, a large inrush current flows. This is something similar to the direct on-line starting problem of induction machines [24]. It has been observed that the initial time constants of an induction machine are higher when it tries to stabilize initially at the normal operating conditions. There is a need to use some type of soft-starting equipment to start the large induction generators. A simple scheme to achieve this is shown in Fig. 23.46. Two thyristors are connected in each phase, back to back. Initially, when the induction generator is connected, the thyristors are used to control the voltage applied to the stator and to limit the large inrush current. As soon as the generator is fully connected, the bypass switch is used to bypass the soft-starter unit.

23.3.6 Control of Wind Turbines

Theory indicates that operation of a wind turbine at fixed tip-speed ratio (C_{pmax}) ensures enhanced energy capture [33]. Wind energy systems must be designed so that above the rated wind speed, the control system limits the turbine output. In normal operation, medium- to large-scale wind turbines are connected to a large grid. Various wind turbine control policies have been studied around the world. Grid-connected wind-turbine generators can be classified as fixed-speed and variable-speed.

23.3.6.1 Fixed-Speed Wind Turbines

In case of a fixed-speed wind turbine, synchronous or squirrel-cage induction generators are employed and are characterized by stiff power-train dynamics. The rotational speed of the wind turbine generator in this case is fixed by the grid frequency. The generator is locked to the grid, thereby permitting only small deviations of the rotor shaft speed from the nominal value. The speed is very responsive to wind-speed fluctuations. The normal method to smooth the surges caused by the wind is to change the turbine aerodynamic characteristics, either passively by stall regulation or actively by blade-pitch regulation. Wind turbines often are subjected to wind

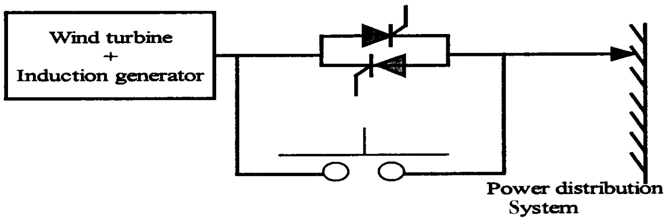


FIGURE 23.46 Soft starting for wind turbine coupled with induction generator.

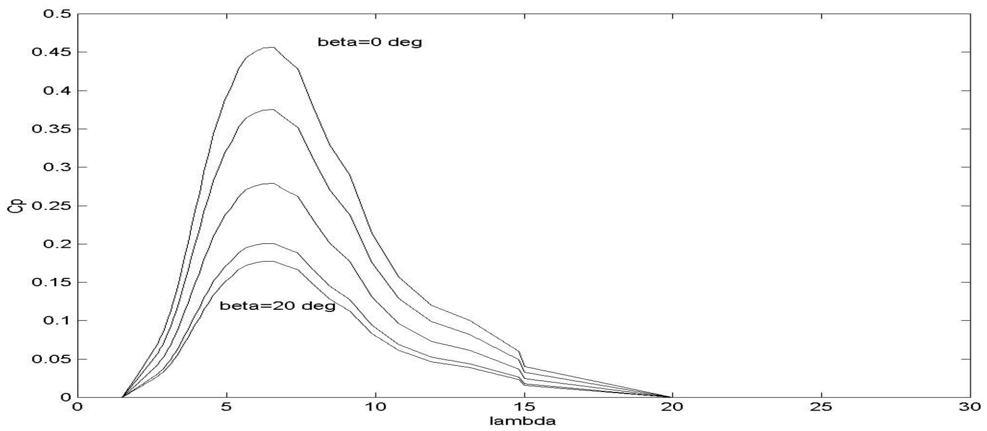


FIGURE 23.47 C_p/λ curves for different pitch settings.

speeds that are very low (below cut-in speed) or high (above rated value). Sometimes they generate below rated power. No pitch regulation is applied when the wind turbine is operating below rated speed, but pitch control is required when the machine is operating above rated wind speed to minimize the stress. Figure 23.47 shows the effect of blade pitch angle on the torque speed curve at a given wind speed.

Blade pitch control is a very effective way of controlling wind turbine speed at high wind speeds, hence limiting the power and torque output of the wind machine. An alternative but cruder control technique is based on airfoil stall [33]. A synchronous link maintaining a fixed turbine speed in combination with an appropriate airfoil can be designed so that, at higher than rated wind speeds, the torque is reduced because of airfoil stall. This method does not require external intervention or complicated hardware, but it captures less energy and has greater blade fatigue.

The aims of variable pitch control of medium- and large-scale wind turbines were to help in startup and shut-down operation, to protect against overspeed, and to limit the load on the wind turbine [34]. The turbine is normally operated between the lower and upper limits of wind speed (typically 4.5 to 26 m/s). When the wind speed is too low or too high, the wind turbine is stopped to reduce wear and damage. The wind turbine must be capable of being started and run up to speed in a safe and controlled manner. The aerodynamic characteristics of some turbines are such that they are not self-starting. The required starting torque may be provided by motoring or by changing the pitch angle of the blade [35]. In the case of grid-connected wind turbine system, the rotational speed of the generator is locked to the frequency of the grid. When the generator is directly run by the rotor, the grid acts as an infinite load. When the grid fails, the load rapidly decreases to zero, causing the turbine rotor to accelerate quickly. Overspeed protection must be provided by rapid braking of the turbine. A simple mechanism of blade pitch-control techniques is shown in Fig. 23.48.

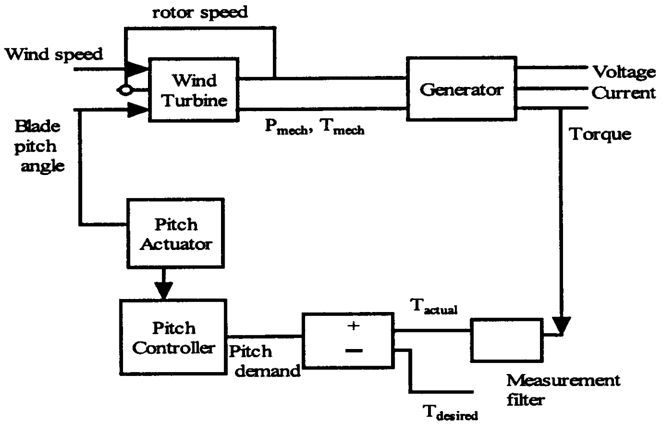


FIGURE 23.48 Pitch-control block diagram.

In this system, the permanent-magnet generator has been used without any gearbox. Direct connection of generator to the wind turbine requires the generator to have a large number of poles. Both induction generators and wound filed synchronous generators of high pole number require a large diameter for efficient operation. Permanent-magnet synchronous generators allow a small pole pitch to be used [36]. The power output, P_{mech}, of any turbine depends mainly on the wind speed, which dictates the rotational speed of the wind turbine rotor. From the wind speed and the rotational speed of the turbine, the tip speed ratio λ is determined. Based on the computed λ, the power coefficient C_p is inferred. In the control strategy just given, the torque output, T_{actual}, of the generator is monitored for a given wind speed and compared with the desired torque, T_{actual}, depending on the load requirement. The generator output torque is passed through the measurement filter. The pitch controller then infers the modified pitch angle based on the torque error. This modified pitch angle demand and computed λ decide the new C_p, resulting in a modified wind generator power and torque output. The controller will keep adjusting the blade pitch angle until the desired power and torque output are achieved.

Some wind-turbine generatora include a gearbox for interfacing the turbine rotor and the generator. The general drive train model [34] for such a system is shown in Fig. 23.49. This system also contains the blade-pitch angle control provision.

The drive train converts the input aerodynamic torque on the rotor into torque on the low-speed shaft. This torque is converted to high-speed shaft torque using the gearbox and fluid coupling. The speed of the wind turbine here is low and the gearbox is required to increase the speed so as to drive the generator at the rated rpm, e.g., 1500 rpm. The fluid coupling works as a velocity-in–torque-out device and transfer the torque [34]. The actuator regulates the tip angle based on the control system applied. The control system here is based on a pitch regulation scheme where the blade-pitch angle is adjusted to obtain the desired output power.

23.3.6.2 Variable-Speed Wind Turbines

Variable-speed, constant-frequency turbine drive trains are not directly coupled to the grid. The power-conditioning device is used to interface the wind generator to the grid. The output of the wind generator can be variable voltage and variable frequency, which is not suitable for grid integration, and appropriate interfacing is required. The wind turbine rotor in this case is permitted to rotate at any wind speed by the power-generating unit.

A number of schemes have been proposed in the past that allow wind turbines to operate with variable rotor speed while feeding the power to a constant frequency grid. Some of the benefits that have been claimed for variable-speed, constant-frequency wind turbine configuration follow [32].

Variable-speed operation results in increased energy capture by maintaining the ratio of blade-tip speed to wind speed near the optimum value. By allowing the wind turbine generator to run at variable speed, the torque can be fixed and the shaft power allowed to increase. This means that the rated power of the machine can be increased with no structural changes.

A variable-speed turbine is capable of absorbing energy in wind gusts as it speeds up and giving back this energy to the system as it slows down. This reduces turbulence-induced stresses and allows capture of a large percentage of the turbulent energy in the wind. More efficient operation can be achieved by avoiding aerodynamic stall over most of the operating range.

Progress in power electronics conversion systems has given a major boost to implementing the concept of variable-speed operation. Research studies have shown that the most significant potential advancement for wind turbine technology is in the area of power-electronic-controlled variable-speed operation. There is much research underway in the United States and Europe on developing variable-speed wind turbines as cost-effectively as possible. In the United States, the NASA MOD-0 and MOD-5B were operated as variable-speed wind turbines [32]. Companies in the United States and Enercon (Germany) made machines incorporate a variable-speed feature. An Enercon variable-speed wind machine is already in operation in Denham, Western Australia.

The ability to operate at varying rotor speed effectively adds compliance to the power-train dynamics of the wind turbine. Although many approaches have been suggested for variable-speed wind turbines, they can be grouped into two main classes: (a) discretely variable speed and (b) continuously variable speed [32, 37].

23.3.6.3 Discretely Variable Speed Systems

The discretely variable speed category includes electrical systems where multiple generators are used, either with different numbers of poles or connected to the wind rotor through different gearing ratios. It also includes those generators that can use different number of poles in the stator or can approximate the effect by appropriate switching. Some of the generators in this category are those with consequent poles, dual winding, or pole amplitude modulation. A brief summary of some of these concepts is presented next.

. . . . ***Pole-Changing Type Induction Generators*** These generators provide two speeds, a factor of two apart, such as four-pole/eight-pole (1500/750 rpm at a supply frequency of 50 Hz or 1800/900 rpm at 60 Hz). They do this by using one-half of the poles at the higher speed. These machines are commercially available and cost about 50 more than the corresponding single-speed machines. Their main disadvantage, in comparison with other discretely variable machines, is

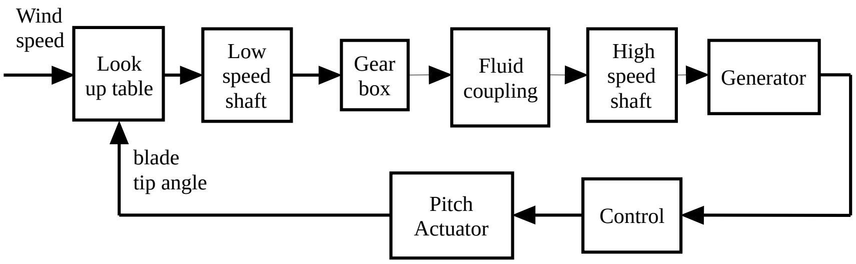


FIGURE 23.49 Block diagram of drive train model.

that the 2-to-1 speed range is wider than the optimum range for a wind turbine [38].

. . . . ***Dual Stator Winding Two Speed Induction Generators*** These machines have two separate stator windings, only one of which is active at a time. Thus, a variety of speed ranges can be obtained depending on the number of poles in each winding. As in the consequent pole machines, only two speeds may be obtained. These machines are significantly heavier than single-speed machines and their efficiency is less, since one winding is always unused, which leads to increased losses. These machines are commercially available. Their cost is approximately twice that of single-speed machines [38].

. . . . ***Multiple Generators*** This configuration is based on the use of a multiple generator design. In one case, there may simply be two separate generators (as used on many European wind turbines). Another possibility is to have two generators on the same shaft, only one of which is electrically connected at a time. The gearing is arranged such that the generators reach synchronous speed at different turbine rotor speeds.

. . . . ***Two-Speed Pole-Amplitude Modulated (PAM) Induction Generator*** This configuration consists of an induction machine with a single stator, which may have two different operating speeds. It differs from conventional generators only in the winding design. Speed is controlled by switching the connections of the six stator leads. The winding is built in two sections that will be in parallel for one speed and in series for the other. The result is the superposition of one alternating frequency on another. This causes the field to have an effectively different number of poles in the two cases, resulting in two different operating speeds. The efficiency of the PAM is comparable to that of a single-speed machine. The cost is approximately twice that of conventional induction generators.

The use of a discretely variable speed generator will result in some of the benefits of continuously variable speed operation, but not all of them. The main effect will be in increased energy productivity, because the wind turbine will be able to operate close to its optimum tip speed ratio over a great range of wind speeds than will a constant speed machine. On the other hand it will perform as a single-speed machine with respect to rapid changes in wind speed (turbulence). Thus it could not be expected to extract the fluctuating energy as effectively from the wind as would the continuously variable speed machine. More importantly, it could not use the inertia of the rotor to absorb torque spikes. Thus, this approach would not result in improved fatigue life of the machine and it could not be an integral part of an optimized design such as one using yaw/speed control or pitch/speed control.

23.3.6.4 Continuously Variable Speed Systems

The second main class of systems for variable-speed operation are those that allow the speed to be varied continuously. For the continuously variable speed wind turbine, there may be more than one control, depending on the desired control action:

- Mechanical control
- Combination of electrical/mechanical
- Electrical
- Electrical/power electronics control

The mechanical methods include hydraulic and variable ratio transmissions. An example of an electrical/mechanical system is one in which the stator of the generator is allowed to rotate. The all-electrical category includes high-slip induction generators and the tandem generator. The power electronic category contains a number of possible options. One option is to use a synchronous generator or a wound rotor induction generator, although a conventional induction generator may also be used. The power electronics is used to condition some or all of the power to a form appropriate to the grid. The power electronics may also be used to rectify some or all of the power from the generator, to control the rotational speed of the generator, or to supply reactive power. These systems are discussed below.

. . . . ***Mechanical Systems***

Variable-Speed Hydraulic Transmission One method of generating electrical power at a fixed frequency, while allowing the rotor to turn at variable speed, is the use of a variable-speed hydraulic transmission. In this configuration, a hydraulic system is used in the transfer of the power from the top of the tower to ground level (assuming a horizontal-axis wind turbine). A fixed-displacement hydraulic pump is connected directly to the turbine (or possibly gearbox) shaft. The hydraulic fluid is fed to and from the nacelle via a rotary fluid coupling. At the base of the tower is a variable-displacement hydraulic motor, which is governed to run at constant speed and drive a standard generator.

One advantage of this concept is that the electrical equipment can be placed at ground level, making the rest of the machine simpler. For smaller machines, it may be possible to dispense with a gearbox altogether. On the other hand, there are a number of problems using hydraulic transmissions in wind turbines. For one thing, pumps and motors of the size needed in wind turbines of greater than about 200 kW are not readily available. Multiples of smaller units are possible, but this would complicate the design. The life expectancy of many of the parts, especially seals, may well be less than 5 years. Leakage of hydraulic fluid can be a significant problem, necessitating frequent maintenance. Losses in the hydraulics could also make the overall system less efficient than conventional electric generation. Experience over many years has not shown great success with wind machines using hydraulic transmissions.

Variable-Ratio Transmission A variable-ratio transmission (VRT) is one in which the gear ratio may be varied continuously within a given range. One type of VRT suggested for wind turbines is using belts and pulleys, such as are used in some industrial drives [32, 39]. These have the advantage of being able to drive a conventional fixed-speed generator, while being driven by a variable-speed turbine rotor. On the other hand, they do not appear to be commercially available in larger sizes, and those that do exist have relatively high losses.

. . . . Electrical/Mechanical Variable Speed Systems

Rotating Stator Induction Generator This system uses a conventional squirrel-cage induction generator whose shaft is driven by a wind turbine through a gearbox [33, 40]. However, the stator is mounted to a support, which allows bidirectional rotation. This support is in turn driven by a dc machine. The armature of the dc machine is fed from a bidirectional inverter, which is connected to the fixed-frequency ac grid. If the stator support allowed to turn in the same direction as the wind turbine, the turbine will turn faster. Some of the power from the wind turbine will be absorbed by the induction generator stator and fed to the grid through the inverter. Conversely, the wind turbine will turn more slowly when the stator support is driven in the opposite direction. The amount of current (and thus the torque) delivered to or from the dc machine is determined by a closed-loop control circuit whose feedback signal is driven by a tachometer mounted on the shaft of the dc machine.

One of the problems with this system is that the stator slip rings and brushes must be sized to take the full power of the generator. They would be subjected to wear and would require maintenance. The dc machine also adds to cost, complexity, and maintenance.

. . . . Electrical Variable-Speed Systems

High-Slip Induction Generator This is the simplest variable-speed system, which is accomplished by having a relatively large amount of resistance in the rotor of an induction generator. However, the losses increase with increased rotor resistance. Westwind Turbines in Australia investigated such a scheme on a 30-kW machine in 1989.

Tandem Induction Generator A tandem induction generator consists of an induction machine fitted with two magnetically independent stators, one fixed in position and the other able to be rotated, and a single squirrel-cage rotor whose bars extend the length of both stators [32, 41]. Torque control is achieved by physical adjustment of the angular displacement between the two stators, which causes a phase shift between the induced rotor voltages.

. . . . Electrical/Power Electronics The general configuration, shown in Fig. 23.50, consists of the following components:

- Wind generator
- Converter
- Inverter

The generator may be dc, synchronous (wound-rotor or permanent-magnet type), squirrel-cage, wound-rotor, or brushless doubly fed induction generator. The input converter is used to convert the variable-voltage, variable-frequency voltage to the dc voltage. This dc voltage is converted into ac of constant voltage and frequency of desired amplitude. The inverter will also be used to control the active/reactive power flow from the inverter. In the case of a dc generator, the converter may not be required or when a cycloconverter is used to convert the ac directly from one frequency to another.

23.3.6.5 Generator Options for Variable-Speed Wind Turbines using Power Electronics

Power electronics may be applied to three types of generators to facilitate variable-speed operation:

- Synchronous generators
- Squirrel-cage induction generators
- Wound-rotor induction generators

. . . . Synchronous Generator In this configuration, the synchronous generator is allowed to run at variable speed, producing power of variable voltage and frequency. Control

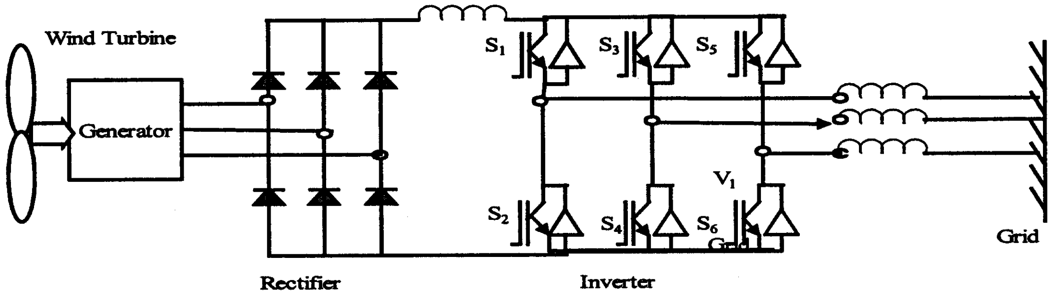


FIGURE 23.50 Grid-connected wind energy system through dc/ac converter.

may be facilitated by adjusting an externally supplied field current. The most common type of power conversion uses a bridge rectifier (controlled/uncontrolled), a dc link, and inverter as shown in Fig. 23.50. The disadvantages of this configuration include the relatively high cost and maintenance requirements of synchronous generators and the need for the power conversion system to take the full power generated (as opposed to the wound-rotor system).

. . . . *Squirrel-Cage Induction Generator* Possible architectures for systems using conventional induction generators that have a solid squirrel-cage rotor have many similarities to those with synchronous generators. The main difference is that the induction generator is not inherently self-exciting and it needs a source of reactive power. This could be done by a generator-side self-commutated converter operating in the rectifier mode. A significant advantage of this configuration is the low cost and low maintenance requirements of induction generators. Another advantage of using the self-commutated double converter is that it can be on the ground, completely separate from the wind machine. If there is a problem in the converter, it could be switched out of the circuit for repair and the wind machine could continue to run at constant speed. The main disadvantage with this configuration is that, as with the synchronous generator, the power conversion system would have to take the full power generated and could be relatively costly compared to some other configurations. There would also be additional complexities associated with the supply of reactive power to the generator.

. . . . *Wound-Rotor Induction Generator* A wound-rotor induction rotor has three-phase winding on the rotor, accessible to the outside via slip rings. The possible methods of accessing the rotor can have the following configurations:

- Slip power recovery
- Use of cycloconverter
- Rotor resistance chopper control

Slip Power Recovery (Static Kramer System) The slip power recovery configuration behaves similarly to a conventional induction generator with very large slip, but in addition energy is recovered from the rotor. The rotor power is first carried out through slip rings, then rectified and passed through a dc link to a line-commutated inverter and into the grid. The rest of the power comes directly from the stator as it normally does. A disadvantage with this system is that it can only allow supersynchronous variable-speed operation. Its possible use in wind power was reported by Smith and Nigim [42].

In this scheme (as shown in Fig. 23.51), the stator is directly connected to the grid. The power converter has been connected to the rotor of the wound-rotor induction generator to obtain the optimum power from the variable-speed wind turbine. The main advantage of this scheme is that the power conditioning unit has to handle only a fraction of the total power so as to obtain full control of the generator. This is very important when wind turbine sizes are increasing for grid-connected applications for higher penetration of wind energy, and a smaller converter can be used in this scheme.

Cycloconverter (Static Scherbius System) A cycloconverter is a converter that converts ac voltage of one frequency to another frequency without an intermediate dc link. When a cycloconverter is connected to the rotor circuit, sub- and supersynchronous operation variable-speed operation is possible. In supersynchronous operation, this configuration is similar to slip power recovery. In addition, energy may be fed into the rotor, thus allowing the machine to generate at subsynchronous speeds. For that reason, the generator is said to be doubly fed [43]. This system has a limited ability to control reactive power at the terminals of the generator, although as a whole it is a net consumer of reactive power. On the other hand, if coupled with capacitor excitation, this capability could be useful from the utility point of view. Because of its ability to rapidly adjust phase angle and magnitude of the terminal voltage, the generator can be resynchronized after a major electrical disturbance without going through a complete stop/start sequence. With some wind turbines, this could be a useful feature.

Rotor Resistance Chopper Control A fairly simple scheme for extracting rotor power in the form of heat has been proposed in [44].

23.3.6.6 Isolated Grid Supply System with Multiple Wind Turbines

An isolated grid supply system with a wind park is shown in Fig. 23.52. Two or more wind turbines can be connected to this system. A diesel generator can be connected in parallel. The converter-connected wind generators will work in parallel and the supervisory control block will control the output of these wind generators in conjunction with the diesel generator. This type of decentralized generation can be a better option where high penetration of wind generation is sought. The individual converter will control the voltage and frequency of the system. The supervisory control system will play an

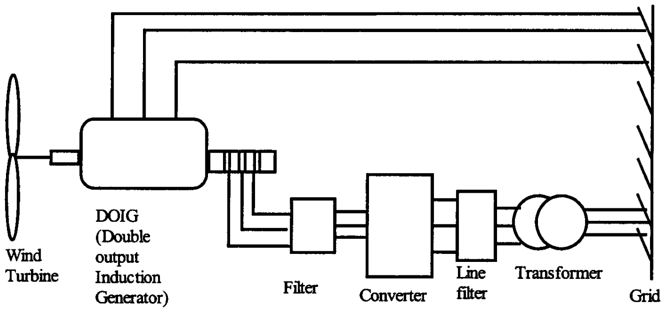


FIGURE 23.51 Schematic diagram of doubly fed induction generator.

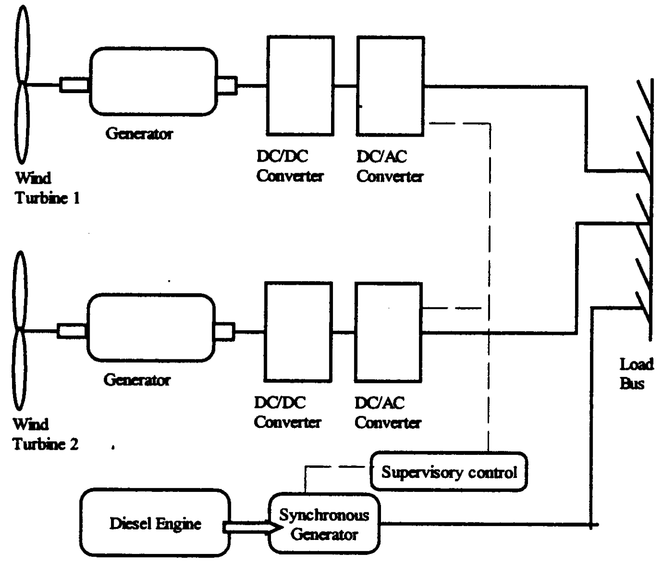


FIGURE 23.52 Schematic diagram of isolated grid system having a wind park.

important part in coordination between multiple power generation systems in a remote-area power supply having weak grid.

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24

DC Transmission

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24.1 Introduction

High-voltage direct current (HVDC) transmission [1–3] is a major user of power electronics technology. HVDC technology first made its mark in the early undersea cable interconnections of Gotland (1954) and Sardinia (1967), and then in long-distance transmission with the Pacific Intertie (1970) and Nelson River (1973) schemes using mercury-arc valves. A significant milestone development occurred in 1972 with the first back-to-back (BB) asynchronous interconnection at Eel River between Quebec and New Brunswick; this installation also marked the introduction of thyristor valves to the technology and replaced the earlier mercury-arc valves.

To understand the rapid growth of dc transmission (Table 24.1) [4] in the past 50 years, it is first necessary to compare it to conventional ac transmission.

24.1.1 Comparison of ac and dc Transmission

Making a planning selection between ac and dc transmission is based on an evaluation of transmission costs, technical considerations, and the reliability/availability offered by the two transmission alternatives.

24.1.1.1 Evaluation of Transmission Costs

The cost of a transmission line comprises the capital investment required for the actual infrastructure [i.e., right-of-way (RoW), towers, conductors, insulators, and terminal equipment] and costs incurred for operational requirements (i.e. losses). Assuming similar insulation requirements for peak voltage levels for both ac and dc lines, a dc line can carry as much power with two conductors (having positive/negative polarities with respect to ground) as an ac line with three

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TABLE 24.1 Listing of HVDC installations

	HVDC Supplier[a]	Year Comm.	Rating (MW)	Dc Voltage (kV)	Line and/or Cable (km)	Location
Gotland I[b]	A	1954	20	±100	96	Sweden
English Channel	A	1961	160	±100	64	England–France
Volgograd–Donbass[c]		1965	720	±400	470	Russia
Inter-Island	A	1965	600	±250	609	New Zealand
Konti–Skan I	A	1965	250	250	180	Denmark–Sweden
Sakuma	A	1965	300	2 × 125	B-B[e]	Japan
Sardinia	I	1967	200	200	413	Italy
Vancouver I	A	1968	312	260	69	Canada
Pacific Intertie	JV	1970	1440	±400	1362	U.S.A.
		1982	1600			
Nelson River I[d]	I	1972	1620	±450	892	Canada
Kingsnorth	I	1975	640	±260	82	England
Gotland	A	1970	30	±150	96	Sweden
Eel River	C	1972	320	2 × 80	B-B	Canada
Skagerrak I	A	1976	250	250	240	Norway–Denmark
Skagerrak II	A	1977	500	±250		Norway–Denmark
Skagerrak III	A	1993 est	440	350	240	Norway–Denmark
Vancouver II	C	1977	370	−280	77	Canada
Shin–Shinano	D	1977	300	2 × 125		Japan
		1992 est	600	3 × 125	B-B	
Square Butte	C	1977	500	±250	749	U.S.A.
David A. Hamil	C	1977	100	50	B-B	U.S.A.
Cahora Bassa	J	1978	1920	±533	1360	Mozambique–S. Africa
Nelson River II	J	1978	900	±250	930	Canada
		1985	1800	±500		
CU	A	1979	1000	±400	710	U.S.A.
Hokkaido–Honshu	E	1979	150	125	168	Japan
	E	1980	300	250		
		1993 est	600	±250		
Acaray	G	1981	50	25.6	B-B	Paraguay
Vyborg	F	1981	355	1 × 170(±85)	B-B	Russia–Finland
	F	1982	710	2 × 170		
			1065	3 × 170		
Duernrohr	J	1983	550	145	B-B	Austria
Gotland II	A	1983	130	150	100	Sweden
Gotland III	A	1987	260	±150	103	Sweden
Eddy County	C	1983	200	82	B-B	U.S.A.
Chateauguay	J	1984	1000	2 × 140	B-B	Canada
Oklaunion	C	1984	200	82	B-B	U.S.A.
Itaipu	A	1984	1575	±300	785	Brazil
	A	1985	2383			
	A	1986	3150	±600		
Inga-Shaba	A	1982	560	±500	1700	Zaire
Pac Intertie upgrade	A	1984	2000	±500	1362	U.S.A.
Blackwater	B	1985	200	57	B-B	U.S.A.
Highgate	A	1985	200	±56	B-B	U.S.A.
Madawaska	C	1985	350	140	B-B	Canada
Miles City	C	1985	200	±82	B-B	U.S.A.
Broken Hill	A	1986	40	2 × 17(±8.33)	B-B	Australia
Intermountain	A	1986	1920	±500	784	U.S.A.
Cross-Channel						
(Les Mandarins)	H	1986	1000	±270	72	France–
(Sellindge)	I	1986	2000	2 × ±270		England
DesCantons–Comerford	C	1986	690	±450	172	Canada–U.S.A.
Sacoi[f]	H	1986	200	200	415	Corsica Island
[g]		1992 est	300			Italy
Itaipu II	A	1987	3150	±600	805	Brazil
Sidney (Virginia Smith)	G	1988	200	55.5	B-B	U.S.A.
Gezhouba–Shanghai	B + G	1989	600	500	1000	China
		1990	1200	±500		
Konti-Skan II	A	1988	300	285	150	Sweden–Denmark

	HVDC Supplier[a]	Year Comm.	Rating (MW)	Dc Voltage (kV)	Line and/or Cable (km)	Location
Vindhyachal	A	1989	500	2 × 69.7	B-B	India
Pac Intertie expansion	B	1989	1100	±500	1362	U.S.A.
Mcneill	I	1989	150	42	B-B	Canada
Fenno-Skan	A	1989	500	400	200	Finland–Sweden
Sileru–Barsoor	K	1989	100	+100	196	India
			200	+200		
			400	±200		
Rihand–Delhi	A	1991	750	+500	910	India
		1991	1500	±500		
HydroQuebec–New Eng.	A	1990	2000[h]	±450	1500	Canada–U.S.A.
Nicolet tap	A	1992	3000			Canada
Welch–Monticello		1995 est	600		B-B	U.S.A.
Etzenricht	G	1993 est	600	160	B-B	Germany–Czech Republic
Vienna South-East	G	1993 est	550	145	B-B	Austria–Hungary
DC Hybrid Link	AB	1992 est	992	+270/ − 350	617	New Zealand
Chandrapur–Padghe		1997 est	1500	±500	900	India
Chandrapur–Ramagundum		1996 est	1000	2 × 205	B-B	India
Gazuwaka–Jeypore		1997 est	500		B-B	India
Leyte–Luzun		1997 est	1600	400	440	Philippines
Haenam–Cheju	I	1993 est	300	±180	100	South Korea
Baltic Cable Project	AB	1994 est	600	450		Sweden–Germany
Victoria–Tasmania			300	300		Australia
Kontek HVDC Intercon.		1995 est	600	400		Denmark
Scotland–N. Ireland		1996 est	250	250		United Kingdom
Greece–Italy		1997 est	500			Italy
Tsq–Beijao		1997 est	1800	500	903	China
Iceland–Scotland link			2000		950	
Sarawak–Malaysia			1600		620	

[a] A, ASEA; B, Brown Boveri; C, General Electric; D, Toshiba; E, Hitachi; F, Russian; G, Siemens; H, CGEE Alsthom; I, GEC (Former Eng. Elec.); J, HVDC W.G. (AEG, BBC, Siemens); K, Independent; AB, ABB Brown Boveri; JV, Joint Venture (GE and ASEA).

[b] Retired from service.

[c] 2 V.G.s replaced with thyristors in 1977.

[d] 2 V.G.s in Pole 1 replaced with thyristors by GEC in 1991.

[e] Back-to-back HVDC system.

[f] 50 MW thyristor tap.

[g] Up-rated w/thyristor valves.

conductors of the same size. Therefore, for a given power level, a dc line requires smaller RoW, simpler and cheaper towers, and reduced conductor and insulator costs. As an example, Fig. 24.1 shows the comparative case of ac and dc systems carrying 2000 MW.

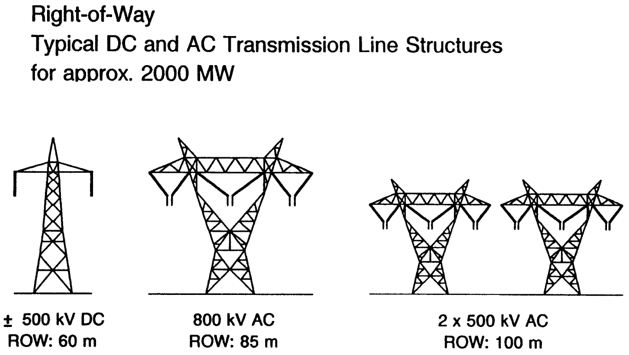


FIGURE 24.1 Comparison of RoW for ac and dc transmission systems.

With the dc option, since there are only two conductors (with the same current capacity as three ac conductors), the power transmission losses are also reduced to about two-thirds of those of the comparable ac system. The absence of skin effect with dc is also beneficial in reducing power losses marginally, and the dielectric losses in the case of power cables are also very much less for dc transmission.

Corona effects tend to be less significant for dc than for ac conductors. The other factors that influence line costs are the costs of compensation and terminal equipment. Dc lines do not require reactive power compensation but the terminal equipment costs are increased because of the presence of converters and filters.

Figure 24.2 shows the variation of costs of transmission with distance for ac and dc transmission. Ac tends to be more economical than dc for distances less than the "breakeven distance" but is more expensive for longer distances. The breakeven distances can vary from 500 to 800 km in overhead lines depending on the per-unit line costs. With a cable system, this breakeven distance approaches 50 km.

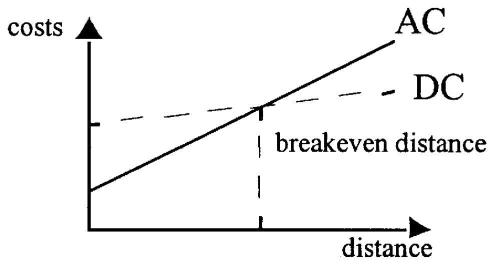


FIGURE 24.2 Comparison of ac–dc lines.

24.1.1.2 Evaluation of Technical Considerations

Because of its fast controllability, dc transmission has full control over transmitted power and the ability to enhance transient and dynamic stability in associated ac networks. It can also limit fault currents in the dc lines. Furthermore, dc transmission overcomes some of the following problems associated with ac transmission.

. . . . ***Stability Limits*** The power transfer in an ac line is dependent on the angle difference between the voltage phasors at the two line ends. For a given power transfer level, this angle increases with distance. The maximum power transfer is limited by the considerations of steady-state and transient stability. The power-carrying capability of an ac line is inversely proportional to transmission distance, whereas the power-carrying ability of dc lines is unaffected by the distance of transmission.

. . . . ***Voltage Control*** Voltage control in ac lines is complicated by line charging and voltage drops. The voltage profile in an ac line is relatively flat only for a fixed level of power transfer corresponding to its surge impedance loading (SIL). The voltage profile varies with the line loading. For constant voltage at the line ends, the midpoint voltage is reduced for line loadings higher than SIL and increased for loadings less than SIL.

The maintenance of constant voltage at the two ends requires reactive power control as the line loading is increased. The reactive power requirements increase with line length.

Although dc converter stations require reactive power related to the power transmitted, the dc line itself does not require any reactive power.

The steady-state charging currents in ac cables pose serious problems and make the breakeven distance for cable transmission around 50 km.

. . . . ***Line Compensation*** Line compensation is necessary for long-distance ac transmission to overcome the problems of line charging and stability limitations. An increase in power transfer and voltage control is possible through the use of shunt inductors, series capacitors, static var compensators (SVCs) and, lately, the new-generation static compensators (STATCOMs). In the case of dc lines, such compensation is not needed.

. . . . ***Problems of ac Interconnection*** The interconnection of two power systems through ac ties requires the automatic generation controllers of both systems to be coordinated using tie line power and frequency signals. Even with coordinated control of interconnected systems, the operation of ac ties can be problematic because of (i) the presence of large power oscillations that can lead to frequent tripping, (ii) an increase in fault level, and (iii) transmission of disturbances from one system to the other.

The fast controllability of power flow in dc lines eliminates all of the above problems. Furthermore, the asynchronous interconnection of two power systems can only be achieved with the use of dc links.

. . . . ***Ground Impedance*** In ac transmission, the existence of ground (zero sequence) current cannot be permitted in steady state because of the high magnitude of ground impedance, which will not only affect efficient power transfer, but also result in telephonic interference.

The ground impedance is negligible for dc currents, and a dc link can operate using one conductor with ground return (monopolar operation). The ground return is objectionable only when buried metallic structures (such as pipes) are present and are subject to corrosion with dc current flow. It is to be noted that even while operating in the monopolar mode, the ac network feeding the dc converter station operates with balanced voltages and currents. Hence, single-pole operation of dc transmission systems is possible for an extended period, whereas in ac transmission, single-phase operation (or any unbalanced operation) is not feasible for more than a second.

. . . . ***Problems of dc Transmission*** The application of dc transmission is limited by factors such as the following:

1. High cost of conversion equipment
2. Inability to use transformers to alter voltage levels
3. Generation of harmonics
4. Requirement of reactive power
5. Complexity of controls

Over the years, there have been significant advances in dc technology, which have tried to overcome the disadvantages just listed above, except for item 2. These are:

1. Increase in the ratings of a thyristor cell that makes up a valve
2. Modular construction of thyristor valves
3. Twelve-pulse operation of converters
4. Use of force-commutation
5. Application of digital electronics and fiber optics in the control of converters

Some of the preceding advances have resulted in improving the reliability and reduction of conversion costs in dc systems.

24.1.2 Evaluation of Reliability and Availability Costs

Statistics on the reliability of HVDC links are maintained by CIGRE and IEEE Working Groups. The reliability of dc links has been very good and is comparable with that of ac systems. The availability of dc links is quoted in the upper 90%.

24.1.3 Applications of dc Transmission

Because of their costs and special nature, most applications of dc transmission generally fall into one of the following four categories:

Underground or underwater cables. In the case of long cable connections over the breakeven distance of about 40–50 km, the dc cable transmission system has a marked advantage over ac cable connections. Examples of this type of application were the Gotland (1954) and Sardinia (1967) schemes.

The recent development of voltage-source converters (VSC) and the use of rugged polymer dc cables, with the so-called "HVDC Light" option, is being increasingly considered. An example of this type of application is the 180-MW Directlink connection (2000) in Australia.

Long-distance bulk power transmission. Bulk power transmission over long distances is an application ideally suited for dc transmission and is more economical than ac transmission whenever the breakeven distance is exceeded. Examples of this type of application abound from the earlier Pacific Intertie to the recent links in China and India.

The breakeven distance is being effectively decreased by the reduced cost of new compact converter stations made possible by the recent advances in power electronics (discussed in a later section).

Asynchronous interconnection of ac systems. In terms of an asynchronous interconnection between two ac systems, the dc option reigns supreme. There are many instances of BB connections where two ac networks have been tied together for the overall advantage to both ac systems. With recent advances in control techniques, these interconnections are being increasingly made at weak ac systems. The growth of BB interconnections is best illustrated with the example of North America, where the four main independent power systems are interconnected with 12 BB links.

In the future, it is anticipated that these BB connections will also be made with VSCs offering the possibility of full four-quadrant operation and the total control of active/reactive power coupled with the minimal generation of harmonics.

Stabilization of power flows in integrated power systems. In large interconnected systems, power flow in ac ties (particularly under disturbance conditions) can be uncontrolled and lead to overloads and stability problems, thus endangering system security. Strategically placed dc lines can overcome this problem because of the fast controllability of dc power and provide much needed damping and timely overload capability. The planning of dc transmission in such applications requires detailed study to evaluate the benefits. Examples are the IPP link in the United States and the Chandrapur–Padghe link in India.

Presently the number of dc lines in a power grid is very small compared to the number of ac lines. This indicates that dc transmission is justified only for specific applications. Although advances in technology and introduction of multiterminal dc (MTDC) systems are expected to increase the scope of application of dc transmission, it is not anticipated that a dc power grid will replace the ac grid in the future. There are two major reasons for this. First, the control and protection of MTDC systems is complex and the inability of voltage transformation in dc networks imposes economic penalties. Second, the advances in power electronics technology have resulted in the improvement of the performance of ac transmissions using FACTS devices, for instance through introduction of static var systems and static phase shifters.

24.1.4 Types of HVDC Systems

Three types of dc links are considered in HVDC applications.

24.1.4.1 Monopolar Link

A monopolar link (Fig. 24.3a) has one conductor and uses either ground and/or sea return. A metallic return can also be used where concerns for harmonic interference and/or corrosion exist. In applications with dc cables (i.e., HVDC Light), a cable return is used. Since the corona effects in a dc line are substantially less with negative polarity of the conductor as compared to positive polarity, a monopolar link is normally operated with negative polarity.

24.1.4.2 Bipolar Link

A bipolar link (Fig. 24.3b) has two conductors, one positive and the other negative. Each terminal has two sets of converters of equal rating, in series on the dc side. The junction between the two sets of converters is grounded at one or both ends by the use of a short electrode line. Since both poles operate with equal currents under normal operation, there is zero ground current flowing under these conditions. Monopolar operation can also be used in the first stages of the development of a bipolar link. Alternatively, under faulty converter conditions, one dc line may be temporarily used as a metallic return with the use of suitable switching.

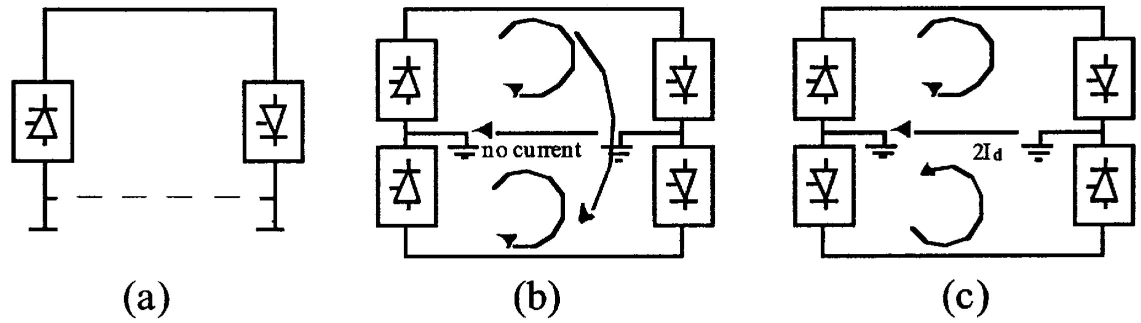


FIGURE 24.3 Types of HVDC links: (a) monopolar link, (b) bipolar link, and (c) homopolar dc link.

24.1.4.3 omopolar Link

In this type of link (Fig. 24.3c) two conductors having the same polarity (usually negative) can be operated with ground or metallic return.

Because of the undesirability of operating a dc link with ground return, bipolar links are mostly used. A homopolar link has the advantage of reduced insulation costs, but the disadvantages of earth return outweigh the advantages.

24.2 Main Components of VDC Converter Station

The major components of an HVDC transmission system are the converter stations at the ends of the transmission system. In a typical two-terminal transmission system, both a rectifier and an inverter are required. The role of the two stations can be reversed, as controls are usually available for both functions at the terminals. The major components of a typical 12-pulse bipolar HVDC converter station (Fig. 24.4) are discussed next.

24.2.1 Converter Unit

This usually consists of two three-phase converter bridges connected in series to form a 12-pulse converter unit. The design of valves is based on a modular concept where each module contains a limited number of series-connected thyristor levels. The valves can be packaged as a single-valve, double-valve, or quadruple-valve arrangement. Converter transformers connected in star/star and star/delta arrangements to form a 12-pulse pair feed the converter.

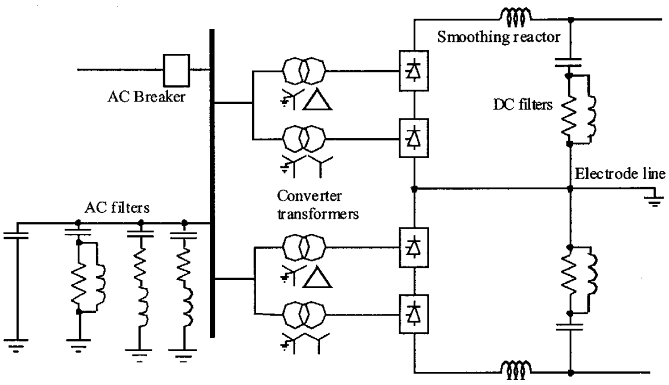


FIGURE 24.4 Typical HVDC converter station equipment.

Air, oil, water or Freon may be used to cool the valves. However, cooling using deionized water is more modern and considered efficient and reliable. The ratings of a valve group are limited more by the permissible short-circuit currents than by the steady-state load requirements. Valve firing signals are generated in the converter control at ground potential and are transmitted to each thyristor in the valve through a fiber-optic light-guide system. The light signal received at the thyristor level is converted to an electrical signal using gate-drive amplifiers with pulse transformers. Recent trends in the industry indicate that direct optical firing of the valves with LTT thyristors is also feasible.

The valves are protected using snubber circuits, protective firing, and gapless surge arrestors.

24.2.1.1 Thyristor Valves

Many individual thyristors are connected in series to build up an HVDC valve. To distribute the off-state valve voltage uniformly across each thyristor level and protect the valve from di/dt and dv/dt stresses, special snubber circuits are used across each thyristor level (Fig. 24.5).

The snubber circuit is composed of the following components:

- A saturating reactor is used to protect the valve from di/dt stresses during turn-on. The saturating reactor offers a high inductance at low current and a low inductance at high currents.
- A dc grading resistor RG distributes the direct voltage across the different thyristor levels. It is also used as a voltage divider to measure the thyristor level voltage.
- RC snubber circuits are used to damp out voltage oscillations varying from power frequency to a few kilohertz.

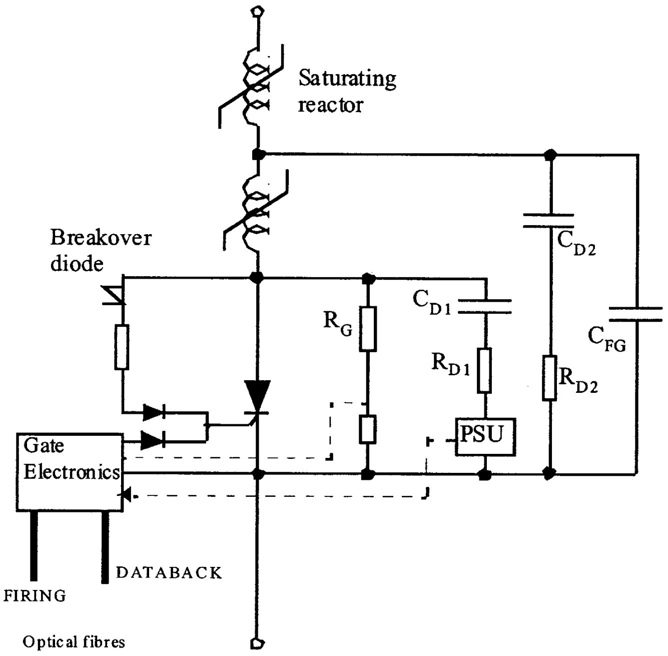


FIGURE 24.5 Electrical circuit of the thyristor level [2].

- A capacitive grading circuit C_{FG} is used to protect the thyristor level from voltage oscillations at a much higher frequency.

A firing pulse sent via a fiber-optic cable from the valve base electronics (VBE) unit at earth potential triggers a thyristor on. A gate electronic unit (GEU), which receives its power from the RC snubber circuit during the valve's off period, amplifies the fiber-optic signal. The GEU can also effect the protective firing of the thyristor independent of the central control unit. This is achieved by a breakover diode (BOD) via a current-limiting resistor that triggers the thyristor when the forward voltage threatens to exceed the rated voltage for the thyristor. This may arise in a case when some thyristors may block forward voltage while others may not.

It is normal to include some extra redundant thyristor levels to allow the valve to remain in service after the failure of some thyristors. A metal-oxide surge arrestor is also used across each valve for overvoltage protection.

The thyristors produce considerable heat loss, typically 30 to 40 W/cm^2 (or over 1 MW for a typical quadruple valve), and so an efficient cooling system is essential.

24.2.2 Converter Transformer

The converter transformer (Fig. 24.6) can have different configurations: (i) three-phase, two-winding, (ii) single-phase, three-winding, and (iii) single-phase, two-winding. The valve-side windings are connected in star and delta with neutral point ungrounded. On the ac side, the transformers are connected in parallel with the neutral grounded. The leakage impedance of the transformer (typical values vary between 15 and 18) is chosen to limit the short-circuit current through any valve.

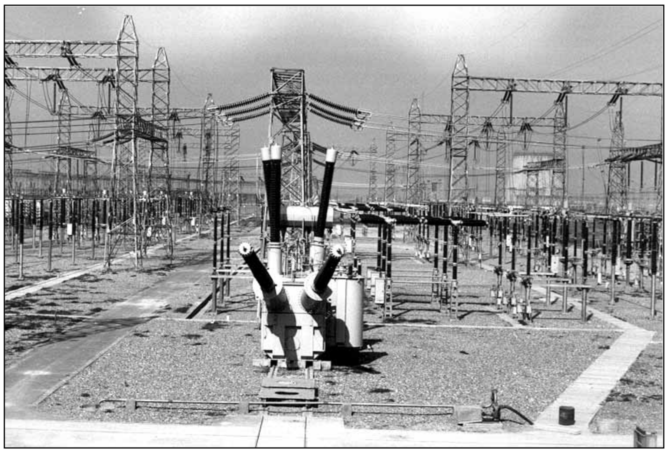


FIGURE 24.6 Spare converter transformer in the switchyard of an HVDC station.

The converter transformers are designed to withstand dc voltage stresses and increased eddy-current losses due to harmonic currents. One problem that can arise is due to the dc magnetization of the core due to unsymmetrical firing of valves.

24.2.3 Filters

Because of the generation of characteristic and noncharacteristic harmonics by the converter, it is necessary to provide suitable filters on the ac–dc sides of the converter to improve the power quality and meet telephonic and other requirements. Generally, three types of filters are used for this purpose: ac, dc, and high-frequency (RF/PLC) filters.

24.2.3.1 AC Filters

AC filters (Fig. 24.7) are passive circuits used to provide low-impedance shunt paths for ac harmonic currents. Both tuned and damped filter arrangements are used. In a typical 12-pulse station, filters at the 11th and 13th harmonics are required as tuned filters. Damped filters (normally tuned to the 23rd harmonic) are required for the higher harmonics. In recent years, filters such as C-type filters have also been used since they provide more economic designs. Double- or even triple-tuned filters exist to reduce the cost of the filter (see the example system discussed in Section 24.6).

The availability of cost-effective active ac filters will change the scenario in the future.

24.2.3.2 DC Filters

These are similar to ac filters and are used for the filtering of dc harmonics. Usually a damped filter at the 24th harmonic is

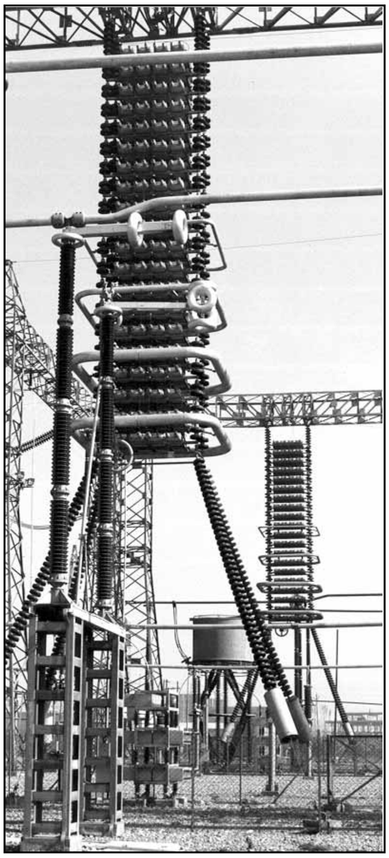


FIGURE 24.7 Installation of an ac filter in the switchyard.

utilized. Modern practice is to use active dc filters (see also the application example system presented later). Active dc filters are increasingly being used for efficiency and space-saving purposes.

24.2.3.3 High-Frequency RF/PLC Filters

These are connected between the converter transformer and the station ac bus to suppress any high-frequency currents. Sometimes such filters are provided on the high-voltage dc bus connected between the dc filter and dc line and also on the neutral side.

24.2.4 Reactive Power Source

Converter stations consume reactive power that is dependent on the active power loading (typically about 50% to 60% of the active power). The ac filters provide part of this reactive power requirement. In addition, shunt (switched) capacitors and static var systems are also used.

24.2.5 DC Smoothing Reactor

A sufficiently large series reactor is used on the dc side of the converter to smooth the dc current and for converter protection from line surges. The reactor (Fig. 24.8) is usually designed as a linear reactor and may be connected on the line side, on the neutral side, or at an intermediate location. Typical values of the smoothing reactor are in the 300–600 mH range for long-distance transmission and about 30 mH for a BB connection.

24.2.6 DC Switchgear

This is usually modified ac equipment and used to interrupt only small dc currents (i.e., employed as disconnecting switches). Dc breakers or metallic return transfer breakers (MRTB) are used, if required, for the interruption of rated load currents.

In addition to the equipment described above, ac switchgear and associated equipment for protection and measurement are also part of the converter station.

24.2.7 DC Cables

In contrast to the use of ac cables for transmission, dc cables do not have a requirement for continuous charging current. Hence the length limit of about 50 km does not apply. Moreover, dc voltage gives less aging and hence a longer lifetime for the cable. The new design of HVDC Light cables from ABB are based on extruded polymeric insulating material instead of classic paper–oil insulation, which has a tendency to leak. Because of their rugged mechanical design, flexibility, and low

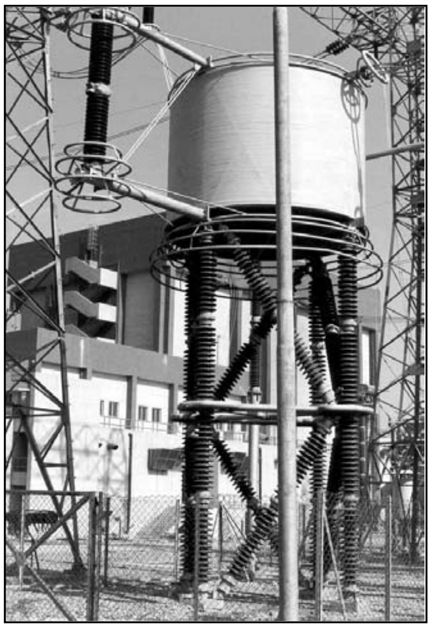


FIGURE 24.8 Installation of an air-cooled smoothing reactor.

weight, polymer cables can be installed underground cheaply with a plowing technique, or in submarine applications can be laid in very deep waters and on rough sea-bottoms. Since dc cables are operated in bipolar mode, one cable with positive polarity and one cable with negative polarity, very limited magnetic fields result from the transmission. HVDC Light cables have successfully achieved operation at a stress of 20 kV/mm.

24.3 Analysis of Converter Bridges

To consider the theoretical analysis of a conventional six-pulse bridge (Fig. 24.9), the following assumptions are made:

- The dc current I_d is considered constant
- Valves are ideal switches
- The ac system is strong (infinite)

Because of the leakage impedance of the converter transformer, commutation from one valve to the next is not instantaneous. An overlap period is necessary and, depending on the leakage, two, three, or four valves may conduct at any time. In the general case, with a typical value of converter transformer leakage impedance of about 13–18 , either two or three valves conduct at any one time.

The analysis of the bridge gives the following dc output voltages:

For a rectifier:

$$V_{dr} = V_{dor} \cdot \cos\alpha - R_{cr} \cdot I_d \tag{24.1}$$

where $V_{dor} = 3/\pi \cdot \sqrt{2} \cdot V_{LL}$ and $R_{cr} = (3/\pi)wL_{cr}$

For an inverter: There are two options possible, depending on choice of either the advance angle β or extinction angle γ as the control variable.

$$-V_{di} = V_{doi} \cdot \cos\beta + R_{ci} \cdot I_d \tag{24.2}$$

$$-V_{di} = -V_{doi} \cdot \cos\gamma + R_{ci} \cdot I_d \tag{24.3}$$

where

V_{dr} and V_{di} are the dc voltage at the rectifier and inverter, respectively

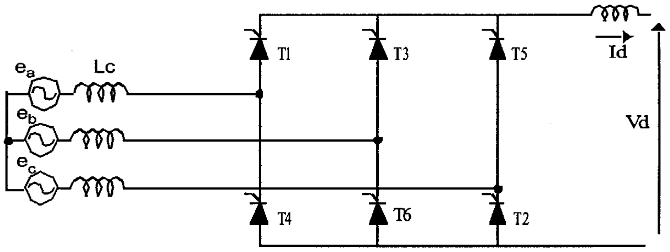


FIGURE 24.9 Six-pulse bridge circuit.

V_{dor} and V_{doi} are the open-circuit dc voltage at the rectifier and inverter, respectively

$V_{dor} = (3/\pi)*1.414*V_{LLr}$

$V_{doi} = (3/\pi)*1.414*V_{LLi}$

V_{LLr} and V_{LLi} are the line–line voltages at the rectifier and inverter, respectively

R_{cr} and R_{ci} are the equivalent commutation resistance at the rectifier and inverter, respectively

L_{cr} and L_{ci} are the leakage inductances of the converter transformer at rectifier and inverter, respectively

$R_{cr} = (3/\pi)*w*L_{cr}$

$R_{ci} = (3/\pi)*w*L_{ci}$

I_d is dc current

α is delay angle

β is advance angle at the inverter ($\beta = \pi - \alpha$)

γ is extinction angle at the inverter ($\gamma = \pi - \alpha - \mu$)

μ is overlap angle at the inverter

24.4 Controls and Protection

In a typical two-terminal dc link connecting two ac systems (Fig. 24.10), the primary functions of the dc controls are as follows:

- Control power flow between the terminals
- Protect the equipment against the current/voltage stresses caused by faults
- Stabilize the attached ac systems against any operational mode of the dc link

The dc terminals each have their own local controllers. A centralized dispatch center will communicate a power order to one of the terminals that will act as a Master Controller and has the responsibility to coordinate the control functions of the dc link. Besides the primary functions, it is desirable that the dc controls have the following features:

- *Limit the maximum dc current.* Because of the limited thermal inertia of the thyristor valves to sustain overcurrents, the maximum dc current is usually limited to less than 1.2 pu for a limited period of time.

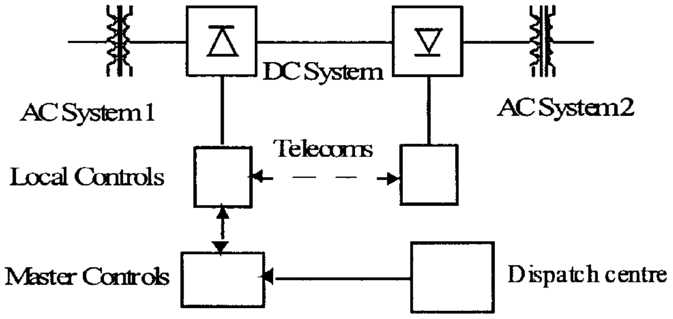


FIGURE 24.10 Typical HVDC system linking two ac systems.

- *Maintain a maximum dc voltage for transmission.* This reduces the transmission losses and permits optimization of the valve rating and insulation.
- *Minimize reactive power consumption.* This implies that the converters must operate at a low firing angle. A typical converter will consume reactive power between 50 and 60 of its MW rating. This amount of reactive power supply can cost about 15 of the station cost and comprise about 10 of the power loss.

The desired features of the dc controls are as follows:

1. Limit maximum dc current: Since the thermal inertia of the converter valves is quite low, it is desirable to limit the dc current to prevent failure in the valves.
2. Maintain maximum dc voltage for transmission purposes to minimize losses in the dc line and converter valves.
3. Keep the ac reactive power demand low at either converter terminal. This implies that the operating angles at the converters must be kept low. Additional benefits of doing this are to reduce the snubber losses in the valves and reduce the generation of harmonics.
4. Prevent commutation failures at the inverter station and hence improve the stability of power transmission.
5. Other features, i.e., the control of frequency in an isolated ac system or enhancement of power system stability, are also desirable.

In addition to these desired features, the dc controls will have to cope with the steady-state and dynamic requirements of the dc link, as shown in Table 24.2.

TABLE 24.2 Requirements of the dc link

Steady-State Requirements	Dynamic Requirements
Limit the generation of non-characteristic harmonics	Step changes in dc current or power flow
Maintain the accuracy of the controlled variable, i.e., dc current and/or constant extinction angle	Startup and fault-induced transients
Cope with the normal variations in the ac system impedance due to topology changes	Reversal of power flow
	Variation in frequency of attached ac system

24.4.1 Basics of Control for a Two-Terminal dc Link

From converter theory, the relationship between the dc voltage V_d and dc current I_d is given as in Eqs. (24.1)–(24.3). These three characteristics represent straight lines on the V_d-I_d plane. Notice that Eq. (24.2), i.e., the beta characteristic, has a positive slope, while Eq. (24.3), i.e., the gamma characteristic, has a negative slope. The choice of the control strategy for a typical two-terminal dc link is made according to conditions in Table 24.3.

Condition 1 implies the use of the rectifier in constant-current control mode; condition 3 implies the use of the inverter in constant extinction angle (CEA) control mode. Other control modes may be used to enhance the power transmission during contingency conditions depending on applications. This control strategy is illustrated in Fig. 24.11.

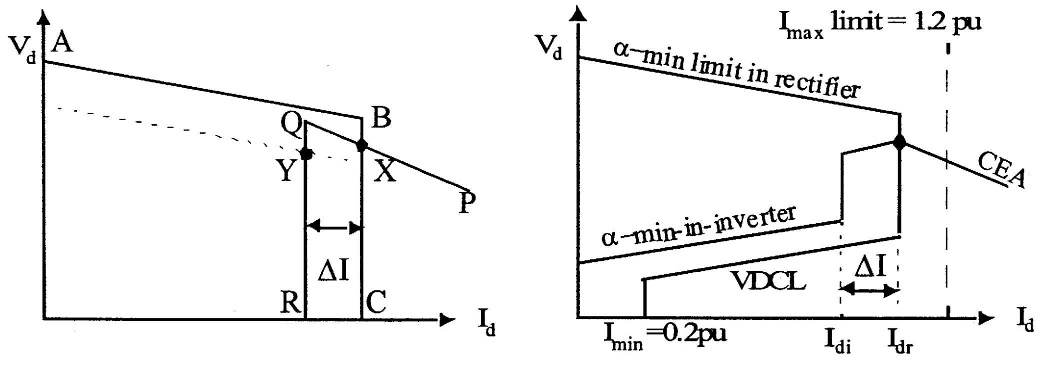
The rectifier characteristic is composed of two control modes: alpha-min (line AB) and constant-current (line BC). The alpha-min mode of control at the rectifier is imposed by the natural characteristics of the rectifier ac system and the ability of the valves to operate at alpha equal to zero, i.e., in the limit the rectifier acts a diode rectifier. However, since a minimum positive voltage is desired before firing of the valves to ensure conduction, an alpha-min limit of about 2–5° is imposed.

The inverter characteristic is composed of two modes: gamma-min (line PQ) and constant-current (line QR). The operating point for the dc link is defined by the crossover point X of the two characteristics. In addition, a constant-current characteristic is also used at the inverter. However, the current demanded by the inverter I_{di} is usually less than the current demanded by the rectifier I_{dr} by the current margin ΔI that is typically about 0.1 pu. The current margin is selected to be large enough that the rectifier and inverter constant-current modes do not interact because of any current harmonics which may be superimposed on the dc current. This control strategy is termed the current margin method.

The advantage of this control strategy becomes evident if there is a voltage decrease at the rectifier ac bus. The operating point then moves to point Y. Consequently, the current transmitted will be reduced to 0.9 pu of its previous value and voltage control will shift to the rectifier. However, the

TABLE 24.3 Choice of control strategy for two-terminal dc link

Condition	Desirable Features	Reason	Control Implementation
1	Limit the maximum dc current, I_d	For the protection of valves	Use constant current control at the rectifier
2	Employ the maximum dc voltage, V_d	For reducing power transmission losses	Use constant voltage control at the inverter
3	Reduce the incidence of commutation failures	For stability purposes	Use minimum extinction angle control at inverter
4	Reduce reactive power consumption at the converters	For voltage regulation and economic reasons	Use minimum firing angles



(a) (b)

FIGURE 24.11 Static V_d–I_d characteristic for a two-terminal link: (a) unmodified and (b) modified.

power transmission will be largely maintained near to 90 of its original value.

The control strategy usually employs the following other modifications to improve the behavior during system disturbances:

1. *At the rectifier:*
    - Voltage-dependent current limit (VDCL). This modification is made to limit the dc current as a function of either the dc voltage or, in some cases, the ac voltage. This modification assists the dc link to recover from faults. Variants of this type of VDCL do exist. In one variant, the modification is a simple fixed value instead of a sloped line.
    - I_d-min limit. This limitation (typically 0.2–0.3 pu) is to ensure a minimum dc current to avoid the possibility of dc current extinction caused by the valve current dropping below the hold-on current of the thyristors, an eventuality that could arise transiently because of harmonics superimposed on the low value of the dc current. The resultant current chopping would cause high overvoltages to appear on the valves. The magnitude of I_d-min is affected by the size of the smoothing reactor employed.
2. *At the inverter:*
    - Alpha-min limit at inverter. The inverter is usually not permitted to operate inadvertently in the rectifier region, i.e., a power reversal occurring because of, say, an inadvertent current margin sign change. To ensure this, an alpha-minimum limit in inverter mode of about 100–110° is imposed.
    - Current error region. When the inverter operates into a weak ac system, the slope of the CEA control mode characteristic is quite steep and may cause multiple crossover points with the rectifier characteristic. To avoid this possibility, the inverter CEA characteristic is usually modified into either a constant beta characteristic or constant voltage characteristic within the current error region.

24.4.2 Control Implementation

24.4.2.1 istorical Background

The equidistant pulse firing control systems used in modern HVDC control systems were developed in the mid-1960s [5,6]; although improvements have occurred in their implementation since then, such as the use of microprocessor-based equipment, their fundamental philosophy has not changed much. The control techniques described in [5,6] are of the pulse-frequency control (PFC) type as opposed to the now-out-of-favor pulse-phase control (PPC) type. All these controls use an independent voltage-controlled oscillator (VCO) to decouple the direct coupling between the firing pulses and the commutation voltage, V_{com}. This decoupling was necessary to eliminate the possibility of harmonic instability detected in the converter operation when the ac system capacity became nearer to the power transmission capacity of the HVDC link, i.e., with the use of weak ac systems. Another advantage of the equidistant firing pulse controls was the elimination of noncharacteristic harmonics during steady-state operation. This was a prevalent feature during the use of the earlier individual phase control (IPC) system where the firing pulses were directly coupled to the commutation voltage, V_{com}.

24.4.2.2 iring Angle Control

To control the firing angle of a converter, it is necessary to synchronize the firing pulses emanating from the ring counter to the ac commutation voltage, which has a frequency of 60 Hz in steady state. However, it was noted quite early on (early 1960s) that the commutation voltage (system) is not constant either in frequency or amplitude during a perturbed state. However, it is the frequency that is of primary concern for the synchronization of firing pulses. For strong ac systems, the frequency is relatively constant and distortion free to be acceptable for most converter-type applications. But, as converter connections to weak ac systems became required more often than not, it was necessary to devise a scheme for synchronization purposes that would be decoupled from the commutation voltage frequency for durations when there were perturbations occurring on the ac system. The most obvious method is to utilize an independent oscillator at 60 Hz that can be synchronously locked to the ac commutation voltage frequency. This oscillator would then provide the (phase) reference for the generation of firing pulses to the ring counter during the perturbation periods, and would use the steady-state periods for locking in step with the system frequency. The advantage of this independent oscillator would be to provide an ideal (immunized and clean) sinusoid for synchronizing and timing purposes. There are two possibilities for this independent oscillator:

- Fixed-frequency operation
- Variable-frequency operation

Use of a fixed-frequency oscillator (although feasible and called a pulse-phase control oscillator) is not recommended, since it is known that the system frequency does drift between, say, 55–65 Hz because of the rotating machines used to generate electricity. Therefore, it is necessary to use a variable-frequency oscillator (called a pulse-frequency control oscillator) with a locking range of between, say, 50 and 70 Hz and a center frequency of 60 Hz. This oscillator would then need to track the variations in the system frequency, and a control loop of some sort would be used for this tracking feature; this control loop would have its own gain and time parameters for steady-state accuracy and dynamic performance requirements.

The control loop for frequency-tracking purposes would also need to consider the mode of operation for the dc link. The method widely adopted for dc link operation is the so-called current margin method.

24.4.3 Control Loops

Control loops are required to track the following variables:

1. The ordered current I_{or} at the rectifier and the inverter
2. The ordered extinction angle (γ_o) at the inverter

24.4.3.1 Current Control Loops

In conventional HVDC systems, a PI regulator is used (Fig. 24.12) for the rectifier current controller. The rectifier plant system is inherently nonlinear and has the relationship given in Eq. (24.1). For constant I_d and for small changes in α, we have

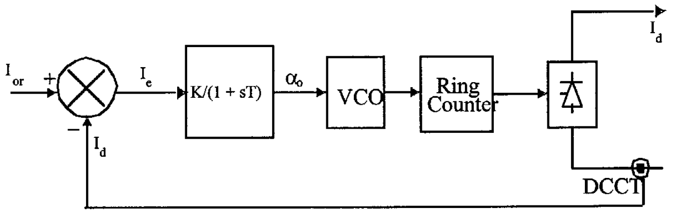


FIGURE 24.12 Control loop for the rectifier.

$$\Delta V_d/\Delta\alpha = -V_{dor}\sin\alpha \tag{24.4}$$

It is obvious from Eq. (24.4) that the maximum gain ($\Delta V_d/\Delta\alpha$) occurs when $\alpha = 90°$. Thus the control loop must be stabilized for this operation point, resulting in slower dynamic properties at normal operation with a within the range 12–18°. Attempts have been made to linearize this gain and have met with some limited success. However, in practical terms, it is not always possible to have the dc link operating with the rectifier at 90° because of harmonic generation and other protection elements coming into operation also. Therefore, optimizing the gains of the PI regulator can be quite arduous and take a long time. For this reason, the controllers are often pretested in a physical simulator environment to obtain appropriate settings. Final (often very limited) adjustments are then made on site.

Other problems with the use of a PI regulator include the following:

- It is mostly used with fixed gains, although some possibility for gain scheduling exists.
- It is difficult to select optimal gains, and even then they are optimal over a limited range only.
- Since the plant system is varying continually, the PI controller is not optimal.

A similar current control loop is used at the inverter (Fig. 24.13). Since the inverter also has a gamma controller, the selection between these two controllers is made via a MINIMUM SELECT block. Moreover, in order to bias the inverter current controller off, a current margin signal ΔI is subtracted from the current reference I_{or} received from the rectifier via a communication link.

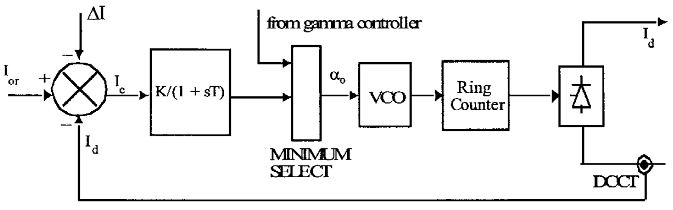


FIGURE 24.13 Current controller at the inverter.

. . . . ***Telecommunication Requirements*** As discussed earlier, the rectifier and inverter current orders must be coordinated to maintain a current margin of about 10 between the two terminals at all times; otherwise, there is a risk of loss of margin and the dc voltage could run down. Although it is possible to use slow voice communication between the two terminals, and maintain this margin, the advantage of fast control action possible with converters may be lost for protection purposes. For maintaining the margin during dynamic conditions, it is prudent to raise the current order at the rectifier first followed by the inverter; in terms of reducing the current order, it is necessary to reduce at the inverter first and then at the rectifier.

24.4.3.2 Gamma Control Loop

At the inverter end, there are two known methods for a gamma control loop. The two variants are different only in the method of determining the extinction angle:

- Predictive method for the indication of extinction angle (gamma)
- Direct method for actual measurement of extinction angle (gamma)

In either case, a delay of one cycle occurs from the indication of actual gamma and the reaction of the controller to this measurement. Since the avoidance of a commutation failure often takes precedence at the inverter, it is normal to use the minimum value of gamma measured for the six- or twelve-inverter valves for the converter(s).

. . . . ***Predictive Method of Measuring Gamma*** The predictive measurement tries to maintain the commutation voltage–time area after commutation larger than a specified minimum value. Since the gamma prediction is only approximate, the method is corrected by a slow feedback loop that calculates the error between the predicted value and actual value of gamma (one cycle later) and feeds it back.

The predictor calculates continuously, by a triangular approximation, the total available voltage–time area that remains after commutation is finished. Since an estimate of the overlap angle μ is necessary, it is derived from a well-known fact in converter theory that the overlap commutation voltage–time area is directly proportional to direct current and the leakage impedance (assumed constant and known) value of the converter transformer.

The prediction process is inherently of an individual phase firing character. If no further measure were taken, each valve would fire on the minimum margin condition. To counteract this undesired property, a special firing symmetrizer is used; when one valve has fired on the minimum margin angle, the following two or five valves fire equidistantly. (The choice of either two or five symmetrized valves is mainly a stability question).

. . . . ***Direct Method of Measuring Gamma*** In this method, the gamma measurement is derived from a measurement of the actual valve voltage. Waveforms of the gamma measuring circuit are shown in Fig. 24.14. An internal timing waveform, consisting of a ramp function of fixed slope, is generated after being initiated from the instant of anode current zero. This value corresponds to a direct voltage proportional to the last value of gamma. From the gamma values of all (either 6 or 12) valves, the smallest value is selected to produce the indication of measured gamma for use with the feedback regulator (Fig. 24.15).

This value is compared to a gamma-ref value and a PI regulator defines the dynamic properties for the controller. Inherently, this method has an individual phase control characteristic. One version of this type of control implementation overcomes this problem by using a symmetrizer for generating equidistant firing pulses. The 12-pulse circuit generates 12 gamma measurements; the minimum gamma value is selected and then used to derive the control voltage for the firing pulse generator with symmetrical pulses.

24.4.4 Hierarchy of dc Controls

Since HVDC controls are hierarchical in nature, they can be subdivided into blocks, which follow the major modules of a converter station (Fig. 24.16). The main control blocks are as follows:

1. The bipole (master) controller is usually located at one end of the dc link and receives its power order from a centralized system dispatch center. The bipole controller derives a current order for the pole controller using a local measurement of either ac or dc voltage. Other inputs may also be used by the bipole controller, such as frequency control for damping or modulation purposes. A communication to the remote terminal

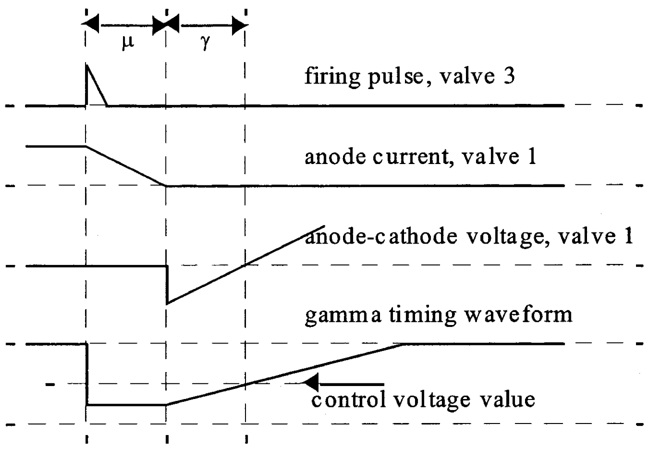


FIGURE 24.14 Waveforms for the gamma measuring circuit [5].

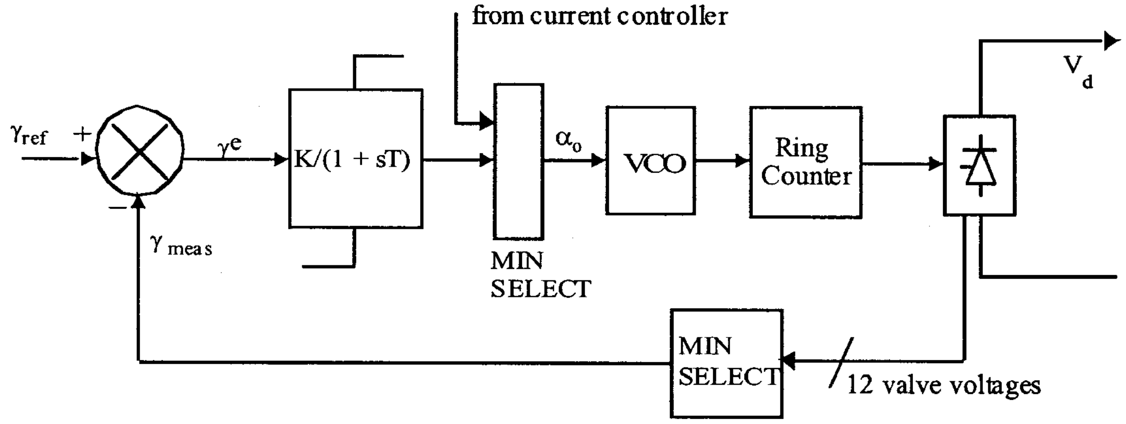

from current controller
γref
+
−
γe
K/(1 + sT)
MIN SELECT
α_o
VCO
Ring Counter
V_d
γ meas
MIN SELECT
12 valve voltages

FIGURE 24.15 Gamma feedback controller.

of the dc link is also necessary to coordinate the current references to the link.

2. The pole controller then derives an alpha order for the next level. This alpha order is sent to both the positive and negative poles of the bipole.
3. The valve group controllers generate the firing pulses for the converter valves. Controls also receive measurements of dc current, dc voltage, and ac current into the converter transformer. These measurements assist in the rapid alteration of firing angle for protection of the valves during perturbations. A slow loop for control of tap changer position as a function of alpha is also available at this level.

24.4.5 Monitoring of Signals

As described earlier, monitoring of the following signals is necessary for the controls (Fig. 24.17) to perform their functions and assist in the protection of the converter equipment:

V_d, I_d: Dc voltage and dc current, respectively

I_{ac}, I'_{ac}: Ac current on line-side and converter-side of the converter transformer

V_{ac}: Ac voltage at the ac filter bus

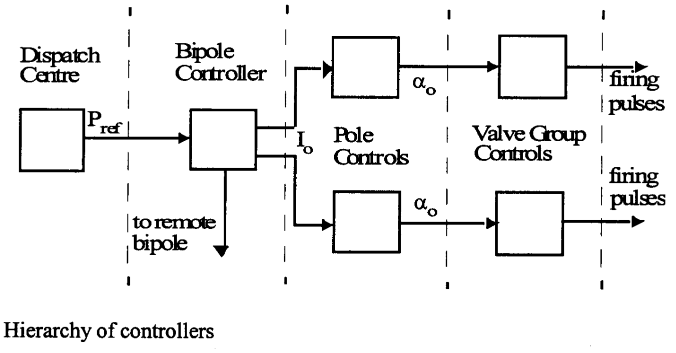

Dispatch Centre
Bipole Controller
P_ref
I_o
α_o
Pole Controls
Valve Group Controls
firing pulses
α_o
firing pulses
to remote bipole
Hierarchy of controllers

FIGURE 24.16 Hierarchy of controllers.

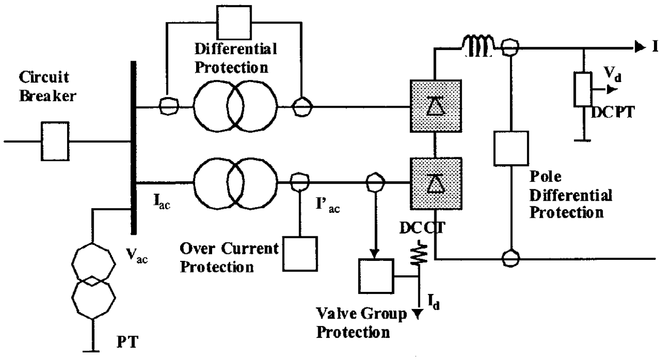

Differential Protection
Circuit Breaker
I_d
V_d
DCPT
Pole Differential Protection
I_ac
I'_ac
DCCT
V_ac
Over Current Protection
Valve Group Protection
I_d
PT

FIGURE 24.17 Monitoring points for the protection circuits.

24.4.6 Protection Against Overcurrents

Faults and disturbances can be caused by either malfunctioning equipment or insulation failures due to lightning and pollution. First, these faults need to be detected with the help of monitored signals. Second, the equipment must be protected by control or switching actions. Since dc controls can react within one cycle, control action is used to protect equipment against overcurrent and overvoltage stresses and minimize loss of transmission. In a converter station, the valves are the most critical (and most expensive) equipment that need to be protected rapidly because of their limited thermal inertia.

The basic types of faults that the station can experience are:

- **Current e tinction (CE).** CE can occur if the valve current drops below the holding current of the thyristor. This can happen at low current operation accompanied by a transient leading to current extinction. Because of the phenomenon of current chopping of an inductive current, severe overvoltages may result. The size of the smoothing reactor and the rectifier I_{min} setting help to minimize the occurrence of CE.
- *Commutation failure (CF) or misfire.* In line-commutated converters, the successful commutation of a valve

requires that the extinction angle γ-nominal be maintained more than the minimum value of the extinction angle γ-min. Note that $\gamma\text{-nominal} = 180 - \alpha - \mu$. The overlap angle μ is a function of the commutation voltage and the dc current. Hence, a decrease in commutation voltage or an increase in dc current can cause an increase in μ, resulting in a decrease in γ. If $\gamma < \gamma$-min, a CF may result. In this case, the outgoing valve will continue to conduct current, and when the incoming valve is fired in sequence, a short circuit of the bridge will occur.

A missing firing pulse can also lead to a misfire (at a rectifier) or a CF (at an inverter). The effects of a single misfire are similar to those of a single CF. Usually a single CF is self-clearing, and no special control actions are necessary. However, a multiple CF can lead to the injection of ac voltages into the dc system. Control action may be necessary in this case.

The detection of a CF is based on the differential comparison of dc current and the ac currents on the valve side of the converter transformer. During a CF, the two valves in an arm of the bridge are conducting. Therefore, the ac current goes to zero while the dc current continues to flow.

Protection features employed to counteract the impact of a CF are indicated in Table 24.4.

- *Short circuits: internal or dc line.* An internal bridge fault is rare as the valve hall is completely enclosed and is air-conditioned. However, a bushing can fail, or valve-cooling water may leak, resulting in a short circuit. The ac breaker may have to be tripped to protect against bridge faults.

  The protection features employed to counteract the impact of short circuits are indicated in Table 24.4.

The fast-acting HVDC controls (which operate within one cycle) are used to regulate the dc current for protection of the valves against ac and dc faults.

The basic protection (Fig. 24.17) is provided by the VGP differential protection, which compares the rectified current on the valve side of the converter transformer with the dc current measured on the line side of the soothing reactor. This method is applied because of its selectivity, made possible by the high impedances of the smoothing reactor and converter transformer.

The OCP is used as a backup protection in case of malfunction in the VGP. The level of overcurrent is set higher than the differential protection.

The pole differential protection (PDP) is used to detect ground faults, including faults in the neutral bus.

24.4.7 Protection against Overvoltages

The typical arrangement of metal-oxide surge arrestors for protecting equipment in a converter pole is shown in Fig. 24.18. In general, the ac bus arrestors limit overvoltages entering from the ac bus; similarly, the dc arrestor limits overvoltages entering the converter from the dc line. The ac and dc filters have their respective arrestors also. Critical components such as the valves have their own arrestors placed close to these components. The protective firing of a valve is used as a backup protection for overvoltages in the forward direction. Owing to their varied duty, these arrestors are rated accordingly for the location used. For instance, the converter arrestor for the upper bridge is subjected to higher energy dissipation than that for the lower bridge.

Since the evaluation of insulation coordination is quite complex, detailed studies are often required with dc simulators to design an appropriate insulation coordination strategy.

24.5 MTDC Operation

Most HVDC transmission systems are two-terminal systems. A multiterminal dc system (MTDC) has more than two terminals, and there are two existing installations of this type. There are two possible ways of tapping power from an HVDC link, i.e., with series or parallel taps.

24.5.1 Series Tap

A monopolar version of a three-terminal series dc link is shown in Fig. 24.19. The system is grounded at only one suitable location. In a series dc system, the dc current is set by one terminal and is common to all terminals; the other

TABLE 24.4 Protection against overcurrents

Fault Type	Occurrence	Fault Current Level	Protection Method
Internal faults	Infrequent	10 pu	Valve is rated to withstand this surge
Dc line faults	Frequent	2–3 pu	• Forced retard of firing angle • Dynamic VDCL deployment • Trip ac breaker CB after third attempt
Commutation failures: single or multiple	Very frequent	1.5–2.5 pu	Single CF: • Self-clearing Multiple CF: • Beta angle advanced in stages • Static VDCL deployment

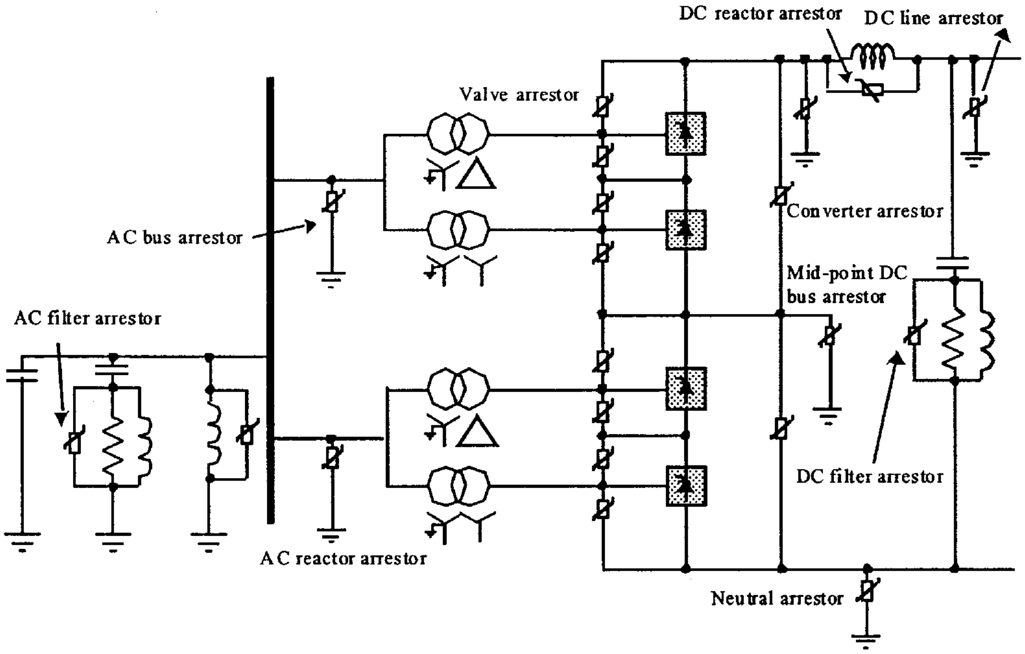


FIGURE 24.18 Typical arrangement of surge arrestors for a converter pole.

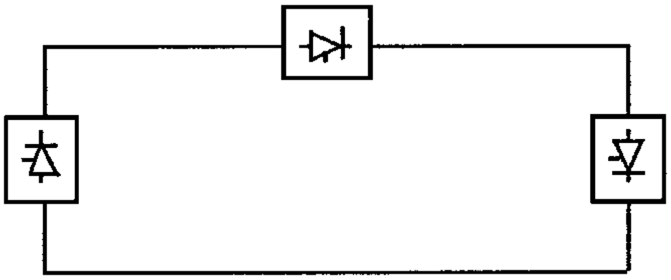


FIGURE 24.19 Series tap.

terminals are operated at a constant delay angle for a rectifier and constant extinction angle for inverter operation with the help of transformer tap changers.

Power reversal at a station is achieved by reversing the dc voltage with angle control.

No practical installation of this type exists in the world at present. From an evaluation of ratings and costs for series taps, it is not practical for the series tap to exceed 20 of the rating for a major terminal in the MTDC system.

24.5.2 Parallel Tap

A monopolar version of a three-terminal parallel dc link is shown in Fig. 24.20. In a parallel MTDC system, the system voltage is common to all terminals. There are two variants possible for a parallel MTDC system: radial or mesh. In a radial system, disconnection of one segment of the system will interrupt power from one or more terminals. In a mesh system, the removal of one segment will not interrupt power flow, provided the remaining links are capable of carrying the required power.

Power reversal in a parallel system will require mechanical switching of the links, as the dc voltage cannot be reversed.

From an evaluation of ratings and costs for parallel taps, it is not practical for the parallel tap to be less than 20 of the rating for a major terminal in the MTDC system.

There are two existing installations of parallel taps in the world. The first is the Sardinia–Corsica–Italy link where a 50-MW parallel tap at Corsica is used. Since the principal terminals are rated at 200 MW, a commutation failure at Corsica can result in very high overcurrents (typically 7 pu); for this reason, large smoothing reactors (2.5 H) are used in this link.

The second installation is the Quebec–New Hampshire 2000-MW link where a parallel tap is used at Nicolet. Since the rating of Nicolet is at 1800 MW, the size of the smoothing reactors was kept to a modest size.

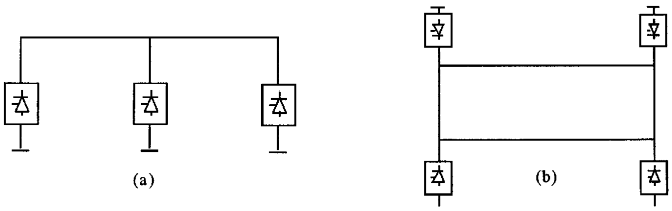


FIGURE 24.20 Parallel tap: (a) radial type and (b) mesh type.

24.5.3 Control of MTDC Systems

Although several control methods exist for controlling MTDC systems, the most widely utilized method is the so-called current margin method that is an extension of the control method used for two-terminal dc systems.

In this method, the voltage setting terminal (VST) operates at the angle limit (minimum alpha or minimum gamma) while the remaining terminals are controlling their respective currents. The control law that is used sets the current reference at the voltage setting terminal according to

$$\sum I_{j-\mathrm{ref}} = \Delta I \tag{24.5}$$

where ΔI is known as the current margin.

The terminal with the lowest voltage ceiling acts as the VST.

An example of the control strategy is shown in Fig. 24.21 for a three-terminal dc system with one rectifier REC and two inverters, INV1 at 40 and INV2 at 60 rating. The REC1 and INV2 terminals are maintained in current control, and INV1 is the VST oerating in CEA mode.

Because of the requirement to maintain current margin for the MTDC system at all times, a centralized current controller, known as the current reference balancer (CRB) (Fig. 24.22), is required. With this technique, reliable two-way telecommunication links are required for current reference coordination purposes. The current orders, $I_{\mathrm{ref}1}-I_{\mathrm{ref}3}$, at the terminals must satisfy the control law according to Eq. (24.5). The weighting factors (K_1, K_2, and K_3) and limits are selected as a function of the relative ratings of the terminals.

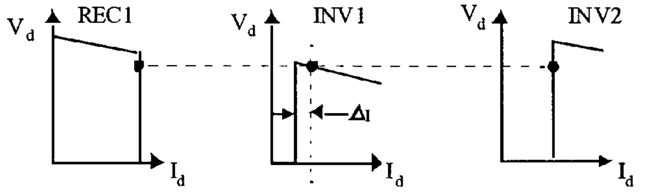


FIGURE 24.21 Current margin method of control for MTDC system.

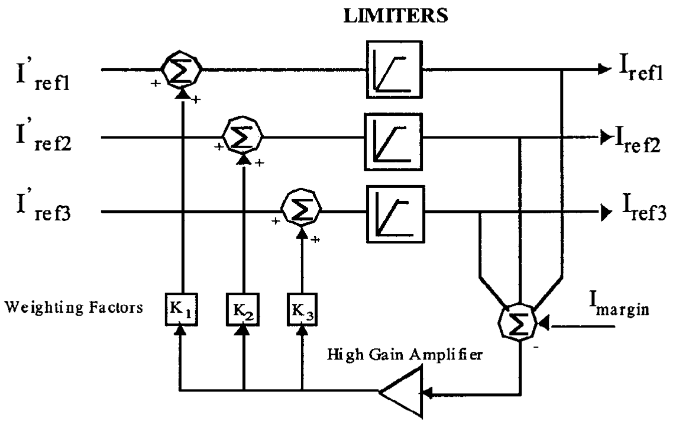


FIGURE 24.22 Current reference balancer.

24.6 Applications

24.6.1 VDC Interconnection at Gurun Malaysia

The 300/600-MW HVDC interconnection between Malaysia and Thailand (Fig. 24.23) is a major first step in implementing electric power network interconnections in the ASEAN region. It is jointly undertaken by two utilities, Tenaga Nasional Berhad (TNB) of Malaysia and Electricity Generating Authority of Thailand (EGAT). This will be the first HVDC project for both these utilities. The HVDC interconnection consists of a 110-km HVDC line (85 km owned by TNB, and 25 km owned by EGAT) with the dc converter stations at Gurun on the Malaysian side and Khlong Ngae on the Thailand side. The scheme is scheduled for commercial operation in July 2000. The interconnection will provide a range of diverse benefits:

- Spinning reserve sharing
- Economic power exchange commercial transactions
- Emergency assistance to either ac system
- Damping of ac system oscillations
- Reactive power support (voltage control)
- Deferment of generation plant-up

24.6.1.1 Power Transmission Capacity

The converter station is presently constructed for monopolar operation for power transfer of 300 MW in both directions with provisions for future extensions to a bipole configuration giving a total power-transfer capability of 600 MW. The HVDC line is constructed with two pole conductors to cater for the second 300 MW pole. Full-length neutral conductors are used instead of ground electrodes because of high land costs and inherently high values of soil resistivity.

The monopole is rated for a continuous power of 300 MW (300 kV, 1000 A) at the dc terminal of the rectifier station. In addition, there is a 10-minute overload capability of up to 450 MW that may be utilized once per day when all redundant cooling equipment is in service.

The HVDC interconnection scheme is capable of continuous operation at a reduced dc voltage of 210 kV (70) over the whole load range up to the rated dc current of 1000 A with all redundant cooling equipment in service.

24.6.1.2 Performance Requirements

A high degree of energy availability was a major design objective. Guaranteed targets for both stations are:

- Energy availability:	99.5
- Forced energy unavailability:	0.43
- Forced outage rates:	5.4 outages per year

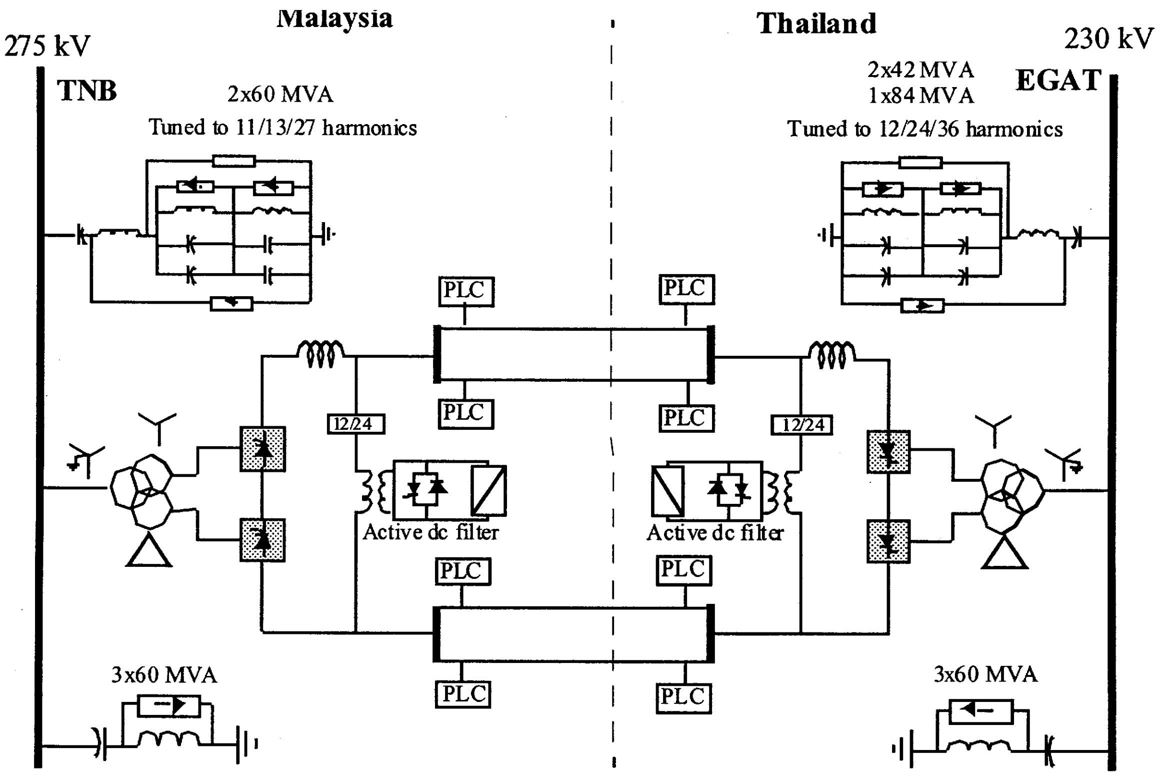


FIGURE 24.23 One-line diagram of HVDC interconnection between Malaysia and Thailand.

24.6.1.3 Major Technical Features

The station incorporates the latest state-of-the-art technology in power electronics and control equipment:

- A fully decentralized control and protection system
- Active dc filter technology
- Hybrid dc current shunt measuring devices
- Triple-tuned ac filter

24.6.1.4 Technical Information

See Fig. 24.23.

24.7 Modern Trends

24.7.1 Converter Station Design of the 2 s

The 1500-MW, ±500-kV Rihand–Delhi HVDC transmission system (commissioned in 1991) serves as an example of a typical design of the last decade. Its major design aspects were the following:

- Stations employ water-cooled valves of indoor design with the valves arranged as three quadruple valves suspended from the ceiling of the valve hall.
- Converter transformers are one-phase, three-winding units situated close to the valve hall with their bushings protruding into the valve hall.
- Ac filtering is done with conventional, passive, double-tuned and high-pass units employing internally fused capacitors and air-cored reactors; these filters are mechanically switched for reactive power control.
- Dc filtering is done with conventional, passive units employing a split smoothing reactor consisting of both an oil-filled reactor and an air-cored reactor.
- DCCT measurement is based on a zero-flux principle.
- Control and protection hardware is located in a control room in the service building in between the two valve halls. The controls still employ some analog parts, particularly for the protection circuits. The controls were duplicated with an automatic switchover to hot stand-by for reliability reasons.

This design was done in the 1980s to meet the requirements of the day for increased reliability and performance requirements, i.e., availability, reduced losses, higher overload capability, etc. However, these requirements led to increased costs for the system.

The next generation equipment is now being spearheaded by a desire to reduce costs and make HVDC as competitive as ac transmission. This is being facilitated by the major developments of the past decade that have taken place in power electronics. Therefore, the following will influence the next generation HVDC equipment.

24.7.1.1 Thyristor Development

HVDC thyristors are now available with a diameter of 150 mm at a rating of 8–9 kV and power-handling capacity of 1500 kW, which will lead to a dramatic decrease in the number of series-connected components for a valve, with consequential cost reductions and improvement in reliability.

The development of the light-triggered thyristor (LTT) (Figs. 24.24 and 24.25) is likely to eliminate the electronic unit (with their high number of electronic components) for generating the firing pulses for the thyristor (Fig. 24.26). The additional functional requirements of monitoring and protection of the device are being incorporated also.

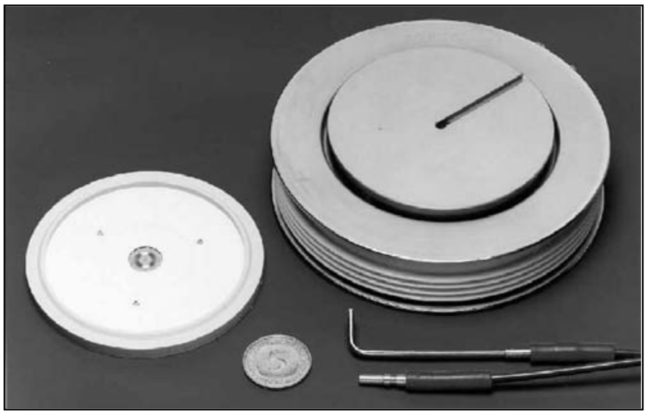


FIGURE 24.24 Silicon wafer and construction of the LTT. The light guides appear in the bottom right-hand corner of the photo.

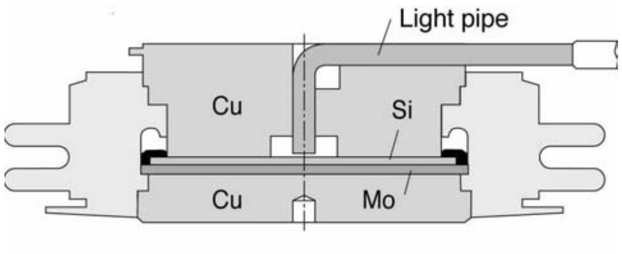


FIGURE 24.25 Cross section of the LTT with the light pipe entry.

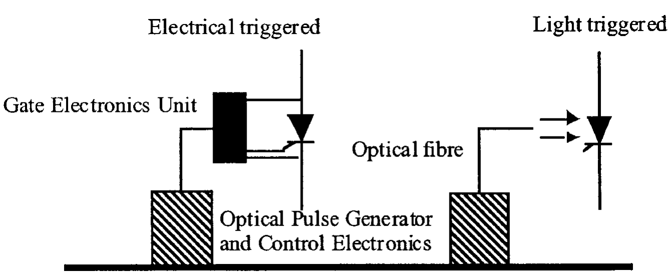


FIGURE 24.26 Conventional firing vs light triggered firing.

Both of the preceding developments present the possibility of achieving compact valves that can be packaged for outdoor construction, thereby reducing the overall cost and reliability of the station.

24.7.1.2 Higher dc Transmission Voltages

For long-distance transmission, there is a tendency to use a high voltage to minimize the losses. The typical transmission voltage has been ±500 kV, although the Itaipu project in Brazil uses 600 kV. The transmission voltage has to be balanced against the cost of insulation. The industry is considering raising the voltage to ±800 kV.

24.7.1.3 Controls

It is now possible to operate an HVDC scheme into an extremely weak ac system, even with short-circuit capacity down to unity.

Using programmable DSPs has resulted in a compact and modular design that is low cost; furthermore, the number of control cubicles has decreased by a factor of 10 times in the past decade. Now all control functions are implemented on digital platforms. The controls are fully integrated, having monitoring, control, and protection features. The design incorporates self-diagnostic and supervisory characteristics. The controls are optically coupled to the control room for reliable operation. Redundancy and duplication of controls results in very high reliability and availability of the equipment.

24.7.1.4 Outdoor Valves

The introduction of air-insulated, outdoor valves will reduce the costly requirement for a valve hall. The use of a modular, compact design, which will be preassembled in the manufacturing plant, will save installation time and provide for a flexible station layout. This design has been feasible because of development of a composite insulator for dc applications, which is used as a communications channel for fiber optics, cooling water, and ventilation air between the valve unit and ground.

24.7.1.5 Active dc Filters

This development, made possible by advances in power electronics and microprocessors, has resulted in a more efficient dc filter operating over a wide spectrum of frequencies and provides a compact design (Fig. 24.27).

24.7.1.6 Ac Filters

Conventional ac filters used passive components for tuning out certain harmonic frequencies. Because of the variations in frequency and capacitance, physical aging and thermal characteristics of these tuned filters, the quality factors for the filters were typically about 100–125, which means that the filters could not be too sharply tuned for efficient harmonic

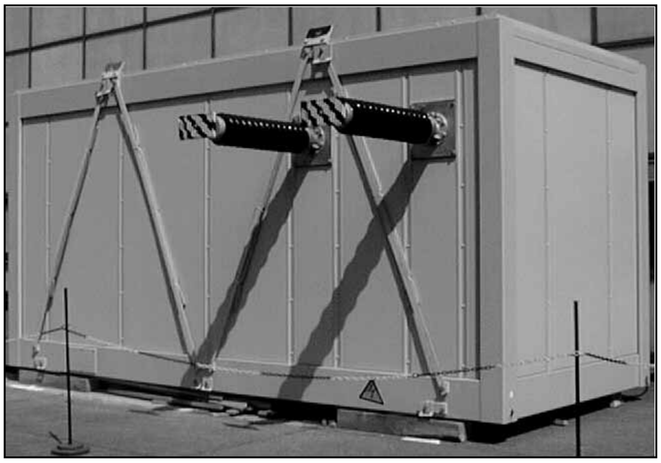


FIGURE 24.27 Compact outdoor container with an active dc filter.

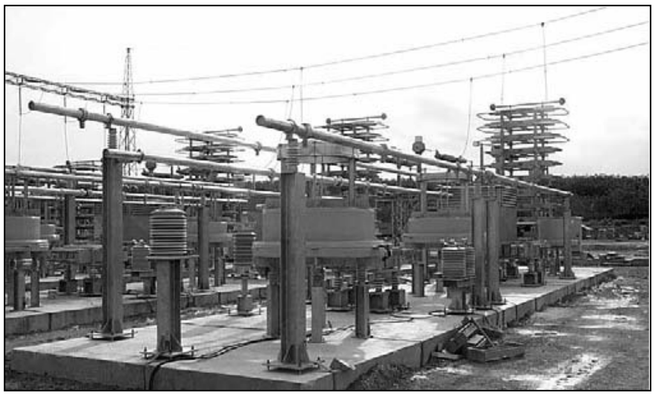


FIGURE 24.28 Installation of triple-tuned filter at the Gurun Station in Malaysia.

filtering. The advent of electronically tunable inductors based on the transductor principle means that the Q-factors can now approach the natural one of the inductor. This will lead to a much more enhanced filtering capacity. (See Fig. 24.28).

24.7.1.7 Ac dc Current Measurements

The new optical current transducers utilize a precision shunt at high potential. A small optical-fiber link between ground and high potential is utilized, resulting in a lower probability of a flashover. The optical power link transfers power to high potential for use in electronics equipment. The optical data link transfers data to ground potential. This transducer results in high reliability, compact design, and efficient measurement (Fig. 24.29).

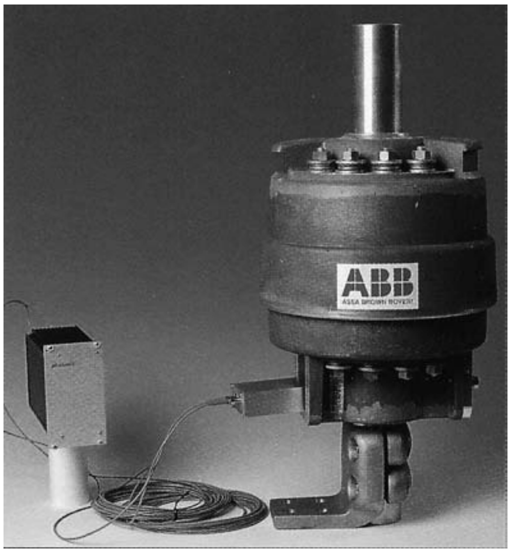


FIGURE 24.29 The optical current transducer.

24.7.1.8 New Topologies

Two new topological changes to the converter design will have a great impact on future designs.

1. *Series-compensated commutation.* There are two variants to this topology: the capacitor commutated converter (CCC) and the controlled series capacitor converter (CSCC). Essentially, the behavior of the two variants is very similar. The insertion of a capacitor in series with the converter transformer results in a major reduction in the commutation impedance of the converter, resulting in a reduction in the reactive power requirement of the converter. The increase in the size of the series capacitor can even result in the operation at leading power factor if so desired. However, the negative impact of lower commutation impedance results in additional stresses on the valves and transformers and additional cost implications. The first CCC back-to-back converter station (2 × 550 MW) has been put into service at Garabi, on the Brazilian side of the Uruguay River. The system interconnects the electrical systems of Argentina and Brazil.
2. *Voltage-source converters (VSC).* The use of self-commutation with the new generation devices (i.e., GTOs and IGBTs) has resulted in the topology of a voltage-source converter (VSC) as opposed to the conventional converter using ordinary thyristors and current-source converter (CSC) topology. The VSC, being self-commutated, can control active/reactive power, and with PWM techniques, control harmonic generation as well. The switching losses and ratings of available devices presently limit the application of such circuits. The ongoing advances in power electronic devices are expected to have a major impact on the application of this type of converter on HVDC transmission. New application areas particularly in distribution systems are being actively investigated with this topology. Table 24.5 provides a list of the HVDC links in operation using this technique.

One major difficulty in using the VSC is the threat posed to the valves from a short circuit on the dc line, unlike the CSC,

TABLE 24.5 Applications of HVDC light technology

	Project	Rating (MVA kV)		Distance (km)	Application	Commissioned
1	Hellsjon	3	±10	10	Ac–dc conversion	Mar. 1997
2	Gotland	50	±80	70	Feed from wind power generation	June 1999
3	Tjaereborg	7	±10	4	Feed from wind power generation	Aug. 1999
4	Directlink	180	±140	65	Asynchronous interconnection	Dec. 1999

where the valves are inherently protected against short-circuit currents by the presence of the smoothing reactor. For this reason, VSC applications are almost always used with dc cables where the dc line short-circuit risk is greatly reduced.

24.7.1. Compact Station Layout

The advances discussed previously have resulted in marked improvement of the footprint requirement of the compact station of the year 2000, which has about 30% of the space requirement of the comparable HVDC station designed in the past decade (Fig. 24.30) [7].

24.8 DC System Simulation Techniques

Modern HVDC systems incorporate complex control and protection equipment. The testing and optimization of these equipment require powerful tools that are capable of modeling all facets of the system and have the flexibility to do the evaluation in a rapid, effective, and cost-efficient manner.

24.8.1 Dc Simulators and TNAs

For decades, this has been achieved with the aid of physical power system simulators or transient network analyzers (TNAs) [8]. These incorporate scaled physical models of all power-system elements [three-phase ac network lines/cables, sources as emf behind reactances, model circuit breakers for precisely timed ac system disturbances, transformers (system and convertor transformers with capacity to model saturation characteristics), filter capacitors, reactors, resistors, arrestors, and machines]. Until the 1970s, these were built with analog components. However, with the developments in microprocessors, it is now feasible to utilize totally digital simulators operating in realtime for even the most complex HVDC system studies. The operating scale of most simulators is in

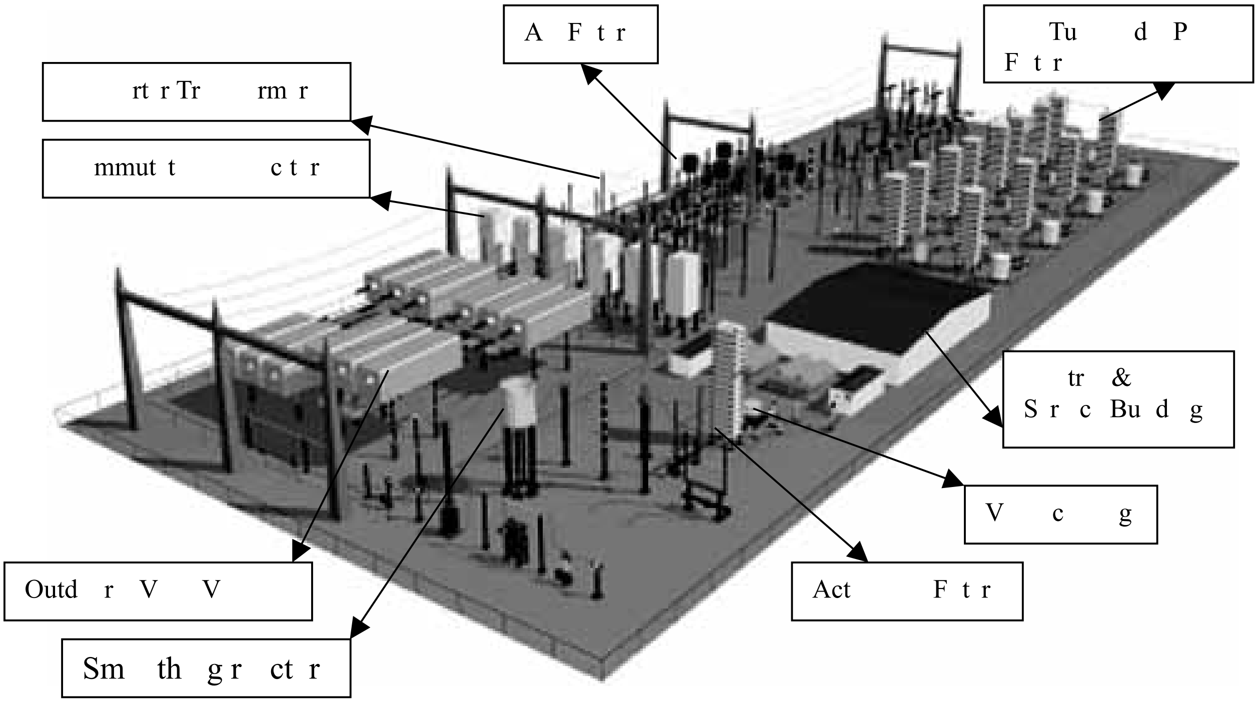


FIGURE 24.30 Graphic layout of a compact HVDC station (graphic reproduced here courtesy of ABB).

the range 20–100 V dc, 0.2–1.0 A ac and at a power frequency of 50 or 60 Hz. The stray capacitance and inductance are, however, not normally represented, since the simulator is primarily used to assess control system behavior and temporary overvoltages of frequencies below 1000 Hz. Because of the developments of flexible ac transmission systems (FACTS) application, most modern simulators now include scaled models of HVDC converters, static compensators, and other thyristor-controlled equipment. The controls of these equipments are usually capable of realistic performance during transients such as ac faults and commutation failure. The limited availability of adequate models of some of the system elements restricts the scope of the studies that can be completed entirely by means of the simulator. Because of the scaling problems, losses in the simulator may be disproportionately high and need to be partly compensated by electronic circuits (negative resistances) to simulate appropriate damping of overvoltages and other phenomena.

24.8.2 Digital Computer Analysis

The main type of program employed for studies is an electromagnetic transient program (EMTP), which solves sets of differential equations by step-by-step integration methods. The digital program must allow for modeling of both the linear and nonlinear components (single- and three-phase) and of the topological changes caused, for example, by valve firing or by circuit-breaker operation. Detailed modeling of the converter control system is necessary depending on the type of study.

The main advantage of digital studies is the possibility of correct representation of the damping present in the system. This feature permits more accurate evaluation of the nature and rate of decay of transient voltages following their peak levels in the initial few cycles, and also a more realistic assessment of the peak current and total energy absorption of the surge arrestors. The digital program also allows modeling of stray inductance and capacitance and can be used to cover a wider frequency range of transients than the dc simulator.

The main disadvantage of the digital studies is the lack of adequate representation of commutation failure phenomena with the use of power electronic converters. However, with the increasing capacity of computers, this is likely to be overcome in the future.

The models used in the simulators and digital programs depend on the assumptions made and on the proper understanding of the component and system characteristics; therefore, they require care in their usage to avoid unrealistic results in inexperienced hands.

24. Conclusion

HVDC technology is now mature, reliable, and accepted all over the world. From its modest beginning in the 1950s, the technology has advanced considerably and maintained its leading-edge image. The encroaching technology of flexible ac transmission systems (FACTS) has learned and gained from the technological enhancements made initially by HVDC systems. FACTS technology may challenge some of the traditional roles for HVDC applications, since the deregulation of the electrical utility business will open up the market for increased interconnection of networks. HVDC transmission has unique characteristics that will provide it with new opportunities. Although the traditional applications of HVDC transmission will be maintained for bulk power transmission in places such as China, India, South America and Africa, the increasing desire for the exploitation of renewable resources will provide both a challenge and an opportunity for innovative solutions in the following applications:

- Connection of small dispersed generators to the grid
- Alternatives to local generation
- Feeding to urban city centers

Acknowledgments

The author pays tribute to the many pioneers whose vision of HVDC transmission has led to the rapid evolution of the power industry. It is not possible here to name all of them individually. A number of photographs of equipment are included in this chapter, and I thank the suppliers (Mr. P. Lips of Siemens and Mr. R. L. Vaughan from ABB) for their valued assistance. I also thank my wife Vinay for her considerable assistance in the preparation of this manuscript.

List of Abbreviations

BB	Back to back
BOD	Break-over diode
CCC	Capacitor-commutated converter
CE	Current extinction
CEA	Constant extinction angle
CF	Commutation failure
CRB	Current reference balance
CSC	Current source converter
CSCC	Controlled series capacitor commutated converter
DSP	Digital signal processors
EGAT	Electricity Generating Authority of Thailand
EMTP	Electromagnetics transient program
FACTS	Flexible alternating current transmission system

GEU	Gate electronic unit
GTO	Gate turn-off thyristor
HVDC	High-voltage direct current
IPC	Individual phase control
LTT	Light-triggered thyristor
MRTB	Metallic return transfer breaker
MTDC	Multiterminal direct current
OCP	Overcurrent protection
PDP	Pole differential protection
PFC	Pulse frequency control
PPC	Pulse phase control
PWM	Pulse-width modulated
SIL	Surge impedance loading
STATCOM	Static compensator
SVC	Static var compensator
TNA	Transient network analyzer
TNB	Tenaga Nasional Berhad
VBE	Valve base electronics
VCO	Voltage-controlled oscillator
VDCL	Voltage-dependent current limit
VGP	Valve group protection
VSC	Voltage source converter
VST	Voltage setting terminal

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25

Multilevel Converters and VAR Compensation

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25.1 Introduction

Reactive power has no real physical meaning, but is recognized as an essential factor in the design and good operation of power systems. Real and reactive power on a transmission line in an integrated network is governed by the line impedance, voltage magnitudes, the angle difference at the line ends, and the role the line plays in maintaining network stability under dynamic contingencies. Power transfer in most integrated transmission systems is constrained by transient stability, voltage stability, and/or power stability. Reactive power (VAR) compensation or control is an essential part in a power system to minimize power transmission losses, to maximize power transmission capability, and to maintain the supply voltage.

It is increasingly becoming one of the most economic and effective solutions to both traditional and new problems in power transmissions systems. It is a well-established practice to use reactive power compensation to control the magnitude of the voltage at a particular bus bar in any electric power system. In the past, synchronous condensers, mechanically switched capacitors and inductors, and saturated reactors have been applied to control the system voltage in this manner [1, 2]. Since the late 1960s, thyristor-controlled reactor (TCR) devices together with fixed capacitors (FCs) or thyristor-switched capacitor (TSCs) have been used to inject or absorb reactive power [3, 4].

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Series compensation is the control of the equivalent line impedance of a transmission line. The induction of external components (either capacitive or inductive) is used to change the apparent reactance of the line. A controllable series compensator such as the thyristor-controlled series compensation (TCSC) has been developed to change the apparent impedance of a line by either inductive or capacitive compensation, facilitating active power transfer control. The thyristors control the conduction period of the reactor to vary the overall effective Z of the circuit. The TCSC suffers from the disadvantage that it generates low-order harmonic components into the power system.

TCSCs are usually connected in series to conventional line series capacitors. They may consist of one or several identical modules. Each module has a small thyristor-controlled reactor in parallel to the segment series capacitor. Although the TCSC is primarily used for regulating the power flow, though varying its effective reactance inserted in series with the transmission line, it may also be used for voltage stabilization. In this case, the o/p reads terminal voltage within a tight band.

Voltage source converters using GTO thyristor have been developed to operate as static VAR compensators [5–7]. These are known as ASVCs. Such converters may resemble the operation of synchronous condensers, but in a static manner. For these devices, a converter transformer is always needed to complement the function of the P.E. switches to perform system VAR compensation and may also be used to connect the device to the HV bus. The converter supplies reactive power to the network by increasing the synthesized inverter o/p voltage. Similarly, the ASVC absorbs VARs from the network by reducing the o/p voltage below the network voltage, i.e., no large power components such as capacitor banks or reactors are used. Only a small capacitor is employed to provide the required reference voltage level to the inverter. In contrast to the TCR/FC or TCR/TSC schemes, bulky and experimental passive elements are not required. The possibility of PWM voltage source converters with high switching frequency for reactive power compensation has also been reported [8, 9]. However, the high-switching-frequency operation of GTOs is not available. In order to apply large-scale reactive power compensation, new svc systems with low-switching-frequency PWM operation have been reported [10–12].

The conventional GTO inverters have dc link voltage limitations of about 2 kV. Hence, the series connections of the existing GTO thyristors have been essential in realizing high voltage, about 4 kV. So there has been great interest in the multilevel level inverter topology, which can overcome series connection problems. The multilevel level inverters are able to generate multiple level outputs line to line voltage without output transformers or reactors, i.e., the harmonics components of the phase voltage are fewer than those of the conventional two-level inverter at the same switching frequency.

Each alternative has its technical and economical advantages, limitations, and drawbacks, and it is the scope of this article to provide a thorough comparison of the various alternatives.

25.2 Reactive Power Phenomena and Their Compensation

In an ideal electroenergetic system, the voltage and frequency in the various points of power distribution must be constant, presenting only the fundamental component (harmonics contents nil) and a near-unity power factor. In particular, these parameters must be independent of the size and characteristics of the consumer loads; this can be obtained only if these loads are equipped with reactive power compensators to make the network independent from probable changes that appear in the distribution points [1].

Compensation of the loads is one of the techniques for the controlling reactive power, so to improve the quality of the energy in the ac transmission lines; this technique is generally used for the compensation of individual or a group of loads. This has three essential objectives:

- Power factor correction
- Improvement of the voltage regulation
- Load balancing

It is noted that power factor correction and load balancing are desired even when the supply voltage is virtually constant and independent of the load.

25.2.1 Power Factor Correction

This is the capacity of generating or absorbing the reactive power to a load without the use of the supply. The major industrial loads have an inductive power factor (they absorb reactive power); hence the current tends to go beyond the necessary value to active power absorption alone. But active power is usually used for the power conversion, and an excessive load current represents a loss for the consumer, who not only pays for the over-dimensioning of the cable, but also for the excess power loss in the cables. The electric companies do not want to transport the useless reactive power of the alternators toward the loads, these and the distribution network cannot be used at high efficiency, and the voltage regulation in the various points becomes complicated. The pricing used by these electric companies almost always penalizes the low power factor of the clients; hence the great development of systems for power-factor improvement for industrial processes.

25.2.2 Voltage Regulation

Voltage regulation is an important and even the only option in the presence of loads when the demand of the reactive power varies considerably, which will lead to variations of the supply voltage that would destroy industrial processes.

25.2.3 Load Balancing

Most of power systems are three-phased and are designed for a balanced operation. An unbalanced operation will lead to the presence of negative and zero sequences. These sequences have a bad effect on the quality of energy, such as additional losses and pulsating torques in electric motors and saturation in transformers.

25.2.4 Classical Solutions for Compensating the Reactive Power

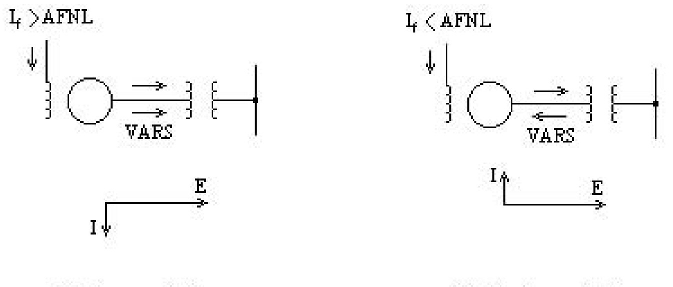
25.2.4.1 Synchronous Compensator

A synchronous compensator is a synchronous machine made to rotate at synchronous speed with no mechanical torque given to the shaft; the active power delivered by the network corresponds to the power loss of the machine. With excitation, the operating point will move practically on the axis of the reactive power and the machine will behave as a condenser (I_f AFNL), or as an inductance (I_f AFNL) as illustrated by Fig. 25.1. However, for this type of compensator to be used at full efficiency, it should be driven in a closed chamber full of hydrogen so as to reduce the losses by ventilation and to increase the specific power. The cost of such system is high and encumbering [13]. This has led the way to the development of a new type of static compensator controlled by thyristors.

25.2.4.2 Bank of Capacitors

Such capacitors are generally designed for compensating parameters that vary slowly, and the capacitors are usually fractioned so as to adjust the reactive power to be compensated.

Since the capacitors are elements that have discrete variations, the techniques for shunt compensation may not allow the rapid variation in the reactive power to be followed. It is better then to have a more elaborate means of compensation.



(a) Over excitation (b) Under excitation

FIGURE 25.1 Synchronous compensator: inductive and capacitative modes.

25.2.4.3 Thyristor-Switched Capacitor

This type of compensator consists of switching capacitors on and off by using static switches. But this type of switching will be possible only for a maximum value of supply voltage, which makes the waveform of the current sinusoidal at half the period at steady state. This means that the capacitors should be kept at maximum level obtained when the current goes to zero. The TSC shown in Fig. 25.2 may be commuted at zero voltage through the commuting of the thyristors and switched off when the current goes to zero; this type of control may be slow, since equating the supply capacitors voltages will lead to a delay in the action.

25.2.4.4 Thyristor-Controlled Reactor

This type of compensator is made up of an inductance supplied through an ac–ac converter made of two thyristors in antiparallel, as illustrated by Fig. 25.3. The TCR current is always inductive; it absorbs only reactive power. In general, TCR is associated with batteries so that it can absorb or supply reactive power, as shown by Fig. 25.4, which illustrates the characteristics of TCR.

The thyristor-controlled inductor, also called the thyristor-controlled reactor (TCR), is of considerable practical importance in an application area of power electronics in ac power systems that is commonly described as static-VAR compensation. VAR stands for "volt ampere reactive." In ac power networks, lagging reactive currents are undesirable because they cause excessive voltage drops and adversely affect stable operation. Therefore, steps are taken to compensate for lagging reactive currents by introducing leading reactive currents. In such schemes, it is now common to use thyristor-controlled inductors in a manner that we shall

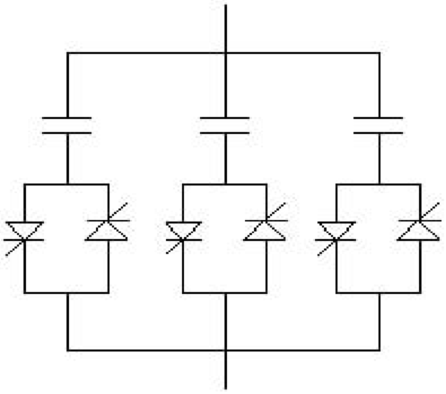


FIGURE 25.2 Configuration of the TSC.

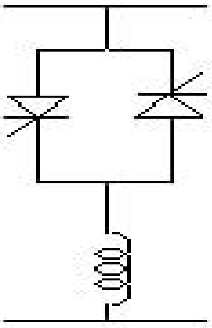


FIGURE 25.3 Configuration of the TCR.

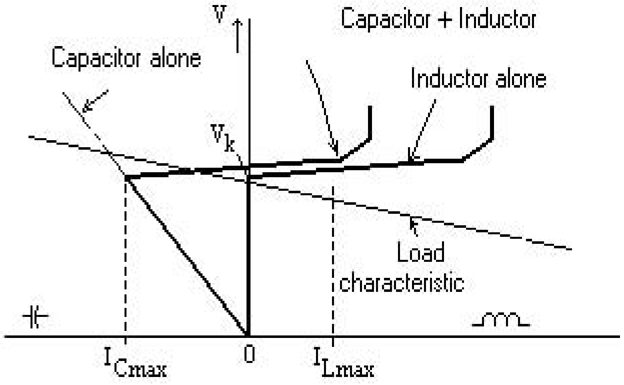


FIGURE 25.4 Characteristics: voltage–current TCR.

explain. Practical systems are three-phase. But it is best to describe the technique using the single-phase version.

The thyristor-controlled inductor is shown in Fig. 25.5a. It is a particular case, for $R = 0$, of the R–L load controlled by an ac switch that we considered earlier. When $R = 0$, the phase angle of the load $\phi = \pi/2$. Therefore, from the results of the case of R–L load, we find that phase control range of α is from $\pi/2$ to π Taking the reference zero of time as the instant labeled 0 in Fig. 25.5b and treating resistance as negligible, the voltage and the loop equation may be written as

$$v = -V_m \sin \omega t$$

$$\frac{di}{dt} = \frac{V_m}{L} \sin \omega t$$

The expression for the current can be obtained by integration as

$$i = \frac{V_m}{\omega L} \cos \omega t + A$$

where the constant A can be obtained from the initial condition, which may be stated (for $\alpha > \pi/2$) as

$$i = 0 \quad \text{at} \quad \omega t = -(\pi - \alpha)$$

This gives

$$A = \frac{V_m}{\omega L} \cos \alpha$$

With the constant A determined on this basis, the final expression for the current becomes

$$i = \frac{V_m}{\omega L} (\cos \alpha + \cos \omega t)$$

The TCI is used primarily as a means of obtaining an adjustable value of the fundamental lagging current. The waveform of the current can be sketched, and from symmetry considerations, we can see that Fourier analysis will give a cosine component that is a current lagging by $\pi/2$ with respect to the voltage. The amplitude of this fundamental component may be found by Fourier analysis as follows:

$$I_1 = \frac{2}{\pi} \int_{-(\pi-\alpha)}^{\pi-\alpha} \frac{V_m}{\omega L} (\cos \alpha + \cos \theta) \cos \theta \, d\theta$$

$$= \frac{V_m}{\omega L} \frac{2}{\pi} \left(\frac{1}{2} \sin 2\alpha + \pi - \alpha \right)$$

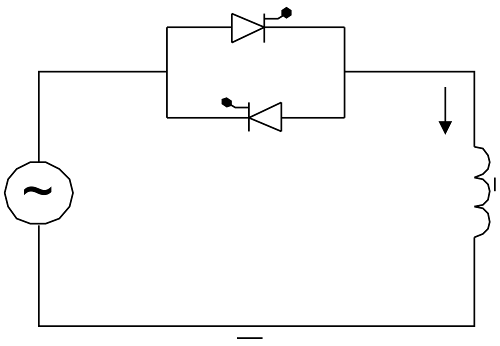


FIGURE 25.5a Thyristor-controlled reactor.

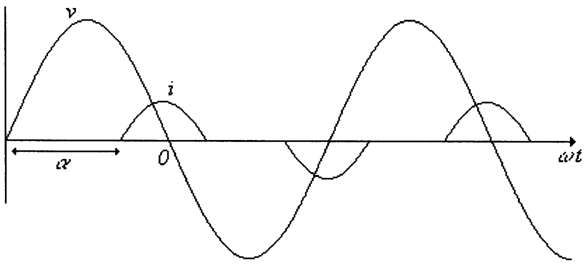


FIGURE 25.5b

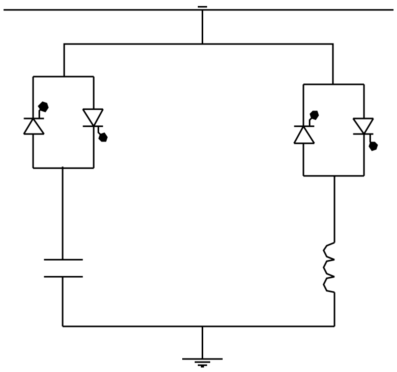


FIGURE 25.6 Static VAR compensation using TSC and TCI.

From this, we see that the maximum amplitude of I_1 occurs for $\alpha = \pi/2$ and is equal to $V_m/\omega L = \sqrt{2}V/\omega L$. This corresponds to an rms value of $V/\omega L$. The minimum value is zero at $\alpha = \pi$. Between these limits, the lagging current and so the lagging reactive VA are adjustable by variation of α.

25.2.4.5 Static VAR Compensation Circuit

Figure 25.6 shows the typical method of static VAR compensation. The leading reactive current necessary for VAR compensation is actually supplied by connecting capacitor banks across the ac lines. Before the development of thyristors, this was done using electromechanical circuit breakers. With the advent of thyristors, bidirectional ac switches using them were developed for connecting and disconnecting the capacitor banks. A capacitor bank connected in this way is called a thyristor-switched capacitor (TSC). The problem to be faced when connecting the capacitor to the high-voltage lines is the large inrush current that will flow at the moment of contact if there is a large instantaneous voltage differential between the line and the capacitor. It is relatively easy to overcome this difficulty, because the TSC uses static thyristor switches that can be gated at any desired instant in an ac cycle by means of a switching controller that will sense the voltage differential and gate the thyristor at the correct instant in the ac cycle when the voltage differential is within permissible limits.

If only TSCs are employed for VAR compensation, the leading VAR to be introduced can only be adjusted in steps, because the switching is to be done one capacitor bank at a time. For precise adjustments of VAR, as dictated by the system requirements, a continually variable feature is desirable. This is achieved in the scheme in Fig. 25.6 by having a thyristor-controlled reactor in parallel with the capacitor bank. If the maximum lagging current drawn by the TCI is equal to the leading reactive VA of the capacitor, the two will cancel and the net reactive VA will be zero. From this point, the lagging VAR of the TCI can be progressively decreased by phase control, thereby increasing the net leading VAR. After the maximum is reached, a further increase can be made by switching in another capacitor bank. In this manner, the TSCs provide VAR in steps, while the TCI will provide the continuous adjustment between steps. This scheme enables precise and fast automatic adjustment of the VAR by means of closed-loop control. A practical system will be invariably a three-phase network, although we have used the single-phase equivalent to describe the technique. Also, in a practical high-voltage system the TSCs and TCIs may be connected to the secondary side of a transformer. In this way, the maximum voltage requirements of the thyristors and the capacitors can be lowered.

25.3 Modeling and Analysis of an Advanced Static VAR Compensator

After introducing classical methods for compensating the reactive power, we propose a new concept, the advanced static VAR compensator [14], based on the exact equivalence with the classical rotating synchronous compensator. This type of compensator uses a source voltage type inverter with a capacitor in the dc side used as energy storage element. First a modeling and analysis of the compensator, which uses a programmed PWM with a constant conversion ratio, is undertaken. Then, the dynamic behavior of the system in the open-loop condition will be identified. Moreover, we apply this new concept of advanced static VAR compensation to improve the stability of a power system network, and prove this through a series of simulation tests.

The proposed ASVC system is modeled using the $d - q$ transform [7] and employs a programmed PWM voltage wave-shaping pattern, which can be easily stored in an EPROM to simplify the logic software and hardware requirements. The programmed PWM has the advantage that there are fewer harmonic components in the current, a better power factor, and lower switching frequencies, and thus less stress on switching devices and reduction of switching losses. At first, an identification of the dynamic behavior of the system in open loop will be the key to the synthesis of such an approach to control, and it will be shown that this control approach is more efficient for industry applications [15–16].

The control of the static VAR compensator (ASVC) system with self-controlled dc bus, which employs a three-phase PWM voltage source inverter, will be modeled and analyzed. Such an SVC is made up of a two-level voltage-source inverter and presents a fast response time and reduced harmonic pollution.

25.3.1 Main Operating Principles of the ASVC

25.3.1.1 Main Circuit Configuration

The major ASVC system component is a three-phase PWM forced commutated voltage source inverter as shown in

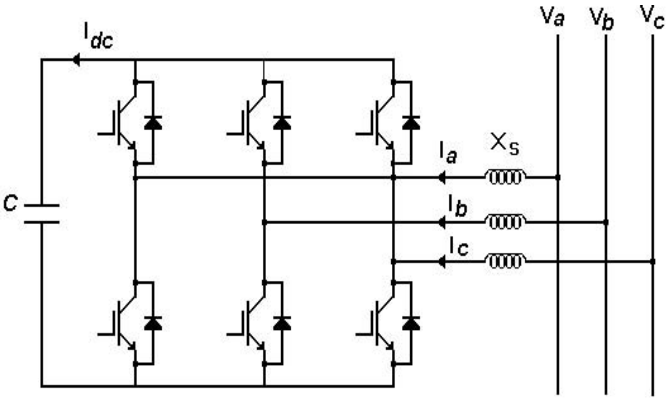


FIGURE 25.7 Main circuit of ASVC.

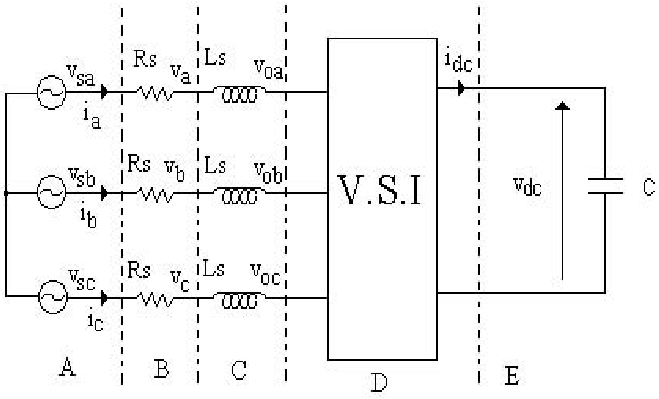


FIGURE 25.8 Equivalent circuit.

Fig. 25.7. The ac terminals of the inverter are connected to the ac mains through a first-order low-pass filter. Its function is to minimize the damping of current harmonics on utility lines. The dc side of the converter system is connected to a dc capacitor, which carries the input ripple current of the inverter and is the main reactive energy storage element. The dc supply provides a constant dc voltage and the real power necessary to cover the losses of the system.

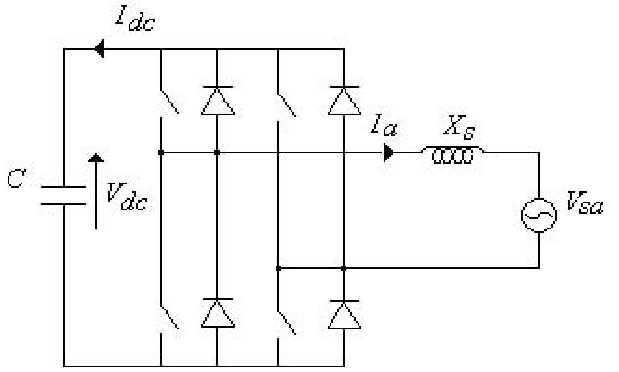


FIGURE 25.9 Equivalent single-phase circuit of the ASVC.

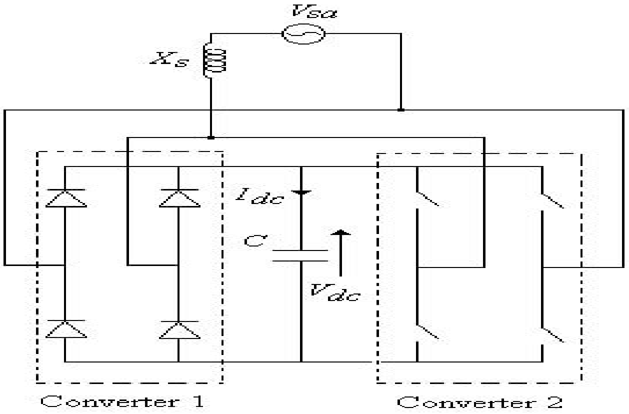


FIGURE 25.10 ASVC single phase diagram as a combination of two converters.

Figure 25.8 shows a simplified equivalent circuit of the ASVC. In this representation, the series inductance L_s accounts for the leakage of the transformer and R_s represents the active losses of the inverter and transformer. C is the capacitor on the dc side. The inverter is assumed to be lossless. V_{oa} and V_{sa} are the amplitude of the fundamental of the output voltage of the converter and phase voltage of the supply, respectively.

25.3.1.2 Operating Principles

The operating principles of the ASVC can be explained by using its equivalent single-phase circuit given by Fig. 25.9, which is inherently a combination of two converters as shown in Fig. 25.10 after rearrangement of the circuit of Fig. 25.9.

If the fundamental component of the output voltage of the inverter V_{oa} is in phase with the supply voltage V_{sa}, the current flowing out the ASVC or toward the ASVC is always at 90° to the network voltage because of reactive coupling. According to the circuit shown in Fig. 25.10, converter 1 operates as an uncontrollable rectifier through which a small quantity of real power flows from the ac to dc side, and converter 2 operates as an inverter when the real power flows in the reverse direction. Initially, when the converter 2 is not conducting, the capacitor C is charged up to the peak value of supply voltage through converter 1, and remains at this voltage for as long as there is no real power transfer between the circuit and the supply. If the switches of converter 2 are operated to obtain the fundamental of the ASVC output voltage slightly leading the ac main voltage, converter 2 conducts for a superior period to the

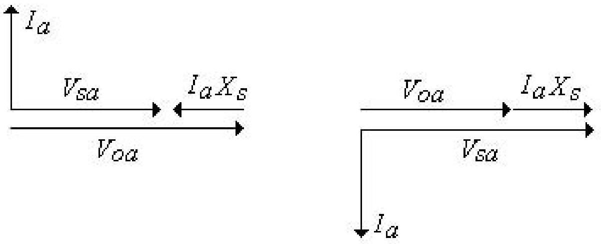


FIGURE 25.11 Phasor diagram for leading and lagging mode.

one of the converter 1, causing a transfer of real power from the dc side to the ac side. In this way the dc capacitor voltage is decreased, and a reactive power is absorbed by the ASVC system (lagging mode).

The inverse is true when the fundamental of the ASVC output voltage slightly lags the supply voltage: The dc capacitor voltage is increased, and a reactive power is generated by the ASVC (leading mode). We can conclude that the reactive power either generated or absorbed by the ASVC can be controlled only by one parameter: the phase angle between the ASVC output voltage and the supply voltage.

Thus, as indicated by the phasor diagram shown in Fig. 25.11, when the amplitude of the inverter output voltage V_{oa} is smaller than the supply voltage V_{sa}, the reactive power is absorbed by the ASVC. Otherwise, the ASVC generates the reactive power when the amplitude of the supply voltage is larger than the output voltage of the inverter.

25.3.2 Modeling of the ASVC System

To achieve an easier modeling of the system [24], the original circuit is subdivided in several basic subcircuits as shown in Fig. 25.8.

25.3.2.1 Transform of Part A

The three-phase supply voltages are given by the following equation:

$$v_{s,abc} = \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} = \sqrt{2/3}V_s \begin{bmatrix} \sin(\omega t - \alpha) \\ \sin(\omega t - 2\pi/3 - \alpha) \\ \sin(\omega t + 2\pi/3 - \alpha) \end{bmatrix} \qquad (25.1)$$

where α is the phase angle difference between the source voltages and those of the inverter. In the $d - q$ frame:

$$v_{s,qdo} = Kv_{s,abc} = V_s \begin{bmatrix} -\sin\alpha \\ \cos\alpha \\ 0 \end{bmatrix} \qquad (25.2)$$

With:

$$K = \sqrt{2/3} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \\ \sin(\omega t) & \sin(\omega t - 2\pi/3 & \sin(\omega t + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}$$

25.3.2.2 Transform of Part B

The relationship between the voltage and the current in the part of the resistor

$$v_{s,abc} = R_s i_{abc} + v_{abc} \qquad (25.3)$$

The $d - q$ transform of (25.3) yields

$$v_{s,qdo} = R_s i_{qdo} + v_{qdo} \qquad (25.4)$$

25.3.2.3 Transform of Part C

The relationship between the voltage and the current in the part of inductor L_s is

$$L_s \frac{d}{dt}(i_{abc}) = v_{abc} - v_{o,abc} \qquad (25.5)$$

The $d - q$ transform of (25.5) yields

$$L_s \frac{d}{dt}(i_{qdo}) = L_s \frac{d}{dt}(K)K_{-1} i_{qdo} + v_{qdo} - v_{o,qdo} \qquad (25.6)$$

$$L_s \frac{d}{dt}(i_q) = -\omega L_s i_d + v_q - v_{oq} \qquad (25.7)$$

$$L_s \frac{d}{dt}(i_d) = \omega L_s i_q + v_d - v_{od} \qquad (25.8)$$

Assembling parts B and C:

$$\frac{d}{dt}\begin{bmatrix} i_q \\ i_d \end{bmatrix} = \begin{bmatrix} -\dfrac{R_s}{L_s} & -\omega \\ \omega & -\dfrac{R_s}{L_s} \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \frac{1}{L_s}\begin{bmatrix} v_{sq} - v_{oq} \\ v_{sd} - v_{od} \end{bmatrix} \qquad (25.9)$$

25.3.2.4 Transform of Parts D and E

Under the assumption that harmonic components generated by the switching pattern are negligible, the switching function S can be defined as follows:

$$S = \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} = \sqrt{2/3}m \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - 2\pi/3) \\ \sin(\omega t + 2\pi/3) \end{bmatrix} \qquad (25.10)$$

The modulation index, being constant for a programmed PWM, is given by:

$$IM = v_{o,peak}/v_{dc} = \sqrt{2/3}m \qquad (25.11)$$

The inverter output voltages are given by

$$v_{o,abc} = Sv_{dc} \qquad (25.12)$$

In the $d - q$ axis:

$$v_{o,qdo} = KSv_{dc} = m \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} v_{dc} \qquad (25.13)$$

So Eq. 25.9 can be written as follows:

$$\frac{d}{dt}\begin{bmatrix} i_q \\ i_d \end{bmatrix} = \begin{bmatrix} -\dfrac{R_s}{L_s} & -\omega \\ \omega & -\dfrac{R_s}{L_s} \end{bmatrix}\begin{bmatrix} i_q \\ i_d \end{bmatrix} + \frac{1}{L_s}\begin{bmatrix} -V_s \sin\alpha \\ V_s \cos\alpha - m v_{dc} \end{bmatrix} \tag{25.14}$$

The dc side current in the capacitor is given by

$$i_{dc} = S^T i_{abc} \tag{25.15}$$

In the $d-q$ axis

$$i_{dc} = S^T K^{-1} i_{qdo} = m[0 \quad 1 \quad 0]\begin{bmatrix} i_q \\ i_d \\ i_o \end{bmatrix} \tag{25.16}$$

$$i_{dc} = m i_d \tag{25.17}$$

The relationship between the voltage and the current in the dc side is given by:

$$i_{dc} = C\frac{dv_{dc}}{dt} \tag{25.18}$$

Thus, replacing Eq. (25.17) in (25.18), we will have:

$$\frac{dv_{dc}}{dt} = \frac{m}{C} i_d \tag{25.19}$$

Collecting all parts of the system, while introducing the third equation (25.19) (the model of the dc part in the system), the complete mathematical model of the ASVC in the $d-q$ axis will be as follows:

$$\frac{d}{dt}\begin{bmatrix} i_q \\ i_d \\ v_{dc} \end{bmatrix} = \begin{bmatrix} -\dfrac{R_s}{L_s} & -\omega & 0 \\ \omega & -\dfrac{R_s}{L_s} & \dfrac{m}{L_s} \\ 0 & \dfrac{m}{C} & 0 \end{bmatrix}\begin{bmatrix} i_q \\ i_d \\ v_{dc} \end{bmatrix} + \frac{v_s}{L_s}\begin{bmatrix} -\sin\alpha \\ \cos\alpha \\ 0 \end{bmatrix} \tag{25.20}$$

From equation system (25.20), we can extricate the following expressions:

$$i_q(p) = \frac{-V_s\left[p_2\dfrac{\sin\alpha}{L_s} + p\left(\dfrac{R_s}{L_s^2}\sin\alpha + \dfrac{\omega}{L_s}\cos\alpha\right) + \dfrac{m_2}{L_s^2 C}\sin\alpha\right]}{p_3 + 2p_2\dfrac{R_s}{L_s} + p\left(\omega_2 + \dfrac{R_s^2}{L_s^2} + \dfrac{m_2}{L_s C}\right) + m_2\dfrac{R_s}{L_s^2 C}} \tag{25.21}$$

$$i_d(p) = \frac{V_s\left[p_2\dfrac{\cos\alpha}{L_s} + p\left(\dfrac{R_s}{L_s^2}\cos\alpha - \dfrac{\omega}{L_s}\sin\alpha\right)\right]}{p_3 + 2p_2}$$

$$\frac{R_s}{L_s} + p\left(\omega_2 + \frac{R_s^2}{L_s^2} + \frac{m_2}{L_s C}\right) + m_2\frac{R_s}{L_s^2 C} \tag{25.22}$$

$$v_{dc}(p) = mV_s\frac{\left[p\dfrac{\cos\alpha}{L_s C} + \dfrac{R_s}{L_s^2 C}\cos\alpha - \dfrac{\omega}{L_s C}\sin\alpha\right]}{p_3 + 2p_2\dfrac{R_s}{L_s} + p\left(\omega_2 + \dfrac{R_s^2}{L_s^2} + \dfrac{m_2}{L_s C}\right) + m_2\dfrac{R_s}{L_s^2 C}} \tag{25.23}$$

Expressions of real and reactive power are given by

$$p_c(p) = v_{sq}i_q + v_{sd}i_d = -V_s(i_q\sin\alpha - i_d\cos\alpha) \tag{25.24}$$

$$q_c(p) = v_{sq}i_d - v_{sd}i_q = -V_s(i_d\sin\alpha + i_q\cos\alpha) \tag{25.25}$$

25.3.3 The ASVC Behavior in Steady State

Equations governing the steady-state behavior of the ASVC can be obtained by equating the term of derivatives in the mathematical model given by Eq. (25.20) to zero, which is similar to short-circuiting the inductors and opening the capacitor, so we will have:

$$i_q = \frac{V_s\sin\alpha}{R_s} \tag{25.26}$$

$$i_d = 0 \tag{25.27}$$

$$v_{dc} = \frac{V_s}{m}\left(\cos\alpha\frac{\omega L_s}{R_s}\sin\alpha\right) \tag{25.28}$$

$$p_c = \frac{V_s^2\sin^2\alpha}{R_s} \tag{25.29}$$

$$q_c = \frac{V_s^2\sin\alpha\cos\alpha}{R_s} \tag{25.30}$$

We note that the active and reactive power depend only on the square of the supply voltage and the resistor of coupling of the ASVC to the ac mains, and are independent of the other parameters of the circuits (L_s and C). In addition, the dc side

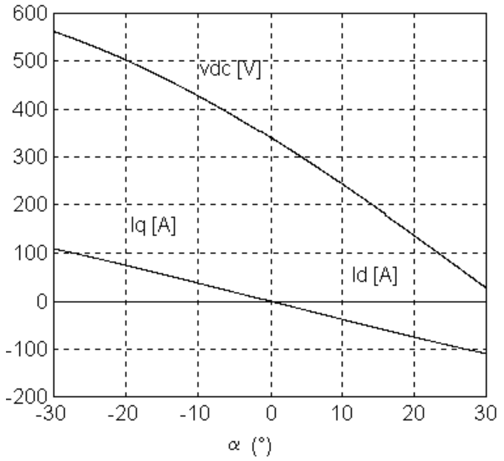


FIGURE 25.12 Steady-state values.

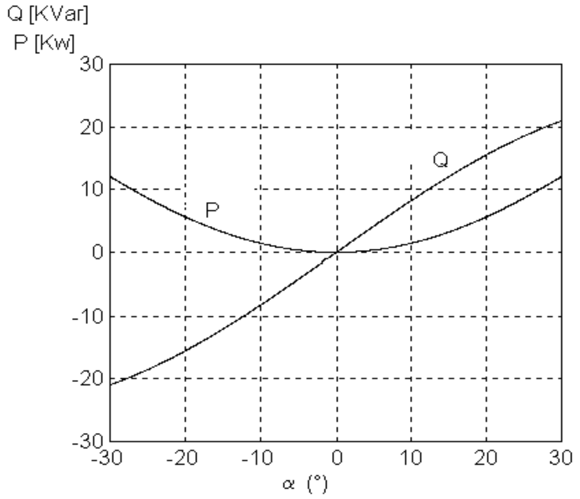


FIGURE 25.13 Real, reactive power in steady state.

voltage depends on α, the modulation index, and the resistor and inductor of the coupling, but is independent of the value of the dc capacitor. The system parameters are given by

$$\text{Supply: } V_s = 220\ \text{V}, \quad f = 50\ \text{Hz}, \quad R_s = 1\ \Omega, \quad L_s = 5\ \text{mH}$$

$$\text{DC side: } C = 500\ \mu\text{F} \quad m = 1.12/\sqrt{3}$$

By varying the angle α in an interval of $-30°$ to $+30°$ which is the linear zone for sine and cosine, we obtain the following responses. Figure 25.12 shows i_q, i_d, and v_{dc} values for different values of α, where we can note that the real current i_d is always zero; on the other hand, the reactive current i_q and the dc voltage v_{dc} are linear according to α.

Figure 25.13 shows the real and the reactive power flowing from or to the ASVC for different values of α, where it is clear that the reactive power has a linear variation according to α, and the real power always exists to cover the losses in the system and to maintain the dc side voltage at the operating level.

25.3.4 ASVC Behavior in Transient State

Taking as an initial condition for the dc side voltage the maximum voltage of the supply, a series of dynamic responses of the system to step changes of ±10° of the angle α have been established [17]: Figure 25.14 shows the response of the reactive current i_q to a step change of $\alpha = -10°$ for Fig. 25.14a and $\alpha = +10°$ for Fig. 25.14b, which after a short transient state attains a stable value of 38 A supplied to the network.

Figure 25.15 shows the response of the dc side voltage v_{dc} to a step change of ($\alpha = -10°$ for Fig. 25.15a and $\alpha = +10°$ for Fig. 25.15b, in which attains a value greater than that of the network: capacitive mode. Figure 25.16 shows the response of the active current i_d ($\alpha = -10°$ for Fig. 25.16a and $\alpha = +10°$ for Fig. 25.16b), which, after the voltage v_{dc} reaches its stable value, it goes to zero, because its action on the transient state is only for charging and discharging the dc side capacitor. Figure

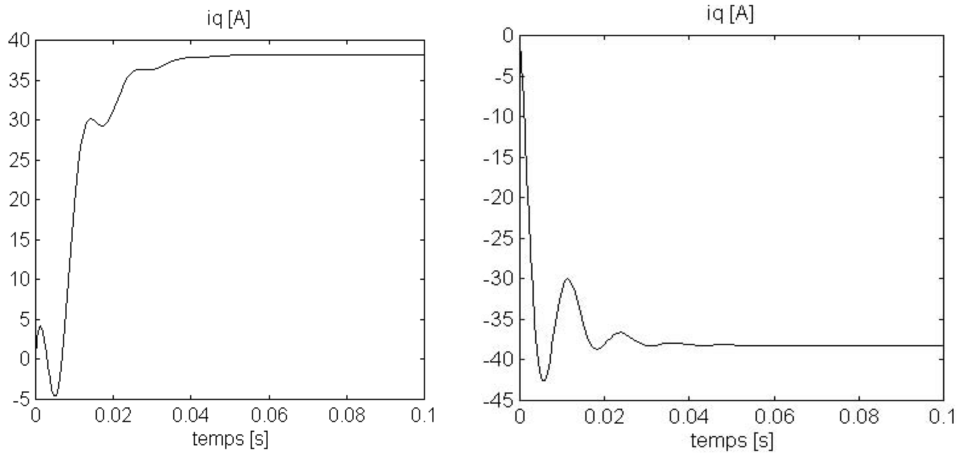


FIGURE 25.14 Transient reactive current response.

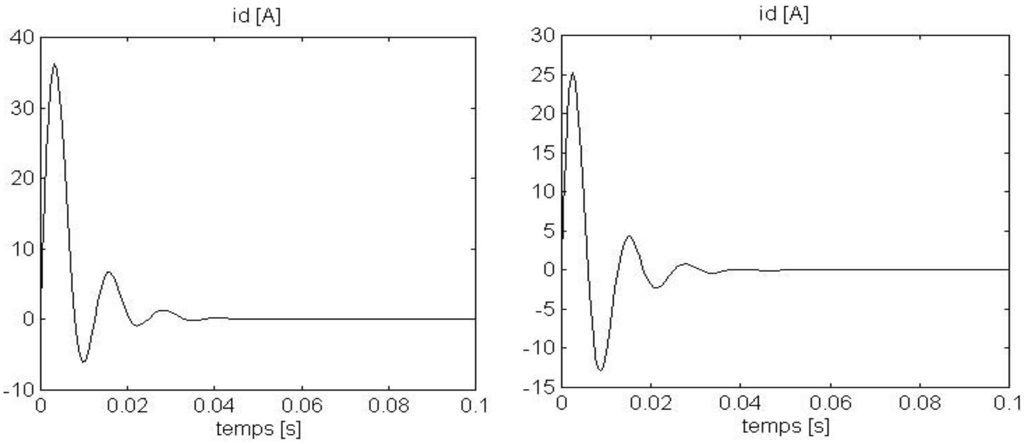


FIGURE 25.15 Active current response to change of α.

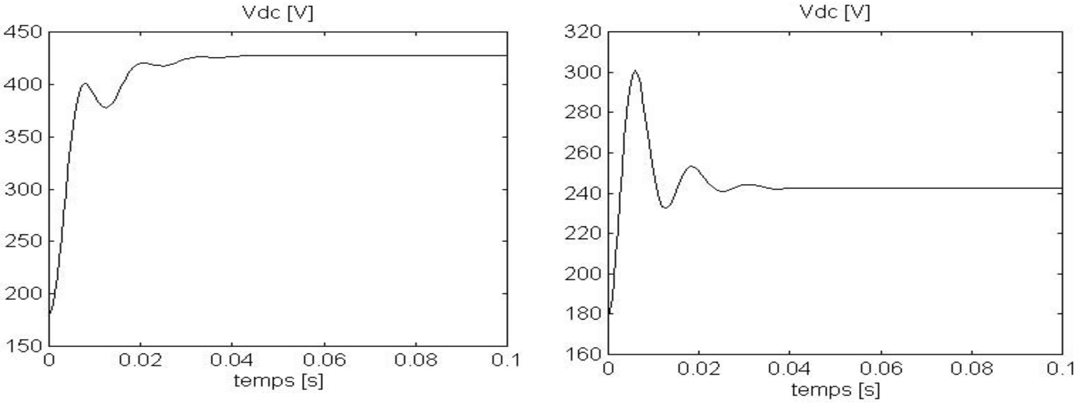


FIGURE 25.16 Dc side voltage response to change of α (°).

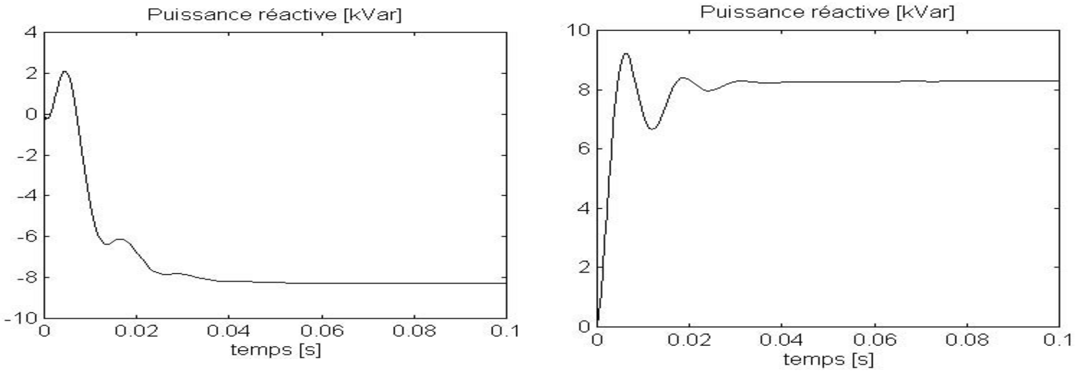


FIGURE 25.17 Reactive power response to change of α.

TABLE 25.1 Switching angles

α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8	α_9	α_{10}	α_{11}
4.4°	10.8°	14.1°	21.1°	23.4°	31.6°	33°	42.3°	43.1°	65.9°	66.3°

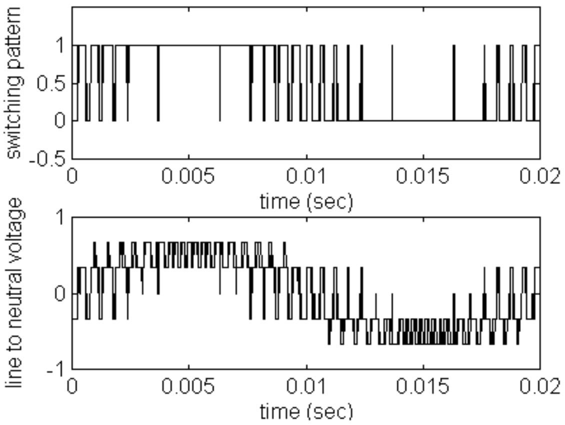


FIGURE 25.18 Switching pattern and line to neutral voltage.

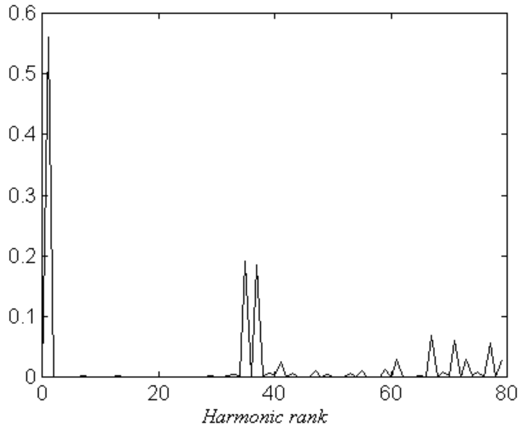


FIGURE 25.19 Harmonic spectrum of line–neutral voltage.

25.17 shows the behavior of the reactive power to a step change of $\alpha = -10^\circ$ for Fig. 25.17a and $\alpha = +10^\circ$ for Fig. 25.17b), which after two cycles reaches a stable value of -8.47 kVar supplied to the network capacitive mode and $+8.47$ kVar for the inductive mode.

A programmed PWM switching pattern, which allows the elimination of a selected number of harmonics, is continuously applied to the six controlled switches (Table 25.1). This method is used because it offers better voltage utilisation and lower switching frequencies, and thus less stress on switching devices and reduction of the switching losses (increase of the efficiency of the converter). For our work, we use a programmed PWM with the parameters given by MI (modulation index) = 1.12.

Figure 25.18 shows the switching pattern, and the corresponding line to neutral output inverter voltage. Figure 25.19 shows the harmonic spectrum of the output inverter voltage, where it is clear that the elimination of harmonics is verified.

The advantages of this programmed PWM over the classical PWM are as follows:

1. Nearly 50 reduction of switching frequency
2. Possibility of high voltage gain due to overmodulation
3. Dc side-current ripples low because of high quality of current and voltage waveforms
4. Reduction of the PWM frequency, which lowers the switching losses and thus can be used for high-power applications
5. Elimination of low-order harmonics, which allows avoiding resonance.

25.3.5 Controller Design

The controller design of the ASVC is based on the linearized model of the system under the following assumptions:

- Disturbance α_Δ is small.
- The second-order terms are dropped.
- The quiescent operating α_0 is near zero.

The trigonometric nonlinearities are treated as follows:

$$\begin{aligned}\cos(\alpha_0 + \alpha_\Delta) &= \cos\alpha_0 \cos\alpha_\Delta - \sin\alpha_0 \sin\alpha_\Delta \\ \sin(\alpha_0 + \alpha_\Delta) &= \cos\alpha_0 \sin\alpha_\Delta + \sin\alpha_0 \cos\alpha_\Delta\end{aligned} \tag{25.31}$$

After development and simplification, the linearized model in state space is given by

$$\begin{aligned}X_\Delta &= AX_\Delta + BU_\Delta \\ q_{c\Delta} &= C_\Delta X_\Delta\end{aligned} \tag{25.32}$$

with

$$X_\Delta = \begin{bmatrix} i_{q\Delta} \\ i_{d\Delta} \\ v_{dc\Delta} \end{bmatrix},$$

$$A = \begin{bmatrix} -\dfrac{R_s}{L_s} & -\omega & 0 \\ \omega & -\dfrac{R_s}{L_s} & -\dfrac{m}{L_s} \\ 0 & \dfrac{m}{C} & 0 \end{bmatrix},$$

$$B = \begin{bmatrix} -\dfrac{V_s}{L_s} \\ 0 \\ 0 \end{bmatrix},$$

$$U_\Delta = \alpha_\Delta,\ C_\Delta = [-V_s \quad 0 \quad 0]$$

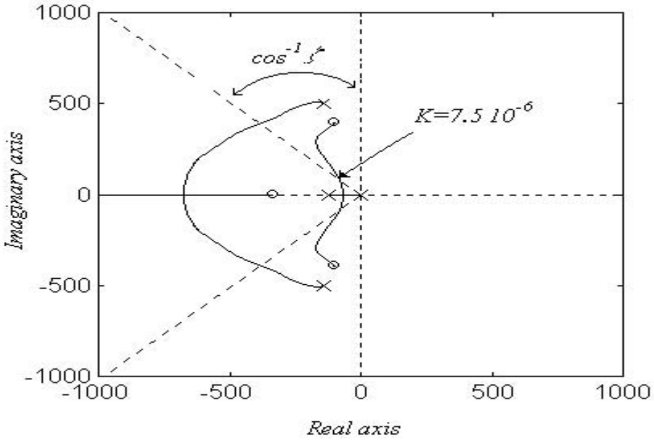


FIGURE 25.20 PI design criteria by root locus.

The transfer function relating the reactive power $q_{c\Delta}$ to the angle α_Δ is given by

$$G(p) = \frac{q_{c\Delta}(p)}{\alpha_\Delta(p)} = C_\Delta[pI - A]^{-1}B$$

$$G(p) = \frac{V_s^2\left[\frac{p^2}{L_s} + p\frac{R_s}{L_s} + \frac{m^2}{L_s^2 C}\right]}{p^3 + 2p^2\frac{R_s}{L_s} + p\left(\omega^2 + \frac{R_s^2}{L_s^2} + \frac{m^2}{L_s C}\right) + m^2\frac{R_s}{L_s^2 C}} \qquad (25.33)$$

Thus the PI controller is conceived so that the ASVC has a desired dynamic performance. The PI transfer function is

$$F_{PI}(p) = K\left(1 + \frac{1}{T_i p}\right) \qquad (25.34)$$

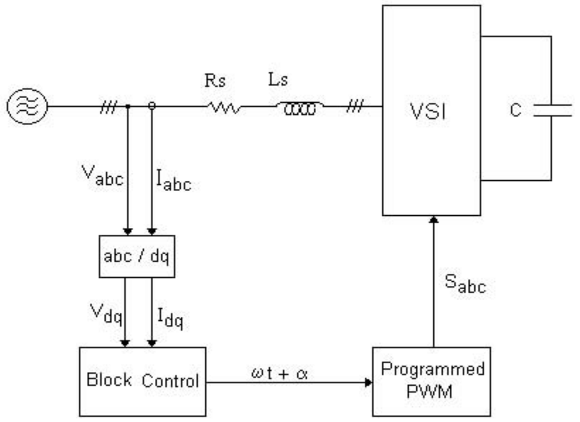

Rs
Ls
VSI
C
Vabc
Iabc
abc / dq
Vdq
Idq
Sabc
Block Control
ωt + α
Programmed PWM

FIGURE 25.21 Main and control circuit for the proposed system.

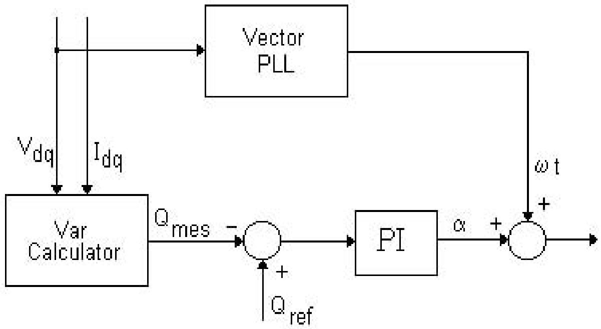

Vector PLL
Vdq
Idq
ωt
+
Var Calculator
Qmes
−
PI
α
+
+
Qref

FIGURE 25.22 Details of the control block diagram.

The closed-loop transfer function of PI associated with the transfer function of the ASVC is given by

$$[F_{PI}G]_{BF}(p) = \frac{F_{PI}G}{1 + F_{PI}G} \qquad (25.35)$$

If we take $T_i = 0.003$, Fig. 25.20 shows the root locus for K varying from zero to infinity. The value of K that gives us a closed loop response with a damping factor $\zeta = 0.7$ is

$$K = 7.5 \times 10^{-6}$$

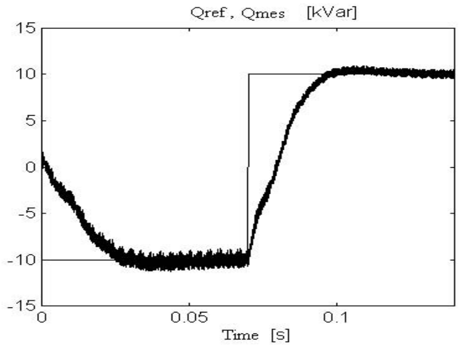


FIGURE 25.23 Simulated reactive power response.

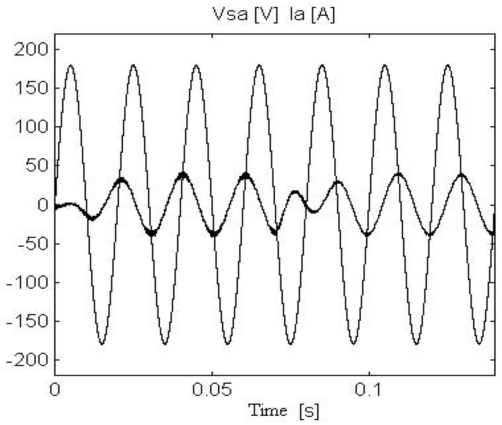


FIGURE 25.24 Simulated current and voltage waveforms.

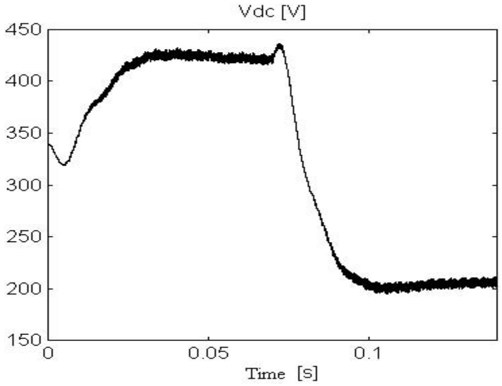


FIGURE 25.25 Simulated inverter dc bus voltage.

The parameters of the PI controller are

$$K_p = K = 7.5 \times 10^{-6}$$
$$K_I = \frac{K}{T_i} = 2.5 \times 10^{-3}$$

25.3.6 Proposed Control Block Diagram

Figure 25.21 shows the main control circuit of the system, representing the different blocks constituting the control system. Details of the control block are illustrated by Fig. 25.22. The source voltage and the ASVC currents are transformed in the $d - q$ axis for calculating the reactive power generated by the system, which is compared to the reference; the vector PLL detects the phase angle of the supply, which is added to the control variable α (output of the PI controller). This sum adjusts the reading frequency of the counter connected to the EPROM where the switching pattern is stored.

To verify key analytical results and the validity of the proposed control scheme [10,18], the aforementioned ASVC structure was tested on a Pentium personal computer. Computer simulation was carried out using Matlab, with the system parameters given by

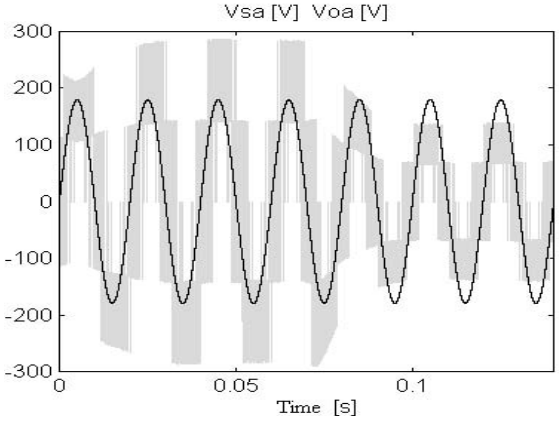


FIGURE 25.26 Simulated inverter line to neutral and source voltage.

Supply: $V_s = 220$ V, $f = 50$ Hz, $R_s = 1\ \Omega$, $L_s = 5$ mH;
dc side: $C = 500\ \mu$F;
PI controller: $K_P = 7.5 \times 10^{-6}$, $K_I = 2.5 \times 10^{-3}$

Testing of the ASVC system shown in Fig. 25.21 was performed for dynamic response. The amplitude of the reference was adjusted to cause the system to swing from leading to lagging mode. Figure 25.23 shows the simulated reactive power response to a reference change from 10 kVar lagging to 10 kVar leading. Performance evaluation of the subject model was also tested for current and voltage responses to step changes. Figure 25.24 shows the simulated current and voltage waveforms to a step reference change from 10 kVar lagging to 10 kVar; leading, this figure confirms that the compensator time response is fast (about 10 ms).

The dc side voltage response to the same change is depicted in Fig. 25.25. Figure 25.26 shows the simulated inverted output voltage and voltage source waveforms to a step reference change from 10 kVar lagging to 10 kVar leading and how the inverter output voltage responds during transients.

25.3.7 Conclusion

A new model of advanced static VAR compensator has been developed. A fast control approach of the ASVC system has been implemented for applications that require leading or lagging power compensation. The proposed control strategy is based on an explicit control of the reactive power implicit in the voltage amplitude of the capacitor of the dc side and is more flexible. The simulation results show that this control strategy has good dynamic performance for generating or consuming of the reactive power.

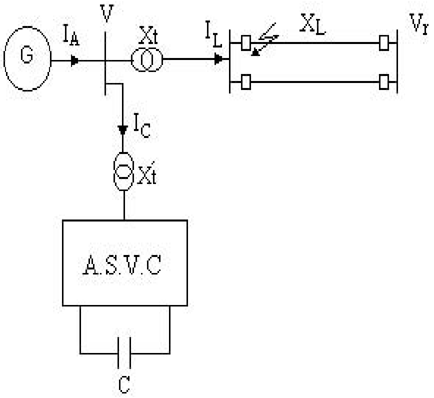


FIGURE 25.27 Schematic diagram of the network ASVC.

25.4 Static VAR Compensator for the Improvement of Stability of a Turbo Alternator

The requirement to design and operate power systems with the highest degree of efficiency, security, and reliability has been the central focus for the power system designer ever since interconnected networks came into existence. To satisfy these requirements, various advances in the technology of ac power transmission have taken place in the context of effective control of reactive power and its compensation. The static VAR compensator (SVC's) is a dynamic reactive power compensation device. Recent developments in solid-state VAR compensators have led to the hope of achieving very efficient control of reactive power. This stems from the fact that the voltage is maintained constant within a specified level, to improve the dynamic stability of the power system and its power factor as well as correcting the phase unbalance. In this section, we will study the case when disturbances occur at the studied machine without affecting the behavior of the other machines (that is, speed and emf are constants). This means that the voltage and frequency of the network can be considered constant. The turbo-alternator is then connected to a distribution network called "infinite."

25.4.1 Mathematical Model of the Network ASVC

Based on Fig. 25.27 we can establish the following equations:

- Machine side:

$$\begin{cases} V_d = -p\Phi_d - \omega\Phi_q - \Phi_q p\delta' - R_a i_{dA} \\ V_q = -p\Phi_q + \omega\Phi_d + \Phi_d p\delta' - R_a i_{qA} \end{cases} \tag{25.36}$$

- Network side:

$$\begin{cases} V_{rd} = V_d - Ri_{dL} - Lpi_{dL} - L\omega i_{qL} - Li_{qL}p\delta' \\ V_{rq} = V_q - Ri_{qL} - Lpi_{qL} + L\omega i_{dL} + Li_{dL}p\delta' \end{cases} \tag{25.37}$$

- ASVC side:

$$\begin{cases} V_{cd} = V_d - R_s i_{dC} - L_s pi_{dC} - L_s\omega i_{qC} \\ V_{cq} = V_q - R_s i_{qC} - L_s pi_{qC} + L_s\omega i_{dC} \end{cases} \tag{25.38}$$

$$\begin{cases} pi_{dc} = \dfrac{1}{L_s}[V_d - V_{Cd} - R_s i_{dC} - L_s\omega i_{qC}] \\ pi_{qc} = \dfrac{1}{L_s}[V_q - V_{Cq} - R_s i_{qC} + L_s\omega i_{dC}] \end{cases} \tag{25.39}$$

with

$$\begin{aligned} i_{dL} &= i_{dA} - i_{dC} \\ i_{qL} &= i_{qA} - i_{qC} \end{aligned} \tag{25.40}$$

By putting (25.40) into (25.37), we get

$$\begin{aligned} V_{rd} &= V_d - R(i_{dA} - i_{dC}) - Lp(i_{dA} - i_{dC}) \\ &\quad - L\omega(i_{qA} - i_{qC}) - L(i_{qA} - i_{qC})p\delta' \\ V_{rq} &= V_q - R(i_{qA} - i_{qC}) - Lpi_{qA} + Lpi_{qC} \\ &\quad - L\omega(i_{dA} - i_{dC}) - L(i_{dA} - i_{dC})p\delta' \end{aligned} \tag{25.41}$$

By developing (25.41) and replacing by (25.39) and after a tedious calculation, we obtain the complete model of the infinite bus bar network with ASVC (or ASVC) :

$$\begin{aligned} pi_{dA} = \Bigg[& \sqrt{2}v_r \sin\delta' - \left(\xi\left(R_a + \frac{B}{\tau'_{do}} + \frac{D}{\tau''_{do}}\right) + R\right)i_{dA} \\ & + \xi\left(-\omega'\Phi_{q2} + \frac{\Phi_{d2}}{\tau'_{do}} + \frac{\Phi_{d3}}{\tau''_{do}}\right) \\ & - \omega'(L + \xi F)i_{qA} - \xi\left(\frac{C}{\tau'_{do}} + \frac{E}{\tau''_{do}}\right)v_f + \lambda i_{dC} \\ & - \frac{L}{L_s}v_{Cd} \Bigg] \Big/ (L + \xi A) \end{aligned} \tag{25.42}$$

$$\begin{aligned} pi_{qA} = \Bigg[& -\sqrt{2}v_r \cos\delta' - \left(\xi\left(R_a + \frac{G}{\tau''_{qo}}\right) + R\right)i_{qA} \\ & + \xi\left(\omega'\phi_{d2} + \omega'\Phi_{d3} + \frac{\Phi_{q2}}{\tau''_{qo}}\right) \\ & + \omega'(L + \xi A)i_{dA} + \lambda i_{qC} - \frac{L}{L_s}v_{Cq} \Bigg] \Big/ (L + \xi F) \end{aligned} \tag{25.43}$$

$$p\Phi_{d2} = (Bi_d Cv_f - \Phi_{d2})/\tau'_{do} \tag{25.44}$$

$$p\Phi_{d3} = (Di_d + Ev_f - \Phi_{d3})/\tau''_{do} \tag{25.45}$$

$$p\Phi_{q2} = (Gi_q - \Phi_{q2})/\tau''_{qo} \tag{25.46}$$

$$p\delta' = \omega' - \omega \tag{25.47}$$

$$p\omega' = (C_m - C_e)/J \tag{25.48}$$

with

$$\xi = \left(1 + \frac{L}{L_s}\right) \quad \text{and} \quad \lambda = \left(R - L\frac{R_s}{L_s}\right)$$

The model of the ASVC is established by taking the voltage of the bus bar as a reference. Hence, we get

$$v_{C,dqo} = KSv_{dc} = m\begin{bmatrix} \sin\alpha \\ \cos\alpha \\ 0 \end{bmatrix} v_{dc} \tag{25.49}$$

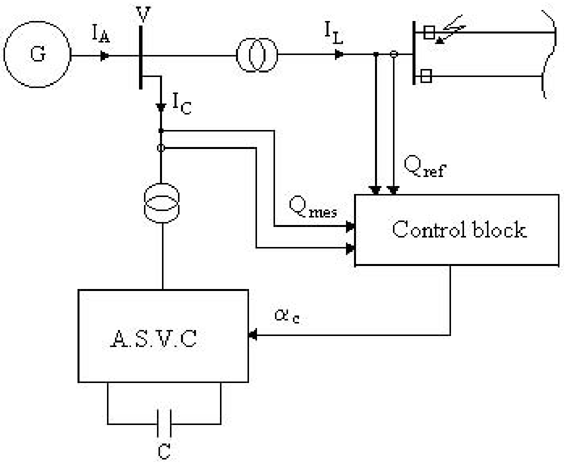


FIGURE 25.28 Main circuit of the control strategy.

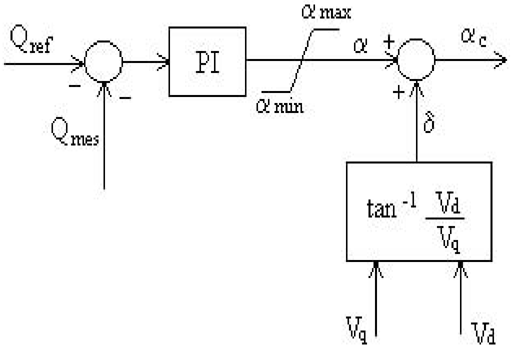


FIGURE 25.29 Details of the control block.

with

$$S = \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} = 2/3m \begin{bmatrix} \sin(\omega t + \alpha) \\ \sin(\omega t + \alpha - 2\pi/3) \\ \sin(\omega t + \alpha + 2\pi/3) \end{bmatrix} \tag{25.50}$$

The current of the dc side capacitor is given (in the Park axis) by

$$i_{dc} = S^T K^{-1} i_{qdo} = m(i_q \sin\alpha + i_d \cos\alpha) \tag{25.51}$$

Hence, the dc side voltage is given by

$$v_{dC} = \frac{m}{pC}(i_{qC}\sin\alpha + i_{dC}\cos\alpha) \tag{25.52}$$

Thus, the model of the ASVC is given as

$$pi_{dC} = (-R_s i_{dC} - \omega' L_s i_{qC} - m v_{dC}\sin(\alpha_c) + v_d)/L_s \tag{25.53}$$

$$pi_{qC} = (-R_s i_{qC} - \omega' L_s i_{dC} - m v_{dC}\cos(\alpha_c) + v_q)/L_s \tag{25.54}$$

$$pv_{dC} = m(i_{dC}\sin(\alpha_c) + i_{qC}\cos(\alpha_c))/C \tag{25.55}$$

with $\alpha_c = \alpha + \delta$, since we have taken the voltage of the bus bar as a reference for the ASVC, i.e., on the phasor diagram the voltages of the ASVC are synchronized to those of the bus bar considered. Hence, our model will be made up of 10 differential equations, seven for the alternator and three for the ASVC. For the initialization of the system, we take for the machine the same conditions given in [13–21], and for the ASVC the following initial conditions:

$$v_{dC} = \frac{\sqrt{2}v}{m}$$

$$i_{dC} = 0$$

$$i_{qC} = 0$$

25.4.2 Proposed Control Strategy

Figure 25.28 shows the main principles of the proposed control of the ASVC: the reactive power demanded is always compensated partly by the capacitive reactive power generated by the ASVC. This method of compensation help ease the alternator and increase the security boundary for the heating of the rotor circuit. Figure 25.29 gives the details of the control block diagram. The reactive power demanded, being inductive, must be compensated by the capacitive reactive power generated by the ASVC.

A PI regulator controls this compensation, which synthesizes the control variable α, which is added to the angle δ that is necessary for synchronizing with the voltages of the bus bar considered. This sum, being α_c, is applied to the ASVC to

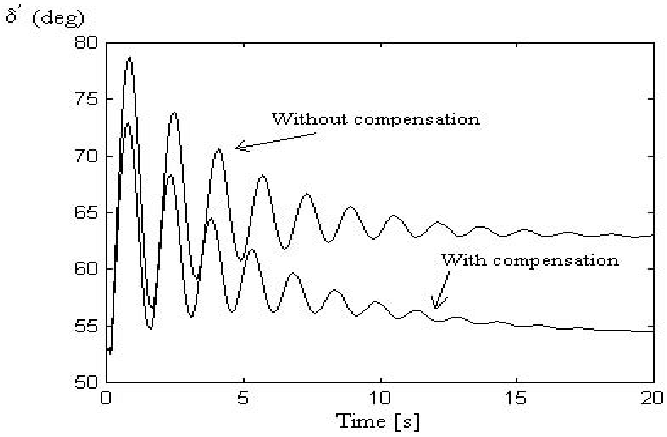


FIGURE 25.30 Load angle variation.

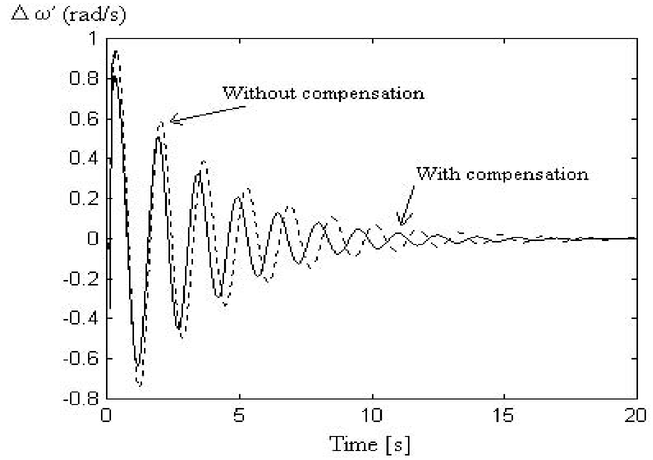


FIGURE 25.31 Variation of the angular speed.

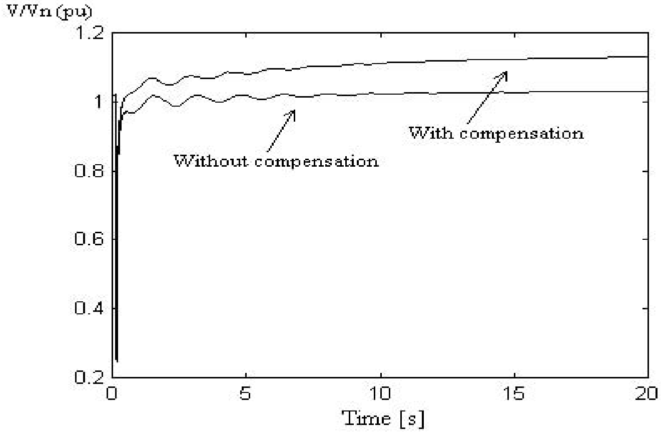


FIGURE 25.32 Variation of the voltage of the first bus bar.

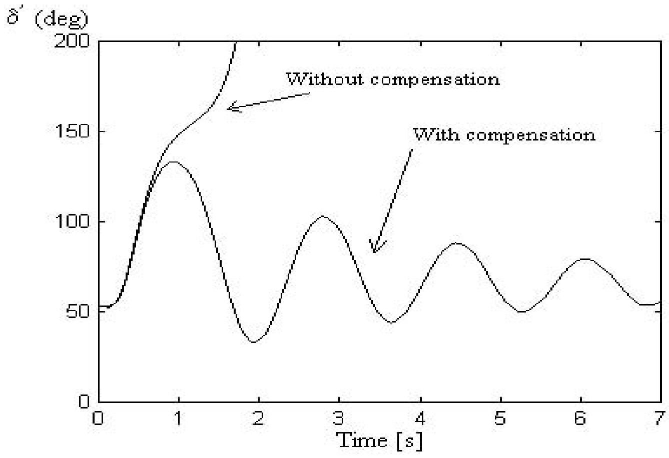


FIGURE 25.33 Load angle variation of the turbo-alternator.

generate the necessary reactive power; the control variable α is limited by two upper and lower levels, which allows preserving the stability of the compensator. If we suppose that the reference is always the voltage of the bus bar connected to the ASVC, the transfer function relating the reactive power to the control angle α is given by [17]

$$G(p) = \frac{q(p)}{\alpha(p)} = \frac{\sqrt{2}V^2\left[\dfrac{p^2}{L_s} + p\dfrac{R_s}{L_s} + \dfrac{m^2}{L_s^2 C}\right]}{p^3 + 2p^2\dfrac{R_s}{L_s} + p\left(\omega^2 + \dfrac{R_s^2}{L_s^2} + \dfrac{m^2}{L_s C}\right) + m^2\dfrac{R_s}{L_s^2 C}}$$

As for the PI regulator, it is designed similarly as given in Section 25.2, with the same constant of time of integration, but the voltage level will change. Hence, by using the root-locus method, the parameters of the regulator are given as follows:

$$K_p = 2.3 \times 10^{-9}$$
$$K_I = 7.7 \times 10^{-7}$$

25.4.3 Simulation Results

To analyse the performance of the stability of the turbo-alternator with ASVC, a series of simulation tests have been carried out, by taking the compensator parameters as follows: ac side: $R_s = 1\ \Omega$, $L_s = 5$ mH; dc side: $C = 500\ \mu$F.

The results obtained for the turbo alternator and ASVC are compared with those of the turbo alternator alone. Figure 25.30 represents the variation of the load angle of the turbo alternator group with and without compensation after clearing the fault of 0.08 s. We notice that the response with the compensation is more damped and the load angle is smaller than that of the turbo alternator without compensation. Figure 25.31 represents the variation of the angular speed centered on the turbo alternator with and without compensation after clearing the fault of 0.08 s. We notice that the response with compensation is more damped than without compensation.

Figure 25.32 represents the variation of the voltage of the first bus bar with and without compensation. The voltage of the compensated system is higher than that without compensation. This is due to the decrease in reactive power in the lines by the ASVC, which generates a capacitive reactive current that nullifies a part of the inductive reactive current absorbed by the line. Figure 25.33 shows the variation of the load angle of the turbo-alternator with and without compensation after the clearing of the fault of 0.3 s, which is the critical time for clearing the fault for the alternator without compensation. We notice that the introduction of the ASVC has allowed improvement of this clearing time and an increase in the level of stability of the system.

25.4.4 Conclusion

In this section a new approach to improve the stability of a turbo-alternator using static VAR compensator has been presented. The mathematical model derived and the transient simulated results obtained are included to confirm the applicability of the proposed control scheme. This control approach is more suitable for industrial applications, which require continuous control of the reactive power. Analysis of the simulation results allows us to conclude that the use of the inverter as a compensator of reactive power brings better performance than classical methods and gives to the electro-energetic system better flexibility.

25.5 Multilevel Inverters

Recent advances in the power-handling capabilities of static switch devices such as IGBTs with voltage rating up to 4.5 kV commercially available, has made the use of the voltage source inverters (VSI) feasible for high-power applications. High-power and high-voltage conversion systems have become very important issues for the power electronic industry handling the large ac drive and electrical power applications at both the transmission and distribution levels. As a result, a variety of VSI-based equipment such as static compensators (STATCOM) is used to make flexible ac transmission systems (FACTS) possible. The ability of this FACTS equipment to control reactive power systems as well as to improve system stability may required the use of VSI with high-voltage and high-power capabilities.

This is not possible for a two-level inverter, as the semiconductor devices must be connected in series to obtain the required high-voltage operation. This can be achieved by summing the outputs of several two-level converters with transformers or inductors, or direct series connection, or by more complex topologies such as the diode clamped inverter and the flying capacitor inverter.

The multilevel pulse-width modulation (PWM) converter topology has drawn tremendous interest in the power industry since it can easily provide the high-power required for high-power applications for such uses as static VAR compensation and active power filters, and so that large motors can also be controlled by high-power adjustable-frequency drives. The most popular structure proposed as a transformerless voltage source inverter is the diode-clamped converter based on the neutral point clamped (NPC) converter proposed by Nabae *et al.* [22]. It has the advantages that the blocking voltage of each switching device is one-half of the dc link voltage and the harmonics contents output voltage is far less than those of two-level inverters at the same switching frequency. A general trend of replacing existing conventional inverter by neutral point clamped (NPC) inverters in high-power applications is taking place. The multilevel voltage source inverters' unique structure allows them to reach high voltages with low harmonics without the use of transformers or series-connected synchronized switching devices, a benefit that many contributors have been trying to appropriate for high-voltage, high-power applications.

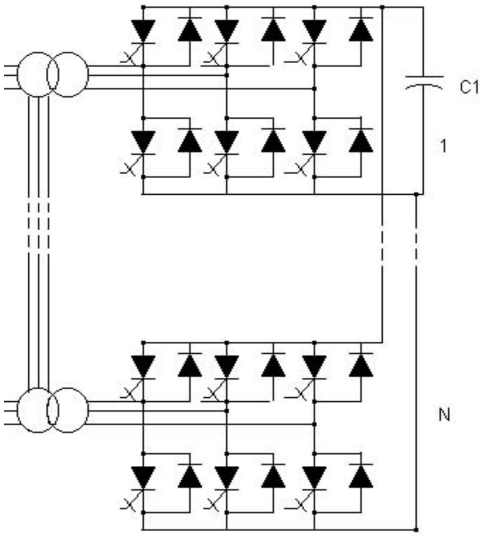


FIGURE 25.34 Schematic diagram of an inverter with 6*N* pulses by transformers.

The general structure of the multilevel converter, which has a multiple of the usual six switches found in a three-phase inverter, is to synthesize a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources. The main motivation for such converters is that current is shared among these multiple switches, allowing a higher converter power rating than the individual switch VA rating would otherwise allow with low harmonics. As the number of levels increases, the synthesized output waveform, a staircase-like wave, approaches a desired waveform with decreasing harmonic distortion, approaching zero as the number of levels increases. The structure of the multilevel inverter starts from three-level, also known as a neutral clamped converter [23–25], and consists of two capacitor voltages in series and uses the center tap as the neutral. Each phase leg of the three-level converters has two pairs of switching devices in series. The center of each device pair is clamped to the neutral through clamping diodes. The waveform obtained from the three-level converters is a quasi-square-wave output.

25.5.1 Different Structures of the Multilevel Inverters

There are roughly three main types of transformerless multilevel inverter topologies, which have been studied and received considerable interest from high-power inverter system manufacturers: the flying-capacitor inverter, the diode-clamped inverter, and the cascaded H-bridge inverter. A detailed overview and comparison of characteristics and their implementa-

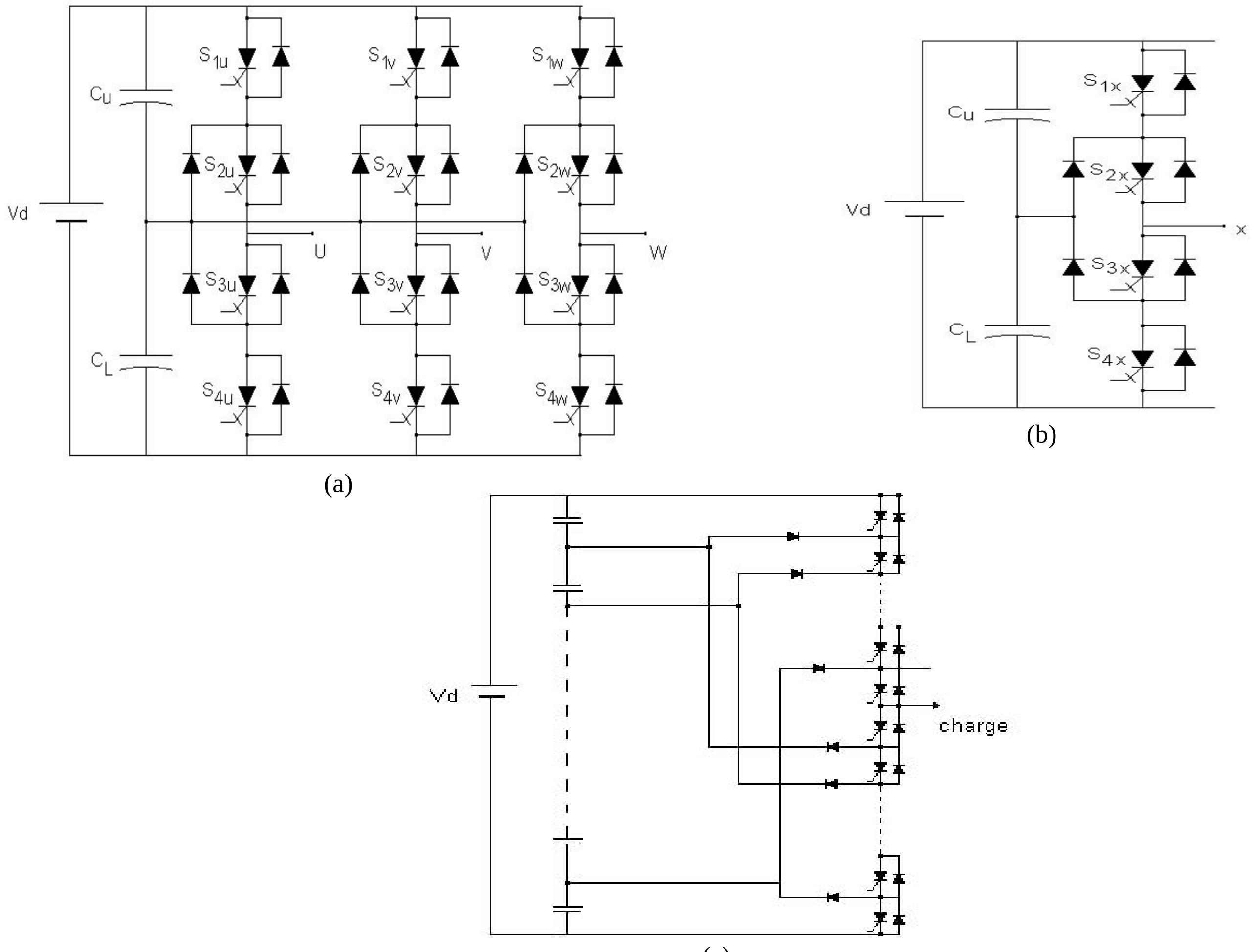


FIGURE 25.35 Schematic diagram of: (a) one leg of converter; (b) three-level converter; (c) one leg of M multilevel converter.

TABLE 25.2 States of the switches for one leg of converter

Symbols of States	States of the Switches				Output Voltages
	S1x	S2x	S3x	S4x	
P	ON	ON	OFF	OFF	Vd
O	OFF	ON	ON	OFF	Vd/2
N	OFF	OFF	ON	ON	0

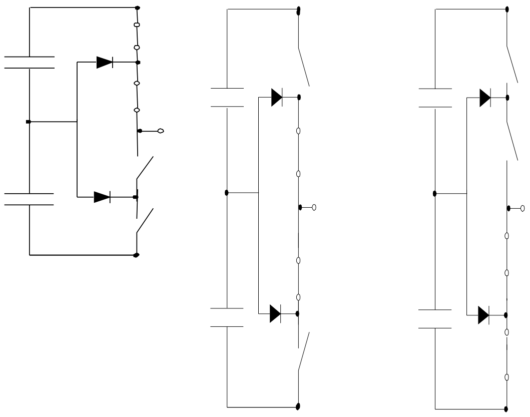


FIGURE 25.36 Switching states.

tion issues is given next. All share the same property, which is that the output filter can be dramatically reduced, and the usual bandwidth limit induced by the switching frequency can be reconsidered.

25.5.1.1 Multilevel Inverters with Transformer

An inverter with M levels that has $P = 6M$ pulses is obtained from an inverter with six pulses at the fundamental thanks to the following operating structure. We operate the inverters through a common dc source with successive phase displacement of $2\pi/6M$.

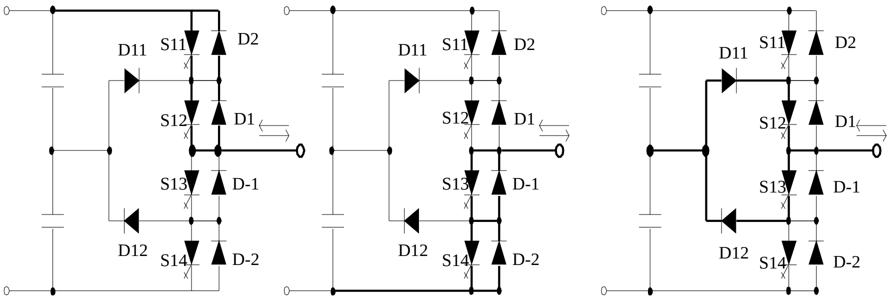


FIGURE 25.37 Current flow.

The transformer secondary windings have appropriate configurations and connections to obtain the three-phase voltage by connecting the primary winding of the transformer in series and parallel, which displaces each waveform of the output voltage likewise obtained. Figure 25.34 shows a model with N pulses used as reactive power generator (SVG) made of eight (8) inverters with six (6) pulses using the transformers with particular connection so to eliminate harmonics and reduce the total harmonic distortion. This first type of multilevel inverter presents the following drawbacks:

1. Total pricing of the system is related mainly to the transformers used.
2. They produce roughly 50 of the total losses of the system.
3. They occupy 40 of the total surface allowed for the system.
4. They make the control difficult because of problems related to overvoltages caused by saturation in the transient state.

25.5.1.2 Neutral-Point-Clamped Inverter

Figure 25.35a shows a schematic diagram of the structure of a three-level (Neutral-point clamped) inverter. It may be coupled directly to a level of voltage of 3.3 kV by using a GTO of 4.5 kV [26, 27]. Taking for reference one leg of the converter as shown in Fig. 25.35b, Table 25.2 gives overall switching states of the GTO, to obtain the voltages 0, $E/2$, and E three (3) states per leg; thus, for a three-phase converter there are 27 states in total.

Figure 25.36 shows a structure of an M multilevel converter; in this case we use $(M-1)\times 2\times 3$ GTO, $(M-1)\times 2\times 3$ diodes in anti-parallel, $(M-1)\times(M-2)\times 3$ clamping diodes, and $(M-1)$ capacitors. Figure 25.37 represents the transitions of the switches of one leg according to the indicated states in Table 25.2. Figure 25.37 also shows the direction of the current flow for each state.

(S11, S14); (S21, S24); (S31, S34) are the main switches; they are switched directly by control pulses. (S12, S13); (S22, S23); (S32, S33) are the auxiliary switches and allow connection of the output of each phase to neutral point (0). (D11–D32) intervene in this operation.

As an example, for $M = 51$ for a direct connection with a 69-kV network, 300 GTOs and diodes in antiparallel, 50 capacitors, and 7350 clamping diodes are needed. This second type of converter presents the following advantages:

1. When M is very high, the distortion level is so low that the use of filters is unnecessary.
2. Constraints on the switches are low because the switching frequency may be lower than 500 Hz (there is a possibility of switching at the line frequency).
3. Reactive power flow can be controlled.

The main disadvantages are:

1. The number of diodes becomes excessively high with the increase in level.
2. It is more difficult to control the power flow of each converter.

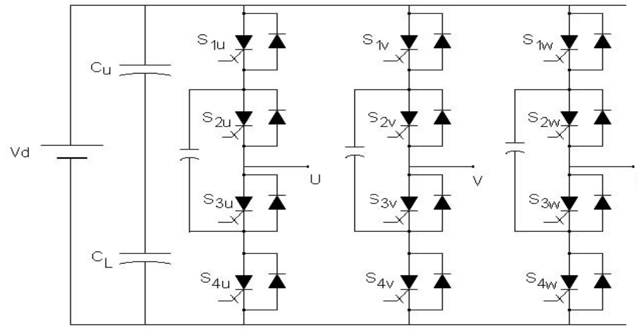


FIGURE 25.38 Schematic diagram of a three-level flying capacitor type converter.

25.5.1.3 lying Capacitors

Figure 25.38 shows the structure of a flying-capacitor type converter. We notice that compared to NPC-type converters a high number of auxiliary capacitors are needed, for M level $(M-1)$ main capacitors and $(M-1)\times(M-2)/2$ auxiliary capacitors. The main advantages of this type of converter are:

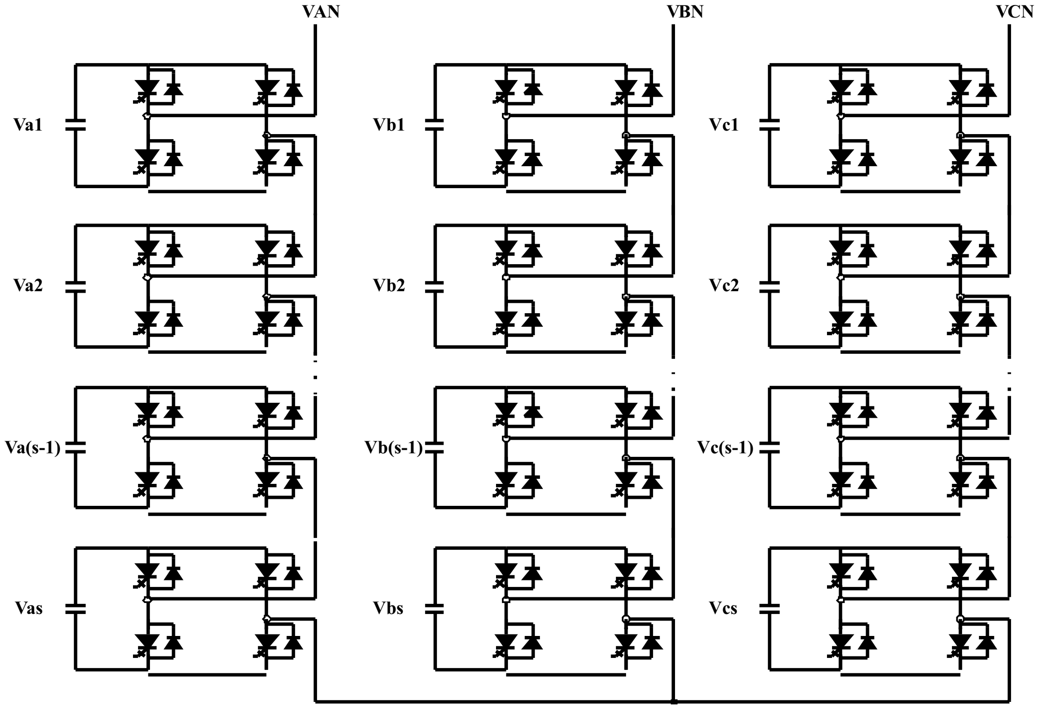


FIGURE 25.39 Schematic diagram of a 9-level cascaded-type converter.

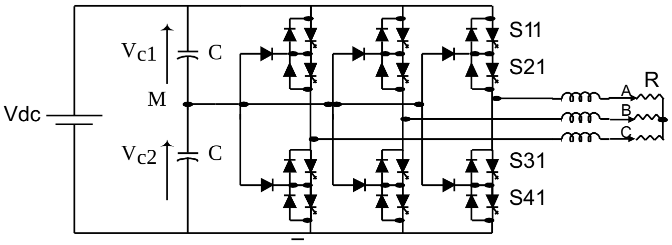


FIGURE 25.40 Topology of a three-level inverter.

1. For a high M level, the use of a filter is unnecessary.
2. Control of active and reactive power flow is possible.

The drawbacks are:

1. The number of capacitors is very high.
2. Control of the system becomes difficult with the increase of M.

25.5.1.4 Cascaded-Type Multilevel Inverter

Figure 25.39 represents the structure of a three-phase cascaded-type converter with separate dc sources; it shows an example of a 9-level converter. This type of converter does not need any transformer clamping diodes, or flying capacitors; each bridge converter generates three levels of voltages (E, 0, and $-E$). For a three-phase configuration, the cascaded converters can be connected in star or delta. It has the following advantages:

1. It uses fewer components than the other types.
2. It has a simple control, since the converters present the same structure.

However, the main drawback is that it needs separate dc sources for the conversion of the active power, which limits its use.

25.5.2 Conclusion

Among these inverter topologies, the flying capacitor inverter is difficult to realize because each capacitor must be charged with different voltages as the voltage level increases. Moreover, the diode-clamped inverter is difficult to expand to multilevel because of the natural problem of the dc link voltage unbalancing, the increase in the number of clamping diodes, and the difficulty of the disposition between the dc link capacitors and the devices as the voltage increases. Though the cascaded inverter has the disadvantage of needing separate dc sources, the modularized circuit layout and package are possible, and the problem of the dc link voltage unbalancing is not occurred. Therefore it is easily expanded to multilevel. Because of these advantages, the cascaded inverter bridge has been widely applied to such areas as HVDC, SVC, stabilizers, and high-power motor drives.

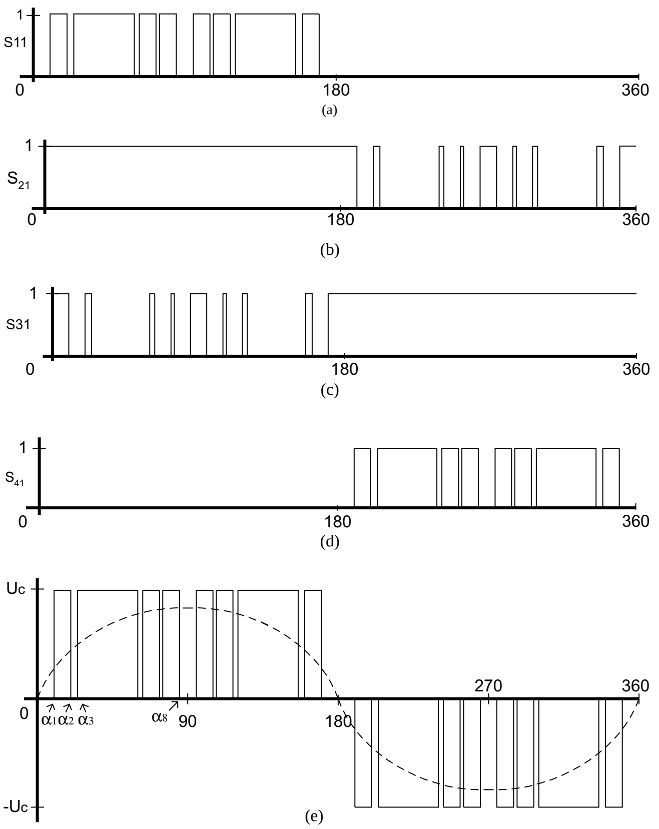


FIGURE 25.41 Voltage waveforms of one leg of inverter for $R = 8$. (a) Pulses for S11, (b) pulses for S21, (c) pulses for S31, (d) pulses for S41, (e) voltage between phases.

25.6 The Harmonics Elimination Method for a Three-Level Inverter

In this section the use of a harmonics elimination method applied to a three-level inverter is shown. The method to calculate the switching angles is exposed. Simulations results using the Pspice program are carried out to validate the mathematical model. It is well known that for a classical inverter, voltages are generated with harmonics of the order $(6K \pm 1)f$, and the input current at steady state contains frequency components equal to $6Kf$, with f the output fundamental frequency and $K = 1, 2, 3 \ldots$. One of the solutions applied is the use of multilevel inverter topology. Figure 25.40 shows the structure of a three-level inverter used as a compensator [28, 29]. Each leg of the inverter is made up of four pairs of diode GTOs, each representing a bidirectional switch and two auxiliary diodes, allowing zero voltage at the output of the inverter. The system obtained is connected to an R, L load; the dc side is composed of two capacitors behaving as a voltage divider supplied from a dc source.

25.6.1 PWM Control for Harmonics Elimination

The switching angles are fixed by the intersection of a reference wave and a modulating signal, in the PWM case, or full-wave control [30]. A third alternative control method is possible when we use a system controlled by microprocessor for switching through precalculated sequences stored in memory. The determination of the control angles may then be done based on complex criteria, since the angles have already been calculated. The performances of the system depend on the choice of the criteria used for calculating the angles; it is interesting to note that any method used will always consist of eliminating the effect obtained by the presence of harmonics on the output voltage of the inverter.

Figure 25.41 shows the control signals of the four switches of one leg of the three-phase, three-level inverter and the phase voltage to the neutral point M. The pulses given in Figs. 25.41a and 25.41b control the switches S11 and S21. The complementary pulses to S11 and S12, respectively, in Figs. 25.41c and 25.41d control the switches S13 and S14. The voltage between a phase and neutral point M is illustrated by Fig. 25.41e. We notice that the voltage V_{AM} is symmetrical with respect to M.

Fourier coefficients for such a signal V_{AM} are given by

$$a_r = \frac{4}{r\pi}\left[\sum_{j=1}^{R}(-1)^{j+1}\cos(r\alpha_j)\right] \tag{25.56}$$

with R the harmonics range $(1, 2 \ldots R)$.

These equations are nonlinear, and multiple solutions are possible. But all the solutions of Eq. 25.56 must satisfy the following constraint:

$$\alpha_1 < \alpha_2 < \alpha_3 < \cdots < \alpha_R < \frac{\pi}{2} \tag{25.57}$$

The nonlinear equations to eliminate $R - 1$ harmonics that are not multiples of three, such as 5, 7, and 11, are written as follows:

$$\begin{bmatrix} \cos\alpha_1 & -\cos\alpha_2 & \ldots & (-1)^{j+1}\cos\alpha_j \\ \cos 5\alpha_1 & -\cos 5\alpha_2 & \ldots & (-1)^{j+1}\cos 5\alpha_j \\ . & . & . & . \\ . & . & . & . \\ \cos x\alpha_1 & \cos x\alpha_2 & \ldots & (-1)^{j+1}\cos x\alpha_j \end{bmatrix} = \begin{bmatrix} \pi a_1/4 \\ 1 \\ . \\ . \\ 1 \end{bmatrix} \tag{25.58}$$

with $x = 3R - 1$ for R even and $x = 3R - 2$ for R odd.

To solve the system of equations (25.58) we use the Newton–Raphson method, from a program developed in Pascal language. The algorithm may be summarized as follows:

We define:

$$h_i(\alpha_i, \ldots, \alpha_R) = 0, \qquad i = 1, 2, \ldots, R \tag{25.59}$$

These R equations are obtained by equating to zero all $R - 1$ equations of harmonics to be eliminated. Hence, Eq. 25.58 is written

$$h(\alpha) = 0 \tag{25.60}$$

where

$$h = [h_1 \quad h_2 \quad \ldots \quad h_R]^T$$
$$\alpha = [\alpha_1 \quad \alpha_2 \quad \ldots \quad \alpha_R]^T$$

Equation (25.58) may be solved around the solution.

1. Initialise the values of α_i:

$$\alpha^0 = [\alpha_1^0 \quad \alpha_2^0 \quad \ldots \quad \alpha_R^0]^T$$

2. Determine the values of

$$h(\alpha^0) = h^0 \tag{25.61}$$

3. Fragmenting (25.61) around α^0:

$$h^0 + \left[\frac{\partial h}{\partial \alpha}\right]^0 d\alpha = 0 \tag{25.62}$$

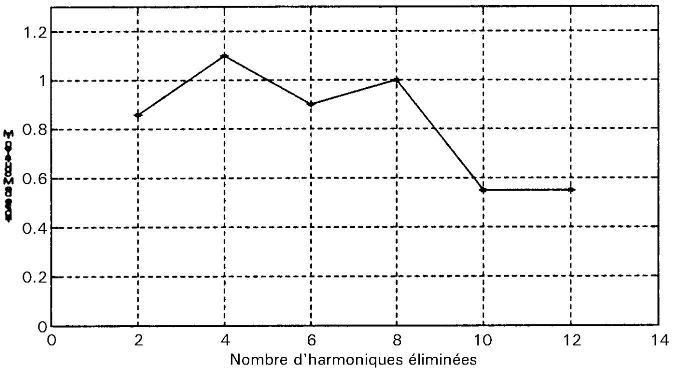


FIGURE 25.42 Evolution of the modulation index as a function of the number of harmonics eliminated.

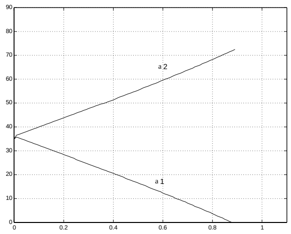


FIGURE 25.43 Simplified model of the switch with its antiparallel diode by PSPICE.

where

$$\left[\frac{\partial h}{\partial \alpha}\right]^0 = \begin{bmatrix} \frac{\partial h_1}{\partial \alpha_1} & \frac{\partial h_1}{\partial \alpha_2} & \cdots & \frac{\partial_1 h}{\partial \alpha_R} \\ \frac{\partial h_2}{\partial \alpha_1} & \frac{\partial h_2}{\partial \alpha_2} & \cdots & \frac{\partial h_2}{\partial \alpha_R} \\ \cdot & \cdot & \cdots & \cdot \\ \cdot & \cdot & \cdots & \cdot \\ \cdot & \cdot & \cdots & \cdot \\ \frac{\partial h_M}{\partial \alpha_1} & \frac{\partial h_M}{\partial \alpha_2} & \cdots & \frac{\partial h_R}{\partial \alpha_R} \end{bmatrix}$$

4. Solve (25.62) for $d\alpha$:

$$d\alpha = -\frac{h^0}{\left[\frac{\partial h}{\partial \alpha}\right]^0}$$

5. Repeat 1 to 4 by correcting at each step by

$$\alpha^1 = \alpha^0 + d\alpha$$

until the required precision is satisfied.

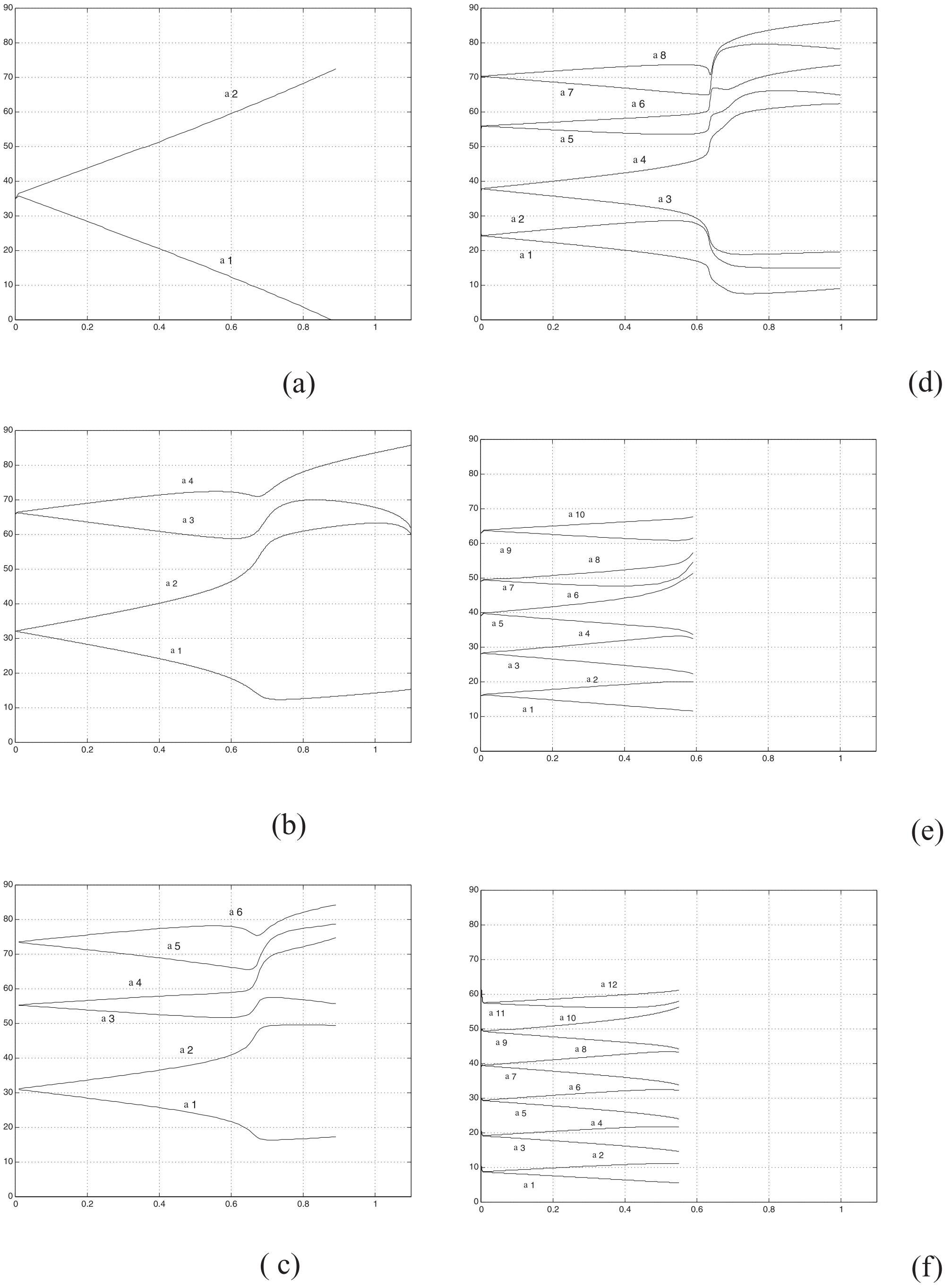
Figure 25.42 shows the trajectory of the solutions for various values of R, with the modulation index MI varying in the interval [0 1.1] [31]. Figure 25.42a shows that there is a linear progression of angles α_1 and α_2 following a negative or positive slope, respectively, in the interval $0 < \text{MI} < 0.6$. This note is also valid for Fig. 25.42b; in Fig. 25.42c and 25.42d, however, in the interval $0.6 < \text{MI} < 1.1$, these trajectories become nonlinear, and thus more refinement of the algorithm is carried out to obtain the solutions in this interval. As for Figs. 25.42e and 25.42f, the system has no solutions beyond $\text{MI} > 0.6$. We conclude from Fig. 25.42 that:

- Maximum of the modulation index diminishes with the increase of the harmonics number eliminated, illustrated in Fig. 25.43.
- For some values of R, the trajectories of the angles get nearer, which implies a decrease in the width of pulses.

25.6.2 Simulation Results using PSPICE

In order to check the validity of the calculated results of the angles, the three-phase inverter system connected to a load is modeled by using PSPICE [32].

The modeling of the switch is a simple version. It consists of an infinite value of resistance for the open state and a low-value resistance for the closed state. Figure 25.44 illustrates this principle. In order to model the inverter system of Fig. 25.40



(a) (d)

(b) (e)

(c) (f)

FIGURE 25.44 Trajectories of solutions for programmed PWM: (a) $R = 2$; (b) $R = 4$; (c) $R = 6$; (d) $R = 8$; (e) $R = 10$; (f) $R = 12$.

by PSPICE, a simplified schematic diagram is adopted by using the following steps:

1. Numbering the ties.
2. Components identification.

PSPICE uses the circuit obtained to establish a program.

25.6.3 Simulated Results of the Programmed P M Control

On the basis of the PSPICE program various simulations have been undertaken. Figure 25.45 illustrates the results for the case $R = 2$ and $\mathrm{MI} = 0.8$, Fig. 25.45a represents the line

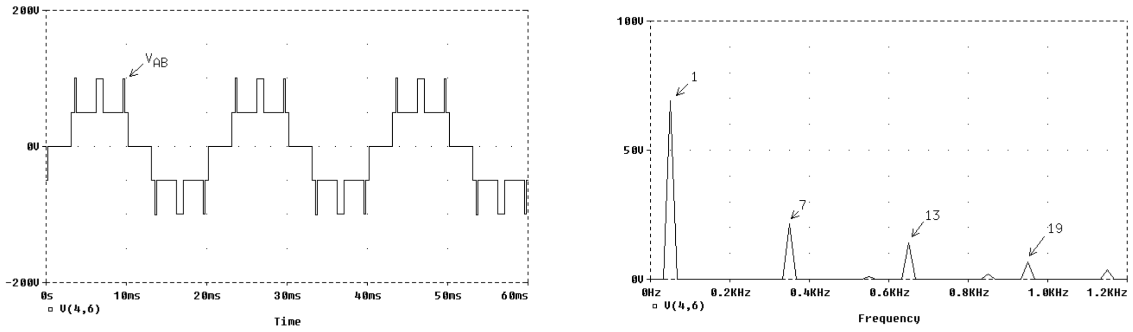


FIGURE 25.45 Simulation results for MI = 0.8 and $R = 2$: (a) Line voltage, (b) harmonics spectra; THD = 31.36%.

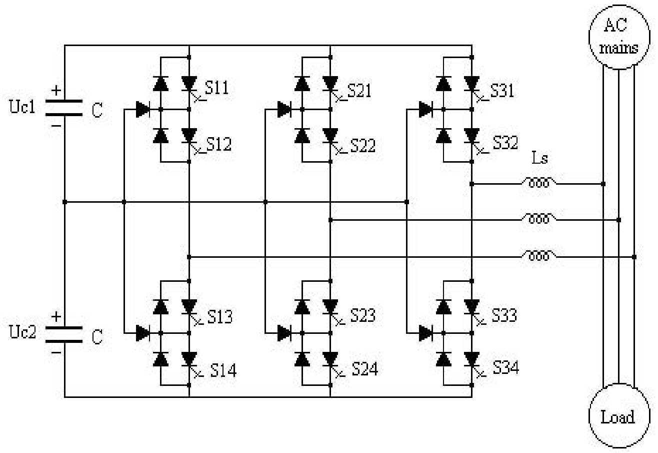

AC mains
Uc1
C
S11
S12
S21
S22
S31
S32
Ls
Uc2
C
S13
S14
S23
S24
S33
S34
Load

FIGURE 25.46 Main circuit of the ASVC.

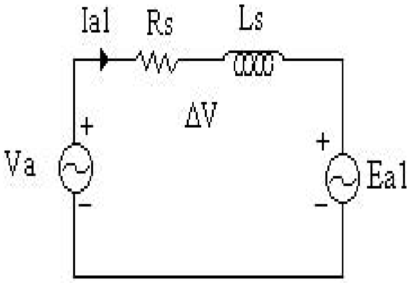

Ia1
Rs
Ls
ΔV
Va
Ea1
+
-
+
-

FIGURE 25.47 Per-phase fundamental equivalent circuit.

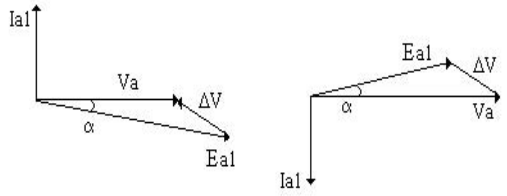

Ia1
Va
ΔV
α
Ea1
Ea1
ΔV
α
Va
Ia1

FIGURE 25.48 Phasor diagram for leading and lagging mode.

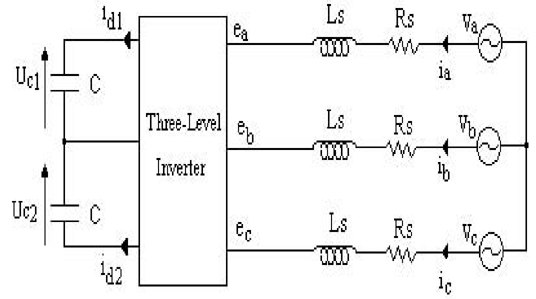

i_{d1}
U_{c1}
C
U_{c2}
C
i_{d2}
Three-Level Inverter
e_a
e_b
e_c
Ls
Rs
Ls
Rs
Ls
Rs
V_a
V_b
V_c
i_a
i_b
i_c

FIGURE 25.49 Equivalent circuit of the ASVC.

voltage and Fig. 25.45b its harmonic spectrum. We notice the total elimination of harmonics of order 5.

25.6.4 Conclusion

The main conclusions are summarised as follows.

The resolution of the nonlinear equations in the case of a three-level inverter must be carried out with a refinement of the calculation step beyond MI > 0.6 so as to obtain a finite solution.

- The increase in the harmonics number eliminated has a negative effect on the modulation index, since with the increase of R a decrease in MI maximum follows.
- The trajectories getting nearer for MI > 0.6 implies a decrease in the switching pulses of the GTOs which itself allows for the increase in commutation losses.

25.7 Three-Level ASVC Structure Connected to the Network

The fast-growing development of ultrarapid power switching devices and the desire to reduce the harmonics has led to an increase in the use of converters for large-scale reactive power compensation. Such an SVC is made up of two-level voltage source inverters and presents a fast response time and reduced harmonic pollution. However, for very high power applications and voltages, these SVCs are unsuitable. In this section we introduce a neutral-point clamped inverter having harmonics contents output voltage far less than those of two-level inverters at the same switching frequency. We also present the modeling and analysis of this new type of inverter used for advanced static VAR compensation. This ASVC uses three-level voltage source inverter (VSI) transforming a dc component to ac through a set of capacitors, which are used as a power storage device. Furthermore, a simplified mathematical model of the ASVC is derived, and various simulation results presented using Matlab.

25.7.1 Operating Principles

The static VAR compensator (ASVC) that uses a three-level converter of the voltage-source type is shown in Fig. 25.46. The main circuit consists of a bridge inverter made up of 12 power GTOs with antiparallel diodes, which is connected to the three-phase supply through a reactor, X$_s$, of small value. Two capacitors are connected to the dc side of the converter.

The operation principles of the system can be explained by considering the per-phase fundamental equivalent circuit of the ASVC system as shown in Fig. 25.47, as well as Figs. 25.48 and 25.49.

In Fig. 25.47, V_a is the ac mains voltage source. I_{a1} and E_{a1} are the fundamental components of current and output voltage of the inverter supply, respectively. The ASVC is connected to ac main through a reactor L_s and a resistor R_s, representing the total loss in the inverter. As shown in Fig. 25.50, by controlling the phase angle 'α' of the inverter output voltage, the dc capacitor voltage U_c can be changed. Thus, the amplitude of the fundamental component E_{a1} can be controlled.

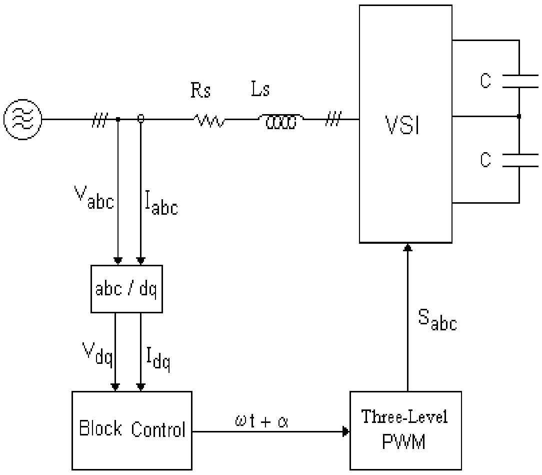


FIGURE 25.50 Main circuit and control block diagram.

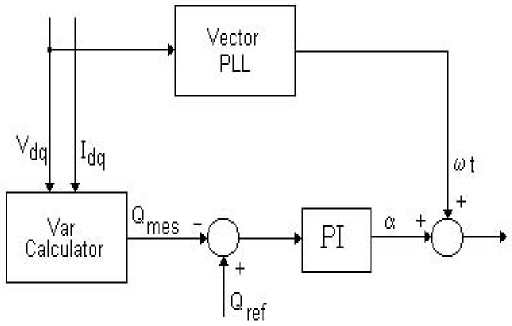


FIGURE 25.51 Details of the control block diagram.

25.7.2 Mathematical Model of the ASVC

The modeling of the system is carried out under the following assumptions:

- All switches are ideal.
- The source voltage are balanced.
- The total losses in the inverter are represented by lumped resistor R_s, and the harmonic contents caused by switching action are negligible.

Using matrix form, the mathematical model per phase is given by

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L_s} & 0 & 0 \\ 0 & -\frac{R_s}{L_s} & 0 \\ 0 & 0 & -\frac{R_s}{L_s} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{L_s}\begin{bmatrix} v_a - e_a \\ v_b - e_b \\ v_c - e_c \end{bmatrix} \tag{25.63}$$

The model of the inverter output voltage is given by

$$\begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \times \left\{ \begin{bmatrix} F_{11} & F_{12} \\ F_{21} & F_{22} \\ F_{31} & F_{32} \end{bmatrix} U_{c1} - \begin{bmatrix} F_{13} & F_{14} \\ F_{23} & F_{24} \\ F_{33} & F_{34} \end{bmatrix} \right\} \tag{25.64}$$

With

F_{ki}: function of connection, defining the state of the switch
$F_{ki} = 1$ if the switch is closed and 0 otherwise
$K =$ number of the arms $(k = 1, 2, 3)$
$I =$ number of the switches of the arm $(I = 1, 2, 3, 4)$

The dc side currents are given by

$$\begin{aligned} i_{d1} &= F_{11}F_{12}i_a + F_{21}F_{22}i_b + F_{31}F_{32}i_c \\ i_{d2} &= F_{13}F_{14}i_a + F_{23}F_{24}i_b + F_{33}F_{34}i_c \end{aligned} \tag{25.65}$$

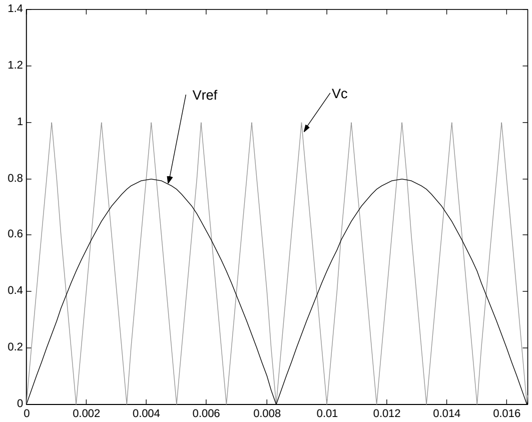


FIGURE 25.52 Three-level PWM switching pattern.

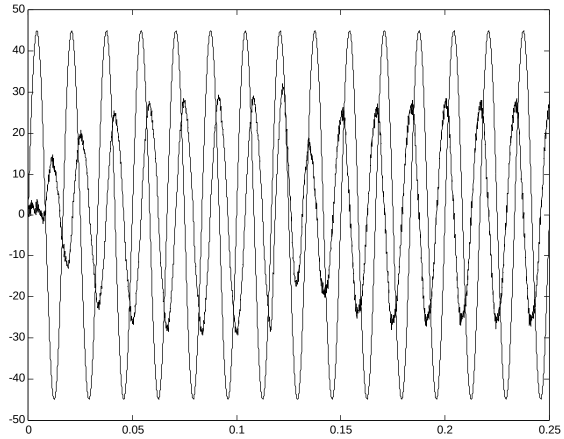


FIGURE 25.53 Simulated voltage and current waveform Vs[vX10], Isa.

The mode of the capacitor voltage is given by

$$\frac{d}{dt}\begin{bmatrix} U_{c1} \\ U_{c2} \end{bmatrix} = \frac{1}{C}\begin{bmatrix} i_{d1} \\ -i_{d2} \end{bmatrix} \tag{25.66}$$

25.7.3 Controller Design

In order to synthesize the control strategy of the system, the analysis is carried out on an analysis on (dq) axes [33–35] and the inverter is controlled by a three-level PWM [36]. The ASVC control scheme is illustrated in the block diagram of Fig. 25.50, and Fig. 25.51 illustrates the detailed control loop of the block diagram. To achieve fast dynamic response, it is required that by controlling the phase angle changes the capacitors U_{c1} and U_{c2} "α." Small signal equivalent model system is used to calculate the transfer function of the system equation (25.67).

$$\frac{Qc(s)}{\alpha(s)} = \frac{N(s)}{M(s)} \tag{25.67}$$

with

$$N(s) = \frac{V_s^2}{L}\left[s_2 + \frac{R_s}{L}s + \frac{d_2}{2LC}\right]$$

and

$$M(s) = s_3 + \frac{2R_s}{L}s_2 + \left\{\left[\frac{R_s}{L}\right]^2 + \frac{d_2}{2LC} + \omega_2\right\}s + \frac{d_2R_s}{2L_2C}$$

This circuit consists of a conventional PI controller and a stored switching pattern device used to study the dynamic behavior of the system.

The source voltage and the ASVC's current are transformed in the $d - q$ frame for calculating the reactive power generated by the system, which is compared to the reactive power reference. The PLL detects the phase angle of the supply

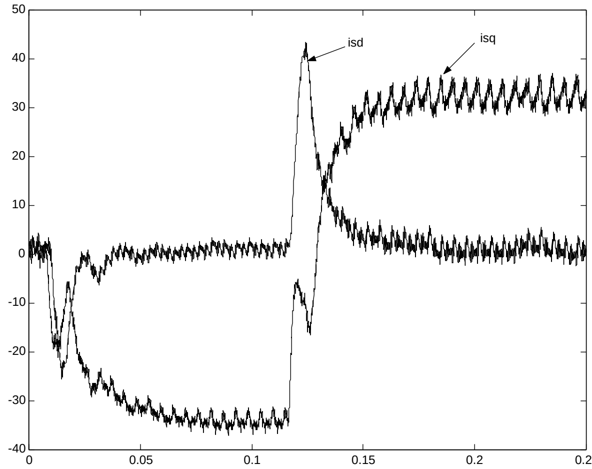


FIGURE 25.54 Phase current in the *dq* axes, active component isd [A] and reactive component isq [A].

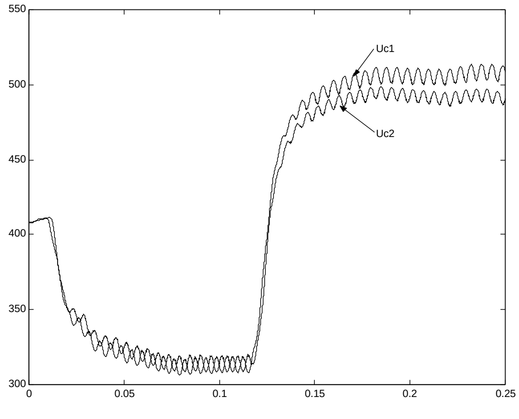


FIGURE 25.55 Inverter dc bus voltages U_{c1} and U_{c2}.

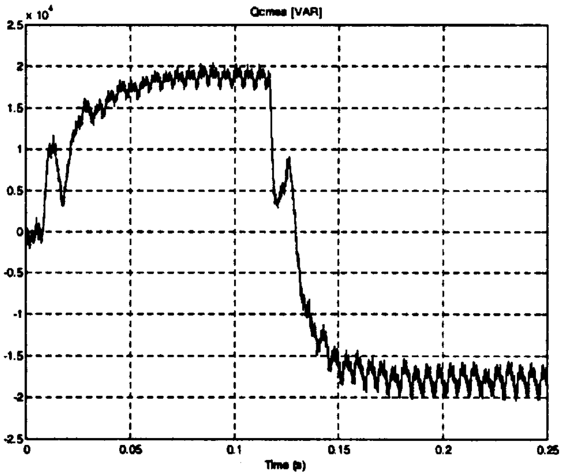


FIGURE 25.56 Reactive power response for 20 kVar step change.

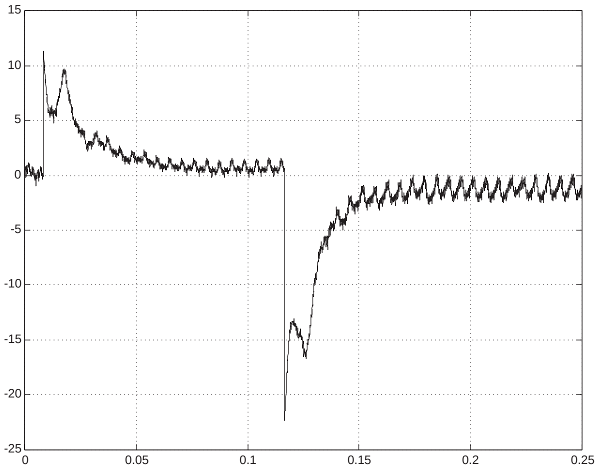


FIGURE 25.57 Variation of the control angle α (°).

voltage, which is added to the control variable α (output of the PI controller). This sum controls the frequency of the memorized switching states which are stored in the EPROM.

Figure 25.52 shows the PWM three-level pattern obtained from the triangular–sinusoidal control strategy by using the following signals:

- The reference signals V_{ref}
- The triangular carrier V_c

The signal control rules are as follows:

> If (Vref(k) 0) and (Vref(k) $\geq$ Vc) Then Fk1 $=$ 1, Fk2 $=$ 1, Fk3 $=$ 0, Fk4 $=$ 0. Else if (Vref(k) $\leq$ 0) And (abs (Vref(k)) $\geq$ Vc) Then Fk1 $=$ 0, Fk2 $=$ 0, Fk3 $=$ 1, Fk4 $=$ 1. Else Fk1 $=$ 0, Fk2 $=$ 1, Fk3 $=$ 1, Fk4 $=$ 0

25.7.4 Simulation Results

To check the validity of the model described above, a set of simulations tests have been carried out to analyse the system under steady-state and transient conditions using Matlab. This will certainly lead to the design of a robust controller [32]. Computer simulation is carried out using the system parameters given by

$$f = 60\ \text{Hz},\ W = 2\pi f,\ V_s = 550\ \text{V},\ R_s = 0.4\ \Omega,\ L = 10\ \text{mH},$$
$$C = 1000\ \mu\text{F},\ \text{MI (modulation index)} = 33$$

Based on the linear model described above and using the root-locus technique, the parameters of the controller are found to be [27]

$$K_p = 8.24 \times 10^{-6}, \qquad K_i = 1.42 \times 10^{-4}$$

The amplitude of the reference was adjusted to cause the system to swing to lagging mode.

Figure 25.53 shows the simulated current and voltage waveforms to step reference changes from standby to 20 Kvar leading and -20 Kvar. Figure 25.54 represents transient phase current in the *dq* axes. isd and isq are the active and reactive components, respectively.

Figure 25.55 represents the dc capacitor voltages. We notice a fluctuation of voltages U_{c1} and U_{c2} around an average value and a difference of amplitude and waveforms of the voltages U_{c1} and U_{c2} for the two operating modes. Figure 25.56 shows the simulated transient response of the reactive power response to a sudden change in reference. Figure 25.57 shows the response of control angle α.

25.7.5 Conclusion

A study and mathematical modeling of the dynamic performance analysis of an advanced static VAR compensator (ASVC) using a three-level voltage source inverter has been presented in this section. The dynamic behavior of the system was analyzed using Matlab through a set of simulation tests, which have led to the design of an inexpensive controller for reactive power applications.

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26

Drive Types and Specifications

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26.1 Overview

26.1.1 Introduction

In every industry there are industrial processes of some form that require adjustment for normal operation or for optimum performance. Such adjustments are usually accomplished with a variable-speed drive (VSD) system. VSD systems are an important part of automation. They help to optimize the process and to reduce investment costs, energy consumption, and energy cost.

There are three basic types of VSD systems: electrical drives, hydraulic drives, and finally mechanical drives. This chapter focuses mainly on electrical drives.

A typical electric VSD system consists of three basic components: the electric motor, the power converter, and the control system, as illustrated in Fig. 26.1. The electric motor is connected directly or indirectly (through gears) to the load. The power converter controls the power flow from an ac supply (often via a supply transformer), to the motor by appropriate control of power semiconductor switches (part of the power converter).

With recent advances in power semiconductor and converter topologies, electric variable-speed drives are witnessing a revolution in applications including computer peripheral drives, machine tools and robotic drives, test benches, fans, pumps, and compressors, paper-mill drives, automation, traction, and ship propulsion, and cement-mill and rolling-mill drives.

For a proper control, the VSD system variables, both mechanical and electrical, are required for control and protections. Signals are usually derived by sensors, whose outputs are very much dependent on the control strategy employed and the functionality required.

This chapter introduces electric variable-speed drives and briefly describes their benefits. It examines their classifications from different perspectives. Their specification requirements to meet applications of different industries are briefly outlined.

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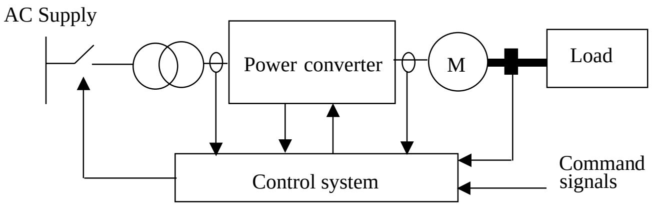

FIGURE 26.1 VSD schematic diagram.

Various VSD topologies have been carefully examined and compared with each other. A selection of modern VSD applications are examined and briefly commented upon.

26.1.2 istorical Review

To provide an appreciation of electric VSDs, significant dates in the evolution of electric drives are summarized in Table 26.1 [1].

The increased popularity of electric VSD systems witnessed in recent years may be explained by the many advantages a VSD can offer. Such advantages include operation at speeds significantly different from the synchronous speed, energy savings, reduced mechanical shock, improved process performance, improved efficiency, reduced mechanical wear, increased plant life, reduced total ownership costs, reduced system fault levels, and reduced ac disturbances in certain applications. Furthermore, modern electric drives are equipped with many features, including serial communication, remote control, diagnostics, and trip history. In the low-voltage, low-power arena, packaged electric drives are becoming a commodity product.

The disadvantages of such a system are also recognized. They include the need for extra space to accommodate the equipment, cooling, capital cost, noise, and power-system harmonic effects. The following is a brief review of some of the benefits and drawbacks of VSDs.

26.1.3 Advantages of VSDs

VSDs arguably benefit most industrial processes. The challenge has often been how to quantify these benefits. The energy-saving potential of VSD can be easily quantified, particularly for fan and pump drive applications.

26.1.3.1 Energy Saving

Electric VSDs provide savings in two ways: (a) directly, by consuming less energy and (b) indirectly, by improving product quality. The latter is often more difficult to quantify.

Direct energy savings are only possible with centrifugal loads such as centrifugal pumps and fans. Such loads are often run at fixed speeds. Traditionally, an automatic valve or some other mechanical means is used to vary fluid-flow rates in pumps. However, if a VSD is used, then the motor speeds can be controlled electronically to obtain a desired flow rate and can result in significant energy savings.

TABLE 26.1 Historical review of electric drives evolution [1]

Year	Key Advancement
1886	The birth of electric variable-speed drive system represented by Ward Leonard system
1889	The invention of squirrel-cage induction motor
1890	The slip ring induction motor drive speed control via rotor resistance control
1904	Kramer drives introduce a dc link between the slip rings and the ac supply
1911	Variable-speed system based on induction motor with a commutator on the rotor
1923	Ignitron made controlled rectification possible
1928	The invention of thyratron and grid controlled mercury arc rectifiers
1930	dc-to-ac power inversion
1931	ac-to-ac power conversion by cyclo converters
1950	Silicon-based power switches
1960	Thyristors (SCRs) became available and variable-speed drives began
1961	Back-to-back reversing dc drive introduced
1960s	Power semiconductor voltage and current ratings grew and performance characteristics improved
1970	The concept of packaging industrial drives introduced
1972	First integrated motors with dc converter
1973	Isolated thyristor packages
1970s	The principle of vector control (field oriented control) evolved
1983	Plastic molding made its first significant impact on VSDs
1985	Direct torque control as a concept
1990	Integrated power modules
1992	A new packaging trend emerged
1996	Universal drives (a general-purpose open-loop vector drive, a closed-loop flux vector drive, and a servo drive)
1998	Complete ac/ac integral converter up to 15 kW
1998	Medium-voltage pulse-width-modulated voltage-source inverter drives became a commercial product

On the basis of the laws of affinity for centrifugal loads:

- Volume of flow is directly proportional to speed
- Pressure is proportional to the square of the speed
- Input power is proportional to the cube of the speed

The affinity law states that the power consumption is proportional to the cube of the motor speed. This implies that if the speed is halved, the power consumption is reduced to one-eighth. So, energy savings occur as the requirement for volume decreases. If, for example, a cooling system calls for operation at 50 airflow volume, it requires only 12.5 of the power needed to run the system at 100 volume. Because power requirements decrease faster than the reduction in volume, there is potential for significant energy reduction at lower volume.

Generally, centrifugal pumps and fans are sized to handle peak volume requirements that typically occur for short periods. As a result, centrifugal pumps and fans mostly operate at reduced volumes.

Opening or closing of a damper allows the airflow of fans to be controlled. Restricting the airflow causes the motor to work hard even with a low throughput.

With a variable-speed drive, the speed of the fan can be reduced, thus giving the opportunity to reduce energy consumption. Adjusting the speed of the motor regulates the airflow. The control can be achieved by monitoring humidity, temperature flow, etc. The lower the required throughput, the more energy is saved.

It has been estimated that the payback period of 50-kW fan or pump VSD equipment, operating 2000 hours/year is 1.9 years for operation at 75 speed, and 1.23 years for 50 speed. It has been assumed that the cost of the VSD is 5.5 k and the cost of power is 0.05/kW.

26.1.3.2 Improved Process Control

Using VSDs to improve process control results in more efficiently operating systems. The throughput rates of most industrial processes are functions of many variables. For example, throughput in continuous metal annealing depends on the material characteristics, the cross-sectional area of the material being processed, and the temperature of one or more heat zones. If constant-speed motors are used to run conveyors on the line, it must either run without material during the time required to change temperature in a heat zone or produce scrap during this period. Both choices waste energy or material.

With VSDs, however, the time needed to change speed is significantly less than the time it takes to change heat-zone temperature. By adjusting the material flow continuously to match the heat zone conditions, a production line can operate continuously. The results are less energy use and less scrap metal.

26.1.3.3 Reduced Mechanical Stress Soft Starts

Starting up a motor direct on line increases stress on the mechanical system, e.g., belts and chains. Direct on-line startup of induction motor is always associated with high inrush current with poor power factor.

VSDs can improve the operating conditions for a system by giving a smooth, controlled start and by saving some energy during starting and running. Smoother startup operation will prolong life and reduce maintenance, but it is difficult to do more than make an estimate of the cost advantages of these. The benefits of soft start, inherent in VSD, is that it eliminates the uncontrolled inrush of current that occurs when a stationary motor is connected to full line voltage, and also the inevitable suddenly applied high startup torque. Benefits are that the power wasted by current inrush is eliminated and that the life of the motor and the driven machine are prolonged by the gentle, progressive application of torque.

26.1.3.4 Improved Electrical System Power Factors

When a diode supply bridge is used for rectification, electric variable-speed drives operate at near unity power factor over the whole speed range (the supply delivers mostly real power). When a fully controlled thyristors supply bridge is used (as in dc, cyclo, and current-source drives), the power factor starts at around 0.9 at full speed, and proportionally worsens as speed declines due to front-end thyristors (typically 0.45 at 50 speed and 0.2 at 25 speed).

Modern pulse-width modulated (PWM) drives convert the three-phase ac line voltage to a fixed-level dc voltage. They do this regardless of inverter output speed and power. PWM inverters, therefore, provide a constant power factor regardless of the power factor of the load machine and the controller installation configuration, for example, by adding a reactor or output filter between the VSD and the motor.

26.1.4 Disadvantages of VSDs

The implications of using a VSD is generally space, cooling and capital cost. Some of the drawbacks are:

- Acoustic noise
- Motor derating
- Supply harmonics

PWM voltage-source inverter (VSI) drives, equipped with fast switching devices, added other possible problems such (a) premature motor insulation failures, (b) bearing/earth current, and (c) electro-magnetic compatibility (EMC).

26.1.4.1 Acoustic Noise

In some installations, placing a VSD on a motor increases the motor's acoustic noise level. The noise occurs when the drive's nonsinusoidal (current and voltage) waveforms produce vibration in the motor's laminations. The nonsinusoidal current and voltage waveforms produced by the VSD are the result of the transistor switching frequency and modulation in the dc-to-ac inverter. The switching frequency, fixed or variable, determines the audible motor noise. In general, the higher the carrier frequency, the closer the output waveform is to a pure sine wave. One method of reducing audible motor noise is full-spectrum switching (random switching frequency). VSD manufacturers accomplish full-spectrum switching by an algorithm within the VSD controller. The motor performance is optimized by evaluating motor characteristics, including motor current, voltage, and the desired output frequency. The resulting frequency band, though audible to humans, produces a family of tones across a wide frequency band. So, the perceived motor noise is considerably less than it would be with a single switching frequency.

Motor noise may not present a problem. Relevant factors include motor locations and the amount of noise produced by other equipment. Traditionally motor noise level is reduced by adding an LC filter between the VSD and the motor, i.e., reducing the high-frequency component of the motor voltage waveform. Modern PWM inverter drives run at very high switching frequency and with random switching frequency, thus reducing the noise level as well. Various methods have been proposed to reduce the magnetically generated noise that is radiated from inverter-fed induction motors.

26.1.4.2 Motor Heating

Most motor manufacturers design their products according to NEMA standards to operate on utility-supplied power. Designers base their motors' heating characteristics and cooling methods on power supplied at fixed voltage and frequency.

For many drive applications, particularly those requiring relatively low power, inverters with a high switching speed can produce variable voltage and variable frequency with little significant harmonic content. With these, either standard or high-efficiency induction motors can be used with little or no motor derating. However, the inverters used in larger drives have limits on switching rate that cause their output voltages to contain substantial harmonics of orders 5, 7, 11, 13, and so on. These, in turn, cause harmonic currents and additional heating (copper and iron losses) in the stator and rotor windings. These harmonic currents are limited mainly by the leakage inductance. For simple six-step inverters, the additional power losses, particularly those in the rotor, may require derating of the motor by 10–15%.

Existing constant-speed drives often have an oversized induction motor. These can usually be converted to variable-speed operation using the original induction motor. Most of the subsequent operation will be at lower load and lower loss than that for which the motor was designed.

Modern PWM VSI drives produce a voltage wave with negligible lower-order harmonics. The wave consists of pulses formed by switching at relatively high frequency between the positive and negative sides of the dc link voltage supply. With larger motors that operate from ac supplies up to 6600 V, the rapid rate of change of the voltage applied to the winding may cause deterioration and failure in the insulation on the entry turns of standard motors.

On self-ventilated (fan-cooled) motors, reducing the motor shaft speed decreases the available cooling airflow. Operating a motor at full torque and reduced speed results in inadequate airflow. This consequently results in increased motor insulation temperature. This potentially can be damaging and can reduce the life of the motor's insulation or cause the motor to fail. One potential solution is to add a constant-speed, separately driven cooling fan to the motor. This approach ensures adequate stator cooling over the whole speed range. However, the rotor will run hotter than designed, as internal airflow remains a function of speed. As there are no windings in the rotor insulation, failure is not an issue, but bearings may run hotter and require more frequent lubrication.

Fan-cooled motors with centrifugal loads present less of a problem. Pumps and fans, for example, do not require full torque at reduced speeds. So, in these cases, there is less thermal stress on motors at reduced speeds. Centrifugal load does not cause the motor to exceed thermal limits defined by the insulation system.

26.1.4.3 Supply Harmonics

Current and voltage harmonics in the ac supply are created by VSD (as a nonlinear load) connected on the power distribution system. Such harmonics pollute the electric plant, which could cause problems if harmonic level increases beyond a certain level. The effect of harmonics can be overheating of transformers, cables, motors, generators, and capacitors connected to the same power supply with the devices generating the harmonics.

The IEEE 519 recommended practices and requirements for harmonic control in electrical power systems. The philosophy of such regulations is to limit the harmonics injection from customers so that they will not cause unacceptable voltage distortion levels for normal system characteristics and to limit the overall total harmonic distortion of the system voltage supplied by the utility.

In order to reduce supply harmonics that are generated by VSDs equipped with a 6-pulse diode bridge rectifier, VSD equipment manufacturers adopt various techniques. Table 26.2 summarizes the most common methods and their advantages and disadvantages [2].

Reference [2] quantifies the cost of these options as a percentage of the cost of a basic system with a 6-pulse diode bridge. For low-power VSDs, the cost of a drive with a line reactor is estimated to be 120% of that without. A VSD with a 12-pulse diode bridge with a polygon transformer is 200%, whereas for a double-wound transformer it is 210%. The most

TABLE 26.2 Techniques used to reduce supply harmonics

Topology	Advantages	Disadvantages
6-pulse bridge with a choke	• Least expensive low cost • Known technology • Simple to apply	• Bulky • Too large a value can reduce available torque • Only applies to the drive • Least effective method of filtering
12-pulse bridge	• Eliminates the 5, 7, 17, 19 harmonics • Known technology • Simple to apply	• Bulky and expensive • Only applies to the drive • Many 12-pulse drives on one site will shift the problem to the 11th and 13th harmonics
6-pulse, fully controlled active front end	• Comprehensive filtering for the drive • Cancels all low-order harmonics	• Very expensive • Not widely available • New technology
Harmonic filters	• Filters the installation • Reduces the harmonics at the point of common coupling • Least expensive filter to install	• Needs a site survey • Only sized to the existing load
Active filter	• Intelligent filter • Extremely efficient • Can be used globally or locally • More than one device can be installed on the same supply	• Very expensive

expensive solution is that with active front end, estimated at 250 .

For a 6-pulse converter, $n6p \pm 1$ (5, 7, 11, 13, 17, 19, etc.)-order harmonics are generated. To minimize the effects on the supply network, recommendations are laid down IEEE 519 as to the acceptable harmonic limits. For higher drive powers, therefore, either harmonic filtering or use of a higher converter pulse number is necessary. It is generally true that the use of a higher pulse number is the cheaper alternative. Reference [2] also quantifies the harmonic levels generated by each of the preceding methods: refer to Table 26.3 for a direct comparison.

TABLE 26.3 Supply harmonics for different supply-bridge configurations

Harmonic Order Number	5th	7th	11th	13th	17th	19th
6-pulse	63	52	10	6	7	5
6-pulse with inductor	30	12	9	6	4	4
12-pulse with polygon transformer	11	6	6	5	2	1
12-pulse with double wound transformer	4	3	8	5	1	1
24-pulse	4	3	1	1	1	1
Active front-end	3	2	1	0	0	0

26.2 Drive Requirements and Specifications

26.2.1 General Market Requirements

Some of the most common requirements of VSDs are high reliability, low initial and running costs, high efficiency across speed range, compactness, satisfactory steady-state and dynamic performance, compliance with applicable national and international standards (e.g., EMC, shock, and vibration), durability, high availability, and ease of maintenance and repairs.

The order and priority of such requirements may vary from one application to another and from one industry to another. For example, for low-performance drives such as fans and pumps, the initial cost and efficiencies are paramount, as the main reason for employing variable-speed drives is energy savings. However, in other industries such as marine applications, the compactness of the equipment (high volumetric power densities) is a priority requirement because of the shortage of space. In such environments direct raw water cooling is the preferred choice as water is plentiful, and forced water cooling results in a more compact drive solution.

In critical VSD applications, such as military marine propulsion, reliability, availability, and physical size are very critical requirements. Cost is relatively less critical. However, achieving these requirements adds to the cost of the basic drive unit. Series and parallel redundancy of components enable the VSD equipment to continue operation even with failed components. These are usually repaired during regular maintenance. In other critical applications (such as hot mill strips or subsea drives) the cost of drive failures could be many times more expensive than the drive itself. For example, accessing a drive down on the seabed, many kilometers below the face, could be very difficult.

This section identifies VSD requirements in various drive applications in different industries.

26.2.1.1 The Mining Industry

The majority of early generation large mine-winders are dc drives. Modern plants and retrofits generally employ cyclo converters with ac motors. However, small mine-winders (below 1 MW) tend to remain dc.

The main requirements are as follows:

- High reliability and availability
- Fully regenerative drive
- Small number requiring single-quadrant operation
- High range of speeds
- High starting torque required
- High torque required continuously during slow speed running
- Low required torque ripple
- Low supply harmonics
- Low audible noise emissions
- Flameproof packaging

26.2.1.2 The Marine Industry

The requirements of this industry are the following:

- Low initial purchase price
- Reliability
- Ease of maintenance, i.e., minimum component count, simple design
- Small size and light weight of equipment
- Transformerless, water-cooled VSD equipment always preferred

Other desirable features include the following:

- A requirement for the integration of power management functions
- High volumetric power density (the smallest possible)
- Remote diagnostics, to allow fault finding by experts onshore in critical situations.

Drive powers are commonly in the range of 1 to 6 MW for thrusters, and 6 to 24 MW for propulsion. The evolution in the commercial market is toward powers from 1 to 10 MW for propulsion. Higher powers are required for naval applications. The package drive efficiency must be equal to, or better than, 96 . Noise and harmonics problems are to be considered when using PWM inverters. The supply-side harmonics produced must be capable of being filtered. Above 1 MW, power converters are usually equipped with 12-pulse supply bridge, given today's technology.

Two-quadrant operation required in general; hence, diode supply bridge is adequate. The occasional requirement for crash stops forces the use of a dynamic brake chopper. A dc bus can be advantageous for supply to wharf loading equipment, but the drive power ranges are such that commercially available products already adequately serve this application.

The use of standard ac machines is desirable; however, if motors matched to the inverter prove to be cheaper, their use could be preferred. Low noise emission (acoustic and electromagnetic) is very important. There is no requirement for high torque at low speed. Programming and expanded input and output capabilities help avoid the need for additional programmable logic control (PLC).

26.2.1.3 The Process Industries

The main requirements of this market are as follows:

- Low initial purchase price (long-term cost of ownership does not generally influence purchasing decision)
- Efficiency in continuous processes
- Reliability
- Ease of maintenance
- Bypass facility

The industry preference is for air-cooled drives. It is perceived that air-cooled drives are less costly than their water-cooled equivalents. Customers often have the belief that water and electricity do not mix well and are wary of problems with leaks. The exception is the offshore industry, where equipment size is paramount, and therefore, water cooling is standard. In general there is no perceived requirement for space saving in the majority of process plants. The desirable features often requested by customers are ease of maintenance and good diagnostic facilities.

The market requirement is for cost-effective, stand-alone drives at various power levels from a fraction of a kilowatt up to 30 MW. The use of standard ac machines is desirable. However, if nonstandard, but simpler and cheaper machines can be offered, an advantage could be gained.

- Two-quadrant operation for fans, pumps, and compressors
- Four-quadrant operation for some test benches
- Control that allows additional functions such as temperature protection, motor bearing temperature, and flow and pressure control
- No requirement, in general, for field weakening
- Harmonics produced by the drive imposed on the power system that should not require a harmonic filter (harmonics must be minimized)

In the low-voltage (LV) arena, the PWM VSI is dominating the market. In the medium-voltage (MV) arena, there are a number of viable drive solutions such as load-commutated inverters (LCIs) and cyclo converters. However, there is a developing market for MV PWM VSI drives.

26.2.1.4 The Metal Industries

The requirements of this industry are as follows:

- Reliability high availability
- Efficiency of the equipment long term costs of ownership
- Low maintenance costs (this has been a key factor in the move from dc to ac)
- Power supply system distortion more onerous regulations from the supply authorities
- Initial purchase cost very competitive market, and large drive costs have a big impact on total project costs
- Confidence in the supplier and their solution

The following is a list of desirable features:

- Programmable system drives with powerful programming tools
- Preference for air-cooled stacks (water-cooled is acceptable if a water-to-air heat exchanger is used)
- Powerful maintenance and diagnostic tools
- Low EMC noise signature
- Ability to interface to existing automation system via network, Fieldbus, or serial link
- Physical size of equipment often not an important consideration
- Fire protection systems integral to drive equipment

The main market concerns are (a) EMC regulations, (b) effects on motor insulation of higher voltage levels, and (c) cooling with "dirty" mill water is not acceptable. The maintenance of de-ionised water circuits is a big issue.

26.2.2 Drive Specifications

Failure to properly specify an electric VSD can result in a conflict between the equipment's supplier and the end user. Often the cost can be delayed project completion and/or loss of revenue.

TABLE 26.4 Typical example of VSD specifications

Variable	Specification
Application	Dynamometer application for a test bench
Motor type	Induction motor
Duty cycle	Continuous at full rating; 150 overload for 1 minute every 60 minutes
Power rating	100 kW
Supply voltage	690 V ± 5
Supply frequency	50 ± 0.05 Hz
Speed range	1000 : 1
Accuracy	0.1
Min/max speed	0/1500 rpm
Torque dynamic response	<10 ms from 100 positive torque to 100 negative torque
Power factor	>96 lagging at all speeds
Efficiency	>98 at full load
Performance	Fully regenerative Full torque at zero speed
Ambient temperature	0–40 °C
Supply harmonics	G5/4 or IEEE519
Life expectancy	>5 years
MTBF	>50,000 hours
MTTR	<2 hours
IP rating	IP45
IEEE 519	IEEE recommended practices and requirements for harmonic control in electrical power systems
IEC 60146	Semiconductor converters; specifications of basic requirements
IEC 61800	Adjustable-speed electrical power drive systems

In order to avoid such a problem, requirement specifications should reflect the operating and environmental conditions (Table 26.4). The equipment supplier and the customer need to work as partners and cooperate from the beginning of the project until successful commissioning and handover. It is advisable that the enduser procure the complete drive system, including system engineering, commissioning, and engineering support, from one competent supplier.

It is one of the first priorities to identify applicable national and international standards on issues related to EMC, harmonics, safety, noise, smoke emissions during faults, dust, and vibration. Overspecifying the requirements could often result in a more expensive solution than necessary. Underspecifying the requirements, result in poor performance and disappointment.

As far as end users are concerned, they need to specify the drive interfaces, and the ac input voltage, shaft mechanical power, and shaft speed the torque and current are calculated from these. Frequency and power factor depend on the choice of motor.

For high-power drive, it is always recommended to carry out a "harmonic survey." Such a survey will reveal the existing level of harmonics and quantify the impact of the new drive on the harmonic levels.

26.3 Drive Classifications and Characteristics

Table 26.5 illustrates the most commonly used classifications of electric VSDs. In this section, particular emphasis will be given to classification by applications and by converter types.

Other classifications, not listed in Table 26.5, include the following:

- Working voltage: Low voltage <690 V, or medium voltage (MV) 2.4–11 kV
- Current type: Unipolar or bipolar drive
- Mechanical coupling: Direct (via a gearbox) or indirect mechanical coupling
- Packaging: Integral motors as opposed to separate motor inverter
- Movement: Rotary movement, vertical or linear
- Drive configuration: Stand-alone, system, dc link bus
- Speed: High speed and low speed
- Regeneration mode: Regenerative or nonregenerative
- Cooling method: Direct and indirect air, direct water (raw water and deionized water)

Section 26.2 deals with the subject of drive requirements and specifications from the applications point of view; Section 26.5 deals with drive topologies from the point of view of motor classifications.

26.3.1 Classification by Applications

Under this classification there are four main groups:

- Appliances (white goods)
- General-purpose drives
- System drives
- Servo drives

Table 26.6 describes the main features of these groups and lists typical applications.

26.3.2 Classification by Type of Power Device

The silicon-controlled rectifier (SCR), also known as the thyristor, is the oldest controllable solid-state power device and still the most widely used power device for MV ac voltages between 2.4 and 11 kV high-power drive applications. Such devices are available at high voltages and currents, but the maximum switching frequency is limited and requires complex commutation circuit for VSI drive. SCRs are therefore most popular in applications where natural commutation is possible (e.g., cyclo converters and LCI current-source converters).

The gate turn-off thyristor (GTO) has made PWM VSI drives viable in LV drive applications. The traction industry was one of the first to benefit from such a device on a large scale. Complex gate drive and limited switching performance, combined with the need for a snubber circuit, limited this device to high-performance applications where the SCR-based drives could not give the required performance.

The main power devices available in the market can be divided into two groups, as shown in Table 26.7 [3]. Bipolar/Mosfet-type transistors experienced significant popularity in the late 1980s; however, they have been replaced by the IGBT, which combines the characteristics of both devices: the current-handling capability of the bipolar transistor and the ease of drive of the MOSFET.

TABLE 26.5 Classifications of electric VSD

By Application	By Devices	By Converter	By Motors	By Industry	By Rating
• Appliances	• Thyristor	• ac/dc (chopper)	• Dc	• Power generation	• Fraction kW power <1 kW
• Low performance (2Q)	• Transistor	• ac/ac direct (cyclo and matrix converter)	• Induction motor (squirrel cage and wound rotor)	• Metal	• Low power ($1 < P < 5$ kW)
• High performance (4Q)	• Gate turn- off thyristor (GTO) • Integrated gate commutated thyristor (IGCT)	• ac/ac via a dc link voltage source	• Synchronous motor	• Petrochemical	• Medium power < 500 kW
• Servo	• Insulated gate bipolar transistor (IGBT)	• ac/ac via a dc link current source	• *Special motors*: SRM, BDCM, stepper, actuators, linear motor	• Process industry	• High power 1–50 MW
	• MOSFET			• Mining • Marine	

TABLE 26.6 Classification of electric VSD by application

Type of Drive	Appliances	General Purpose	System	Servo
Performance	Low	Low	High	Very high
Power rating	Very low	Whole range	Whole range	Low
Motor	Universal and Induction motor; recently, PM and SRM are being used	Dc motor, induction motor, and synchronous motor	Dc motors Induction motors Synchronous motors	Dc motors Brushless dc motors Induction motor Stepper motors Actuators
Converter	Simple, low cost	Ac and dc drives with open-loop controller	PWM drives with dc bus Cyclo converter Good quality control with closed-loop control Needs encoder or observer	Dc drives, ac drives, special motor drives Tendency toward brushless dc motors
Typical industry	Home	Process	Metal	Automation
Feature	Mass production Low cost Price sensitive Very low power	Nonregenerative Cost sensitive Low or no overload Low startup Low-performance stand-alone	Accuracy with encoders <0.1 in steady-state and dynamic Good precision and linearity of I/O and control Flexible with operations capability Setup and configuration Communication and feedback	Closed-loop, PM motor >1000 Hz torque response Precise and rapid response Frequent full- speed reversal High precision Linearity of I/Os
Applications	Home appliances such as washing machines, dishwashers, tumble-dryers, freezers	Fans, pumps, and compressors Mixers Simple elevators	Test benches Winders Sectional process lines Elevators Cranes Hoists	Positioning, pick and place, robotics, coordinate control, machine tools

Traction inverters are designed for dc link voltages between 650 V dc and 3 kV dc with ratings up to 3 MW. The first generation of widely used traction inverter equipment was GTO based; the latest generation is almost exclusively IGBT based. Conversion to IGBT has enabled a 30 to 50 reduction in cost, weight, and volume of the equipment.

Early attempts to use GTOs in MV applications failed because of their high cost, snubber requirements, and associated snubber energy loss, which is proportional to the square of the supply voltage. Energy recovery circuitry enables recovery of most of the snubber energy but added to the cost and complexity of the converter. With high-voltage IGBT and IGCT, MV PWM VSI have become commercially available with supply voltage up to 6.6 kV, and power rating in excess of 19 MW.

26.3.3 Classification by Type of Converter

The power converter is capable of changing both its output voltage magnitude and frequency. However, in many applica-

TABLE 26.7 Power devices used in VSD converters [3]

Group 1: Thyristors	Group 2: Transistors
This group covers devices having a four-layer, three-junction monolithic structure. They are characterized by by low conduction losses and high surge and current carrying capabilities. They operate as an on/off switch. The most popular types of devices listed under this group: • Silicon-controlled rectifier (SCR) • Gate turn-off thyristor (GTO) • MOSFET- controlled thyristor (MCT) • Field-controlled thyristor (FCT) • Emitter-switched thyristor (EST) • MOS turn-off thyristor (MTO) • Integrated-gate commutated thyristor (IGCT)	Switches listed under this group are basically three-layer two junction structure devices, which operate in switching and linear modes. They are best recognized for ruggedness of their turn-off capabilities. • Bipolar junction transistor (BJT) • Darlington transistor • MOSFET • Injection-enhanced gate transistor (IEGT) • Carrier stored trench-gate bipolar transistor (CSTBT) • Insulated-gate bipolar transistor (IGBT)

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tions these two functions are combined into a single converter by the use of the appropriate switching function, e.g., PWM. By appropriate control of the stator frequency of ac machines, the speed of rotation of the magnetic field in the machine's air gap and thus output speed of the mechanical drive shaft can be adjusted. As the magnetic flux density in the machine must be kept constant under normal operation, the ratio of motor voltage over stator frequency must be kept constant.

The input power of the majority of VSD systems is obtained from sources with constant frequency (e.g., ac supply grid or ac generator). In order to achieve a variable-frequency output energy, an ac/ac converter is needed. Some converters achieve direct power conversion from ac/ac without an intermediate step (e.g., cyclo converters and matrix converters). Other converters require a dc link (as current source or voltage source).

In all ac variable-speed drives, the direction of shaft rotation is reversed by simply changing the phase rotation of the inverter through the sequence of driving the switches.

26.3.3.1 Dc Static Converter

This drive employs the simplest static converter. It is easily configured to be a regenerative drive with a wide speed range. Table 26.8 summarizes its key features.

High torque is available throughout the speed range with excellent dynamic performance. Unfortunately, the motor requires regular maintenance and the top speed often is a limiting factor. Commutator voltage is limited to around 1000 V, and this limits the maximum power available. The continuous stall torque rating is very limited because of the motor's commutator.

26.3.3.2 Direct ac/ac converters

. . . . ***Cyclo Converter*** A typical cyclo converter comprises the equivalent of three antiparallel 6-pulse bridges (for regenerative converter) whose output may be operated in all four quadrants with natural commutation. The main features of cyclo converters are listed in Table 26.8. This type of drive is best suited to high- performance, high-power >2 MW drives where the maximum motor frequency is less than 33 of the mains frequency.

. . . . ***Matrix Converter*** The force-commutated cyclo converter (better known as a matrix converter) represents possibly the most advanced state of the art at present, enabling a good input and output current waveform, as well as eliminating the dc link components with very little limitation in input to output frequency ratio. This type of converters is still at its early stages of development. The main advantage of this drive is the ability to convert ac fixed-frequency supply input to ac output without a dc bus. It is ideal for integrated motor drives with relatively low power ratings. Major drawbacks include (a) the increased level of silicon employed (bidirectional switches), (b) the fact that its output voltage is always less than its input voltage, and (c) the complexity of commutation and protection.

Matrix converters provide direct ac/ac power conversion without an intermediate dc link and the associated reactive components. They have substantial benefits for integrated drives as outlined below:

- Reduced volume due to the absence of dc link components
- Ability to operate at the higher thermal limit imposed by the power devices
- Reduced harmonic input current compared to diode bridge
- Ability to regenerate into the supply without dumping heat in dynamic braking resistors

Matrix converters have not been commercially exploited because of voltage ratio limitation, device count, and difficulties with current commutation control and circuit protection.

26.3.3.3 Current-Source Inverter CSI

The output of this inverter is rectangular blocks of current from the motor bridge supplied from a supply converter whose output is kept at constant current by a dc link reactor and current servo. This type of inverter is typically based on fast thyristors.

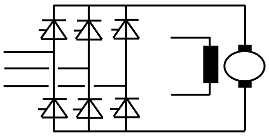
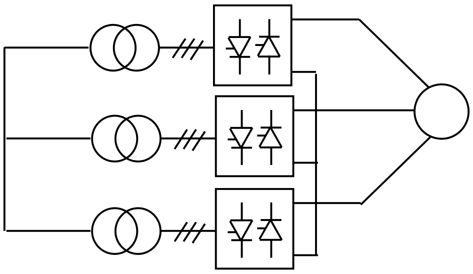
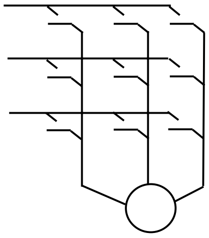
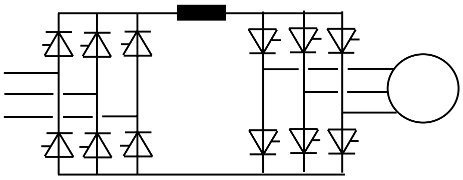
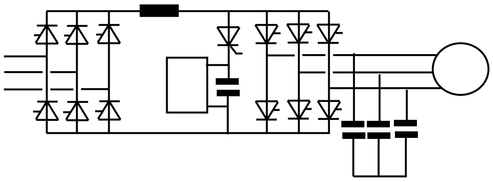
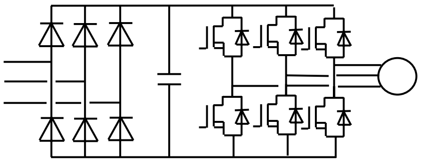
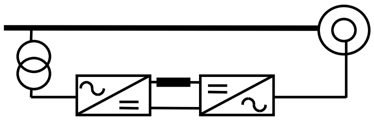
. . . . ***Load-Commutated Inverter (LCI)*** Natural commutation of thyristors is usually achieved with synchronous machines at speeds >10 . Natural commutation is induced as a result of the presence of the motor's electromotive force (EMF). This is called load commutation; hence the drive's other name of LCI. At low speeds the motor voltage is too low to give motor bridge commutations. This is achieved by using the supply converter. Induction-motor LCI drives can be supplied by adding a large capacitor on the motor terminals.

The LCI drive covers a wider speed range (up to 10,000 rpm) with power rating up to 100 MW. It gives full-load torque throughout the speed range with moderate dynamic performance. Its simple converter design combined with a maintenance-free motor design (both induction and synchronous) has increased the popularity of these drives. It is still a popular solution for high-power drives (e.g., conveyors, pumps, fans, compressors, and marine propulsion).

The LCI drive has limited performance at low speeds. It also suffers from torque pulsation at 6 and 12 times motor's frequency and beat frequencies. Critical speeds can excite mechanical resonance. Its ac power factor varies with speed. Torque pulsations can be reduced in 12-pulse systems if required.

. . . . ***Forced Commutated Inverter (FCI)*** Externally commutated current source converters with an induction motors are also a viable solution. To compensate for the

TABLE 26.8 Converter topologies

Converter	Schematic	Features
(a) Controlled rectifier		Dc motor Fully controlled SCR converter Controlled dc voltage Simple converter topology Power factor is a function of speed
(b) Cyclo		Induction motor and synchronous motor Direct ac/ac power conversion 3 × 6-pulse SCR-based fully controlled converters APT for fully regen Natural commutation Low supply harmonics, 18-pulse Power factor is a function of speed
(c) Matrix		Squirrel-cage induction motor Synchronous motor Direct ac/ac power conversion Forced commutated, reverse conducting switches 4-quadrant operation inherent PWM in/PWM out Controlled power factor
(d) LCI		Synchronous motor Simple converter arrangement Power factor is function of speed Load-commutated SCRs Synch motor requires excitation Suffers from torque pulsation at low speeds
(e) FCI		Squirrel-cage induction motor Similar to LCI Requires output capacitors for commutation Requires a diverter commutation circuit for commutation at low speeds Torque pulsation and resonance
(f) VSI		Synchronous and squirrel-cage induction motors. 6-pulse diode front end Good power factor across speed range Dc link voltage source PWM output voltage
(g) Kramer		Wound-rotor induction motor with slip rings. Small energy recovery converter Any type converter may be used between slip ring and ac input

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inductive component in the motor current, a bank of capacitors is usually used at the motor terminals. The capacitor current is proportional to the motor voltage and frequency. Load commutation occurs at high speed where the compensation current is high enough. Forced commutation occurs at lower speed where the capacitive current is too low for compensation. Forced commutation is achieved using various techniques. The one shown in Table 26.8 is based on a dc link diverter that consists of a GTO and loading equipment in parallel with the diverting/compensating capacitor. Modern drives employ forced commutated devices, such as reverse blocking GTOs and IGCTs.

26.3.3.4 Slip Power Recovery ramer

In this type of converter, which is described in Table 26.8, the rotor current of a slip ring wound rotor induction motor is rectified and the power then reconverted to ac at fixed frequency and fed back into the supply network. For traditional designs, the low-frequency slip-ring currents are rectified with a diode bridge and the dc power is then inverted into ac power at mains frequency.

The traditional designs had poor ac mains dip immunity, high torque pulsation, and high levels of low-frequency ac supply harmonics. The latest generation of this type of drive is called the rotor drive and uses PWM-VSI inverters for the rotor and ac supply bridges. This keeps sine wave currents in the ac rotor circuits.

The drive has many advantages over traditional circuits:

- No torque pulsation
- Low ac harmonics
- Very high immunity to ac supply dips

TABLE 26.9 Drive features

Type	Dc Drive dc	Ac Drives				
		Cyclo	CSI (FCI)	CSI (LCI)	Kramer	PWM-VSI
Motor type	Dc motor	Induction and synchronous motors	Induction motor	Synchronous motor	Slip-ring wound- rotor induction motor	Induction or synchronous
Power	Up to 10 MW	2 to 30 MW	1 to 10 MW	1 to 100 MW	0.5 to 50 MW	0.5 to 2 MW
Speed range	1000 : 1	1000 : 1	10 : 1	10 : 1	0.8 : 1.2	1000 : 1
Accuracy	0.01	± 0.01	± 1	± 0.01	0.1	0.01
Max. speed	Limited by motor capability	1000 rpm	6000 rpm	10,000 rpm	<1200 rpm	10,000 rpm
Performance	High torque over speed range High dynamic performance	High torque over speed range High dynamic performance	Poor dynamic response Low starting torque	High torque over speed range Reasonable dynamic performance	High torque over speed range High dynamic performance	High torque over speed range High dynamic performance
Advantages	Simple Regenerative	High stall torque (induction) Inherently regenerative Robust motors Low maintenance motor High overload capacity	Standard robust maintenance-free motor Minimal derating	Simple Inherent regenerative Maintenance-free motor	Regenerative (new) Robust Slip-ring wound rotor High overload capacity	Good power factor Tolerant to supply dips Standard robust maintenance-free motor Minimal derating
Disadvantages	Stall torque rating Motor maintenance Custom motor design	Motor custom design Low ac supply power factor	Complex Poor dynamic performance Torque pulsation and resonance	Motor custom design Torque pulsation	Complex Motor custom design	Complex Expensive Regeneration at extra cost
Applications	Mill drives (ball and sag) Marine propulsion Mine winders Process lines Conveyors	Mill drives (ball and sag) Marine propulsion Mine winders Conveyors	Pumps, fans, and compressors Soft-starter	Pumps, fans, and compressors Soft- starter Marine propulsion Conveyors Mill drives	Pumps, fans, and compressors Power generation Mills (ball and sag)	Process lines Paper machines Traction

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- Very cost effective if a limited speed range is required, but still requires a separate starter
- Inherent ability to run at rated speed without electronic circuits
- Converter cost reduced by 2 : 1 if uses the ± speed ability to give a speed range

26.3.3.5 PWM VSI Converter

The availability of power electronics switches with turn-off capability, e.g., FETs, BJTs, IGBTs, and GTOs, has currently favored drives with voltage-fed PWM converters on induction.

PWM VSI drives offer the highest possible performance of all variable speed drives; refer to Table 26.9. Recent improvements in switching technology and the use of microcontrollers have greatly advanced this type of drive. The inverters are now able to operate with an infinite speed range. The supply power factor is always near unity. Additional hardware is easily added if there is a requirement to regenerate power back into the mains supply. Motor ripple current is related to the switching frequency and in large drives the motor may be derated by less than 3%.

26.3.3.6 Comparison

Table 26.9 summarizes the main features of all types of converter drives discussed above and assess their merits and drawbacks. It also illustrates typical applications.

26.4 Load Profiles and Characteristics

The way the drive performs is very much dependent on the load characteristics. Four load characteristics are now described.

26.4.1 Load Profile Types

In the literature, four different load profiles have been described [4] (see Table 26.10):

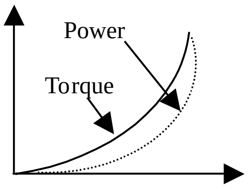
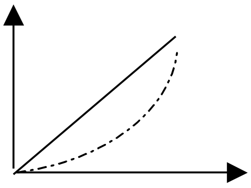
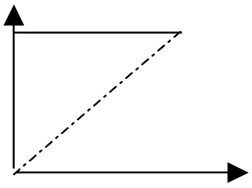
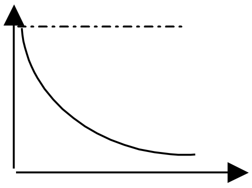
I. Torque proportional to the square of the shaft speed (variable torque)
II. Torque linearly proportional to speed (inear torque)
III. Torque independent of speed (constant torque)
IV. Torque inversely proportional to speed (inverse torque)

26.4.2 Motor-Drive Duty

26.4.2.1 Duty Cycle

The size of the driven motors is generally chosen for continuous operation at rated output, yet a considerable proportion of motor drives are used for duties other than continuous. As the output attainable under such deviating conditions may differ from the continuous rating, fairly accurate specification

TABLE 26.10 Load characteristics

Type I	Type II	Type III	Type IV
$T = f(\text{speed}^2)$ $P = f(\text{speed}^3)$ Low startup torque Best suited for energy saving Torque–speed curve is required when specifying a drive	$T = f(\text{speed})$ $P = f(\text{speed}^2)$ Information about process is needed (e.g., density, consistency, viscosity, temperature)	$T =$ Constant $P = f(\text{speed})$ At startup the torque may be higher than nominal, e.g., static friction with conveyor belts Vertical and horizontal forces need to be taken into consideration for inclined conveyors	$T = f(1/\text{speed})$ $P =$ Constant Mostly dominated by dc drives, but modern PWM VSI is talking over Certain loads such as windind and reeling machinery required closed-loop controls
Axial and centrifugal pumps Axial and centrifugal ventilators Screw and centrifugal compressors Centrifugal mixers Agitators	Mixers Stirrers	Extrusions, draw-benches Paper and printing continuous machines Volumetric gear pumps/pistons pumps, etc. Piston compressors Conveyor machines Lift machines	Lift machines Reciprocating rolling mills Winding machines Lathes Winders Reelers Wire drawers Web-feed printing machines
			

of the duty is an important prerequisite for proper planning. There is hardly a limit to the number of possible duty types.

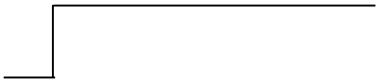
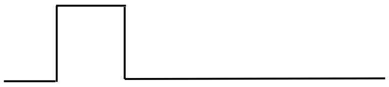
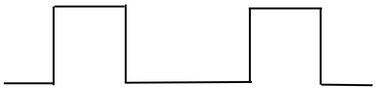
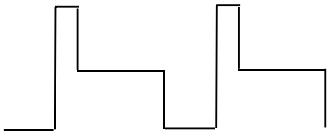
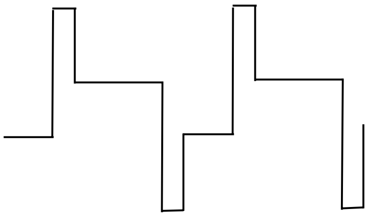
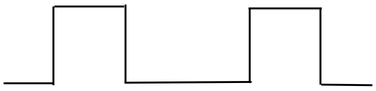
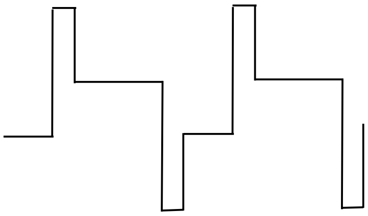
In high-performance applications, such as traction and robotics, the load and speed demands vary with time. During acceleration of traction equipment, a higher startup torque (typically twice the nominal torque) is required; this is usually followed by cruising and deceleration intervals. As the torque varies with time, so does the motor current (and motor flux linkage level). The electric, magnetic, and thermal loading of the motor and the electric and thermal loading of the power electronics converter are definite constraints in a drive specification.

Table 26.11 categorizes operating duties into eight major types [5].

26.4.2.2 Mean Output

Variation of the required motor output during the periods of loaded operation is among the most frequent deviations from the duty types defined in Table 26.11. In such cases the load

TABLE 26.11 Definition of load cyclic duties: VDE0530, in accordance with IEC 34-1 [5]

Duty Type	Representation	Description
S1: Continuous running duty		Operation at constant load of sufficient duration for the thermal equilibrium to be reached.
S2: Short-time duty		Operation at constant load during a given time, less than required to reach thermal equilibrium, followed by a rest and deenergized period of sufficient duration to reestablish machine temperatures within 2 °C of the coolant.
S3: Intermittent periodic duty with a high startup torque		A sequence of identical duty cycles, each including a period of operation at constant load and a rest and deenergized period. In this duty type the cycle is such that the starting current does not significantly affect the temperature rise.
S4: Intermittent periodic with a high startup torque		A sequence of identical duty cycles, each cycle including a significant period of starting, a period of operation at constant load, and a rest and deenergized period.
S5: Intermittent periodic duty with high startup torque and electric braking		A sequence of identical cycles, each cycle consisting of a period of starting, a period of operation at constant load, a period of rapid electric braking, and a rest and deenergized period.
S6: Continuous-operation periodic duty		A sequence of identical duty cycles, each cycle consisting of a period of operation at constant load and a period of operation at no load. There is no rest and deenergized period.
S7: Continuous-operation periodic duty with high startup torque and electric braking		A sequence of identical duty cycles, each cycle consisting of a period of starting, a period of operation at constant load, and a period of electric braking. There is no rest and deenergized period.
S8: Continuous-operation periodic duty with related load/speed changes		A sequence of identical duty cycles, each cycle consisting of a period of operation at constant load corresponding to a predetermined speed of rotation, followed by one or more periods of operation at other constant loads corresponding to different speeds of rotation. There is no rest and de-energized period.

(defined as current or torque) is represented by the mean load. This represents the RMS value, calculated from the load vs time characteristics. The maximum torque must not exceed 80% of the breakdown torque of an induction motor.

If the ratio of the peak torque to the minimum power requirements is greater than 2 : 1, the error associated with using the RMS output becomes excessive and the mean current has to be used instead. No such mean value approximation is possible with duty type S2, which therefore necessitates special enquiry.

Careful assessment of duty types S2 to S8 reveals that there exist two distinct groups:

1. Duties S2, S3 and S6 permit up rating of motors relative to the output permissible in continuous running duty (S1).
2. Duties S4, S5, S7 and S8 requiring derating relative to the output permissible in continuous running duty (S1).

26.4.2.3 Thermal Cycling

The drive duty cycle also affects the reliability and the life expectancy of power devices. Repetitive load cyclic duty results in additional thermal stresses on power devices. Frequent acceleration and deceleration of drives results in repetitive junction temperature rise and falls at the cyclic duty. The life expectancy of devices is often determined by the maximum allowed number of cycles for a given power device junction temperature rise.

Although this is true for all types of power devices, it is more critical for IGBTs where wire bonds and solder layers are used.

In modern IGBT-based converter design, the maximum junction temperature rise of the IGBTs is limited to a level, which ensures a conservative number of thermal cycles over the lifetime of the drive. Typical junction temperature rise is 30 °C for a repetitive cyclic duty (e.g., steel mill) and 40 °C for nonrepetitive cyclic duty (e.g., fan pumps).

26.4.2.4 Multiquadrant Operation

Fully regenerative electric VSDs offer a rapid regenerative dynamic braking in both forward and reversed directions. Operation in motoring implies that torque and speed are in the same direction (QI, III). In regenerative braking the torque is opposite to the speed direction (QII, IV) and the electric power flow in the motor is reversed. (See Fig. 26.2.)

Positive power flow of electric energy means that electric power is drawn from the power supply via the power electronics converter by the motor; negative power flow refers to electric power delivered by the motor in the generator mode to the power electronics converter. This could be regenerated back to the supply, or dissipated as heat in the dynamic brake dissipative mechanism.

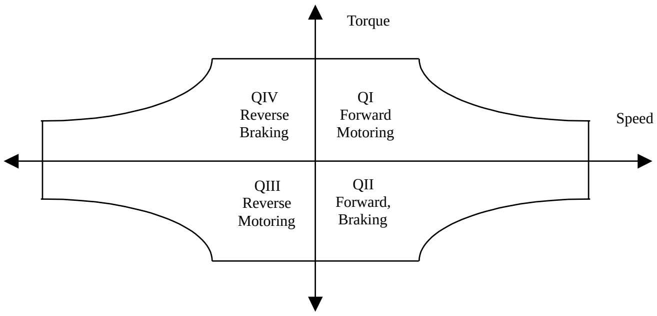


FIGURE 26.2 Operating regions of electric VSD.

For regenerative drive, the power electronics converter has to be designed to be able to handle bidirectional power flow. In low- and medium-power converters (say <500 kW) with slow dynamic braking demands, the generated power during the braking periods is interchanged with the strong filter capacitor of power electronics converter, or dc (dynamic) braking is used.

26.4.2.5 Dynamic Braking Energy

There exist two types of energy stored in VSD, which need to be dealt with during dynamic braking:

- *Inertia or kinetic energy loads.* Typically moving (rotating or linear) machines. These would decelerate naturally to rest. Braking can speed up the process cycle for the sake of productivity.
- *Mass or potential energy loads.* Typically hoists or lifts which would run on or even accelerate. Braking must apply full power to maintain constant speed while the load is lowered.

The drive losses, mechanical resistance, and transmission efficiency work in favor of deceleration, reducing the braking power demand. The energy regenerated by potential energy loads depends on maximum power and both the overrun time and the decelerating time.

The braking time and the duty cycle time are decided by the requirements of the process system, but note particularly the effect of varying the braking duty cycle time and the deceleration time. For dc injection braking, the kinetic energy of the motor–load system is converted to heat in the motor rotor. For fast and frequent generator braking, the power electronics converter has to handle the generated power either by a controlled dynamic brake chopper (with braking resistor) or through bidirectional power flow. The power losses in the converter can assist in dynamic braking.

For a fast speed response, modern variable-speed drives may develop a maximum transient torque up to base speed and maximum transient power up to maximum speed, provided that both the motor and the power electronics converter can handle these powers. For a 200-kW dynamometer drive application, a rapid change of torque from full positive torque to full negative torque is required in less than 10 ms.

26.5 Variable-Speed Drive Topologies

In this section drive topologies are classified according to the motor they employ. Various publications have dealt with this subject [6, 7]. The most common motors are illustrated in Fig. 26.3.

26.5.1 Dc Motor Drives

Until recently, the dc motor drive was the most commonly used type of electric-variable speed drive; with very few exceptions it is the least expensive. The mechanical commutator is an electromechanical dc to ac bidirectional power flow power converter, as the currents in the rotor armature coils are ac while the brush current is dc. The dc drive is well known, well proven, and widely applied, yet its popularity is in relative decline because of the emergence of the more robust, lower-cost squirrel-cage induction motor drive.

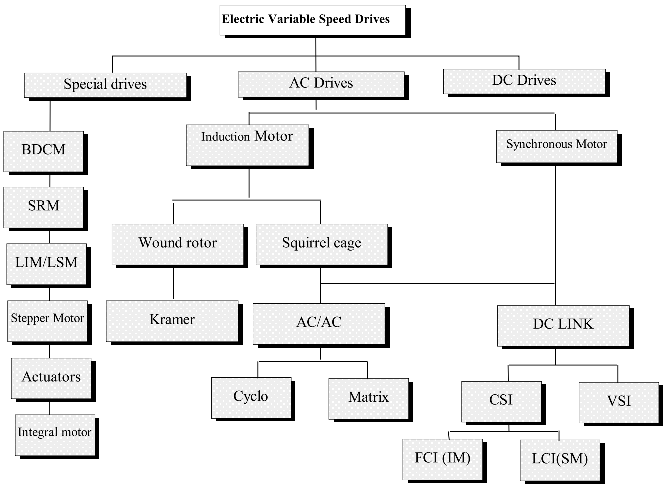


FIGURE 26.3 Classification of electric VSDs.

Unfortunately, the mechanical commutator, though not bad in terms of losses and power density, has serious commutation current and speed limits and thus limits the power per unit to 1–2 MW at 1000 rpm and may not be at all accepted in chemically aggressive or explosion-prone environments. The application of the dc drive has been restricted in hazardous areas because of the very limited availability of flameproof dc machines. Commutator and brush maintenance is difficult in such environments. Furthermore, continuous sparking at the brushes is virtually inevitable at full load output.

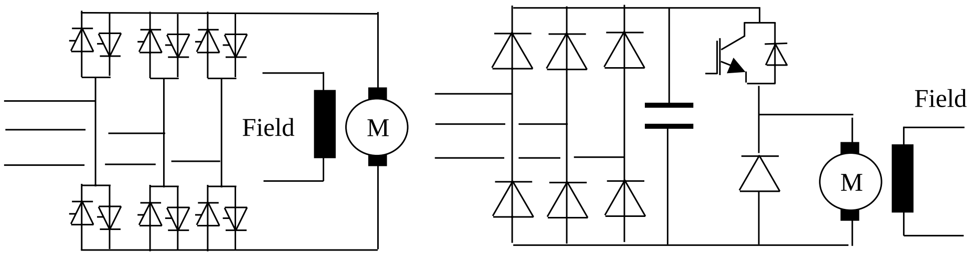
Because of the inherent ease of speed control of the separately excited dc machine, dc drives found popularity in early electric drive applications, by varying the applied armature voltage. This variable armature voltage is simply generated by phase-controlled rectification, and this technique has now almost entirely replaced the Ward–Leonard systems previously used.

The ac/dc converter offers a variable dc voltage, which is capable of four-quadrant operation (positive and negative dc voltage and dc current output). Permanent magnet–excited brushed motors have been used in numerous applications for sometime, particularly in nonregenerative drive applications.

Motor output torque is approximately proportional to armature current and motor speed approximately proportional to converter output voltage. Speed control by sensing armature voltage is therefore feasible, giving an accuracy of around 5 .

Provided the motor excitation is kept constant, the dc drive power factor is proportional to motor speed. Since most pumps, compressors, and fans demand a torque proportional to the square of speed, constant excitation systems are used and so the preceding relationship applies: A typical power factor at maximum rated speed for a dc drive is 0.85. This relationship applies to many other types of electric drives.

If a slow dynamic response is satisfactory, regeneration to the mains supply is achieved by reversing either the motor field or the armature connection. Alternatively, regeneration with faster response is achieved by connecting another thyristor bridge in antiparallel with the main bridge (Fig. 26.4a). In this case fast response is possible with changeover times of <15 ms between full torque motoring to full torque regenerating. The 6-pulse drive configuration is acceptable for powers



(a) (b)

FIGURE 26.4 Dc drive: (a) with fully controlled antiparallel supply bridge; (b) diode rectifier with dc chopper.

up to 1 MW. This limitation does not arise from any semiconductor device limitation, but is due to ac line current harmonics the converter generates.

A force-commutated or "chopper" converter for dc motors uses the principle of variable mark-space control using a thyristor or transistor solid-state switch. With a diode front-end converter, a fixed, smoother dc supply is derived from the mains by uncontrolled rectification and is rapidly applied, removed, and reapplied to the machine for adjustable intervals, thus applying a variable mean dc voltage to the dc motor; refer to Fig. 26.4b. This type of dc drive has the advantage of high (near-unity) power factor at all motor speeds and much reduced harmonic spectrum.

26.5.2 Induction Motor Drive

26.5.2.1 Squirrel-Cage Induction Motor

Squirrel-cage induction motors are simpler in structure than dc motors and are most commonly used in the VSD industry. They are robust and reliable. They require little maintenance and are available at very competitive prices. They can be designed with totally enclosed motors to operate in dirty and explosive environments. Their initial cost is substantially less than for commutator motors and their efficiency is comparable. All these features make them attractive for use in industrial drives.

The stator windings develop a rotating magnetic flux rotating at synchronous speed. This speed depends on the motor pole number and supply frequency: The rotating flux intersects the rotor windings and induces an EMF in the rotor winding, which in turn results in circulating current. The rotor currents produce a second magnetic flux, which interacts with the stator flux to produce torque to accelerate the machine. As the rotor accelerates, the induced rotor voltage falls in magnitude and frequency until an equilibrium speed is reached. At this point the induced rotor current is sufficient to produce the torque demanded by the load. The rotor speed is slightly lower than the synchronous speed by the slip frequency, typically 3%.

In order to ensure constant excitation of the machine, and to maximize torque production up to the base speed, the ratio of stator voltage to frequency needs to be kept approximately constant.

An induction motor drive has three distinct operating regions:

(a) *Constant torque.* The inverter voltage is controlled up to a maximum value limited by the supply voltage. As the motor speed and the voltage are increased in proportion, constant V/F, the rated flux linkage is maintained up to the base speed. Values of torque up to the maximum value can be produced at speeds up to about this base value. The maximum available torque is proportional to the square of the flux linkage. Typically, the induction motor is designed to provide a continuous torque rating of about 40–50% of its maximum torque.

(b) *Constant power.* For higher speed, the frequency of the inverter can be increased, but the supply voltage has to be kept constant at the maximum value available in the supply. This causes the stator flux linkage to decrease in inverse proportion to the frequency. Constant power can be achieved up to the speed at which the peak torque available from the motor is just sufficient to reach the constant power curve. A constant-power speed range of 2–2.5 can usually be achieved. Within this range, the motor frequency is increased until the machine limit is reached.

(c) *Machine limit (pullout torque).* Once the machine limit has been reached, the torque falls off in proportion to the square of motor frequency. Operation at the higher end of this speed range may not be feasible as the motor power factor worsens. This in turn results in a higher stator current than the rated value. The motor heating may be excessive unless the duty factor is low.

Induction motors are used in applications requiring fast and precise control of torque, speed, and shaft position.

The control method widely used in this type of application is known as vector control; a transient response at least equivalent to that of a commutator motor can be achieved.

The voltage, current, and flux linkage variables in this circuit are space vectors from which the instantaneous values of the phase quantities can be obtained by projecting the space vector on three radial axes displaced 120° from each other. The real and imaginary components of the space vectors are separated, resulting in separate direct and quadrature axis equivalent circuits but with equal parameters in the two axes.

Changes in the rotor flux linkage can be made to occur only relatively slowly because of the large value of the magnetizing inductance of the induction motor. Vector control is based on keeping the magnitude of the instantaneous magnetizing current space vector constant so that the rotor flux linkage remains constant. The motor is supplied from an inverter that provides an instantaneously controlled set of phase currents that combine to form the space vector, which is controlled to have constant magnitude to maintain constant rotor flux linkage. The second component is a space vector, which is in space quadrature with the instantaneous magnetizing current space vector. This component is instantaneously controlled to be proportional to the demand torque.

To the extent that the inverter can supply instantaneous stator currents meeting these two requirements, the motor is capable of responding without time delay to a demand for torque. This feature, combined with the relatively low inertia of the induction motor rotor, makes this drive attractive for high-performance control systems.

Vector control requires a means of measuring or estimating the instantaneous magnitude and angle of the space vector of the rotor flux linkage. Direct measurement is generally not feasible. Rapid advances are being made in devising control configurations that use measured electrical terminal values for estimation.

26.5.2.2 Slip-Ring Wound-Rotor Induction Motor Drive

Wound-rotor induction motors with three rotor slip rings have been used in adjustable-speed drives for many years. In an induction motor, torque is equal to the power crossing the air gap divided by the synchronous mechanical speed. In early slip-ring induction motor drives, power was transferred through the motor to be dissipated in external resistances, connected to the slip-ring terminals of the rotor. This resulted in an inefficient drive over most of the speed range. More modern slip-ring drives use an inverter to recover the power from the rotor circuit, feeding it back to the supply system.

The speed of slip-ring induction motor can be controlled by:

- Stator frequency control
- Rotor frequency control
- Rotor resistance control
- Slip energy recovery (Kramer drive)

The last two methods are traditionally used on cost grounds.

Addition of rotor resistance for starting large induction motors is well known. Adding rotor resistance alters the speed at which maximum motor torque is developed. Unfortunately, power dissipates as heat in the rotor resistance bank. Earlier means to overcome this shortcoming were to convert the rotor power to dc, and feed a dc motor on the same shaft. The rotor slip energy, when running at reduced speed, is therefore reconverted to mechanical power. This is the Kramer system. The disadvantages of this approach were the extra maintenance and capital costs.

The Kramer drive overcomes these shortcomings by replacing the dc machine with a line-commutated inverter that returns the slip energy directly to the ac line. A key advantage of the Kramer drive system is that the slip energy recovery equipment need only be rated for a fraction of the maximum motor rating, typically 30%. This is true when a small speed range is required and provided that a separate means is provided of starting the motor. This is because the motor rotor current is proportional to torque and the rotor voltage inversely proportional to speed.

If the slip-energy recovery converter can be rated to withstand full rotor voltage (at start up), a controlled speed range of zero to maximum could be achieved. However, this is generally only feasible on motors below 2000 kW where the rotor voltage is sufficiently low for an economic inverter package. Secondly, if a full speed range is needed, the slip-energy recovery converter has to be rated at full motor power, so Kramer drives become uneconomic for wide speed ranges. The overall system power factor would be very low for a wide-speed-range system.

For these reasons, Kramer drives are very suitable for high-power drives (>200 kW) where a small speed range is required. Pump and fan drives therefore present good economic applications. Kramer drives have also been used for low-speed-range endurance dynos using the recovery system to the control torque of the induction generator. As with all line-commutated converters and inverters, current harmonics are produced, and these can be reduced to acceptable values. However, as the slip-energy recovery network is only power-rated in direct proportion to the speed reduction required (assuming constant load torque), the magnitudes of the harmonic currents generated are proportionally less than with drives where the solid-state converters have to handle the whole drive power. Harmonics of the rotor rectifiers are transmitted through the rotor and appear as noninteger harmonics in the main supply.

The main disadvantages of the slip-ring induction motor drive are (a) the increased cost of the motor in comparison with a squirrel cage, (b) the need for slip-ring maintenance, (c) difficulty in operating in hazardous environments, (d) the need for switchable startup resistors, and (e) the poor power factor compared with other types of drive.

26.5.3 Synchronous Motor Drives

If the induction motor were to rotate at the synchronous speed by an external means, the frequency and magnitude of the rotor currents would become zero. If an external dc power supply were connected to the rotor winding, then the rotor would become polarized in a similar way to a permanent magnet. The rotor would pull into step with the air-gap-rotating magnetic field, generated by the stator but lagging it by a small constant angle referred to as the load angle. The load angle is proportional to the torque applied to the shaft, and the rotor keeps rotating at synchronous speed, provided that the dc supply is maintained to the rotor field winding. The magnetic flux produced by the rotor winding intersects the stator windings and generates a back EMF, which makes the synchronous motor significantly different from the induction motor.

As with the induction motor drive, the requirement is to keep the ratio V/F constant (i.e., to vary both the stator frequency and the applied voltages in proportion to the desired motor speed).

The supply bridge converter is phase controlled, generating an adjustable dc current in the dc link choke. To generate maximum torque from the synchronous motor, this current is switched into the motor stator windings at the correct phase position with respect to the rotor angular position as detected by the position sensor by the inverter bridge. When running above about 10 speed, the back EMF generated by the synchronous motor is sufficient to commutate the current into the next arm of the inverter bridge. So, as this type of inverter is machine (motor) commutated, the inverter configuration is merely that of a conventional dc drive. The complexity, expense, and limited power capability of the force-commutated circuitry is therefore avoided.

The motor back EMF is insufficient for thyristor commutation at low speeds. The technique here, therefore, is to rapidly phase back the supply converter bridge to reduce the dc link current to zero and after a short delay (to ensure that all thyristors in machine bridge are turned off) reapply dc current when the correct thyristor trigger pattern has been reestablished. As the motor speed, and thus back EMF, increase to a value sufficient for machine commutation, changeover to continuous dc link current operation is effected.

During the starting mode, the correct inverter bridge firing instant is determined by a rotor position sensor mounted on the motor shaft whose angular position is detected by opto or magnetic probes. In the machine-commutated mode, sensing of stator voltage is used. To develop maximum torque in the low-speed or pulsed mode, angular rotor position sensing is necessary. However, if less than full load torque availability at low speed can be tolerated, the inverter system can be set to produce a low fixed frequency in the pulsed mode. This frequency is then increased, as motor rotation is detected (either in steps or on a preset ramp rate) until sufficient back EMF is generated to facilitate changeover to the voltage-sensing mode.

As previously stated, the key advantage of this type of drive is that all thyristor devices are line or machine commutated. Complex forced commutation circuitry is avoided and fast turn-off thyristors are unnecessary. Inverter systems of this type can therefore be built at very high powers, up to 100 MW. Also, as a result of avoiding force commutation, converter efficiency is high, typically 98 .

The thyristors in the machine inverter bridge must be triggered at an angle that gives sufficient time for commutation from one device to the next. This results in the synchronous motor operating at a high leading power factor. However, the power factor is proportional to speed.

This type of drive is inherently reversible and regenerative. For regenerative operation, the inverter bridge is triggered in the fully advanced position. A dc output voltage is generated at the dc side of the supply converter bridge. This converter bridge is now triggered in the regenerative mode, thus back-feeding power to the supply system. Speed reversal is achieved by altering the sequence in which the thyristors in inverter bridge are triggered.

This type of drive is widely applied over a wide power range, as it comprises an efficient motor and simple and efficient converter. At lower powers, permanent magnet motors are more popular.

Unlike the induction motor, the synchronous type requires two types of converter. The first is for main power conversion; the second is low power for field excitation. The field converter feeds the rotor exciter winding through slip rings and brushes, or alternatively a brushless exciter can be used. Coordinated control of the two converters provides for active power and reactive power control and for efficient wide-speed-range control in high-power applications.

For high-power applications, synchronous motors are preferred because of their ability to control reactive power flow through appropriate control of excitation. Synchronous motors tend to have wider speed range and higher efficiency. However, synchronous motors are generally more expensive than induction motors.

With modern high-power PWM VSI drives, a synchronous motor can be driven for same inverter with vector control methods.

26.5.4 Special Motors

Motors under this category employ power electronics converters for normal operation. Generally, this type of motor has a large number of phases in order to limit torque pulsation and self-start from any rotor initial position. This is a new breed of motors, which can be fed through a unipolar or bipolar current. Also, they have singly salient or doubly salient magnetic structures with or without permanent magnets on the rotor.

26.5.4.1 Brushless dc Motor BDCM Drive

This type of machine has a similar construction to a standard synchronous machine, but the rotor magnetic field is produced by permanent-magnet material. A position sensor is used to ensure synchronism between the rotor position and the stator MMF via drive signals to the inverter. The use of new magnet materials characterized by high coercive-force levels has reduced magnet sizes and largely overcome the demagnetization problem. The absence of the field copper losses improves the machine efficiency.

As the permanent magnet is the source for excitation, the BDCM can be viewed as a constant-flux motor. A limited amount of flux weakening can be achieved by increasing the load angle of the stator current. Achieving a useful constant-power range is not usually practical with this type of motor. A large demagnetizing component of stator current would be required to produce a significant reduction in magnet flux, and this would increase the stator loss substantially.

The required base torque determines the motor size, and the losses are essentially independent of the number of stator turns. At speeds up to the base speed of the constant power range, the efficiency of the motor is essentially the same as for one designed for rated voltage at base speed. For operation above base speed, the stator current from the inverter is reduced in inverse proportion to the speed. This mode of operation in the high-speed range reduces the dominant stator winding losses relative to a machine in which the flux is reduced and the current kept constant. The losses in the inverter are, however, increased because of its higher current rating. For an electric road vehicle that must carry its energy store, the net energy saving may be sufficiently valuable to overcome the additional cost of the larger inverter. A further advantage of this approach is that, if the dc supply to the inverter is lost, the open circuit voltage applied to the inverter switches will be within their normal ratings.

BDCM has higher volumetric power density compared to other types of motors (induction or synchronous). It is particularly suited when high values of acceleration are required in drive (e.g., machine tools). These are often operated with high acceleration for a short time followed by a longer period of low torque. At such low values of load factor, the cooling capability is frequently not a limitation. The major interest is in obtaining the maximum acceleration from the motor. The short-term stator current of a BDCM is limited to the value required for magnet protection. These values of acceleration are significantly higher than can be achieved with either induction or dc motors of similar maximum torque rating.

26.5.4.2 Switched-Reluctance Motor SRM Drive

This motor can be regarded as a special case of a salient synchronous machine in which the field MMF is zero and the torque is produced by reluctance or saliency action only. The rotor has no winding. The SRM drive needs an inverter whose frequency is locked to the shaft speed, but since the torque is linearly proportional to the square of the stator current, the use of unidirectional current involves little sacrifice in performance.

Generally, the use of position sensors in the SRM and BDCM is something of a disadvantage in both cases. The SRM does not require permanent magnets, which can increase cost, may involve demagnetization risks, and may limit top speeds because of centrifugal forces. The SRM hence has a simpler construction and is more robust. However, the need to magnetize the motor from the ac side adds to inverter costs and may increase peak current levels significantly, hence raising stator copper losses.

Switched-reluctance synchronous motors have a cylindrical stator with three ac windings and a solid rotor (without any winding) with a moderate orthogonal axis magnetic saliency up to 4 (6) to 1. High magnetic saliency is obtained with multiple flux barriers. The conventional SRMs are to some extent (up to 100 kW) used in low-dynamics variable-speed drives with open-loop speed control, as the speed does not decrease with load. Consequently, the control is simpler than with induction motors.

The main drawback of the conventional SRD is the low motor power factor and the relatively poor torque density, which leads to a higher kVA rating of the power converter (approximately 20). The main advantage of the synchronous reluctance motor over the induction motor of similar rating is the higher efficiency. Compared to squirrel-cage induction motor, the rotor loss is small or negligible in synchronous reluctance machines. If the saliency ratio is sufficient to produce a power factor equal to that of the induction motor, the stator winding loss will be the same. Also, the stator iron losses will be similar for the two motors.

The reluctance motor is capable of operation in the constant-power mode of operation. As with all ac drives, when the supply voltage limit is reached above the base speed, the flux linkage is reduced in inverse proportion to the shaft speed, and the torque is inversely proportional to speed squared.

26.5.4.3 Linear Motors

There are applications in which linear motion, as opposed to rotational, is required. A linear machine has the same operating principles as apply to all other rotating machines. The PWM VSI converters and motor control principles discussed in this chapter are also applicable to this type of motor.

There are two types of linear motors:

- LIM (linear induction motor)
- LSM (linear synchronous motor with permanent magnetic excitation)

The LSM type has the following advantages over the LIM:

- Better power factor
- More responsive control
- Higher efficiency

The disadvantages of LSMs are as follows:

- Very accurate position feedback required
- The use of PM expensive and heavy

Transport, material handling, and extrusion processes are a few examples in which linear motors have successfully been employed.

26.5.4.4 Stepper Motors

Stepper motors are built in a similar manner to BDCMs, with permanent magnets embedded in or bonded to the rotor, or have a rotor with no magnets. The latter type is made of a ferrite magnetic material and its circumference is cut to form a number of slots, forming teeth lengthwise to the rotor axis.

Torque production can be based on (a) magnetic reluctance (as in SRM), (b) magnetic attraction (as in BDCM), or (c) both magnetic reluctance and attraction.

Stepper drives do not offer dynamic speed control, and the main action is to accelerate at full torque to full speed, maintain the speed, and decelerate at full torque. In comparison to reluctance type stepper motor, the permanent magnet type offers greater torque for a given speed, particularly at start and low speeds.

Most drives incorporate controllers with connections for a communications link for supervisory control by PLC and hard-wiring connectors for analog/digital inputs and outputs, and some are equipped with software for communications with a computer or hand held key-pad. Table 26.12 lists typical options.

Unlike the preceding motor drives, the stepper motor can achieve precise position control without the need for any external feedback.

26.5.4.5 Actuators

Actuators are widely used in industry, primarily for positioning tasks. Their designs are based on all sorts of force producing principles. Reference [9] describes several types of direct drive electric actuators, including (a) the dc actuator (moving-coil type), (b) induction actuators, (c) synchronous actuators (moving-magnet dc type), (d) reluctance actuators, and (e) inductor actuators (polarized reluctance type).

Electric actuators are used increasingly in control systems and automated electromechanical equipment. Typical specification factors include range of motion, type of motion (linear or rotary, stepwise or continuous), resolution needs, speed of response, environmental conditions, supply conditions, allowable electromagnetic noise emission level, need for integrated position and velocity sensors, maintenance needs, eligibility, cost, and peak and continuous torque.

The main demands of industry for high performance systems are as follows:

(a) A convenient supply and low power consumption
(b) Reliability and robustness
(c) Low initial cost and maintenance
(d) Fast response
(e) Linear "torque–excitation" characteristics

26.5.4.6 Integrated Motors

The integrated motor consists of a standard ac motor with an integrated frequency inverter and EMC filter. It is robust and specified for reliable operation, and often designed to handle rough working conditions, including ambient temperatures -25 to $40\,^{\circ}\mathrm{C}$ and dusty and corrosive as well as humid environments (Enclosure IP55). This type of drive uses a standard induction motor with the ac/ac converter integrated in the motor frame, often as a separate converter box mounted directly above the motor frame in place of the terminal box.

This type of motor offers the following advantages:

- Save space by eliminating the need for a separate controller
- Reduce installed costs because cabling between motor and converter is eliminated
- Eliminate motor problems caused by high voltage transient due to output cable capacitance
- Minimize EMC due to high dV/dt

TABLE 26.12 Control features for servo and stepper motor drives [8]

Control Features	Servo Drive	Stepper Drive
Acceleration/deceleration time	Adjustable	Accelerate at maximum torque, time is dependent on maximum torque and inertia
Maximum speed	Part of the motor specification	Part of the motor specification
Speed control	Permit a range of speed settings	Not necessarily available
Torque control	Many offer speed and torque control	Always operate at maximum torque
Auto tuning	A feature of some servo drives	Not applicable
Reversing	Commonly available by digital control signal	Commonly available by digital control signal
Zero speed clamp	Applies full torque to hold the position constant	Applies full torque to hold the position constant
Dynamic braking	Controlled deceleration, may require dissipative brake resistor	Usually standard
Regenerative braking	Dedicated circuit for controlled braking	Not applicable
Travel limits	Definition of travel limits in the forward and reverse directions	Standard
Jog or inch	Digital command to "jog" one step (with defined distance)	Optional feature
Closed-loop configuration	Most drives accept external signals for closed-loop control	Most drives accept external signals for closed-loop control
Programming functions	Many drives incorporate programming functions as in PLCs, reset all functions to default states, return to a home position, enable or disable repetition or a preset sequence, select a particular set of control inputs, increased or decreased speed, change the torque boost, etc.	

The integrated drive includes most features found in packaged drives, including start, stop, forward, reverse, speed and torque controls, and controlled acceleration and deceleration.

Due to complex thermal management with a high IP rating, maximum power rating of this type of drive is limited to less than 15 kW.

26.6 PWM VSI Drive

In recent years, the popularity of PWM VSI has increased beyond recognition. Its dynamic performance and controllability are better than those of the dc drive. Its power range has extended to areas dominated for years by traditional solutions such as the cyclo converter and LCI drives.

26.6.1 Drive Comparison

Table 26.13 shows a direct comparison between the cycloconverter, LCI, and PWM VSI drives. The dc drive and the slip-power recovery converter type are not listed because ac drives have already replaced dc drives in most applications as a result of the low maintenance and better reliability of ac motors. Slip recovery is only suitable for applications with a limited speed range and requires a slip-ring wound rotor.

In comparison with the cyclo converter and LCI current-source converter drives, the PWM VSI drive offers the following advantages:

- Excellent dynamic response
- Smooth torque/speed control over full speed range (0–200 Hz)
- High volumetric power density
- Ride through of dips in supply voltage
- Use of standard motors (squirrel-cage induction motor or synchronous motor)
- Improved ac supply power factor over full speed range
- Reduced cabling and transformer size and cost in comparison with cyclo converters
- No significant torque pulsation
- Lower noise level
- Low maintenance

26.6.2 Medium-Voltage PWM VSI

The maximum power rating of LV VSD is limited by the practical current ratings of power components such as motor, cable, and transformer (typically 1500 A), giving a limit of about 2 MVA at 600 V. At this rating, motor manufacturers always prefer a MV machine design significant savings and improved thermal performance of power components can be achieved by operating at medium voltages instead of low voltages. Many variable-speed drive applications will benefit from the availability of economic MV alternatives.

When adequately rated high blocking voltage devices are available, a simple two-level inverter or alternatively three-level (NPC) has always been the choice to meet required output voltages. These topologies offer a simple and cost-effective solution.

Series connection of power devices is the traditional solution for high-power, high-voltage thyristor-based drives. This approach is perceived to be complex with fast-switching IGBTs because of simultaneous switching and correct static and dynamic voltage sharing of series devices.

The "multilevel" inverter drive is seen to offer a better solution for high-power, high-voltage inverter drives. The output waveform is high quality, even at very high modulation frequencies, which inherently results in lower harmonic content in the output voltage waveform (less loss, less torque pulsation, and lower insulation voltage stresses).

Reference [10] and Fig. 26.5 categorizes MV converter topologies as follows:

(a) Series-connected two-level (SC2L)
(b) Three-level neutral-point clamped (3LNPC)
(c) Multilevel: diode-clamped multilevel (DCML), capacitor-clamped multilevel (CCML)
(d) Isolated series H-bridge (ISHB)

TABLE 26.13 Drive comparison [17]

Control Features	Cyclo	LCI	PWM VSI	Matrix
Speed	Limited	Wide	Wide	Wide
Dynamic response	Excellent	Good	Excellent	Excellent
Torque pulsation	Low	High	Very low	Very good
Power factor at low speed	Poor	Poor	Very good	Very good
Stability	Good	Moderate	Very good	Very good
Motor	Custom	Custom	Standard	Standard[a]
Regeneration	Inherent	Inherent	Needs extra hardware	Inherent
Volumetric power density	Moderate	Good	Very good	Excellent

[a] The ac output voltage of the matrix converter is always less than the input voltage — derating is expected or a larger frame size is required.

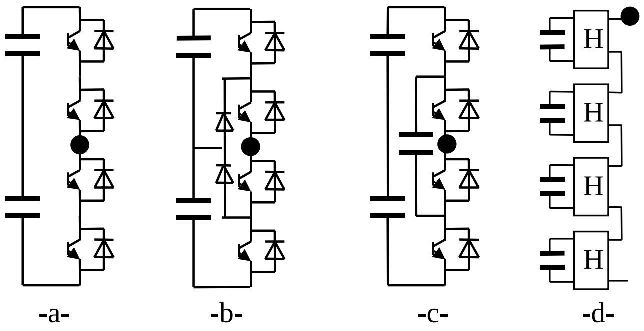


FIGURE 26.5 MV stack topologies [3].

26.6.3 Control Strategies

Several control techniques can be found in the VSD industry, (refer to Fig. 26.6) these include:

- Open-loop inverter with fixed V/Hz control
- Open-loop inverter with flux vector control
- Closed-loop inverter with flux vector control (induction motor)
- Direct torque control

Table 26.15 summarizes the main features, advantages, and disadvantages of each technique [11].

26.6.4 Communication in VSDs

The use of a high-speed advanced digital communication (Fieldbus) to build industrial automation system for realtime

TABLE 26.14 Comparison between different MV converter stack topologies

Topologies	Advantages	Disadvantages
2-level with series devices (SC2L)	Simple and proven technology Same converter design over supply voltage range Standard fully developed PWM control Provision for series redundancy of power switches per inverter phase arm $(n+1)$	Static and dynamic voltage sharing of series devices High dV/dt due to synchronous commutation of series devices High switching frequency harmonic content in inverter o/p voltage
3-level NPC (3LNPC)	Well proven Reduced harmonic content Better utilization of switches Reduced dV/dt (half the SC2L equivalent)	Series redundancy is difficult to achieve More complex PWM control is needed than 2-level Requires extra clamping diodes Requires split dc link Requires midpoint voltage balance control Even number of power devices per arm is always needed Switches require snubbers
Diode clamped multilevel (DCML)	Reduced harmonic contents Reduced dV/dt	Series redundancy is very difficult to achieve Very complex PWM control is needed Requires many steering diodes Requires split dc link Requires voltage balance control of split dc link capacitors Uneven current stresses on power devices Requires snubbers
Capacitor clamped multilevel (CCML)	This configuration has all the advantages of a multilevel converter plus: Simpler arrangement, modular building block Fewer components Snubberless operation is possible Easier capacitor voltage balance than 3LNPC	Possible parasitic resonance between decoupling capacitors Complex to provide series redundancy More complex PWM control strategy than for 2-level Voltage redistribution of capacitors during supply voltage surges Too many capacitors (bulky stack design and poor capacitor utilization at high ratings) Complex converter arrangement (for low stray inductance) Inverter rating is limited by the load current flowing through the capacitors
Series-connected isolated h- bridges (ISHB)	Modular design of the converter power modules The basic building block is based on a dc supply bridge, decoupling capacitor and a H-bridge arrangement In the ac supply the combined diode bridge rectifiers act like a multipulse bridge (18p for 4-level and 24p for 5-level), reducing harmonic injection into the ac supply Its output has very low harmonic content in spite of the low switching frequency	Employs a special (bulky and expensive) transformer Complex to achieve series redundancy Different supply transformer designs are required for applications operating at different ac line voltages Power pulsation for poor power factor loading Poor utilization of capacitors Not suitable for common dc bus applications Dynamic Braking difficult

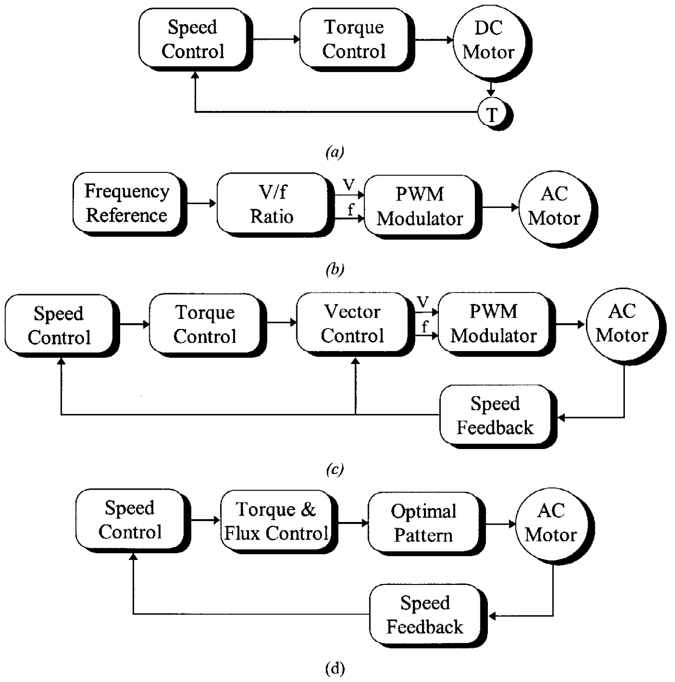


FIGURE 26.6 Electrical drive control techniques. (a) DC drive; (b) Frequency Control (PWM scalar control); (c) Flux Vector Control (Field-oriented control); (d) Direct Torque Control.

control or simply for data logging has become well established in modern industries. Digital communication resulted in replacing wiring looms with a digital serial network; this resulted in a lower cost installation and more reliable solution. Over the past few years many industrial fieldbuses emerged, and end-users, system integrators, and original equipment manufacturers (OEMs) chose the optimum system for their applications.

A fieldbus is a digital communication system that allows a control system to exchange data with remote sensors, actuators, and drives using a single communication link. The major benefits seen are reduced installation and cabling cost, and better overall immunity of the system. Both factors result in more reliable operation and reduced maintenance costs.

There exist two main types of network:

(a) *Centralized network.* Requires a network master controller, typically a PLC. The master device is entirely responsible for controlling communications over the network, while the slave devices tend to be "dumb" devices with no local intelligence.

(b) *Decentralized network.* Requires some local intelligence at each node, but no overall master device. This is ideal for realtime application environments, as all nodes are effectively running in parallel.

TABLE 26.15 Comparison between various control methods used in VSD

Drive Type	Dc	Ac	Ac	Ac
Control method	Field oriented	Frequency control	Flux vector control	Direct torque control
Features	Field orientation via mechanical commutator Controlling variables are armature current and field current Torque control is direct Typical response 10–20 ms	Voltage and frequency control Simulation of variable-speed using modulator Flux provided with a constant V/F ratio Open-loop drive Load dictate torque level Typical torque dynamic response 100 ms	Field oriented control similar to dc drive Motor electrical characteristics are modeled (observer) Closed-loop drive Torque controlled indirectly Typical torque dynamic response 10–20 ms	Use advance control theory Controlled variable are magnetizing flux and motor control Typical torque dynamic response is <5 ms
Advantages	Accurate and fast torque control High dynamic speed response Simple to control	Low cost No feedback devices are required Simple	Good torque response Accurate speed control Full torque at zero speed Performance approaching dc drive	Simple No feedback requirements No need for an observer
Disadvantages	Reduced motor reliability Regular maintenance Motor costly to purchase Needs encoder for feedback	Field orientation not used Motor status ignored Torque is not controllable Delaying modulator used	Feedback is needed Costly Modulator is needed	

Most modern VSDs are equipped with hardware and software that enable local and remote communication with plant automated system via a fieldbus system. The most popular fieldbuses are Profibus, Interbus, Worldfib, and Devicenet.

26.6.5 PWM Techniques

Different PWM techniques have been employed in PWM VSD converters. Figure 26.7 identifies the most commonly used techniques.

26.6.6 Impact of PWM Waveform

26.6.6.1 PWM Voltage Waveform

Fast switching of IGBTs (typically $<1\,\mu s$) results in high dV/dt, typically 3–5 kV/µs, and possible voltage overshoot at turn-off that can last for a few microseconds. The fast rate of rise/fall of voltage combined with high peak voltage at the turn-off results in a premature failure of motors as well as EMC. References [12–14] deal with the effect of PWM waveforms of VSD. The following is a brief summary of the effect of the unfiltered waveforms.

26.6.6.2 Effect on Motor

- Premature insulation failure due to partial discharge as a result of peak voltage, high dV/dt and high frequency
- Motor shaft voltage, which forces current into the shaft bearing, leading to early bearing failure
- Motor stray capacitance (between windings and earthed frame) leading to earth-current flow caused by high dV/dt
- High dV/dt creating nonuniform distribution of voltage across the winding, with high voltage drop across the first few turns and consequential failures
- In a large motor, voltage differential on the frame that is likely to develop in spite of protective earthing of the motor; more than one earthing point is needed

26.6.6.3 Effect on Cables

- Voltage doubling effect at the rising/falling edges of voltage waveform due to wave propagation in long cables [12]
- Earth-current flows in cable stray capacitance due to dV/dt
- Restriction on cable type used and earthing methods employed
- Cable type (armored, screen, multicore)
- Likelihood of crosstalk with other surrounding cables running in parallel
- For PWM drives, cost of cabling that is likely to be significant because of special requirements of cables, and termination methods employed

26.6.6.4 Effect on EMC/Insulation/Earthing

- Inductive and capacitive couplings between live components and earth result in common-mode and differen-

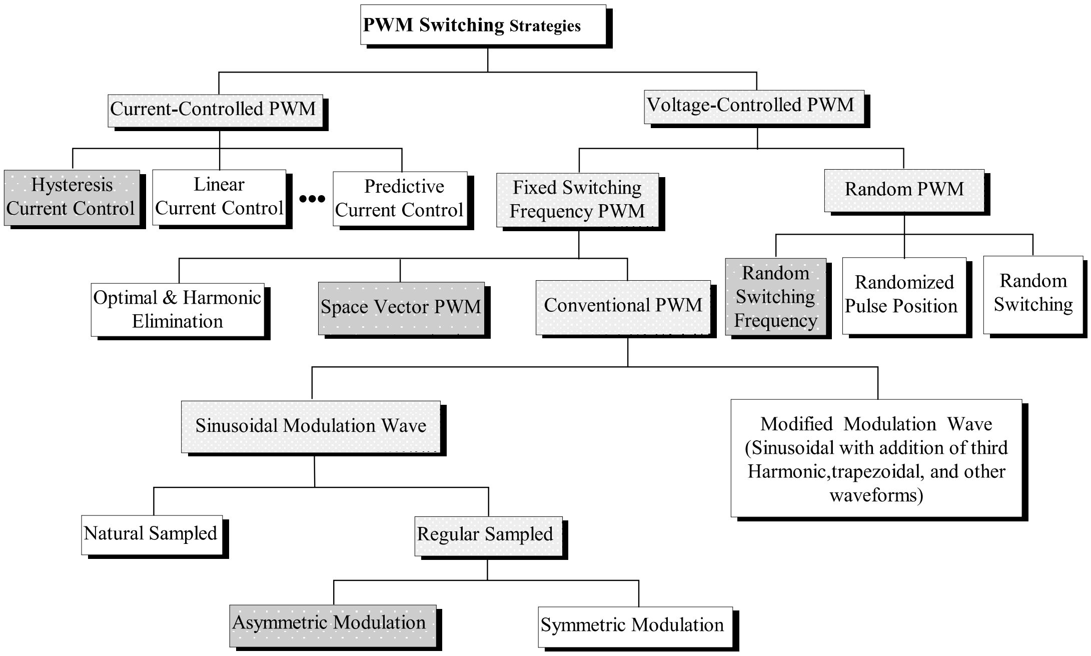

PWM Switching Strategies
Current-Controlled PWM
Voltage-Controlled PWM
Hysteresis Current Control
Linear Current Control
•••
Predictive Current Control
Fixed Switching Frequency PWM
Random PWM
Optimal & Harmonic Elimination
Space Vector PWM
Conventional PWM
Random Switching Frequency
Randomized Pulse Position
Random Switching
Sinusoidal Modulation Wave
Modified Modulation Wave (Sinusoidal with addition of third Harmonic,trapezoidal, and other waveforms)
Natural Sampled
Regular Sampled
Asymmetric Modulation
Symmetric Modulation

FIGURE 26.7 Classifications of PWM techniques.

tial-mode noise. This could lead to malfunctioning of nearby sensitive equipment.

- The voltage to earth applied on drive components pulsates at the switching frequency, adding voltage stresses (worst at low speeds, low modulation index). This poses additional insulation requirements on main power components (motor, cable, output filter, and transformer).
- A fourth wire may be required between the motor frame and the converter virtual earth so that a low-impedance path is provided for the motor earth current.
- Strict rules must be observed when cabling and earthing.

26.6.6.5 Motor Insulation

High peak voltages can be experienced at the motor terminals, especially when long cable is employed (10–100 m depending on the size of motor). This is usually caused by voltage-doubling phenomena of a transmission line with unequal line and load impedance. Motor-line voltage can reach twice the dc link voltage with long cables.

Fast voltage rise times of 5000 V/μs can be measured at the motor terminals. Under these conditions, the motor insulation becomes stressed and can lead to a premature breakdown of a standard motor insulation. When the motor fails as a result of insulation stress caused by high peak voltage and fast voltage rise times, failure occurs in the first turn as phase-to-phase short or phase-to-stator short. The highest voltage is normally seen by the first turn of the winding.

Standard motor capabilities, established by the National Electric Manufacturers Association (NEMA) and expressed in the MG-I standard (part 30), indicate that standard NEMA type B motors can withstand 1000 V peak at a minimum rise time of 2 μs (500 V/μs). Reference [13] describes the effect of PWM inverter waveforms on motor insulation in more detail.

. . . . ***Partial Discharge*** The phenomenon that starts deterioration of the motor insulation is called partial discharge (PD). When electric stresses in insulation voids exceed the breakdown voltage of the air, a partial discharge occurs. Successive PDs destroy the insulation slowly.

. . . . ***Voltage Strength Phase-to-Phase and Phase-to-Frame*** Both NEMA and IEC are proposing (a) maximum 1000 V at rise time less than 2 μs and (b) a maximum rate of rise of 500 V/μs. It is believed that low-voltage standard motors can withstand much larger voltage stresses than specified by NEMA and IEC, possibly up to 1300 V, almost regardless of the rise time.

. . . . ***Voltage Strength urn-to- urn*** In low-voltage ac motors, the conductor insulation is designed for 245 V RMS (350 V peak). The insulation strength, however, is higher depending on the impregnation method.

26.6.6.6 Bearing Current

Bearing current and shaft voltages under 50/60 Hz sine-wave operation has been recognized since 1924. The bearing impedance characteristics largely determine the resulting bearing current that will flow for a given shaft voltage [14].

The rotating machines have three basic sources of shaft voltage:

- Electromagnetic induction from the stator winding to the rotor shaft (due to small dissymmetries of the magnetic field in the air gap that is inherent in a practical machine design. The design limit is <1 VRMS.
- Electrostatic coupled from internal sources. Such a voltage in motors where rotor charge accumulation may occur (belt driven coupling, ionised air passing over rotor fan blades).
- Electrostatic coupled from external sources such as PWM inverter. The presence of high dV/dt across the stator neutral to frame ground causes a portion of the voltage to ground due to capacitor divider action. The presence of PWM related voltage component is undesirable and lead to a premature bearing failure.

The fundamental cause of the shaft voltage is magnetic dissymmetry between the stator and the rotor or possibly a phase shift of the motor voltage waveform. System ground may also contribute to this condition through unbalance system voltage. NEMA-500 recommends the consideration of insulated bearing for motor frame of certain sizes.

26.6.6.7 EMI

The main sources of electromagnetic interference (EMI) of PWM VSI drives are described in reference [15] as follows:

> *ac/dc converter*. Supply harmonics caused by supply bridge rectifier (100 Hz–2.5 kHz). As already explained, the input bridge circuit with an SCR or diode bridge is a source of supply harmonics in the input current.
>
> *dc/ac inverter*. Harmonics caused by the switching of the inverter bridge (3 kHz–20 MHz). The inverter bridge uses fast switching devices to create PWM voltage output. The inverter is a source of a wide band of frequencies, typically extending from the basic switching frequency (several kilohertz) to the radio high-frequency bands at 20 MHz. The radio-frequency current spreads out into both the supply and motor connections. An EMC filter is often used to limit spread of high-frequency harmonics into the supply.
>
> *Control electronics*. The control circuit employs a microprocessor with clock frequency of several megahertz, typically 20 MHz. The clock wave produces frequencies that are multiples of 20 MHz up to 300 MHz.

Table 26.16 summarizes main techniques used to overcome problems associated with EMI at source as well as at load.

TABLE 26.16 Overview of techniques used as a countermeasures to EMI [15]

Effect	Frequency Range (f)	Countermeasure	
		At Source	At Load
Mains	≤ 100 Hz	Avoid circulating currents	Balanced signal circuits Avoid earth loops in signal paths
Mains harmonics	$100 < f \leq 2.5$ Hz	Line and/or dc link reactor on rectifiers Higher pulse number rectifier (e.g., 12, 18, or 24) Low-impedance supply Harmonic filters	Balanced signal circuits Avoid loops in signal paths Filtering
Intermediate	$2.5\text{ k} < f \leq 150$ kHz	Filters	Filtering Screening Balanced signal circuits
Low-frequency	$150\text{ k} < f \leq 30$ MHz	Filters one per apparatus Cable screening	Filtering Screening
High frequency	$30\text{ M} < f \leq 1$ GHz	Screening Internal filtering	Screening

26.6.7 Techniques Used to Reduce the Effect of PWM Voltage Waveform

26.6.7.1 Output Line Reactor

A reactor increases the rise time but the benefit of its connection may be negated as follows:

- Beneficial connection if cable length is short enough for reflections to be superimposed within rise time, i.e., if rise time is increased beyond critical value of cable length
- Harmful connection if cable length is too long; the reactor may have negligible effect on peak voltage (theoretically its presence is insignificant in this case) or ringing period, but it will increase the duration of each overshoot, thus increasing the probability of partial discharge

Adding a series line reactor between the motor and inverter is not as simple as illustrated previously, because the reactor adds or adjusts other resonant modes where the reactor rings with lumped capacitances. These resonant modes are pure transmissions line modes and can double voltage. Some line inductance helps short-circuit protection. If earth current is limited by other means, then the coupled reactors may be helpful.

26.6.7.2 Sine-Wave Filter

This mechanism filters the PWM carrier frequency; thus, the converter output voltages are sinusoidal. This type of filter is best suited for low- performance drives and/or retrofit applications (old or standard motors). Reference [16] and Table 26.17 illustrate the filtering options for high-power VSDs.

Employing a filter at the inverter output has some practical consequences:

- Cost and weight of converter increase
- Filter power losses, voltage drop across filter inductance
- A small derating of power switches due to circulating current between filter L, C, and dc link capacitor
- Reduced torque response due to time delay in the filter, sine-wave type
- Potential oscillations that have to be electronically dampened
- Potential induction motor self-excitation

TABLE 26.17 Filtering options for PWM VSI drives [16]

Option	No Filter	dV/dt Filter	Sine-Wave Filter
Motor dV/dt	High	Acceptable	Low
Motor insulation	Must be increased	Normal	Normal
EMC ground noise	Very high	Low	Very low
PWM carrier at motor	100	100	Very low
Motor audible noise	Higher	Decreased a little	Minimum
Motor derating	Approx. 13	Approx. 3	0
Torque response	Fast	Fast	Suits most applications
Motor cost	Typically +10 cost	Normally no extra cost	No extra cost
Conclusions	Impractical	Suitable only for high dynamic torque response	Best choice for most drives

First published in Power Engineering Journal, Feb. 2000, Vol. 14, No. 1, pp. 12–20. Used with permission, ©2000, IEE.

26.6.7.3 PWM *dV/dt* Filter

This reduces the dV/dt seen by the motor to a level that does not compromise the motor or EMC. It is ideal for high-performance drives with custom-built motors.

26.6.7.4 RC Filter at Motor Terminals

A simple RC network is used at the motor terminal; the capacitor would represent a short circuit for the high-frequency components (sharp dV/dt). Wave reflection will not happen if the resistor value is similar to the cable characteristic impedance. Resistor losses are generally small, as current flow will only occur at the rising and falling edges of the PWM waveform.

26.6.7.5 Common-Mode Reactor

The presence of capacitive current due to the high dV/dt can be improved by employing a common-mode reactor. It is well established that such a choke is not effective in reducing the RMS and mean values of the leakage current, but only effective in reducing the peak value. The presence of such a choke in the circuit increases the inductance and resistance of the zero sequence impedance.

26.6.8 Supply Front End for PWM VSI Drives

There are many types of PWM voltage source drive depending on the supply front-end type and regenerative technique employed (Table 26.18):

(I) PWM VSI with a diode supply front end
(II) As above, but with a dynamic brake chopper
(III) Fully controlled thyristor front end
(IV) As above, but with a dynamic brake chopper
(V) Fully controlled antiparallel thyristor supply bridge
(VI) PWM supply front end

The use of a higher pulse number than 6-pulse would necessitate the use of a supply transformer. This is always considered to be an unnecessary "evil" because of additional cost, losses, and the need for extra space to accommodate this component. For MV applications, this is considered to be a necessity for isolation and protection.

26.6.8.1 Regenerative Braking

Several techniques are usually used for regenerative braking.

A simple diode front-end supply bridge will operate in two quadrants (positive and negative speeds). There is no regenerative power capability, as any regeneration of power would result in an increase in the dc link voltage, and the drive will trip on overvoltage.

If a small amount of regeneration is required, during stopping or speed reversal, then a dynamic brake chopper may be used. This is a simple chopper with a dynamic brake resistor. The size of the resistor is very much dependent on the regenerative brake energy, its magnitude, and its repetition rate.

TABLE 26.18 Types of supply front-end bridges of PWM VSI drives

Type	Power Device	Motor Speed Reversal	Regenerative Capability	Regenerative With ac Supply Loss	Comment
I	Diode	Yes	No	No	Good power factor across speed range Needs precharge circuit Lack of protection
II	Diode	Yes	Dissipative	Yes	Ditto
III	SCR	Yes	No	No	Power factor is function of speed Fully controlled dc link Phase back when (a) supply voltage rises, (b) fault on dc bus side Needs gate drivers for SCRs
IV	SCR	Yes	Dissipative	Yes	Ditto
V	SCR	Yes	Regenerative into supply	No	Ditto
VI	Forced commutated devices (e.g., IGBT/IGCT)	Yes	Regenerative into supply	No	Can operate with controlled power factor (unity, lagging, leading) High-frequency harmonics Dc link voltage higher than the crest of the supply voltage Fully controlled dc link, even during a supply dip Output voltage equal to input voltage Requires a precharge circuit

Full-power regeneration is possible by employing a fully controlled antiparallel thyristor front end. This is similar to that used on dc drives or cyclo converters.

A more modern approach is to use a pulse converter front-end (fully controlled bridge). This is a four-quadrant converter with the ability to control the power factor and the dc link. Such an option necessitates the use of a precharge circuit for the dc link, and smoothing inductance on the ac side.

For fully regenerative drives, the supply needs to be receptive.

By using a PWM rectifier as a primary converter in this composite structure, both the problems of regeneration and line current distortion are successfully solved with the penalty of having a much more complicated converter structure and control system.

With modern PWM VSI VSD controller, the supply bridge can be fully controlled. Such an option offers the following benefits:

- Fully regenerative drive
- Unity power factor all the time
- Sine-wave input voltage and current
- Can operate with controlled power factor (e.g., leading power factor)
- Can operate as an active filter while supplying power to the load; possible elimination of low-order supply harmonics (5th and 7th)
- Output voltage equal to the input voltage

26.7 Applications

26.7.1 VSD Applications

Table 26.19 summarizes main industries and applications. Present solutions for drives, and electric drive application examples from various industries have been described in this section.

26.7.2 Applications by Industry

26.7.2.1 Deep Mining

Reference [17] lists various high-power MV VSI inverter drive applications for the mining industry. In deep-mine conveyor-belt applications, a PWM VSI drive offers significant advantages over other conventional alternatives. The following benefits have been identified for deep-mine conveyor-belt applications:

- Improved drive starting and stopping
- Improved reliability
- Matching belt speed to production
- Easier belt inspection
- Reduced belt wear, increased belt life
- Possible to use lower specification belt material
- Low-speed running to reduce coal removed by windage
- Manpower savings less coal spillage
- Unity power factor with low harmonic content
- Reduced ac supply disturbances

TABLE 26.19 Application analysis of VSDs

Industry	Current Drive Topology	Preferences	Applications
Power generation	Direct on line (DOL) Soft start CSI	6.6 kV to 11 kV	Boiler feed pump, startup converter, coal mills
Petrochemical	LCI DOL CSI	Air-cooled, stand- alone Induction motors up to 10 MW Synchronous above 10 MW	Petrochemical and derivatives, gas liquefaction Pipelines and storage, oil on/off shore and pipelines
Mining	Cyclo-converters	Low maintenance Reliability Low power-supply distortion	Mine winders, conveyor belts, coal mills, ventilation fans, underground machinery
Stand-alone and process industries		Low cost Efficiency Ease of repair and maintenance	Water and sewage pumps, windmills, material handling (extruders), test benches, paper and plastic machines
Metals	Mill drives, cyclo-converters	Air cooled High dynamic performance Low-maintenance motor	Hot mills, medium section mills, finishing section mills, cold mills
Marine	LCI Cyclo-converters	Small size Low-maintenance, water-cooled	Warships, drilling vessels (mono-hulls), chemical tankers, shuttle tankers, cruise liners, icebreakers, semi-submersibles, fishing vessels, cable layers, floating exploration rigs, ferries, research vessels, container vessels

The PWM VSI drives can also be used to replace dc and cyclo-converter drives for mine hoist applications. The benefits are as follows:

- Improved drive control, with 100 continuous stall torque available with induction motors
- Reduced ac supply disturbances
- Very little need for reactive MVAR correction even at high ratings
- Improved immunity to ac supply dips

The use of electrically coupled mine-hoist systems has many advantages, especially for deep mines, and is set to become an essential feature of many new mine-shaft systems. The circuit is shown in Fig. 26.8.

The power flows naturally from motor 1 to motor 2 such that at the point of balance the ac supply current is virtually zero and at near unity power factor. This technology is the natural successor to the dc electrically coupled winders and totally solves the poor ac power factor that would result if twin-drive cyclo motors were used.

26.7.2.2 Industrial Processes

In the industry, there are a number of viable drive solutions available for the major-market power ranges, from LCIs to FCI. However, there is a developing market for MV variable-speed drives. The PWM VSI using new high-power IGBTs or IGCTs appears to be the best solution for the future. Benefits include better power factor, no limit on frequency, and higher voltages.

PWM VSI converter cost is likely to be higher than that of other equivalent well-established technologies (e.g., LCI). Hence, the flexibility in choice of motors and improved control must be exploited. The advantage of offering an MV solution may prove significant. Possible means of reducing motor costs are as follows:

1. Higher frequencies are achievable, allowing the use of high-speed motors and gearboxes.
2. Higher pole number machines can be used, giving cost savings.
3. Power factor is better over the speed range, giving power-supply savings.
4. Induction motors with rotors adapted for use with VSDs can be used with resultant cost savings over standard DOL, fixed-speed motors.
5. Voltages are higher and conductors smaller.

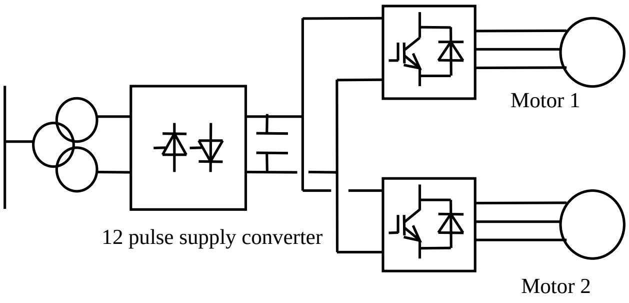


FIGURE 26.8 PWM-VSI electrically coupled mine hoist drive.

However, at low powers the relative cost of the machines is less significant versus the cost of the converters. Hence, the viability of this technology in this market requires close examination.

The cyclo-converter drive with a synchronous motor is used when four-quadrant operation is required, particularly drive requirements are high power rating with high torque at low speed and at standstill but with a rather low maximum speed. Gearless cement mill drives were the first applications of cyclo converters. The mill tube is driven from a low-speed wrap around motor with a high number of poles.

26.7.2.3 Metal Industry

The majority of installed hot-mill drives are cyclo converters. A few LCI drives have been used, but applications are limited for such technology on mill main drives. Most early-generation plants are equipped with dc drives. The trend is to replace dc with ac.

Direct current drive applications were universally used in the first generation of rolling mills. The market for new mills requiring this technology is declining as the steel industry moves to ac as a preference. On early-generation mills where motors are retained, dc drives are likely to be required. In their enquiries, some customers request ac alternatives, but others are still requesting dc drive solutions.

Dc drives are probably still the most economic for the power range 750 to 1500 kW. The number of manufacturers producing dc motors, however, is declining, particularly large dc motor manufacture. The lower price of dc solutions is offset by the advantage of use of ac motors in ac solutions, making ac the more popular choice.

Current-source inverter LCIs can be applied to roughing stands of rod and bar Mills. Technical limitations include the risk of torque pulsation and a minimum drive output frequency of 8 Hz.

The cyclo converter is the solution most often used. However, it is relatively expensive compared to alternative technology. Major cost penalties arise from supply transformers, cabling, and bridge configurations. In some cases, active power-supply compensation equipment may be required, taking the costs even higher. Cyclo-converter solutions will still be cost effective for medium- to high-power, low-speed, low-frequency (say below 21 Hz max operating frequency) applications. This would include hot reversing mills, with direct drive, for the primary rolling processes, albeit a declining application area, and possibly for direct-drive, low-speed, high-torque roller-table applications. Technical limitations include limited output frequency (typically 29 Hz for 12-pulse, at 60-Hz supplies), which can necessitate the use of two-pole motors to reach application speeds.

The high-power PWM VSI using new power devices (IGBT/IGCT) appears to be the best solution for the future. Benefits include better power factor, no limit on frequency, and higher voltages. Potentially either the two-level or the multilevel solution will meet the market requirements.

In some applications, such as coilers/uncoilers, the system is composed of several drives, which have different power cycles, when some drives are furnishing power and other are braking. A common dc bus system will allow the energy fed from drives operating in the regenerative braking mode to be utilized by other drives connected to the same dc bus, but operating in the motoring mode. The supply bridge, i.e., rectifier, feeding the dc bus system will only be rated for the total system power.

The benefits of dc bus systems include the following:

- Good operating power factor
- Low harmonics (lowest when using 12-pulse or 18-pulse front ends)
- Possibility of energy transfer on the common dc link solutions (reducing front-end converter and transformer sizes with attendant energy savings; possibility of using kinetic energy to allow controlled stopping)

26.7.2.4 Marine and Offshore

Drive powers are commonly in the range of 0.75 to 5.8 MW for thrusters, and 6 to 24 MW for propulsion. The evolution in the commercial market is toward powers from 1 to 10 MW for propulsion. Higher powers are required for naval applications with package drive efficiency better than 96%.

PWM inverters at these powers would allow the use of induction machines, rather than the more expensive synchronous alternatives required for LCI drives. This could provide savings in the price of the motor.

Current-source inverter drive LCI is used for all applications except for icebreakers, where cyclo-converter drives are used. The PWM (voltage source) inverter using new force-commutated drives appears to be the best solution for the future. Benefits include better power factor, no limit on frequency, and higher voltages. Many ice breakers and some other ships are equipped with diesel-generator-fed cyclo-converter synchronous motors with power ratings up to about 20 MW per unit.

26.7.3 Examples of Modern VSD Systems

26.7.3.1 Integrated Power System for All-Electric Ship

This is a full-scale main propulsion drive for the U.S. Navy [18]. It consists of a main-propulsion 19-MW induction-motor drive system. The power converter consists of three 6-pulse rectifier stages, three 6-kV dc links, and 15 IGBT-based H-bridges feeding a 15-phase induction motor (Fig. 26.9).

This drive demonstrates the potential of modern power electronics over more traditional solutions such as cyclo converters and LCIs. The volumetric power density of the new converter is reported to be 905 kW/m^3, compared to 455 kW/m^3 for cyclo and 313 kW/m^3 for LCI.

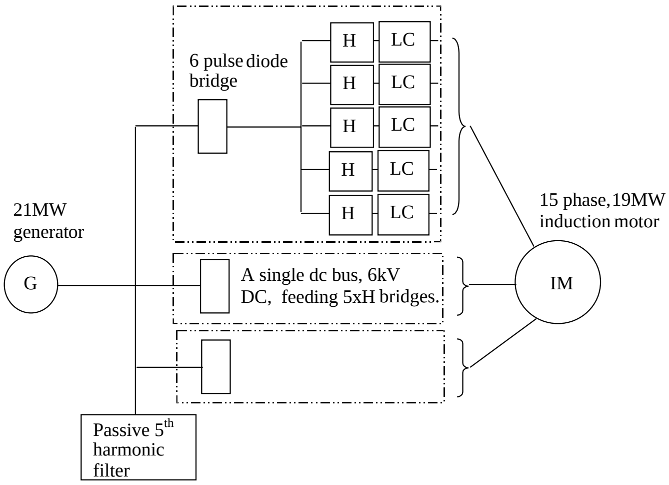

6 pulse diode bridge
H
LC
H
LC
H
LC
H
LC
H
LC
21MW generator
G
A single dc bus, 6kV DC, feeding 5xH bridges.
15 phase, 19MW induction motor
IM
Passive 5th harmonic filter

FIGURE 26.9 Schematic diagram of the IPS drives system [18].

26.7.3.2 Subsea Separation and Injection System

This is a full-scale pilot plant developed to increase recovery and improve the economics of offshore oil and gas fields. The system comprises several VSD units, typically 500-kW oil pump. 1 MW multiphase booster, and 1–2.5 MW water injection drive unit; such a system is called "SUBSIS" [19]. The main task for such a system is to separate the bulk water from the well stream and treat it either for discharge into the sea or reinjection into the reservoir.

This system employs subsea-based rotating machinery for pumping, boosting, and compression. The Subsea Electrical Power Distribution System (SEPDIS) provides innovative and cost-effective subsea processing (Fig. 26.10). The pump motors are mounted in a pressurized vessel and positioned on the seabed. Reference [19] identifies the benefits of subsea drives as follows:

- Three to six percent increase in oil and gas recovery
- Improved pipeline transportation conditions by removing water from the well stream
- Reduced environmental impact due to lower energy consumption and reduction in chemicals used to inhibit corrosion
- Reduced size and cost of new platforms
- Cost-effective development of marginal fuels through reuse of existing infrastructure

26.7.3.3 Shaft Generator for Marine Application

During cruising at sea, up to 3.5 MW of electric power is extracted from the ship's main diesel engine/propeller shaft (90,000 hp per ship) via a salient pole shaft generator, which is fitted to the main propeller shaft. The converter output voltage (set at 60 Hz) is stepped up to 6.6 kV [20].

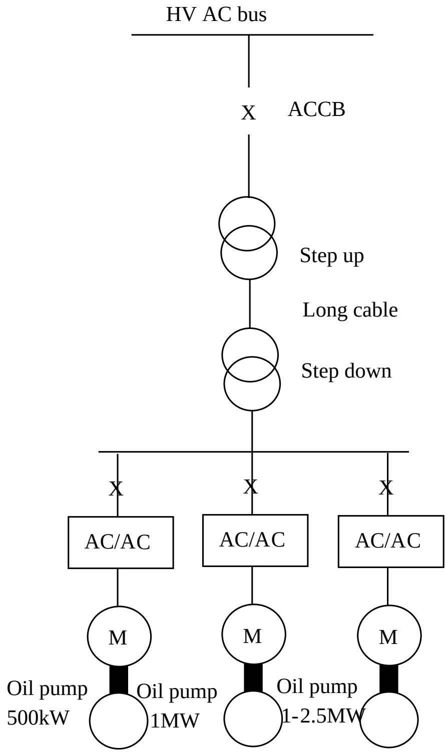


FIGURE 26.10 Schematic diagram of SEPDIS [19].

The converter is based on 24-pulse-converter (LCI) technology, which is traditionally used as main ship propulsion. The shaft generator output frequency varies between 14 and 25.7 Hz, 6-phase generator and the output stage is configured as 24-pulse, via a step-up transformer. At the output a passive LC filter is employed, with a synchronous condenser, started by a pony motor.

This type of application is likely to significantly benefit from the higher volumetric power density of the PWM VSI with fully controlled front end. Such a system will eliminate the need for a passive filter at the output stage, and will use a standard three-phase generator.

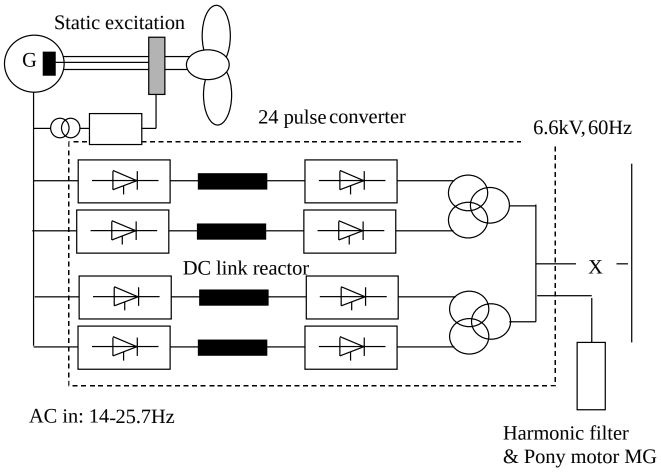


FIGURE 26.11 Schematic diagram of shaft generator [20].

The same technology is also applicable to high-speed generators and windmill energy. The ability of the active front end to sustain fixed dc link voltage over a relatively wide shaft speed range results in a very good control of the output voltage, irrespective of the shaft speed.

In wind power plants, the optimal efficiency of the wind turbine depends on the speed when the wind conditions change. It is, therefore, advantageous to vary the speed of the generator and link it via a frequency converter to the ac system.

For high-speed generators, driven by diesel engines or gas turbines, the fully controlled converters enable direct power conversion from ac high-frequency (hundreds of hertz) to fixed power frequency (50/60) Hz fixed output voltage. The magnitude of the output voltage is kept constant irrespective of speed variation on the generator speed.

26.7.3.4 Linear Motor Drive for Roller Coaster

This drive involves a fully regenerative PWM VSI. The supply front end is made of antiparallel thyristors; the machine bridge is based on PWM IGBT VSI. "The Escape" has been developed for Six Flags California at Magic Mountain. The inverter output frequency is 0–230 Hz, and 525 V ac RMS. The power rating is 1.8 MW. The duty cycle is 1.8 MW for 7 seconds, followed by 16 seconds at zero power, and 1.3 MW for 5 seconds and a stop period of 32 seconds. This ride involves acceleration at 4.5 g, speed, and free fall (6.5 seconds of weightlessness, during which a height of 415 ft is achieved [21]).

The same concept employed in this application could be used for airplane launchers on aircraft carriers, instead of the conventional catapult.

26.8 Summary

The benefits of VSD are there to be quantified, and energy savings have been the prime reason for employing a VSD in stand-alone drive applications. Other benefits such as improve process control or increase life expectancy are often difficult to quantify in real terms.

There is a large selection of VSD systems to meet a wide range of applications. At low and medium power, the induction motor and PWM VSI are supreme. At higher power ratings, MV PWM VSIs are gaining popularity, but LCI and cyclo-converter drives would remain key technologies with very high-power applications.

Modern drives are becoming more available at competitive prices with good reliability records. However, there are concerns with regard to the impact of fast switching on the motor and the environment.

To ensure successful implementation of VSD system, both the supplier and end users need to work in partnership. Ideally, one competent supplier should supply the full drive package, with some after-sale service support. Understanding the nature of the load plays an important role in specifying the power rating of VSDs correctly to meet performance requirements and required life expectancy.

New areas of VSD applications are emerging as power electronics advances and become more reliable at affordable prices. Packaged drive up to several hundred kilowatts are becoming a commodity product, and end users do not need to involve a third party during specification, installation, and commissioning. Integrated motors are likely to increase in popularity, possibly with new types of power converters, e.g., matrix.

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Table of abbreviations

BDCM	brushless dc motor
CCML	capacitor clamped multi-level
CSI	current source inverter
DCML	diode clamped multi-level
DOL	direct on line
EMC	electromagnetic compatibility
EMF	electro-motice force
EMI	electromagnetic interference
FCI	forced commutated inverter
GTO	gate turn-off thyristor
IGBT	insulated gate bipolar-transistor
IGCT	integrated gate commutated thyristor
ISHB	isolated series H-bridge
LCI	load commutated inverter
LIM	linear induction inverter
LSM	linear synchronous motor
LV	low voltage
MMF	magneto-motive force
MV	medium voltage
NPC	neutral point clamp
OEM	original Equipment Manufacturer
PLC	programmable logic control
PM	permanent magnet
PWM	pulse width modulation
SC2L	series connected 2 level
SRM	switched reluctance motor
3LNPC	3 level neutral point clamp
VSD	variable speed drive
VSI	voltage source inverter

27

Motor Drives

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27.1 Introduction

The widespread proliferation of power electronics and ancillary control circuits into motor control systems in the past two or three decades have led to a situation where motor drives, which process about two-thirds of the world's electrical power into mechanical power, are on the threshold of processing all of this power via power electronics. The days of driving motors directly from the fixed ac or dc mains via mechanical adjustments are almost over.

The marriage of power electronics with motors has meant that processes can now be driven much more efficiently with a much greater degree of flexibility than previously possible. Of course certain processes are more amenable to certain types of motors, because of the more favorable match between their characteristics. Historically, this situation was brought about by the demands of the industry. Increasingly, however, power electronic devices and control hardware are becoming able to easily tailor the rigid characteristics of the motor (when driven from a fixed dc or ac supply source) to the requirements of the load. Development of novel forms of machines and control techniques therefore has not abated, as recent trends would indicate.

It should be expected that just as power electronics equipment has tremendous variety, depending on the power level of the application, motors also come in many different types, depending on the requirements of application and power level. Often the choice of a motor and its power-electronic drive circuit for application are forced by these realities, and the application engineer therefore needs to have a good understanding of the application, the available motor types, and the suitable power-electronic converter and its control techniques. Table 27.1 gives a rough guide of combinations of suitable motors and power electronic converters for a few typical applications.

For many years, the brushed dc motor has been the natural choice for applications requiring high dynamic performance. Drives of up to several hundred kilowatts have used this motor. In contrast, the induction motor was considered for low-performance, adjustable-speed applications at low and medium power levels. At very high power levels, the slip-ring induction motor the synchronous motor drive were the natural choice. These boundaries are increasingly becoming blurred, especially at the lower power levels.

Another factor for motor drives was the consideration for servo performance. The ever-increasing demand for greater productivity or throughput and higher quality of most of the industrial products that we use in our everyday lives means that all aspects of dynamic response and accuracy of motor drives have to be increased. Issues of energy efficiency and harmonic proliferation into the supply grid are also increasingly affecting the choices for motor-drive circuitry.

A typical motor drive system is expected to have some of the system blocks indicated in Fig. 27.1. The load may be a conveyor system, a traction system, the rolls of a mill drive, the cutting tool of a numerically controlled machine tool, the compressor of an air conditioner, a ship propulsion system, a control valve for a boiler, a robotic arm, and so on. The power electronic converter block may use diodes, MOSFETS, GTOs, IGBTs, or thyristors. The controllers may consist of several control loops, for regulating voltage, current, torque, flux, speed, position, tension, or other desirable conditions of the load. Each of these may have their limiting features purposely placed in order to protect the motor, the converter, or the load. The input commands and the limiting values to these

TABLE 27.1 Typical motor, converter, and application guides

Motor	Type of Converter	Type of Control	Applications
Brushed dc motor	Thyristor ac–dc converter	Phase control, with inner current loop	Process rolling mills, winders, locomotives, large cranes, extruders, elevators
	GTO/IGBT/MOSFET chopper	PWM control with inner current loop	Drives for transportation, machine tools, office equipment
Induction motor (cage)	Back–back thyristor	Phase control	Pumps, compressors
	IGBT/GTO inverter/cycloconverter	PWM V–f control	General-purpose industrial drive such as for cranes, pumps, fans, elevators, material transport and handling, extruders, subway trains
	IGBT/GTO	Vector control	High-performance ac drives in transportation, motion control, and automation
Induction motor (slip-ring)	Thyristor ac–dc converter	Phase control with dc-link current loop	Large pumps, fans, cement kilns
Synchronous motor (excited)	Thyristor ac–dc	Dc-link current loop	Large pumps, fans, blowers, compressors, rolling mills
Synchronous motor (PM)	IGBT/MOSFET inverter	PWM current control	High-performance ac servo drives for office equipment, machine tools, and motion control

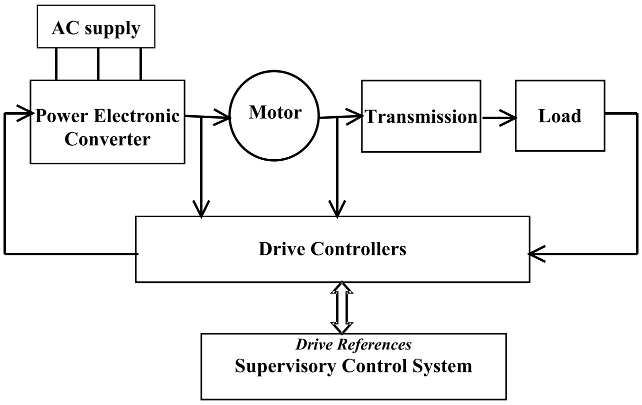


FIGURE 27.1 Block diagram of a typical drive system.

controllers would normally come from supervisory control systems that produce the required references for a drive. This supervisory control system is normally more concerned with the overall operation of the process rather than the drive.

Consequently, a vast array of choices and technologies exist for a motor-drive application. Against this background, this chapter gives a brief description of the dominant forms of motor drives in current usage. The interested reader is expected to consult the further reading material listed at the end of each section for more detailed coverage.

27.2 DC Motor Drives

M. . ah an

27.2.1 Introduction

Direct-current motors are extensively used in variable-speed drives and position-control systems where good dynamic response and steady-state performance are required. Examples are in robotic drives, printers, machine tools, process rolling mills, paper and textile industries, and many others. Control of a dc motor, especially of the separately excited type, is very straightforward, mainly because of the incorporation of the commutator within the motor. The commutator brush allows the motor-developed torque to be proportional to the armature current if the field current is held constant. Classical control theories are then easily applied to the design of the torque and other control loops of a drive system.

The mechanical commutator limits the maximum applicable voltage to about 1500 V and the maximum power capacity to a few hundred kilowatts. Series or parallel combinations of more than one motor are used when dc motors are applied in applications that handle larger loads. The maximum armature current and its rate of change are also limited by the commutator.

27.2.2 Dc Motor Representation and Characteristics

The dc motor has two separate sources of fluxes that interact to develop torque. These are the field and the armature circuits. Because of the commutator action, the developed torque is given by

$$T \approx K i_f i_a \tag{27.1}$$

where i_f and i_a are the field and the armature currents, respectively, and K is a constant relating motor dimensions and parameters of the magnetic circuits.

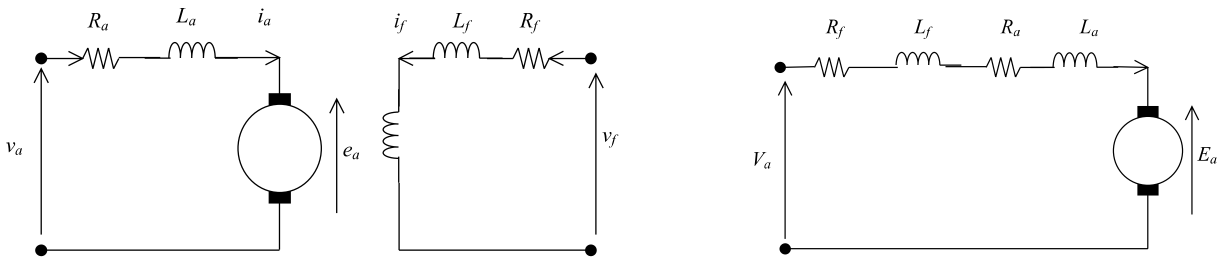
The dynamic and the steady-state responses of the motor and load are given by

$$\begin{array}{llr} \text{Dynamic} & \text{Steady-state} & \\ v_a = R_a i_a + L_a \dfrac{di_a}{dt} + e & V_a = R_a I_a + E & (27.2) \\ v_f = R_f i_f + L_f \dfrac{di_f}{dt} & V_f = R_f I_f & (27.3) \\ e = K i_f \omega & E = K I_f \omega & (27.4) \\ T = J \dfrac{d\omega}{dt} + D\omega + T_L & T = J\omega + T_L & (27.5) \end{array}$$

where J, D, and T_L are the moment of inertia, damping factor, and load torque, respectively, referred to the motor, and the subscripts a and f refer to the armature and field circuits, respectively.

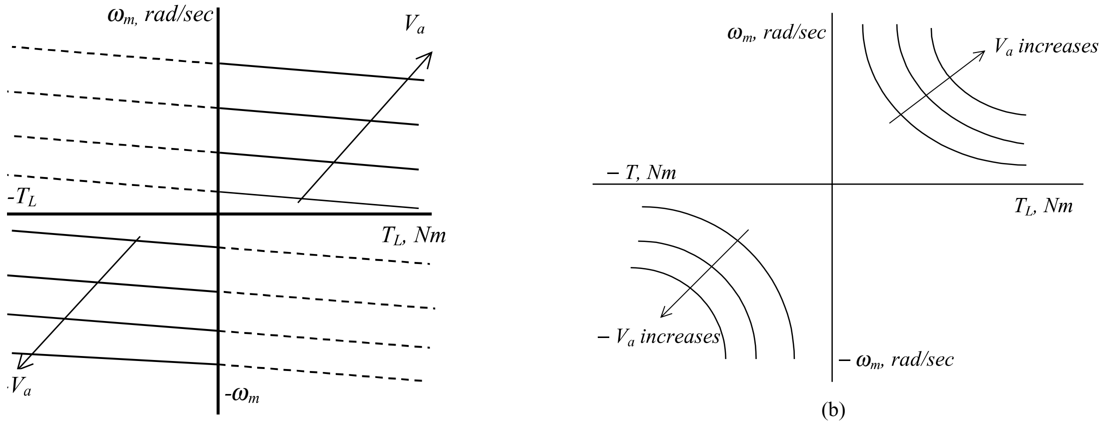
Small servo-type dc motors normally have permanent magnet excitation for the field, whereas larger size motors tend to have separate field-supply V_f for excitation. The separately excited dc motors represented in Fig. 27.2a have fixed field excitation, and these motors are very easy to control via the armature current that is supplied from a power electronic converter. Thyristor ac–dc converters with phase angle control are popular for the larger motors, whereas duty-cycle controlled pulse-width modulated switching dc–dc converters are popular for servo motor drives. The series-excited dc motor has its field circuit in series with the armature circuit as shown in Fig. 27.2b. Such a connection gives high torque at low speed and low torque at high speed, a pseudo-constant-power-like characteristic that may match traction-type loads well.

Torque–speed characteristics of the separately and series excited dc motors are indicated in Figs. 27.3a and 27.3b, respectively. The speed of the separately excited dc motor drops with load, the net drop being about 5 to 10 of the base speed at full load. The voltage drop across the armature resistance and the armature reaction are responsible for this. Operation of the motor above the base speed at which the armature voltage reaches for the rated field excitation is by means of field weakening, whereby the field current is reduced



(a) (b)

FIGURE 27.2 (a) Separately excited dc motor circuit. (b) Series excited dc motor circuit.



(a) (b)

FIGURE 27.3 Torque-speed characteristics of (a) separately and (b) series-excited motors.

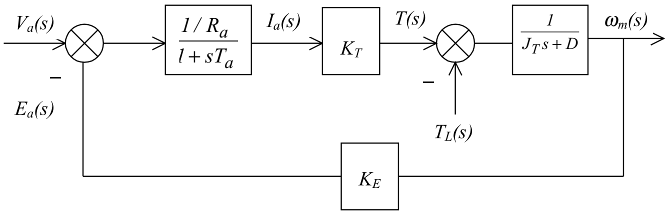


FIGURE 27.4 Transfer characteristic block diagram of a separately excited motor.

in order to increase speed beyond the base speed. The armature voltage is now maintained at the rated value actively, by overriding the field control if required. Note that the range of field control is limited because of the magnetic nonlinearity of the field circuit and the problem of good commutation at weak field. Usually the top speed is limited to about three times the base speed. Note also that field weakening results in reduced torque production per ampere of armature current. Depending on the type of load, the armature current and speed change dictated by Eqs. (27.1)–(27.5).

For the separately excited dc motor, assuming that the field excitation is held constant, the transfer characteristic between the shaft speed and the applied voltage to the armature can be expressed as indicated in the block diagram of Fig. 27.4. If we ignore the load torque T_L, the transfer characteristic is given by

$$\frac{\omega_m}{V_a} = \frac{K_T}{(sL_a + R_a)(Js + D) + K_E K_T} \tag{27.6}$$

the characteristic roots of which are given by

$$\left(s + \frac{1}{T_a}\right)\left(s + \frac{D}{J}\right) + \frac{1}{T_a T_m} = 0 \tag{27.7}$$

If we compare this with a standard second-order system, the undamped natural frequency and damping factor are given by

$$\omega_n = \sqrt{\frac{1}{T_a}\left(\frac{1}{T_m} + \frac{D}{J}\right)} \tag{27.8}$$

and

$$\sigma = \xi\omega_n = \frac{1}{2}\left[\frac{1}{T_a} + \frac{D}{J}\right] \tag{27.9}$$

where

$$T_m = \text{mechanical time constant} = \frac{R_a J}{K_E K_T}$$

in which $K_E = Ki_f = K_T$ in SI units and

$$T_a = \text{electrical time constant} = \frac{L_a}{R_a}.$$

The speed response of the motor around an operating speed to the application of load torque on the shaft is given by

$$\frac{\Delta\omega_m}{\Delta T_L} = \frac{1 + sT_a}{(1 + sT_a)(Js + D) + \dfrac{K_E K_T}{R_a}} \tag{27.10}$$

27.2.3 Converters for dc Drives

Depending on application requirements, the power converter for a dc motor may be chosen from a number of topologies. For example, a half-controlled thyristor converter or a single-quadrant PWM switching converter may be adequate for a drive that does not require controlled deceleration with regenerative braking. On the other hand, a full four-quadrant thyristor or transistor converter for the armature circuit and a two-quadrant converter for the field circuit may be required for a high-performance drive with a wide speed range.

The frequency at which the power converter is switched, e.g., 100 Hz for a single-phase thyristor bridge converter supplied from a 50-Hz ac source (or 300 Hz for a three-phase thyristor bridge converter), 20 kHz for a PWM MOSFET H-bridge converter, and so on, has a profound effect on the dynamics achievable with a motor drive. Low-power switching devices tend to have faster switching capability than high-power devices. This is convenient for low-power motors since these are normally required to be operated with high dynamic response and accuracy.

27.2.3.1 Thyristor Converter Drive

Consider the dc drive of Fig. 27.5, for which the armature supply voltage v_a to the motor is given by

$$v_a = \frac{2V_{\max}}{\pi}\cos\alpha \tag{27.11}$$

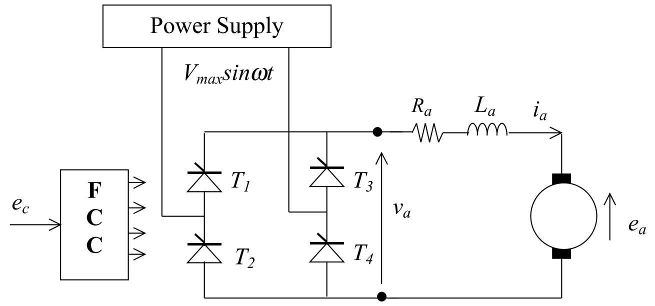


FIGURE 27.5 A two-quadrant single-phase thyristor bridge converter drive.

where $V_{\max}$ is the peak value of the line–line ac supply voltage to the converter and α is the firing angle. The dc output voltage v_a is controllable via the firing angle α, which in turn is controlled by the control voltage e_c as input to the firing control circuit (FCC). The FCC is synchronized with the mains ac supply and drives individual thyristors in the ac–dc converter according to the desired firing angle. Depending on the load and the speed of operation, the conduction of the current may become discontinuous as indicated in Fig. 27.6a. When this happens, the converter output voltage does not change with control voltage as proportionately as with continuous conduction. The motor speed now drops much more with load as indicated by Fig. 27.6b. The consequent loss of gain of the converter may have to be avoided or compensated if good control over speed is desired.

The output voltage of the simple, two-pulse ac–dc converter of Fig. 27.5 is rich in ripples of frequency nf, where n is an even integer starting with 2 and f is the frequency of the ac supply. Such low-frequency ripple may derate the motor considerably. Converters with higher pulse number, such as the 6- or 12-pulse converter, deliver much smoother output voltage and may be desirable for more demanding applications.

A high-performance dc drive for a rolling mill drive may consist of such converter circuits connected for bi-directional operation of the drive, as indicated in Fig. 27.7. The interfacing of the firing control circuit to other motion-control loops, such as speed and position controllers, for the desired motion is also indicated.

Two fully-controlled bridge ac–dc converter circuits are used back-to-back from the same ac supply. One is for forward and the other is for reverse driving of the motor. Since each is a two-quadrant converter, either may be used for regenerative braking of the motor. For this mode of operation, the braking converter, which operates in inversion mode, sinks the motor current aided by the back emf of the motor. The energy of the overhauling motor now returns to the ac source. It may be noted that the braking converter may be used to maintain the braking current at the maximum allowable level right down to zero speed. A complete acceleration–deceleration cycle of such a drive is indicated in Fig. 27.8. During braking, the firing angle is maintained at an appropriate value at all times so that controlled and predictable deceleration takes place at all times.

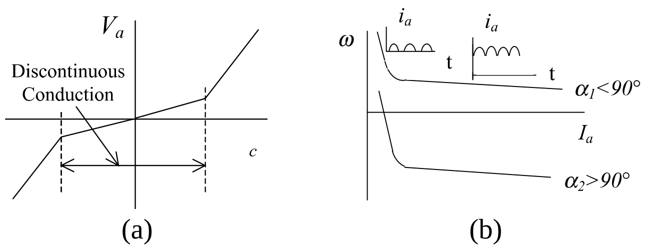


FIGURE 27.6 (a) Converter output voltage and (b) motor torque–speed characteristics with discontinuous conduction.

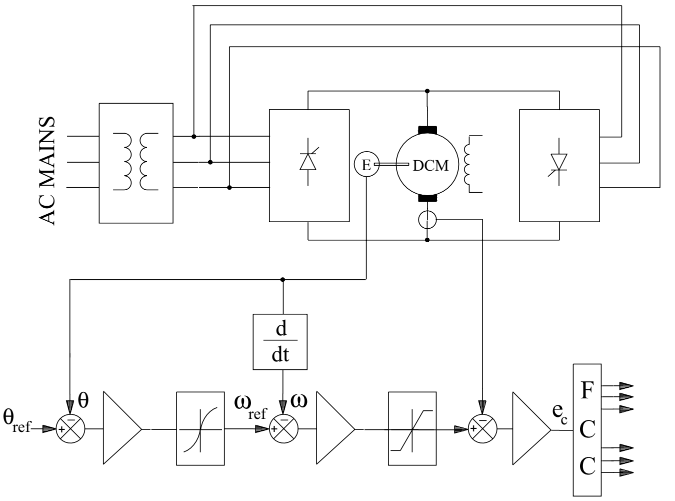


FIGURE 27.7 Bidirectional speed and position control system with a back-to-back (dual) thyristor converter.

The innermost control loop indicated in Fig. 27.7 is for torque, which translates to an armature current loop for a dc drive. Speed- and position-control loops are usually designed as hierarchical control loops. Operation of each loop is sufficiently decoupled from the other so that each stage can be designed in isolation and operated with its special limiting features.

27.2.3.2 PWM Switching Converter Drive

PWM switching converters have traditionally been referred to as choppers in many traction- and forklift-type drives. These are essentially PWM dc–dc converters operating from rectified dc or battery mains. These converters can also operate in one, two, or four quadrants, offering a few choices to meet application requirements. Servo drive systems normally use the full four-quadrant converter of Fig. 27.9, which allows bidirectional drive and regenerative braking capabilities.

For forward driving, the transistors T_1 and T_4 and diode D_2 are used as a buck converter that supplies a variable voltage, v_a, to the armature given by

$$v_a = \delta V_{DC} \tag{27.12}$$

where V_{DC} is the dc supply voltage to the converter and δ is the duty cycle of the transistor T_1.

The duty cycle δ is defined as the duration of the on time of the modulating (switching transistor) as a fraction of the switching period. The switching frequency is normally dictated by the application and the type of switching devices selected for the application.

During regenerative braking in the forward direction, transistors T_2 and diode D_4 are used as a boost converter that regulates the braking current through the motor by automatically adjusting the duty cycle of T_2. The energy of the overhauling motor now returns to the dc supply through diode D_1, aided by the motor back emf and the dc supply. Again, note that the braking converter, comprising T_2 and D_1, may be used to maintain the regenerative braking current at the maximum allowable level right down to zero speed.

Figure 27.10 shows a typical acceleration–deceleration cycle of such a drive under the action of the control loops indicated in Fig. 27.9.

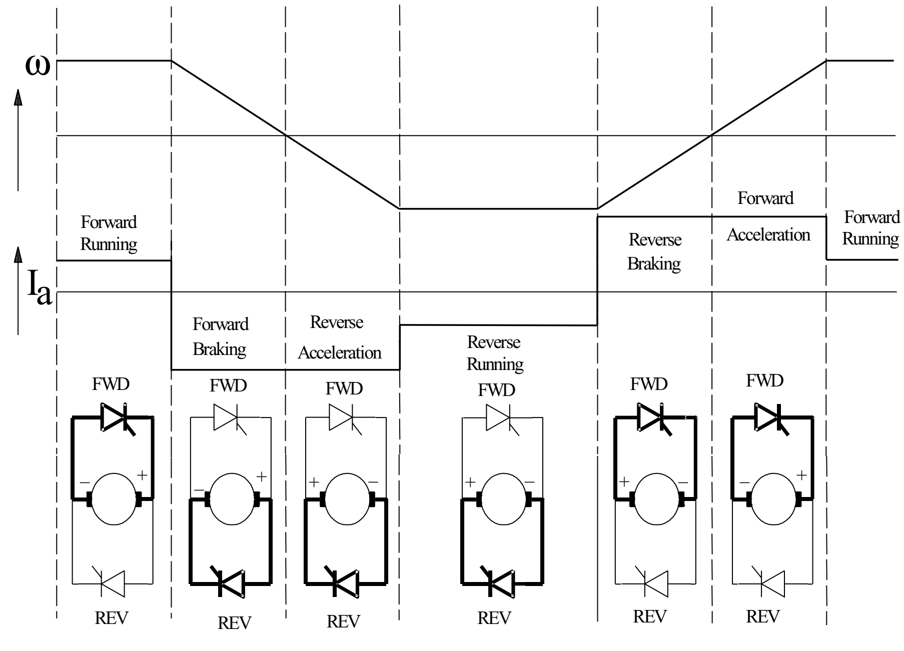


FIGURE 27.8 Converter conduction and operating duty of a bidirectional drive.

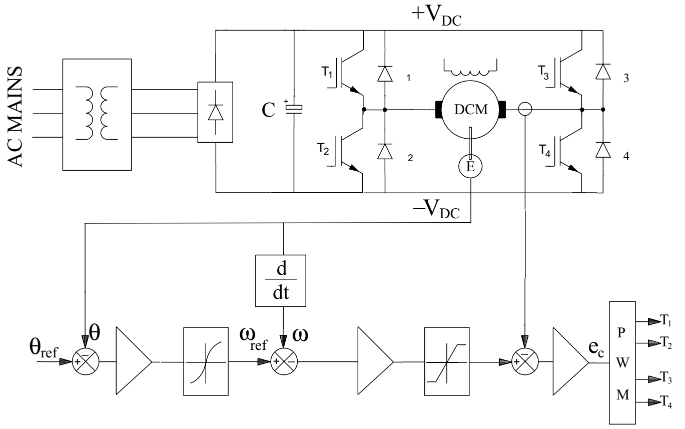

$+V_{DC}$
AC MAINS
C
T_1
1
T_2
2
T_3
3
T_4
4
DCM
E
$-V_{DC}$
d/dt
θ_{ref}
θ
ω_{ref}
ω
e_c
PWM
T_1
T_2
T_3
T_4

FIGURE 27.9 Bidirectional speed and position control system with a PWM transistor bridge drive.

Four-quadrant PWM converter drives such as that in Fig. 27.10 are widely used for motion-control equipment in the automation industry. Because of significant development of power switching devices, switching frequencies of 10–20 kHz are easily attainable. At such frequencies, virtually no derating of the motor is necessary.

In order to satisfy the requirements of a drive application, simpler versions of the drive circuits indicated in Figs. 27.7 and 27.9 may be used. For instance, for a unidirectional drive half of the converter circuits indicated earlier may be used. Further simplification of the drive circuit is possible if regenerative braking is not required.

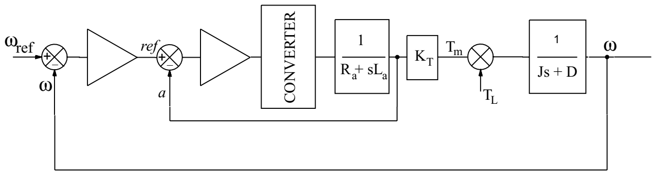

ω_{ref}
ω
ref
a
CONVERTER
$\frac{1}{R_a + sL_a}$
K_T
T_m
T_L
$\frac{1}{Js + D}$
ω

FIGURE 27.11 Structure of a closed-loop speed-control system with a dc drive.

27.2.4 Drive System Integration

A complete drive system has a torque controller (armature current controller for a dc drive) as its innermost loop, followed by a speed controller as indicated in Fig. 27.11.

The inner current loop is often regulated with a proportional plus integral (PI) type controller of high gain. The rest of the inner loop consists of the converter, the motor armature, which is essentially an *R–L* circuit with armature back emf as disturbance, and the current sensor. The current sensor is typically an isolated circuit, such as a Hall sensor or a direct-current transformer (DCCT). A well-designed torque (armature current) loop behaves essentially as a first-order lag system. Together with the mechanical inertia load, this loop can be indicated as the middle Bode plot of Fig. 27.12, in which $1/T_i$ represents the current-controlled system bandwidth. (Note that the damping factor D and the load torque T_L indicated in Fig. 27.11 have been neglected in this description for simplicity.) The current loop is normally designed by analyzing the block diagram of Fig. 27.11, the converter, and

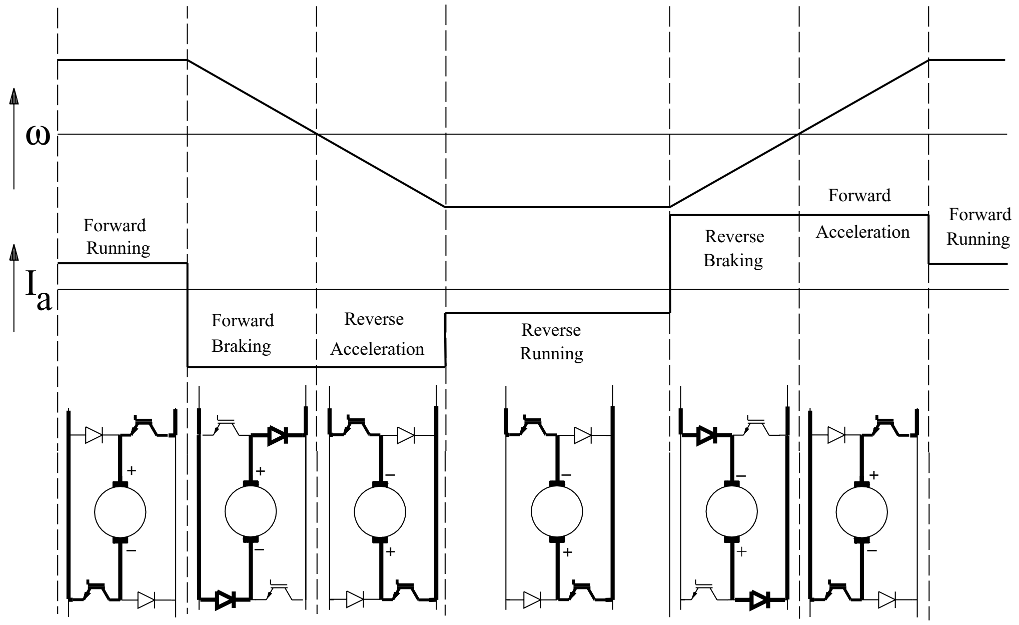

ω
I_a
Forward Running
Forward Braking
Reverse Acceleration
Reverse Running
Reverse Braking
Forward Acceleration
Forward Running

FIGURE 27.10 Converter conduction and operating duty with a PWM bridge transistor drive.

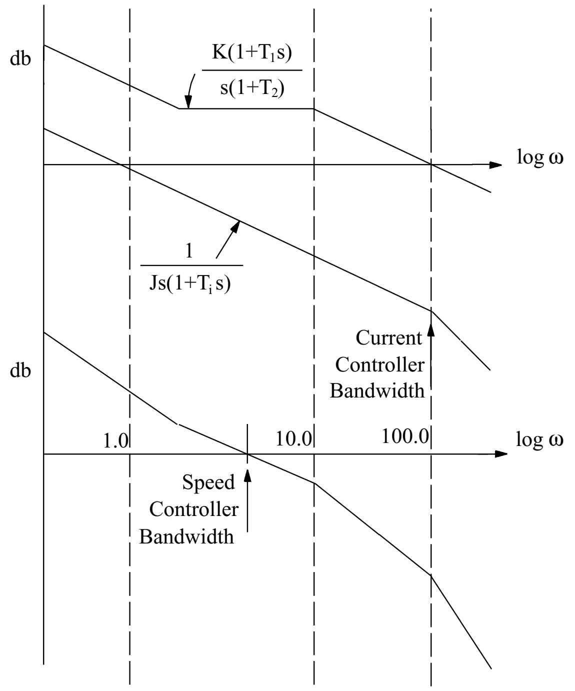


FIGURE 27.12 Typical current and speed control loop designs for the system of Fig. 27.11.

the PI controller for the current loop using Bode analysis or other control-system design tools.

The next step is usually the design of the speed controller. The 0-db intercept of $1/Js(1 + T_i s)$ is normally much too low. Again, if a PI controller is selected for the speed loop, its Bode plot is superimposed on the current controlled system as indicated in Fig. 27.12 to obtain the desired speed-control bandwidth.

27.2.5 Converter DC Drive System Considerations

Several operational factors need to be considered in applying a dc drive. Some of the important ones are as follows:

1. The armature current may be rich in harmonics. This is particularly true for thyristor converters. The feedback of these current ripples into the firing-control circuit may cause overloading of individual switches and tripping. Adequate filtering is necessary to avoid such problems.
2. Since the converter is switched at regular intervals while the current controller operates continuously, current overshoot may occur because of the delay in the firing-control circuit. The current controller gains must be limited to limit this overshoot.
3. The switching frequency of the converter should be selected according to the desired motor-current ripple, supply-input current harmonics, and dynamic performance of the drive.
4. Ripple in the speed sensor output limits the performance of the speed controller. Analog tachogenerator output is particularly noisy and defines the upper limit of the speed control bandwidth. Digital speed sensors, such as encoders and resolvers, alleviate this limit significantly.

27.2.6 Further Reading

1. G. K. Dubey, *Power Semiconductor Controlled Drives.* Prentice Hall, 1989.
2. W. Leonard, *Control of Electric Drives.* Springer-Verlag, 1985.
3. V. Subrahmanyam, *Electric Drives; Concepts and Applications.* McGraw-Hill, 1994.
4. M. A. El-Sharkawi, *Fundamentals of Electric Drives.* Thompson Learning, 2000.

27.3 Induction Motor Drives

M. . ah an

27.3.1 Introduction

The ac induction motor is by far the most widely used motor in the industry. Traditionally, it has been used in constant and variable-speed drive applications that do not cater for fast dynamic processes. Because of the recent development of several new control technologies, such as vector and direct torque controls, this situation is changing rapidly. The underlying reason for this is the fact that the cage induction motor is much cheaper and more rugged than its competitor, the dc motor, in such applications. This section starts with induction motor drives that are based on the steady-state equivalent circuit of the motor, followed by vector-controlled drives that are based on its dynamic model.

27.3.2 Steady-State Representation

The traditional methods of variable-speed drives are based on the equivalent circuit representation of the motor shown in Fig. 27.13.

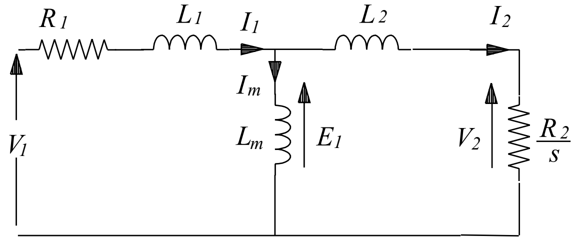


FIGURE 27.13 Steady-state equivalent circuit of an induction motor.

From this representation, the following power relationships in terms of motor parameters and the rotor slip can be found

$$\text{Power in the rotor circuit, } P_2 = 3I_2^2\frac{R_2}{s} = 3V_2I_2$$

$$= \frac{3sR_2E_1^2}{R_2^2 + (s\omega_1L_2)^2} \tag{27.13}$$

$$\text{Output power, } P_0 = P_2 - 3I_2^2R_2$$

$$= (1-s)P_2 = \omega_0 T$$

$$= \frac{(1-s)\omega_1}{P}T \tag{27.14}$$

where

$$\text{slip, } s = \frac{\omega_1 - \omega_r}{\omega_1} = \frac{\omega_1 - p\omega_0}{\omega_1}, \tag{27.15}$$

$P =$ number of pole pairs

$\omega_0 = \dfrac{2\pi N}{60}$ rad/s; N is the rotor speed in rev/min

$\omega_r =$ rotor speed in electrical rad/s

and

$\omega_1 = 2\pi f_1$ rad/s (electrical), f_1 being the supply frequency

The developed torque

$$T = \frac{P_2}{\grave{u}_1/P}\ \text{Nm} \tag{27.16}$$

The slip frequency, sf_1, is the frequency of the rotor current, and the airgap voltage E_1 is given by

$$E_1 = \grave{u}_1 L_m I_m = \grave{u}_1 \ddot{e}_m \tag{27.17}$$

where λ_m is the stator flux linkage due to the airgap flux. If the stator impedance is negligible compared to E_1, which is true when f_1 is near the rated frequency f_0,

$$V_1 \approx E_1 = 2\pi f_1 \lambda_m \tag{27.18}$$

and

$$T = \frac{3P}{\omega_1}\frac{sR_2V_1^2}{R_2^2 + (s\omega_1L_2)^2} = \frac{3P}{\omega_1}\frac{sR_2(2\pi f_1)^2\lambda_m^2}{R_2^2 + (s\omega_1L_2)^2} \tag{27.19}$$

27.3.3 Characteristics and Methods of Control

The preceding analysis suggests several speed control methods. The following are some of the widely used methods:

1. Stator voltage control
2. Slip power control
3. Variable-voltage, variable-frequency (V–f) control
4. Variable-current, variable-frequency (I–f) control

These methods are sometimes called *scalar controls* to distinguish them from *vector controls*, which are described in Section 27.3.4. The torque–speed characteristics of the motor differ significantly under different types of control, as will be evident in the following sections.

27.3.3.1 Stator Voltage Control

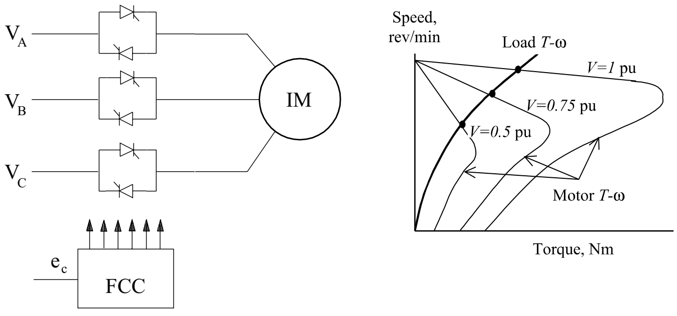
In this method of control, back-to-back thyristors are used to supply the motor with variable ac voltage, as indicated in the converter circuit diagram of Fig. 27.14a.

The analysis of Section 27.3.1 implies that the developed torque varies inversely as the square of the input RMS voltage to the motor, as indicated in Fig. 27.14b. This makes such a drive suitable for fan- and impeller-type loads for which torque demand rises faster with speed. For other types of loads, the suitable speed range is very limited. Motors with high rotor resistance may offer an extended speed range. It should be noted that this type of drive with back-to-back thyristors with firing-angle control suffers from poor power and harmonic distortion factors when operated at low speed.

If unbalanced operation is acceptable, the thyristors in one or two supply lines to the motor may be bypassed. This offers the possibility of dynamic braking or plugging, desirable in some applications.

27.3.3.2 Slip Power Control

Variable-speed, three-phase, wound-rotor (or slip-ring) induction motor drives with slip power control may take several forms. In a passive scheme, the rotor power is rectified and dissipated in a liquid resistor or in a multitapped resistor that may be adjustable and forced cooled. In a more popular scheme, which is widely used in medium- to large-capacity pumping installations, the rectified rotor power is returned to the ac mains by a thyristor converter operating in naturally commutated inversion mode. This static Scherbius scheme is



(a) (b)

FIGURE 27.14 (a) Stator voltage controller. (b) Motor and load torque–speed characteristics under voltage control.

indicated in Fig. 27.15. In this scheme, the rotor terminals are connected to a three-phase diode bridge that rectifies the rotor voltage. This rotor output is then inverted into mains frequency ac by a fully controlled thyristor converter operating off the same mains as the motor stator.

The converter in the rotor circuit handles only the rotor slip power, so that the cost of the power converter circuit can be much less than that of an equivalent inverter drive, albeit at the expense of the more expensive motor. The dc link current, smoothed by a reactor, may be regulated by controlling the firing angle of the converter in order to maintain the developed torque at the level required by the load. The current controller (CC) and speed controller (SC) are also indicated in Fig. 27.15. The current controller output determines the converter firing angle α from the firing control circuit (FCC).

From the equivalent circuit of Fig. 27.13 and ignoring the stator impedance, the RMS voltage per phase in the rotor circuit is given by

$$V_R = \frac{V_s}{n}\frac{\omega_r}{\omega_s} = \frac{V_s}{n}\frac{s\omega_s}{\omega_s} = \frac{V_s s}{n} \tag{27.20}$$

where ω_s and ω_r are the angular frequencies of the voltages in the stator and rotor circuits, respectively, and n is the ratio of the equivalent stator to rotor turns. The dc-link voltage at the rectifier terminals of the rotor, v_d, is given by

$$v_d = \frac{3\sqrt{6}V_R}{\pi}$$

Assuming that the transformer interposed between the inverter output is and the ac supply has the same turn ratio n as the effective stator-to-rotor turns of the motor,

$$v_d = -\frac{3\sqrt{6}}{\pi}\frac{V_s}{n}\cos\alpha \tag{27.21}$$

The negative sign arises because the thyristor converter develops negative dc voltage in the inverter mode of operation. The dc-link inductor is mainly to ensure continuous current through the converter so that the expression (27.21) holds for all conditions of operation. Combining the preceding three equations gives

$$s\omega_s = -\omega_s\cos\alpha \qquad \text{so that} \qquad s = -n\cos\alpha$$

and the rotor speed

$$\omega_0 = \frac{1}{P}(1-s)\omega_s = \frac{1}{P}\omega_s(1+n\cos\alpha)\ \text{rad/s}. \tag{27.22}$$

Thus, the motor speed can be controlled by adjusting the firing angle α. By varying α between 180° and 90°, the speed of the motor can be varied from zero to full speed, respectively. For a motor with low rotor resistance and with the assumptions taken earlier, it can be shown that the developed torque of the motor is given by

$$T = 3P\frac{V_s}{\omega_s}i_d \approx 3P\lambda_m i_d\ \text{Nm} \tag{27.23}$$

where i_d is the dc link current. Thus, the inner torque control loop of a variable-speed drive using the Scherbius scheme

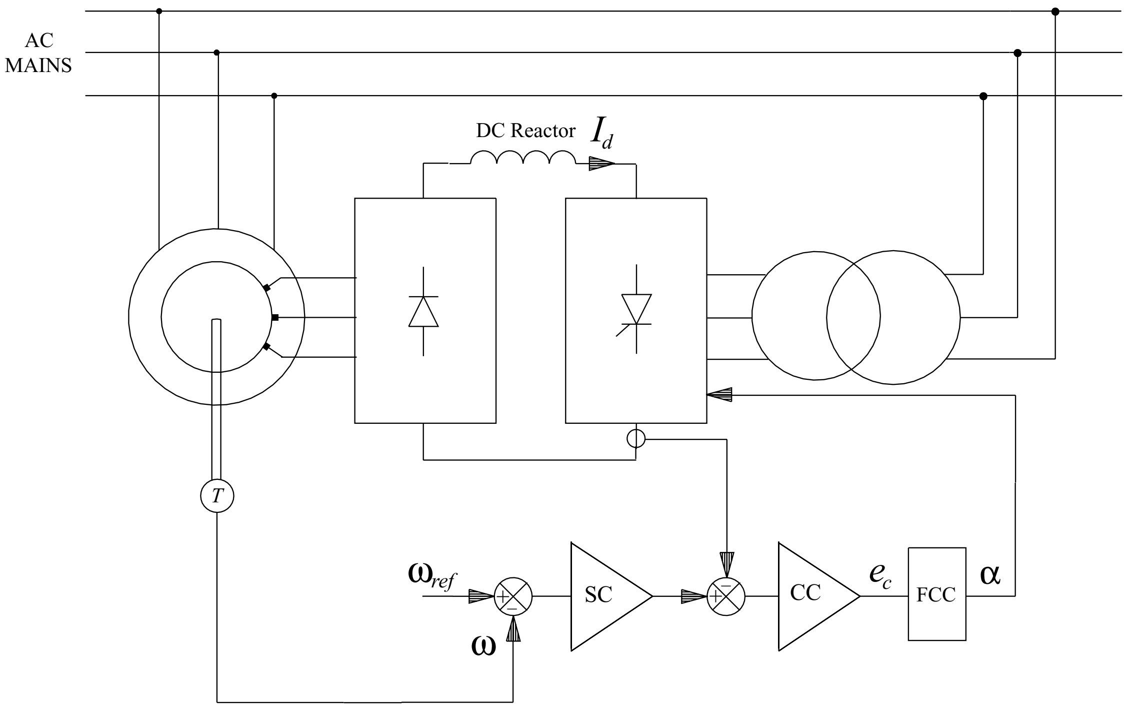


FIGURE 27.15 The static Scherbius drive scheme of slip power control.

normally employs a dc-link current loop as the innermost torque loop. Figure 27.16 shows transient responses of the dc-link, rotor, and stator currents of such a drive when the motor is accelerated between two speeds. The drive is normally started with a short-time-rated liquid resistor, and the thyristor speed controller is started when the drive reaches a certain speed.

By replacing the diode rectifier of Fig. 27.16 with another thyristor bridge, power can be made to flow to and from the rotor circuit, allowing the motor to operated at higher than synchronous speed. For very large drives, a cycloconverter may also be used in the rotor circuit with direct conversion of frequency between the ac supply and the rotor and driving the motor above and below synchronous speed.

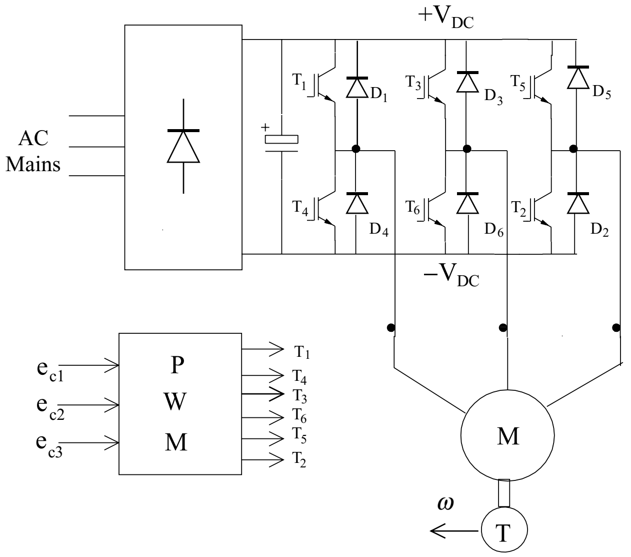


FIGURE 27.17 *V–f* drive with SPWM inverter.

27.3.3.3 Variable-Voltage, Variable-Frequency *V f* Control

. . . . SPWM Inverter Drive When an induction motor is driven from an ideal ac voltage source, its normal operating speed is less than 5 below the synchronous speed, which is determined by the ac source frequency and the number of motor poles. With a sinusoidally modulated (SPWM) inverter, indicated in Fig. 27.17, the supply frequency to the motor can be easily adjusted for variable speed. Equation (27.18) implies that if rated airgap flux is to be maintained at its rated value at all speeds, the supply voltage V_1 to the motor should be varied in proportion to the frequency f_1. The block diagram of Fig. 27.18a shows how the frequency f_1 and the output voltage V_1 of the SPWM inverter are proportionately adjusted with the speed reference. The speed reference signal is normally passed through a filter that only allows a gradual change in the frequency f_1. This type of control is widely referred to as the *V–f* inverter drive. Control of the stator input voltage V_1 as a function of the frequency f_1 is readily arranged within the inverter by modulating the switches T_1–T_6. At low speed, however, where the input voltage V_1 is low, most of the input voltage may drop across the stator impedance, leading to a reduction in airgap flux and loss of torque.

Compensation for the stator resistance drop, as indicated in Fig. 27.18b, is often employed. However, if the motor becomes lightly loaded at low speed, the airgap flux may exceed the rated value, causing motor to overheat.

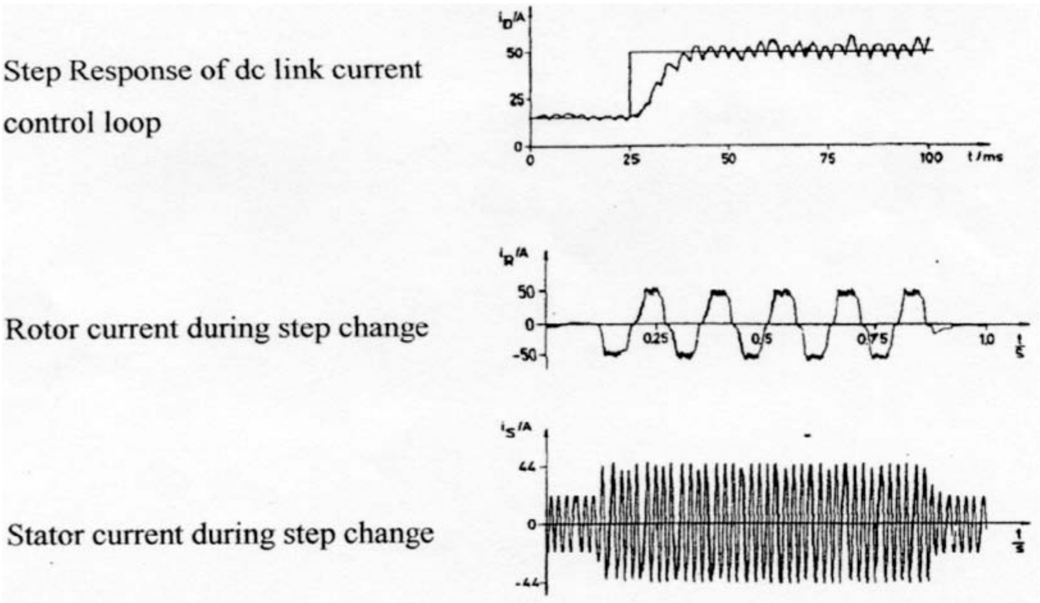


FIGURE 27.16 Transient responses of a slip power controlled drive under acceleration.

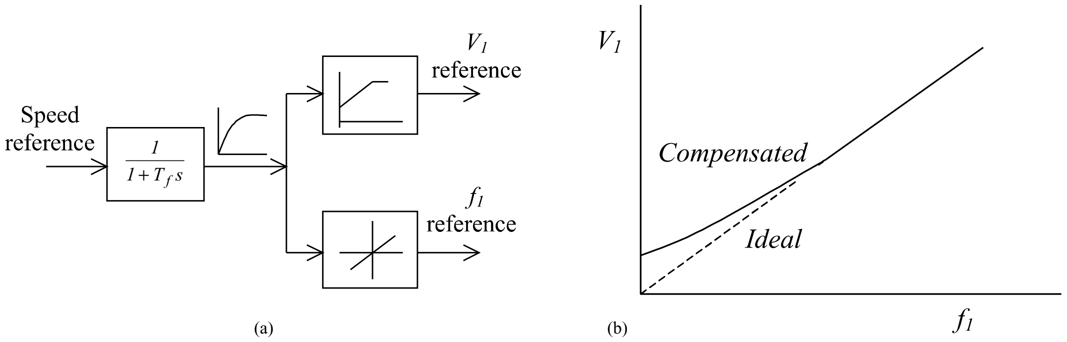


FIGURE 27.18 (a) Input reference filter and voltage and frequency reference generation for the V–f inverter drive. (b) Voltage compensation at low speed.

From the equivalent circuit of Fig. 27.13 and neglecting rotor leakage inductance, the developed torque T and the rotor current I_2 are given by

$$I_2 = \frac{E_1 s\omega_1}{R_2\omega_1} = \frac{\lambda_m}{R_2} s\omega_1 \qquad (27.24)$$

and

$$T = 3P\frac{R_2}{\omega_r} I_2^2 \qquad (27.25)$$

where $s\omega_1$ is the slip frequency, which is also the frequency of the voltages and currents in the rotor. Equation (27.24) implies that by limiting the slip s, the rotor current can be limited, which in turn limits the developed torque [Eq. (27.25)]. Consequently, a slip-limited drive is also a torque-limited drive. Note that this true only at steady state. A speed-control system with such a slip limiter is shown in Fig. 27.19. In this scheme, the motor speed is sensed and added to a limited speed error (or limited slip speed) to obtain the frequency (or speed reference for the V–f drive).

Many applications of the V–f controller, however, are open-loop schemes, in which any demanded variation in V_1 is passed through a ramp limiter (or filter) so that sudden changes in the slip speed ω_r are precluded, thereby allowing the motor to follow the change in the supply frequency without exceeding the rotor current and torque limits.

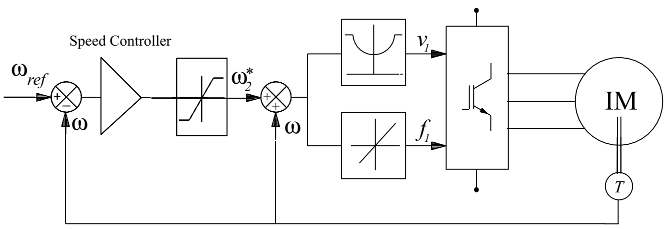


FIGURE 27.19 Closed-loop speed controller with an inner slip loop.

From the foregoing analyses, it is obvious that the V–f inverter drive essentially operates in all four quadrants, with rotor speed dropping slightly with load, and developing full torque at the same slip speed at all speeds. This assumes that the stator input voltage is properly compensated so that the motor is operated with constant (or rated) airgap flux at all speed. The motor can be operated above the base speed by keeping the input voltage V_1 constant while increasing the stator frequency above base frequency in order to run the motor at speeds higher than the base speed. The airgap flux and hence maximum developed torque now fall with speed, leading to constant power type characteristic. Figure 27.20

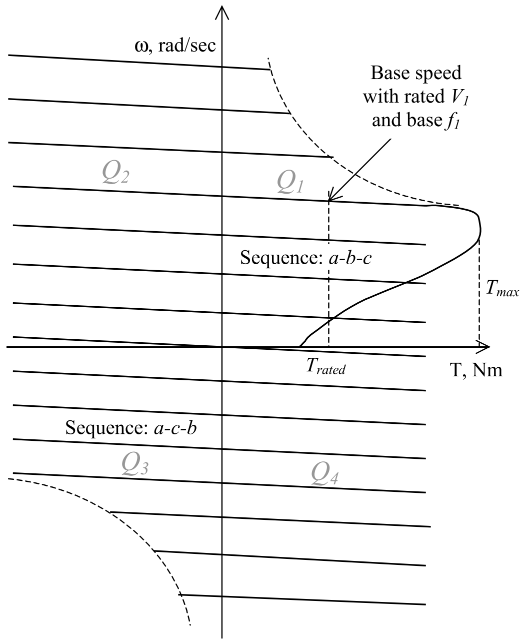


FIGURE 27.20 Typical T–ω characteristics of V–f drive with input frequency f_1 and voltage V_1 below and above base speed.

depicts the T–ω characteristics of such a voltage- and frequency-controlled drive for various operating frequencies.

In this figure, the T–ω characteristic for base speed has been drawn in full, indicating the maximum developed torque T_{max} and the rated torque. Below base speed, the V_1/f_1 ratio is maintained to keep the airgap flux constant. Above base speed, V_1 is kept constant, while f_1 increases with speed, thus weakening the airgap flux. Forward driving in quadrant $Q1$ takes place with an inverter output voltage sequence of *a–b–c*, whereas reverse driving in quadrant $Q3$ takes place with sequence *a–c–b*. Regenerative braking while forward driving takes place by adjusting the input frequency f_1 in such a way that the motor operates in quadrant $Q2$ (quadrant $Q4$ for reverse braking) with the desired braking characteristic.

Note that the characteristics in Fig. 27.20 are based on the steady-state equivalent circuit model of the motor. Such a drive suffers from poor torque response during transient operation because of time-dependent interactions between the stator and rotor fluxes. Figure 27.21 indicates the machine airgap flux during acceleration with V–f control obtained from a dynamic model. Clearly, the airgap flux does not remain constant during dynamic operation.

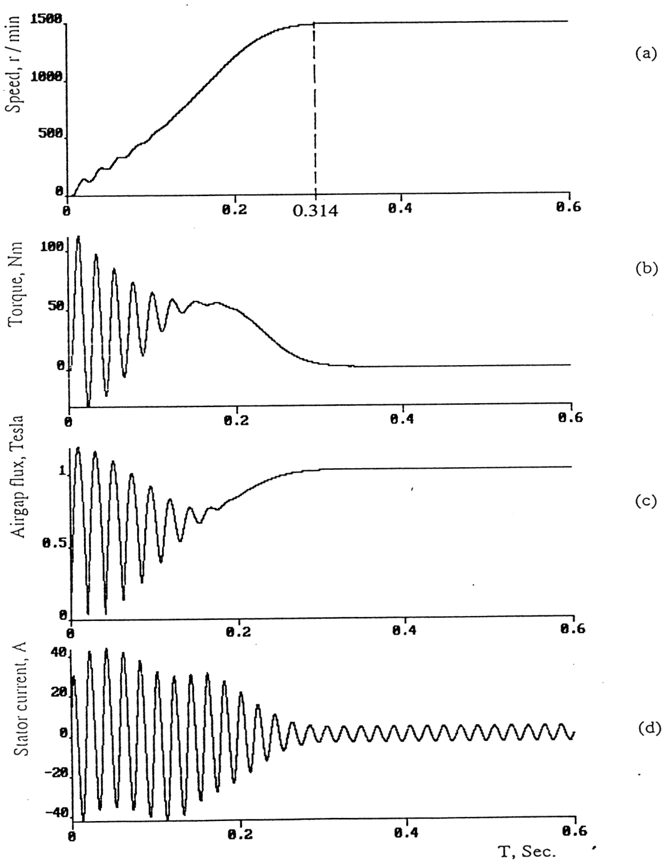


FIGURE 27.21 Transient response of torque, speed, current, and airgap flux during acceleration from standstill using a V–f inverter drive.

. . . . *Cycloconverter Drive* For large-capacity induction motor drives, the variable-frequency supply at variable voltage is effectively obtained from a cycloconverter in which back-to-back thyristor converter pairs are used, one for each phase of the motor, as indicated in Fig. 27.22. Each thyristor block in this figure represents a fully controlled thyristor ac–dc converter. The maximum output frequency of such a converter can be as high as about 40 of the supply frequency. In view of the large number of thyristor switches required, cycloconverter drives are suitable for large-capacity but low-speed applications.

27.3.3.4 Variable-Current Variable-Frequency *I f* Control

In this scheme, medium- to large-capacity induction motors are driven from a variable but stiff current supply that may be obtained from a thyristor converter and a dc link inductor as indicated in Fig. 27.23. The frequency of the current supply to the motor is adjusted by a thyristor converter with auxiliary diodes and capacitors. The diodes in each inverter leg and the capacitors across them are needed for turning off the thyristors when current is to be commutated from one to the next in sequence. The motor current waveforms are normally six-step, or quasi square, as indicated in Fig. 27.24. The switching states of the inverter thyristors are also indicated in this figure. The motor voltage waveforms are determined by the load. These waveforms are more nearly sinusoidal than the current waveforms.

The thyristor converter supplying the quasi-square current waveforms to the motor has firing angle control, in order to regulate the dc-link current to the inverter. The dynamics of the dc-link current control is such that this current may be considered to be constant during the time the inverter switches commutate the dc-link current from one switch to the next. Such a current-source drive offers four-quadrant operation, with independent control of the dc-link current and output frequency. One drawback is that the motor voltage waveforms have voltage spikes due to commutation.

From the analysis of Section 27.3.2, if the higher order harmonics of the current waveforms in Fig. 27.24 are neglected, and it is assumed that the motor voltage and current waveforms are taken to be sinusoidal, the magnetizing current I_m in Fig. 27.13 can be kept constant (for constant-airgap flux operation) if the RMS value of the stator supply current I_1 is defined according to Eq. (27.26). This relationship is also shown in graphical form in Fig. 27.25.

$$I_m = I_1 \left[\frac{R_2^2 + (2\pi f_1 s L_2)^2}{R_2^2 + 2\pi f_1 (L_2 + L_m)^2} \right]^{1/2} = \text{constant} \qquad (27.26)$$

The control scheme for variable-speed operation with a current source drive is indicated the block diagram of Fig. 27.26. The speed reference defines the stator current reference

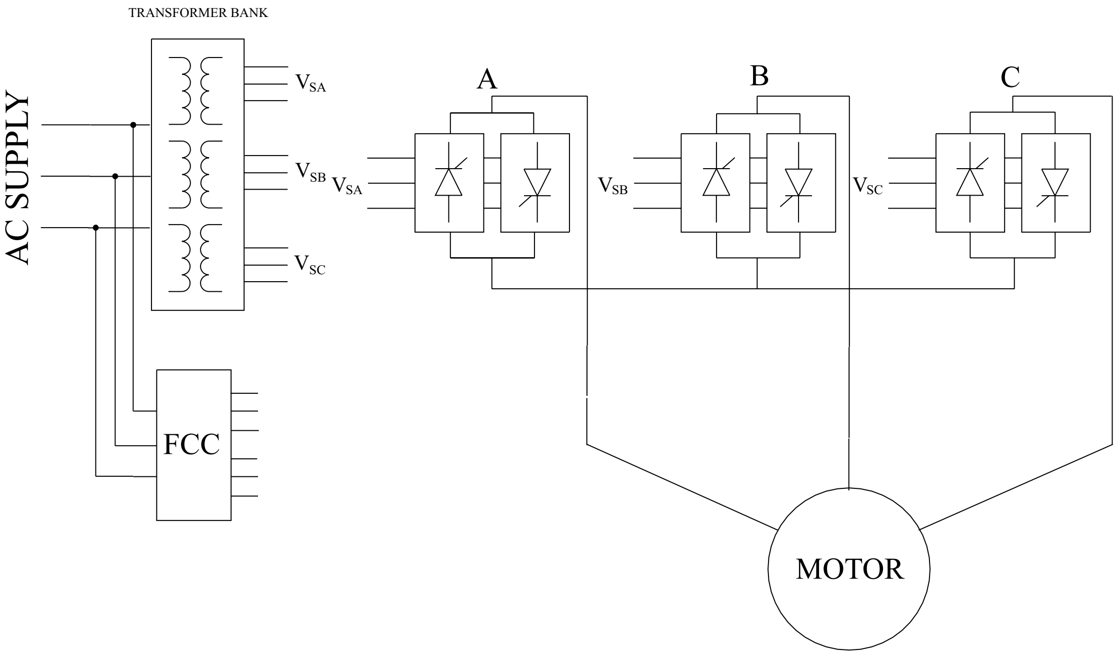


FIGURE 27.22 *V–f* drive with cycloconverter drive.

according to Eq. (27.26) and the frequency reference is obtained by adding the rotor frequency to the actual speed of the motor. The inverter drive may consist of the thyristor current source and inverter of Fig. 27.23 or the diode-rectifier-supplied SPWM transistor inverter of Fig. 27.17 with independent current regulators, one for each phase.

The dynamic performance of such current-controlled induction motor drives is not very satisfactory, just as for the voltage source inverters. Furthermore, the current-source inverter drive cannot normally be operated open-loop, like the *V–f* inverter drive. For high dynamic performance, vector-controlled drives are becoming popular.

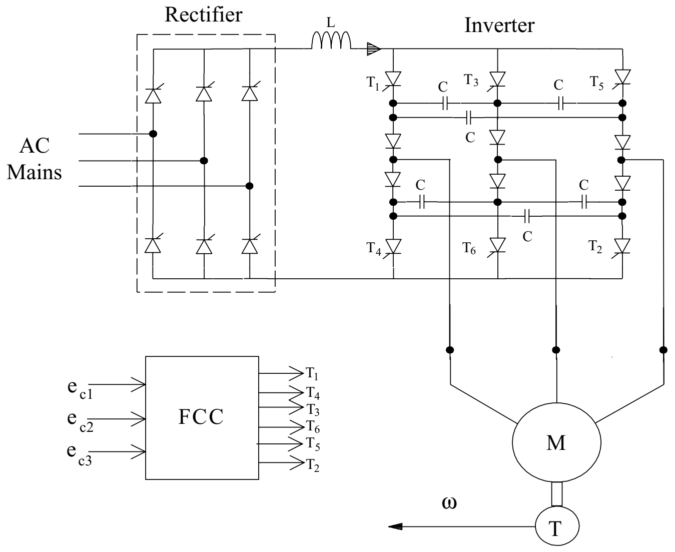


FIGURE 27.23 Dc-link current-source thyristor inverter drive.

27.3.4 Vector Controls

The foregoing scalar control methods are only suitable for adjustable-speed applications in which the load speed or position is not controlled as in a servo system. The vector control technique allows a squirrel-cage induction motor to be driven with high dynamic performance, comparable to that of a dc motor. For this, the controller needs to know the rotor speed (in the indirect method) or the airgap flux vector accurately, using sensors. The latter method is not practical because of the requirement of attaching airgap flux sensors.

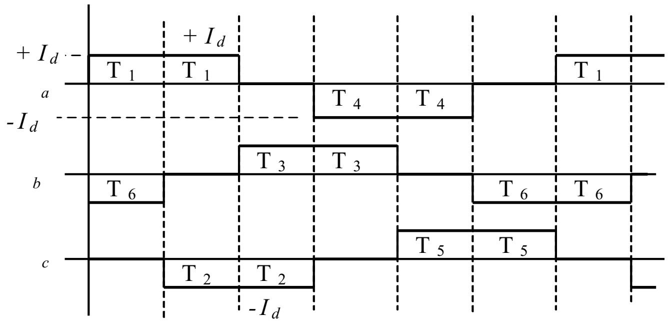


FIGURE 27.24 Motor-current waveforms and the thyristor switching states for a current-source drive.

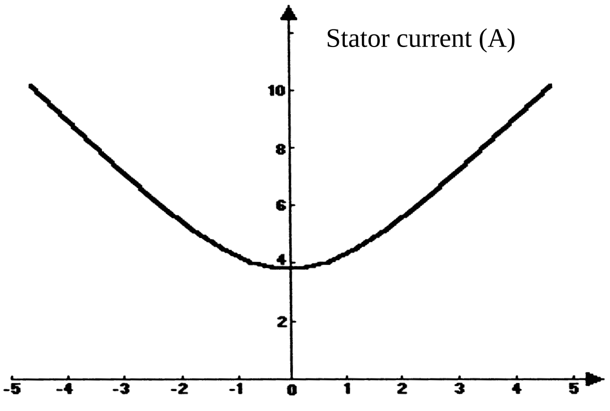


FIGURE 27.25 Stator current vs rotor (slip) frequency for constant-airgap flux operation.

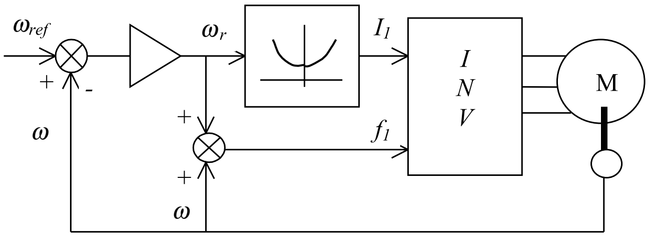


FIGURE 27.26 Variable-current, variable-frequency inverter drive scheme.

The indirect method, which is being widely accepted in recent years, requires the controller to be matched with the motor being driven. This is because the controller needs also to know some rotor parameter(s), which may vary according to the conditions of operation, continuously.

27.3.4.1 Basic Principles

The methods of vector control are based on the dynamic equivalent circuit of the induction motor. There are at least three fluxes (rotor, airgap, and stator) and three currents or mmfs (stator, rotor, and magnetizing) in an induction motor. For high dynamic response, interactions among current, fluxes, and speed must be taken into account in determining appropriate control strategies. These interactions are understood only via the dynamic model of the motor.

All fluxes rotate at synchronous speed. The three-phase currents create mmfs (stator and rotor) that also rotate at synchronous speed. Vector control aligns axes of an mmf and a flux orthogonally at all times. It is easier to align the stator current mmf orthogonally to the rotor flux.

Any three-phase sinusoidal set of quantities in the stator can be transformed to an orthogonal reference frame by

$$\begin{bmatrix} f_{\alpha s} \\ f_{\beta s} \\ f_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{4\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{4\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_{as} \\ f_{bs} \\ f_{cs} \end{bmatrix} \tag{27.27}$$

where θ is the angle of the orthogonal set α–β–0 with respect to any arbitrary reference. If the α–β–0 axes are stationary and the α axis is aligned with the stator a axis, then $\theta = 0$ at all times, Thus

$$\begin{bmatrix} f_{as} \\ f_{bs} \\ f_{os} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_{as} \\ f_{bs} \\ f_{cs} \end{bmatrix} \tag{27.28}$$

If the orthogonal set of reference rotates at the synchronous speed ω_1, its angular position at any instant is given by

$$\theta = \int_0^t \omega_1 t + \theta_0 \tag{27.29}$$

The orthogonal set is then referred to as d–q–0 axes. The three-phase rotor variables, transformed to the synchronously rotating frame, are

$$\begin{bmatrix} f_{dr} \\ f_{qr} \\ f_o \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\omega_e - \omega_r)t & \cos\left((\omega_e - \omega_r)t - \frac{2\pi}{3}\right) & \cos\left((\omega_e - \omega_r)t - \frac{4\pi}{3}\right) \\ \sin(\omega_e - \omega_r)t & \sin\left((\omega_e - \omega_r)t - \frac{2\pi}{3}\right) & \sin\left((\omega_e - \omega_r)t - \frac{4\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} f_{ar} \\ f_{br} \\ f_{cr} \end{bmatrix} \tag{27.30}$$

It should be noted that the difference $\omega_e - \omega_r$ is the relative speed between the synchronously rotating reference frame and the frame attached to the rotor. This difference is the also slip frequency, ω_{sl}, which is frequency of the rotor variables. By applying these transformations, voltage equations of the motor in the synchronously rotating frame reduce to

$$\begin{bmatrix} v_{qs} \\ v_{ds} \\ v_{qr} \\ v_{dr} \end{bmatrix} = \begin{bmatrix} R_s + pL_s & \omega_e L_s & pL_m & \omega_e L_m \\ -\omega_e L_s & R_s + pL_s & -\omega_e L_m & pL_m \\ pL_m & (\omega_e - \omega_r)L_m & R_r + pL_r & (\omega_e - \omega_r)L_r \\ -(\omega_e - \omega_r) & pL_m & -(\omega_e - \omega_r)L_r & R_r + pL_r \end{bmatrix} \times \begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{qr} \\ i_{dr} \end{bmatrix} \tag{27.31}$$

where the speed of the reference frame, ω_e, is equal to ω_1 and

$$L_s = L_{ls} + L_m, \qquad L_r = L_{ir} + L_m.$$

Subscripts l and m stand for leakage and magnetizing, respectively, and p represents the differential operator d/dt. The equivalent circuits of the motor in this reference frame are indicated in Figs. 27.27a and 27.27b.

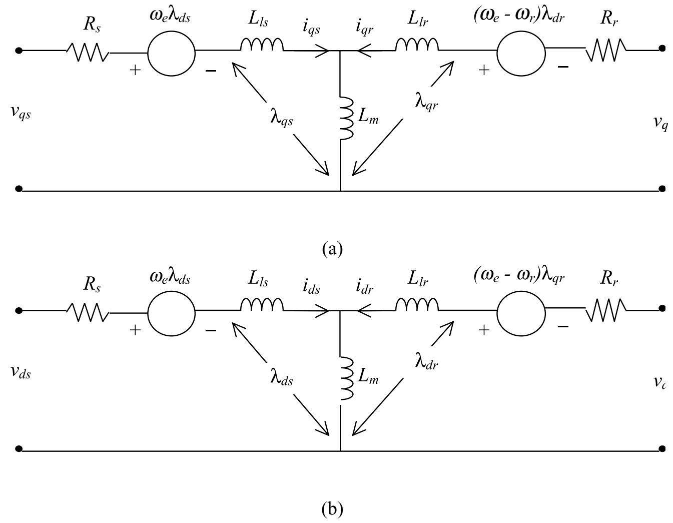


FIGURE 27.27 Motor dynamic equivalent circuits in the synchronously rotating (a) q- and (b) d-axes.

The stator flux linkage equations are

$$\lambda_{qs} = L_{ls}i_{qs} + L_m(i_{qs} + i_{qr}) = L_s i_{qs} + L_m i_{qr} \tag{27.32}$$

$$\lambda_{ds} = L_{ls}i_{ds} + L_m(i_{ds} + i_{dr}) = L_s i_{ds} + L_m i_{dr} \tag{27.33}$$

$$\hat{\lambda}_s = \sqrt{(\lambda_{qs}^2 + \lambda_{ds}^2)} \tag{27.34}$$

The rotor flux linkages are given by

$$\lambda_{qr} = L_{lr}i_{qr} + L_m(i_{qs} + i_{qr}) = L_r i_{qr} + L_m i_{qs} \tag{27.35}$$

$$\lambda_{dr} = L_{lr}i_{dr} + L_m(i_{ds} + i_{dr}) = L_r i_{dr} + L_m i_{ds} \tag{27.36}$$

$$\hat{\lambda}_r = \sqrt{(\lambda_{qr}^2 + \lambda_{dr}^2)} \tag{27.37}$$

The airgap flux linkages are given by

$$\lambda_{mq} = L_m(i_{qs} + i_{qr}) \tag{27.38}$$

$$\lambda_{md} = I_m(i_{ds} + i_{dr}) \tag{27.39}$$

$$\hat{\lambda}_m = \sqrt{(\lambda_{mqs}^2 + \lambda_{mds}^2)} \tag{27.40}$$

The torque developed by the motor is given by

$$T = \frac{3P}{2}[\lambda_{ds}i_{qs} - \lambda_{qs}i_{ds}] \tag{27.41}$$

From Eq. (27.39), the rotor voltage equations are

$$v_{qr} = 0 = L_m\frac{di_{qs}}{dt} + (\omega_e - \omega_r)L_m i_{ds} + (R_r + L_r)\frac{di_{qr}}{dt} + (\omega_e - \omega_r)L_r i_{dr} \tag{27.42}$$

$$v_{dr} = 0 = L_m\frac{di_{ds}}{dt} + (\omega_e - \omega_r)L_m i_{qs} + (R_r + L_r)\frac{di_{dr}}{dt} + (\omega_e - \omega_r)L_r i_{qr} \tag{27.43}$$

Using (27.35) and (27.36),

$$\frac{d\lambda_{qr}}{dt} + R_r i_{qr} + (\omega_e - \omega_r)\lambda_{dr} = 0 \tag{27.44}$$

and

$$\frac{d\lambda_{dr}}{dt} + R_r i_{dr} + (\omega_e - \omega_r)\lambda_{qr} = 0 \tag{27.45}$$

Also from (27.35) and (27.36),

$$i_{qr} = \frac{1}{L_r}\lambda_{qr} - \frac{L_m}{L_r}i_{qs} \tag{27.46}$$

$$i_{dr} = \frac{1}{L_r}\lambda_{dr} - \frac{L_m}{L_r}i_{ds} \tag{27.47}$$

The rotor currents i_{qr} and i_{dr} can be eliminated from (27.44) and (27.45) by using (27.46) and (27.47). Thus

$$\frac{d\lambda_{qr}}{dt}+\frac{L_r}{R_r}\lambda_{qr}-\frac{L_m}{L_r}R_r i_{qs}+(\omega_e-\omega_r)\lambda_{dr}=0 \tag{27.48}$$

$$\frac{d\lambda_{qr}}{dt}+\frac{L_r}{R_r}\lambda_{qr}-\frac{L_m}{L_r}R_r i_{qs}+(\omega_e-\omega_r)\lambda_{dr}=0 \tag{27.49}$$

A condition for elimination of transients in rotor flux and the coupling between the two axes is to have

$$\lambda_{qr}=0 \qquad \text{and} \qquad \hat{\lambda}_r=\lambda_{dr} \tag{27.50}$$

The rotor flux should also remain constant so that

$$\frac{d\lambda_{dr}}{dt}=0=\frac{d\lambda_{qr}}{dt} \tag{27.51}$$

From (27.50) and (27.51),

$$\omega_e-\omega_r=\omega_{sl}=\frac{L_m}{\hat{\lambda}_r}\frac{R_r}{L_r}i_{qs} \tag{27.52}$$

and

$$\frac{L_r}{R_r}\frac{d\hat{\lambda}_r}{dt}+\hat{\lambda}_r=L_m i_{ds} \tag{27.53}$$

Substituting the expressions for i_{qr} and i_{dr} into (27.35) and (27.36),

$$\lambda_{qs}=\left(L_s-\frac{L_m^2}{L_r}\right)i_{qs}+\frac{L_m}{L_r}\lambda_{qr} \tag{27.54}$$

$$\lambda_{ds}=\left(L_s-\frac{L_m^2}{L_r}\right)i_{ds}+\frac{L_m}{L_r}\lambda_{dr} \tag{27.55}$$

Substituting λ_{qs} and λ_{ds} from (27.54) and (27.55) into the torque equation of (27.41)

$$T=\frac{3P}{2}\frac{L_m}{L_r}(\lambda_{dr}i_{qs}-\lambda_{qr}i_{ds})=\frac{3P}{2}\frac{L_m}{L_r}\hat{\lambda}_r i_{qs} \tag{27.56}$$

It is clear from (27.53) that the rotor flux $\hat{\lambda}_{dr}$ is determined by i_{dr}, subject a time delay T_r that is the rotor time constant (L_r/R_r). Current i_{qs}, according to Eq. (27.56), controls the developed torque T without delay. Currents i_{ds} and i_{qs} are orthogonal to each other and are called the flux and torque-producing currents, respectively. This correspondence between flux and torque-producing currents is subject to maintaining the conditions in (27.50) and (27.51). Normally, i_{ds} would remain fixed for operation up to the base speed. Thereafter, it is reduced in order to weaken the rotor flux so that the motor may be driven with a constant-power-like characteristic.

Based on how the rotor flux is detected and regulated, two methods of control are available. One is the more popular indirect-rotor flux-oriented control (IFOC) method, and the other is the direct vector control method; both are described hereafter.

27.3.4.2 Indirect-Rotor Flux-Oriented (IFOC) Vector Control

In the indirect scheme, the relationship between slip frequency and i_{qs} given by (27.52) is used to relate the compensated speed error $\omega_1-\omega_r$ to i_{qs}. The i_{qs}, in turn, is used to develop to the demanded torque T according to (27.56). The rotor flux is maintained at the base value for operation below speed, and it may be reduced to a lower value for field weakening above base speed. The orthogonal relationship between the torque-producing stator current i_{qs} and the flux-producing stator current i_{ds} is maintained at all times by generating the stator current references in the synchronously rotating dq reference frame using sine and cosine functions of angle θ_1. This angle is obtained as indicated in Fig. 27.28.

The compensated speed error produces the current reference i_{qs}^* according to (27.56). i_{qs}^* also gives the slip speed ω_{sl}, according to (27.53). The slip speed ω_{sl} is added to the rotor speed ω, to obtain the stator frequency ω_1. This frequency is integrated with respect to time to produce the required angle θ_1 of the stator mmf relative to the rotor flux vector. This angle is used to transform the stator currents to the dq reference frame. Two independent current controllers are used to regulate the i_q and i_d currents to their reference values. The compensated i_q and i_d errors are then inverse transformed into the stator a–b–c reference frame for obtaining switching signals for the inverter via PWM or hysteresis comparators.

It is clear that this scheme uses a feed-forward scheme, or a machine model, in which the current reference for i_{qs} is also determined by the rotor time constant T_r. This also indicated in Fig. 27.28. The rotor time constant T_r cannot be expected to remain constant for all conditions of operation. Its considerable variation with operating conditions means that the slip speed ω_{sl}, which directly affects the developed torque and the rotor flux vector position, may vary widely. Many rotor time-constant identification schemes have been developed in recent years to overcome the problem.

The mandatory requirement for a rotor-speed sensor is also a significant drawback, because its presence reduces the reliability of the IFOC drive. Consequently, sensorless schemes of identifying the rotor flux position have also drawn considerable interest in recent years.

Figure 27.29 shows the transient response of an induction motor that was for the results of Fig. 27.21 under the IFOC

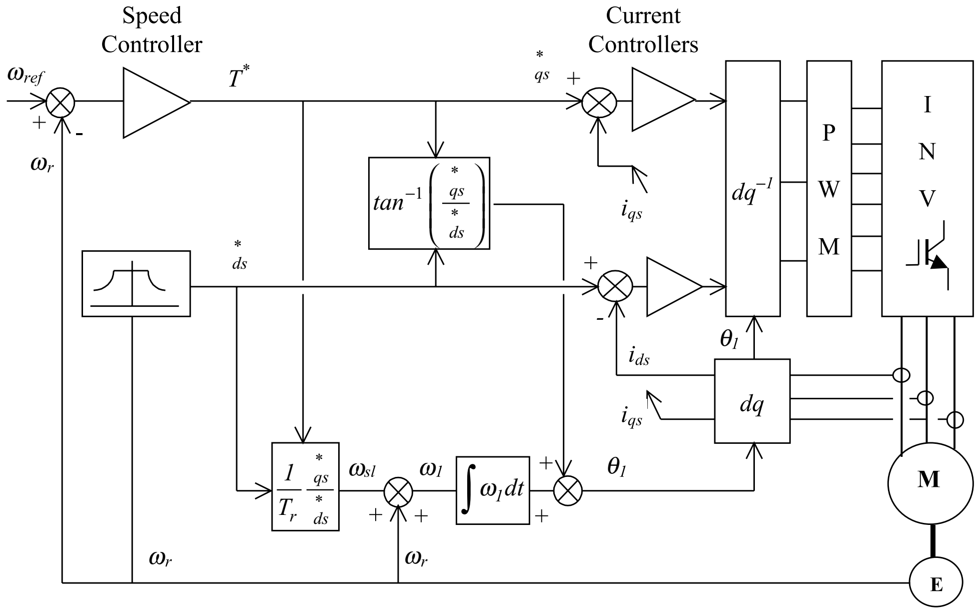

Speed Controller
Current Controllers
ω_{ref}
T^*
$*_{qs}$
$\tan^{-1}\left(\frac{*_{qs}}{*_{ds}}\right)$
$*_{ds}$
i_{qs}
i_{ds}
dq^{-1}
P W M
I N V
θ_1
dq
M
E
$\frac{1}{T_r}\frac{*_{qs}}{*_{ds}}$
ω_{sl}
ω_1
$\int \omega_1 dt$
ω_r

FIGURE 27.28 Indirect-rotor flux-oriented vector control scheme.

drive scheme of Fig. 27.28. In this case, the drive accelerates a large inertia load from standstill to the base speed of 1500 rev/min. It is clear that the overcurrent transients of Fig. 27.21 are eliminated, while the motor accelerates under constant torque (implied by the constant rate at which the speed increases) and settles at the final speed with little over- or undershoot in speed. Obviously, rotor and airgap fluxes remain constant at all times.

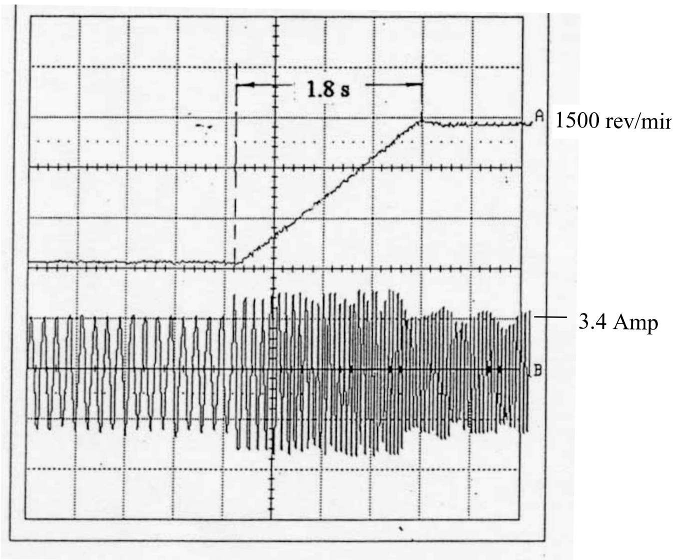


FIGURE 27.29 Speed and current responses of an induction motor drive under the IFOC scheme of Fig. 27.28.

27.3.4.3 Direct Vector Control with Airgap Flux Sensing

In the direct scheme, use is made of the airgap flux linkages in the stator *d*- and *q*-axes, which are then compensated for the respective leakage fluxes in order to determine the rotor flux linkages in the stator reference frame. The airgap flux linkages are measured by installing quadrature flux sensors in the airgap, as indicated in Fig. 27.30.

By returning to Eqs. (27.32)–(27.40) in the stator reference frame and using some simplifications, it can be shown that

$$\lambda_{qr}^s = \frac{L_r}{L_m}\lambda_{qm}^2 - L_{lr}i_{qs}^s \tag{27.57}$$

$$\lambda_{dr}^s = \frac{L_r}{L_m}\lambda_{dm}^s - L_{lr}i_{ds}^s \tag{27.58}$$

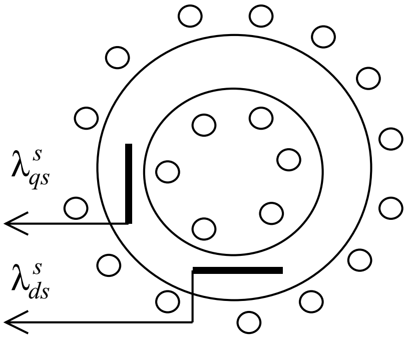

λ_{qs}^s
λ_{ds}^s

FIGURE 27.30 Quadrature sensors for airgap flux for direct vector control.

where the superscript s stands for the stator reference frame. Since the rotor flux rotates at synchronous speed with respect to the stator reference frame, the angle θ_1 used for the coordinate transformations in Fig. 27.27 can be obtained from

$$\cos\theta_1 = \frac{\lambda^s_{dr}}{\hat{\lambda}_r} \tag{27.59}$$

and

$$\sin\theta_1 = \frac{\lambda^s_{qr}}{\hat{\lambda}_r} \tag{27.60}$$

where

$$|\hat{\lambda}_r| = \sqrt{(\lambda^2_{dr})^2 + (\lambda^s_{qr})^2}.$$

The control of torque via i_{qs} and rotor flux via i_{ds}, subject to satisfying conditions (27.50) and (27.51); remain as indicated in Fig. 27.28, according to the basic principle of vector control.

The requirement of airgap flux sensors is rather restrictive. Such fittings also reduce reliability. Even though this method of control offers better low-speed performance than the IFOC, this restriction has practically precluded the adoption of this scheme. In an alternative method, the d- and q-axis stator flux linkages of the motor may be computed from integrating the stator input voltages.

27.3.5 Further Reading

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27.4 Synchronous Motor Drives

M. . ah an

27.4.1 Introduction

Variable-speed synchronous motors have been widely used in very large capacity (>MW) pumping and centrifuge type applications using naturally commutated current-source thyristor converters. At the low-power end, the current-source SPWM inverter-driven synchronous motors have become very popular in recent years in the form of permanent-magnet brushless dc and ac synchronous motor drives in servo-type applications. There are certain features of three-phase synchronous motors that have allowed them, especially the lower capacity motors, to be controlled with high dynamic performance using cheaper control hardware than is required for the induction motor of similar capacity. Since the average speed of the synchronous motor is precisely related to the supply frequency, which can be precisely controlled, multimotor drives with a fixed speed ratio among them are also good candidates for synchronous motor drives. This section begins with the performance of the variable-speed nonsalient-pole and salient-pole synchronous motor drive using the steady-state equivalent circuit followed by dynamics of the vector-controlled synchronous motor drive.

27.4.2 Steady-State Equivalent-Circuit Representation of the Motor

Some of the operating characteristics of variable-frequency voltage- and current-source-driven synchronous motors can be readily obtained from their steady-state equivalent representation, as was the case with the scalar controls of induction motor drives. Assuming balanced, sinusoidal distribution of stator and rotor MMFs and an uniform airgap (nonsalient-pole motor), the per-phase equivalent circuit of Fig. 27.31 represents the motor at a constant speed.

The representation in the figure is in terms of the RMS voltage V applied to the motor phase winding, which consists of the phase resistance R, synchronous reactance X_s (in Ω/phase), and the per-phase induced voltage E_f. The back emf E_f develops in the stator phase winding as a result of rotor excitation supplied from an external dc source via slip rings or by permanent magnets in the rotor. The phasor E_f has an arbitrary phase angle δ with respect to the input voltage V. This is the load angle of the motor.

Unlike the induction motor, a synchronous motor may derive part or all of its excitation from the rotor via rotor excitation. For small synchronous motors that are used in

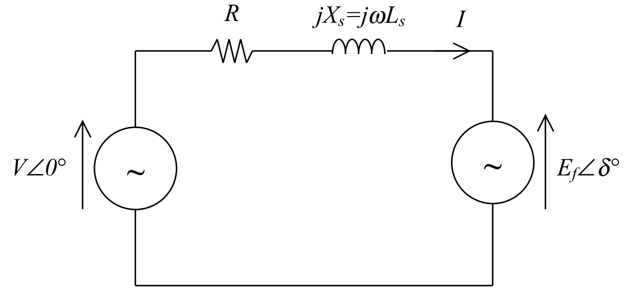


FIGURE 27.31 Equivalent circuit of a nonsalient-pole motor.

brushless dc and ac servo applications, this excitation is derived from permanent magnets in the rotor. This is readily and economically obtained with modern permanent magnets, thus dispensing with the slip-ring-brush assembly. The i^2R losses in the rotor windings with external excitation are also eliminated. These magnets also allow considerable reduction in space requirement for the rotor excitation. For large synchronous motors, this excitation is supplied more economically from an external dc source via slip rings or via an exciter.

The phasor diagrams of Fig. 27.32 may be used to analyze characteristics of the nonsalient-pole synchronous motor drive. Since the rotor magnetic field may be such that the motor may develop a back emf that is smaller or larger than the ac supply voltage to the stator windings, the motor may accordingly be under- or overexcited, respectively. The overexcited motor will normally operate at a leading power factor, as is the case in Fig. 27.32b. This is desirable in high-power applications.

In the phasor diagrams of Fig. 27.32c, the stator current I has been resolved into two components I_d and I_q, which are current phasors responsible for developing MMFs in the rotor d- and q-axes. These representations are in the stator reference frame, and hence are sinusoidal quantities at the frequency of the stator supply.

If the voltage drop across the stator resistance is neglected, which may be acceptable when the stator frequency is near the base frequency or higher, the developed torque T of the motor can be found from the phasor relationships of Fig. 27.32. Thus,

$$T = \frac{3}{\omega_r}\,\frac{EV}{X_s}\sin\delta = \frac{3P}{\omega}\,\frac{EV}{\omega L_s}\sin\delta = \frac{3PK_\phi}{L_s}\,\frac{V}{\omega}\sin\delta \quad \text{Nm} \tag{27.61}$$

for the nonsalient-pole motor (also for the sine-wave PM ac motor with rotor magnets at the surface of the rotor) and

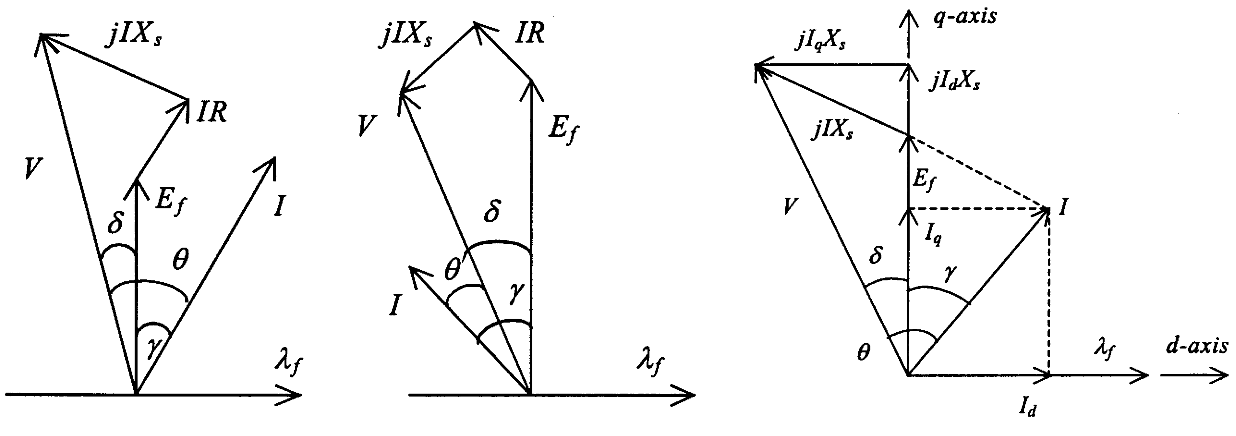
$$\begin{aligned} T &= \frac{3P}{\omega_r}\left[\frac{EV}{\omega L_d}\sin\delta + \frac{V^2}{2}\left(\frac{L_d - L_q}{\omega L_d L_q}\right)\sin 2\delta\right] \\ &= 3P\left[\frac{K_\phi}{L_d}\,\frac{V}{\omega}\sin\delta + \frac{V^2}{2\omega^2}\left(\frac{L_d - L_q}{L_d L_q}\right)\sin 2\delta\right] \end{aligned} \quad \text{Nm} \tag{27.62}$$

for the salient-pole motor (also for the interior-magnet motor in which the rotor magnets are buried inside the rotor). Here the flux constant of the motor, K_ϕ, is the ratio of the RMS value of the phase voltage E_f induced in the stator due to rotor excitation only and speed. Note that for a given rotor excitation, the ratio $K_\phi = E_f/\omega$ remains constant at all speeds.

27.4.3 Performance with Voltage Source Drive

Equations (27.61) and (27.62) imply that if the motor is driven from a voltage-source supply and if the input voltage to frequency ratio, V/f, is kept constant, the motor will develop the same maximum torque at all speeds. For the nonsalient-pole motor, this maximum torque will occur for a load angle $\delta = 90°$. For the salient-pole motor, this will occur for a load angle which is also influenced by the relative values of L_d and L_q.

At low speed, where the supply voltage V is small, the voltage drop in the stator resistance may become significant compared to E_f. This may lead to a significant drop in the maximum available torque, as given by the torque Eqs. (27.63) and (27.64), which are derived from the phasor diagrams of



(a) (b) (c)

FIGURE 27.32 Phasor diagrams of synchronous motors. (a) Underexcited nonsalient-pole motor, (b) overexcited nonsalient-pole motor, (c) underexcited salient-pole motor.

Fig. 27.32. The stator per phase resistance R is now included in the analysis. The developed torque is then given by

$$T = \frac{3PE_{fo}V_1}{\omega_o} \frac{\lambda X_{so}\sin\delta + R\left(\cos\delta - \dfrac{\lambda E_{fo}}{V_1}\right)}{R^2 + (\lambda X_{so})^2} \quad \text{Nm} \qquad (27.63)$$

for the nonsalient-pole motor and

$$T = \frac{3P}{\omega_o} \times \left[\frac{\dfrac{V_1^2}{\lambda}R + VE_{fo}\lambda X_{qo}\sin\delta + \dfrac{V^2}{2}(X_{do}-X_{qo})\sin 2\delta - VRE_{fo}\cos\delta}{R^2 + \lambda^2 X_d X_q}\right] \times \text{Nm} \qquad (27.64)$$

for the salient-pole motor, where the subscript o refers to base quantities and λ refers to the per unit input frequency f_1/f_o.

Equations (27.63) and (27.64) indicate that the maximum torque that the motor can develop diminishes at low speed because of the voltage drop across the stator resistance R. This drop in maximum available torque at low speed can be avoided by boosting the input voltage at low speed, as indicated in Fig. 27.33a. This voltage boosting is similar to the IR compensation applied to a variable-frequency induction motor drive.

Figures 27.33 indicate an open-loop V–f inverter drive scheme, similar to the same scheme for an induction motor drive in which the RMS stator input voltage is made proportional to frequency. The speed reference is passed through a first-order filter, as shown in Fig. 27.33a, so that a large and abrupt change in the input frequency command to the inverter is avoided. The filtered speed reference is translated into a proportional frequency reference f_1. The voltage reference V_1 is also proportional to frequency reference, but with a zero frequency bias. The variable RMS input voltage V_1 to the motor may be obtained from an inverter by SPWM methods or from a cycloconverter with phase angle control.

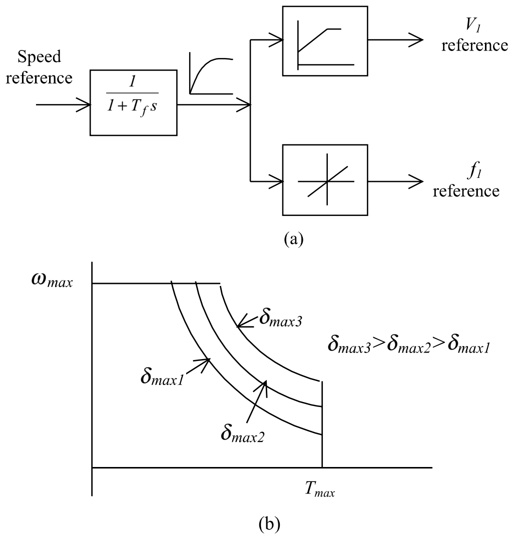


FIGURE 27.33 (a) V–f controller for open-loop inverter drive; (b) T–ω characteristics with limited maximum δ for constant-power operation.

The available input voltage V_1 is normally limited by the available dc-link voltage to the inverter or the ac supply voltage to a cycloconverter. This limit is normally arranged to occur at base speed. Above this speed, the stator flux drops, leading to field weakening and constant-power-like operation, as indicated in Fig. 27.33b. In some control schemes, the maximum load angle δ is not allowed to exceed a certain limiting value $\delta_{\max}$. By selecting $\delta_{\max}$, constant-power operation at various power levels is possible.

27.4.4 Characteristics under Current-Source Inverter CSI Drive

A current-source-driven synchronous motor drive generally gives higher dynamic response. It also gives better reliability because of the automatic current-limiting feature. In a variable-speed application, the synchronous motor is normally driven from a stiff current source. A rotor position sensor is used to place the phase current phasor I of each phase at a suitable angle with respect to the back emf phasor (E_f) of the same phase. The rotor position sensor is thus mandatory.

Two converter schemes have generally been used. In one scheme, as indicated in Fig. 27.34, a large dc-link reactor (inductor) makes the current source to the inverter stiff. The scheme is suitable for large synchronous motors for which thyristor switches are used in the inverter. A current loop may also be established by sensing the dc link current and by using a closed-loop current controller that continuously regulates the firing angle of the controllable rectifier in order to supply the inverter with the desired dc-link current. It can be shown that the motor-developed torque is proportional to the level of the dc-link current.

The inverter drives the motor with quasi-square-wave current waveforms as indicated in Fig. 27.35. The current waveforms are switched according to measured rotor position information, such that the current waveform in each phase has a fixed angular displacement, γ, with respect to the induced emf of the corresponding phase. Because of this, the drive is sometimes referred to as self-controlled. The angular displacement of these current waveforms (or their fundamental components) with the respective back emf waveforms is indicated in Fig. 27.35. Because of the large dc-link inductor, phase currents may be considered to remain essentially constant between the switching intervals. The quasi-square current waveforms contain many harmonics and are responsible for large torque pulsations that may become troublesome at low speed.

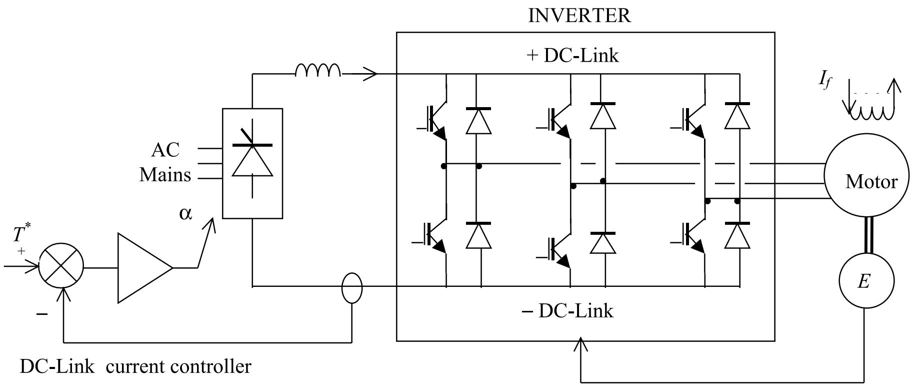


FIGURE 27.34 Schematic of a current-source-inverter–driven synchronous motor.

In the foregoing scheme, the motor can be reversed easily by reversing the sequence of switching of the inverter. It can also be braked regeneratively by increasing the firing angle of the input rectifier beyond 90° while maintaining the dc-link current at the desired braking level until braking is no longer required. The rectifier now returns the energy of the overhauling load to the ac mains regeneratively.

In another scheme, which is preferred for lower capacity drives for which higher dynamic response is frequently sought, phase currents are regulated within the inverter. The inverter typically employs gate turn-off switches, such as the IGBT, and pulse-width modulation techniques, as indicated in Fig. 27.36. Motor currents are sensed and used to close independent current controllers for each phase. Normally, two current

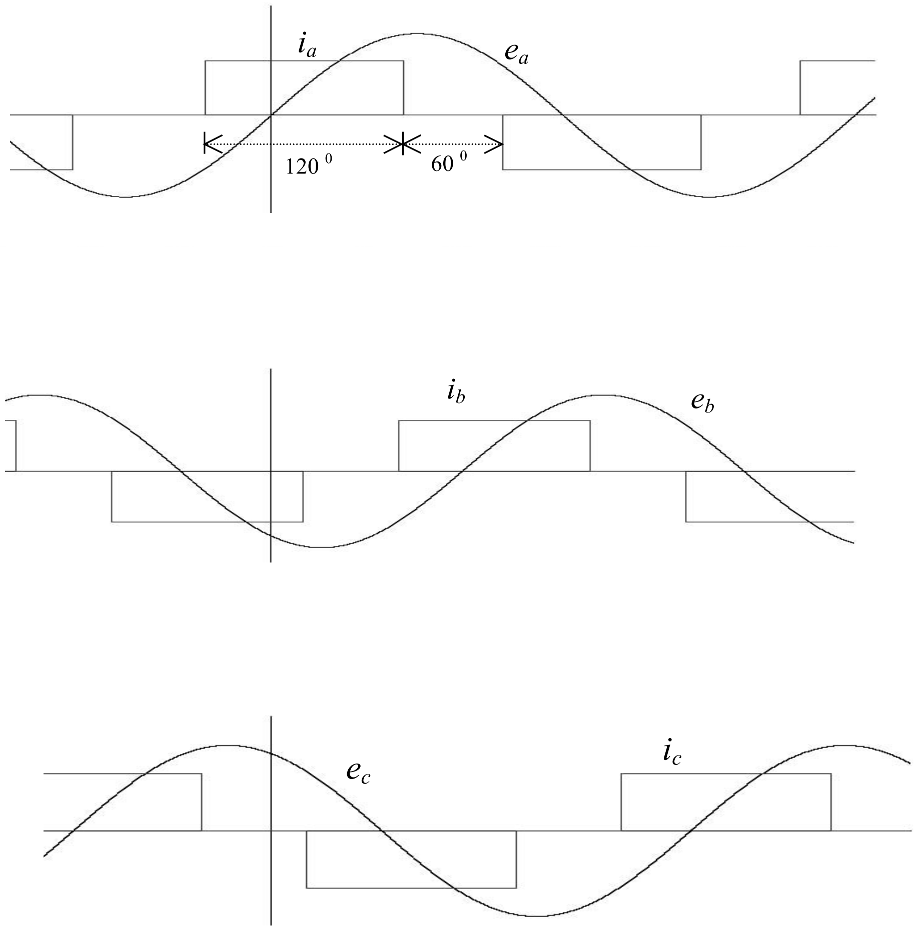


FIGURE 27.35 Current waveform in the dc-link current-source-driven motor.

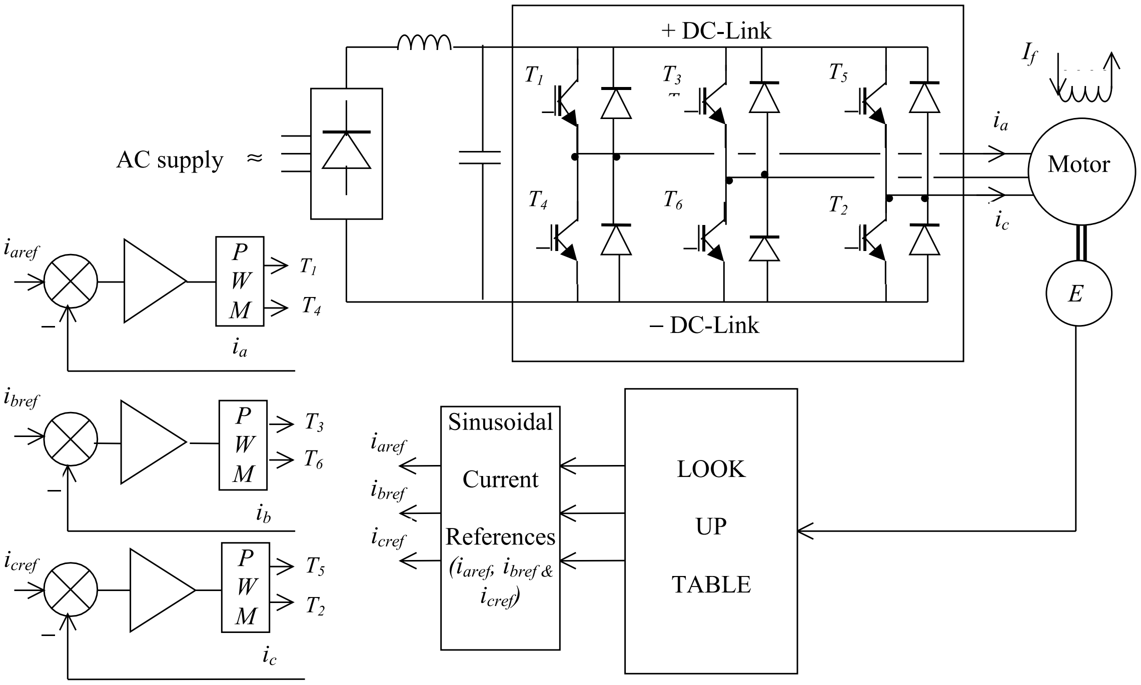


FIGURE 27.36 Control scheme of the SPWM current-source drive.

controllers suffice for a balanced star-connected motor. Three-phase sinusoidal ac currents are supplied to the motor, the amplitude and phase angle of which can be independently controlled as required. The references for the current controllers are obtained from a three-phase current reference generator that is addressed by the feedback of the rotor position. The rotor position is continuously measured by a high-resolution encoder. In this way, the current references, and hence the actual rotor currents, are synchronized to the rotor.

27.4.5 Brushless dc Operation of the CSI Driven Motor

The torque characteristic of the CSI drive scheme of the foregoing section can be easily analyzed using the phasor diagrams shown earlier if the harmonics in the motor current waveform are neglected or if the motor current waveforms are indeed sinusoidal as in the second scheme described earlier. In the following analysis, it is assumed that the supply current waveforms are sinusoidal. It is also assumed that the phase angle of these current sources with respect to the induced voltage in each phase can be arbitrarily chosen.

The phase back-emf and the current waveforms and the phasor diagram of the nonsalient-pole motor are shown in Fig. 27.37. The phase angle γ between the E_f and I phasors and the rms value (or amplitude) of I are determined according to the desired torque and power-factor considerations. The developed torque is found from the phasor diagram to be

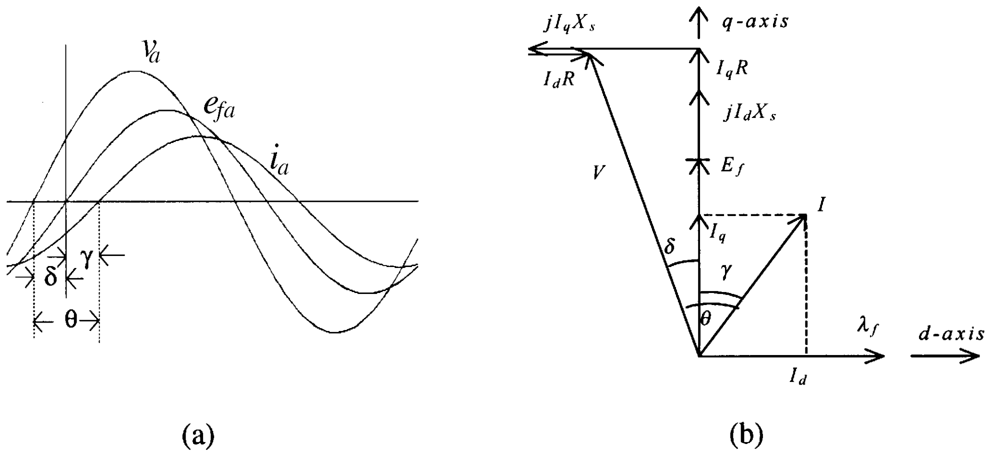
$$T = \frac{3E_f I \cos\gamma}{\omega_r} = K\phi I \cos\gamma \quad \text{Nm} \tag{27.65}$$

If the angle $\gamma = 0°$ is chosen, the familiar dc-motor-like torque characteristic is obtained. It should be noted from the foregoing that the developed torque at any speed is independent of R since a high gain (stiff) current source drive is used. Note also that the ratio E_f/ω at any operating speed is proportional to the amplitude of the stator flux linkage, λ_f, due to rotor excitation. For fixed rotor excitation this ratio is a constant.

Equation (27.65) indicates that the developed torque of a nonsalient-pole synchronous motor can be controlled by controlling the amplitude of the rotor field (field control) or, more conveniently, by controlling the amplitude of the stator phase current. The highest torque-per-ampere characteristic is achieved when $\gamma = 0°$. Note that operation with a fixed γ angle is key to this dc-motor-like torque characteristic.

27.4.5.1 Operation with Field Weakening

If the stator impedance drop is neglected, the maximum E_f is largely determined by the dc-link voltage and, $E_f = K\lambda_f\omega$ implies that speed ω can be increased by decreasing λ_f. Consequently, operation above base speed is normally achieved with field weakening. In this speed range, because of the limited dc-link voltage, the rotor field must be



(a) (b)

FIGURE 27.37 Phasor relationships of CSI-driven motor: (a) back emf and current waveforms; (b) the phasor diagram.

weakened; otherwise, the amplitude of the phase-induced emf will exceed the dc-link voltage and current control will not be effective. Field weakening is a means of keeping this voltage at the rated level for speeds higher than the base speed.

The flux linkage due to the rotor excitation, λ_f, can be adjusted when a variable rotor supply is available. This may also be achieved by demagnetizing the rotor mmf by using the mmf produced by the stator currents. For motors with permanent magnet excitation, the latter is the only means of weakening the λ_f. Referring to the phasor diagram of Fig. 27.38, if I is made to lead E_f, the d-axis component of I, i.e., I_d, will lead E_f by 90°. The mmf due to I_d then opposes the rotor d-axis mmf. The net rotor flux linkage along the q-axis is then given by

$$\lambda_f' = \lambda_f + L_d I_d \tag{27.66}$$

where I_d is negative when I leads E_f. If the airgap is small, the d-axis component of the armature current may reduce the rotor flux to the required extent.

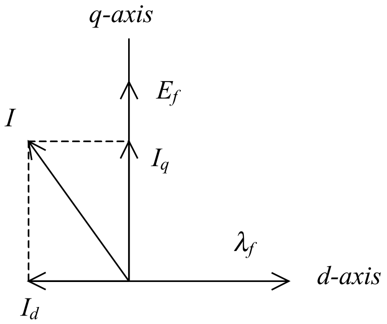


FIGURE 27.38 Field weakening using stator mmf.

27.4.6 Operating Modes

A synchronous motor may driven with various operating characteristics, such as with power factor compensation, with maximum torque per ampere and with field weakening. The power factor at which a synchronous motor operates is an important issue, especially for a large drive. A large angle θ between the input voltage and current to the motor results in a poor power factor. Operation of the synchronous motor with a current source inverter allows interesting power factor compensation possibilities. Consider the following three cases.

27.4.6.1 Case A Operation with *I* Lagging *E*

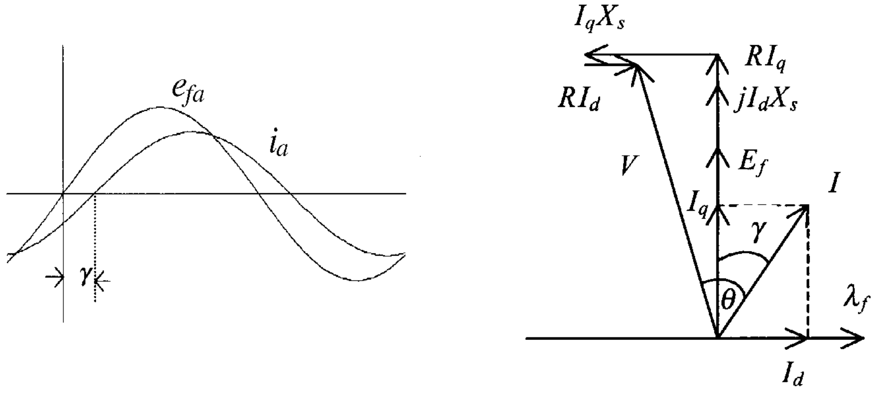
In this case, the motor is underexcited and I lags E_f, by an angle γ, as indicated in Fig. 27.39. The overall power factor in this case is lagging, since I lags V by angle θ. The power factor angle θ is larger than γ. Note that I_d now magnetizes the rotor field.

27.4.6.2 Case B *I* Is in Phase with *E* Maximum Torque per Ampere Operation $\gamma = 0°$

If $\gamma = 0°$ is used, the motor input current i_a is in phase with the back emf e_a, as indicated in the waveforms of Fig. 27.40a. From Eq. (27.65), the developed torque is given by

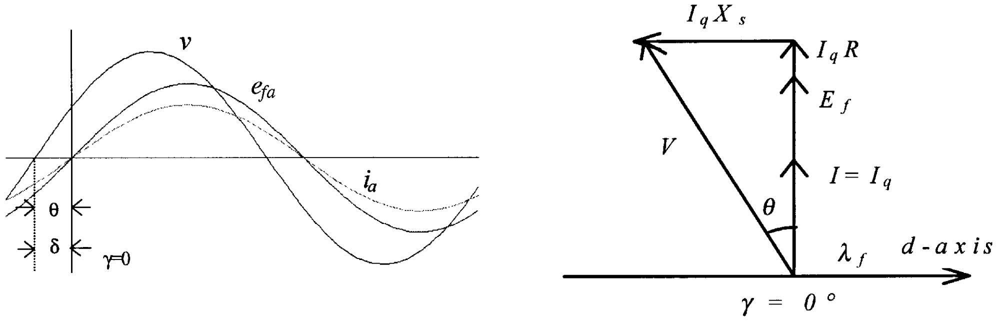
$$T = K\phi I \tag{27.67}$$

Thus, for a fixed rotor excitation, the developed torque is the highest that can be achieved per ampere of stator current I. In other words, if $\gamma = 0°$ is chosen, the drive operates with its maximum torque per ampere characteristic. From the phasor diagram of Fig. 27.40b, it is clear that the input current phasor I phasor now lags the voltage V phasor at the motor terminals. (see the phasor diagram below). Note that the level of E_f,


e_{fa}
i_a
γ
I_qX_s
RI_q
RI_d
jI_dX_s
V
E_f
I
I_q
γ
θ
λ_f
I_d

(a) (b)

FIGURE 27.39 (a) Phase back emf and current waveforms and (b) the phasor diagram with I lagging E_f.


v
e_{fa}
i_a
θ
δ
γ=0
I_qX_s
I_qR
E_f
V
$I = I_q$
θ
λ_f
d-axis
$\gamma = 0°$

(a) (b)

FIGURE 27.40 (a) Phase back emf and current waveforms and (b) phasor diagram for I in phase with E_f.

which is determined by the level of excitation, also determines the angle θ to some extent. Clearly, when maximum torque per ampere characteristic is required, a power factor less than unity has to be accepted.

27.4.6.3 Case C Operation with *I* Leading *E*

If I is chosen to lead E_f, the overall power factor can be higher, including unity, as is indicated in Fig. 27.41. Note that the motor now operates with less than maximum torque per ampere characteristic. Note also that the d-axis component of I now tends to demagnetize the rotor and that operation with field weakening is implied.

With a CSI-driven motor, the amplitude and the angle of the phase current relative to the back emf can be selected according to one of the desirable operating characteristics mentioned above. Additionally, other operational limits such as the inverter/motor current limit, the maximum stator voltage limit, and the maximum power limit can also

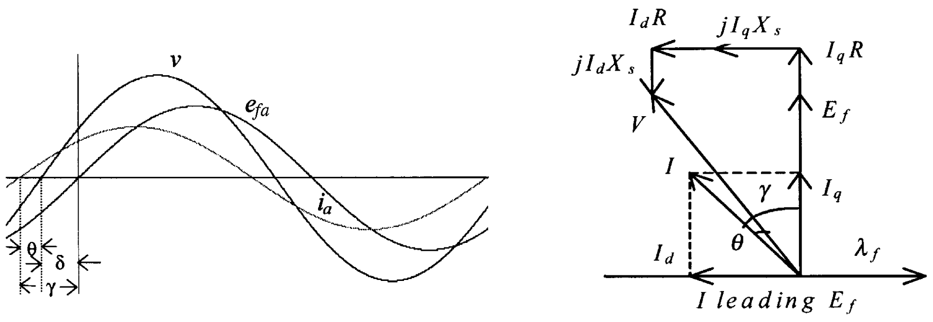

v
e_{fa}
i_a
θ
δ
γ
I_dR
jI_qX_s
I_qR
jI_dX_s
E_f
V
I
γ
I_q
θ
I_d
λ_f
I leading E_f

FIGURE 27.41 Back emf and current waveforms and phasor diagram for I leading E_f.

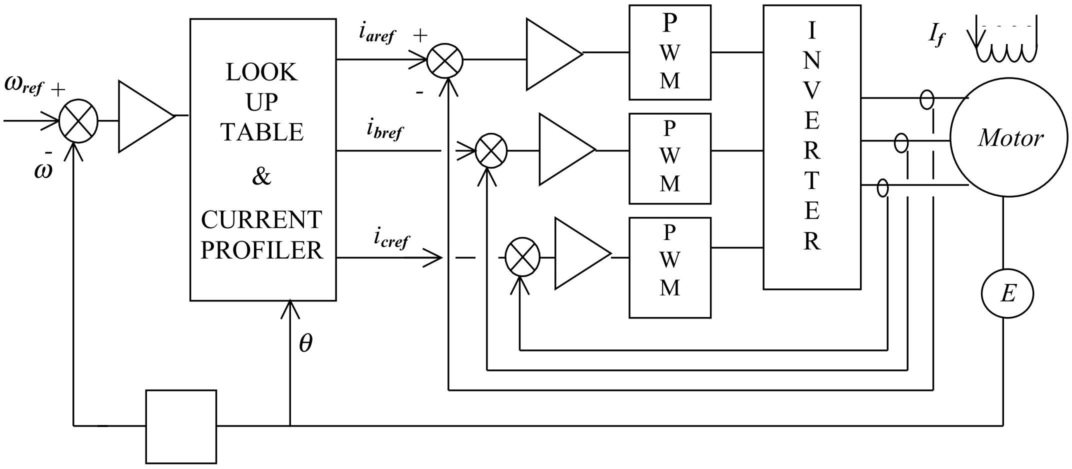


FIGURE 27.42 Structure of a speed-control system with a CSI-driven synchronous motor.

addressed. The amplitude of the stator current I clearly determines the developed torque of the motor. Consequently, the error of the speed controller is used to determine the amplitude of I. The overall control system with an inner torque loop may be described by Fig. 27.42.

27.4.7 Vector Controls

The foregoing controls were based on the steady-state equivalent circuit of the motor. Even though the torque equation (27.65) for a current-source drive evokes vector-control-like relationships, they do not address the dynamics of the current controls as is possible in an orthogonal reference frame. Using an orthogonal set of reference attached to the rotor, a simple set of decoupled, dc-motor-like torque control relationships is readily obtained. Following the transformation technique used in Section 27.3.3, the stator voltage equations of a synchronous motor with fixed rotor excitation in the rotor reference frame are

$$\begin{bmatrix} v_q \\ v_d \end{bmatrix} = \begin{bmatrix} R + pL_q & \omega L_d \\ -\omega L_q & R + pL_d \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} + \begin{bmatrix} \omega\lambda_f \\ 0 \end{bmatrix} \tag{27.68}$$

$$T = \frac{3}{2} P(\lambda_f i_q + (L_d - L_q) i_d i_q) \tag{27.69}$$

where all the quantities in lowercase represent instantaneous quantities in the rotor dq-frame. λ_f is the flux linkage per phase due to the rotor excitation, ω is the electrical angular velocity in rad/s, and P is the number of pole pairs. p is the time derivative operator d/dt. Assuming magnetic linearity, the stator flux linkages are

$$\begin{aligned} \lambda_d &= L_d i_d + \lambda_f \\ \lambda_q &= L_q i_q \end{aligned} \tag{27.70}$$

Note that Eq. (27.68) can be written down directly from (27.31), taking into account fixed rotor excitation so that the third and fourth rows and columns of Eq. (27.31) need to be dropped. Since the reference frame now rotates at the speed of the rotor, $\omega_e = \omega$. The induced back emf due to the fixed rotor excitation occurs in the rotor q-axis and is included in (27.68) as a separate term. Similarly, the torque expression of (27.69) may also be written down from Eq. (27.41), using the flux linkages of Eq. (27.70).

Equations (27.67)–(27.69) are for a salient pole motor for which $L_d \neq L_q$. For a nonsalient-pole motor, L_d is equal to L_q and the developed torque is proportional to i_q only. In either case, the inner torque loop consist of two separate current loops; one for i_d and the other for i_q, as indicated in Fig. 27.43. The i_q current loop generally derives its reference signal from the output of the speed controller and constitutes the inner torque loop. The reference for the i_d current loop is normally specified by the extent of field weakening for which a negative

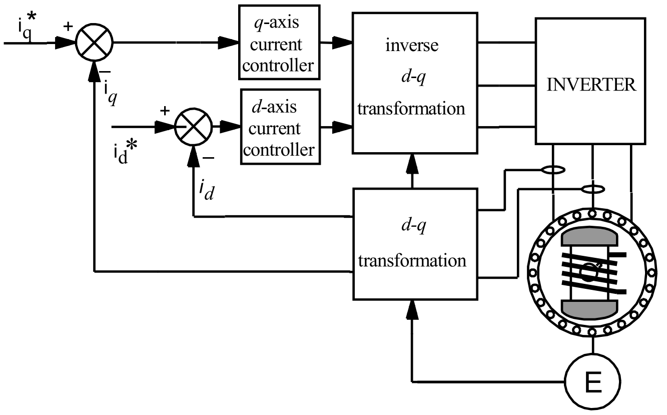

i_q^*
+
–
i_q
+
i_d^*
–
i_d
q-axis current controller
d-axis current controller
inverse d-q transformation
d-q transformation
INVERTER
E

FIGURE 27.43 Inner torque loop of a vector-controlled synchronous motor drive.

i_d reference is used. Otherwise, the d-axis current is maintained at zero. Note that for large synchronous motors with variable external excitation, field weakening is normally applied through adjustment of the rotor excitation, using a spillover signal from the output of the speed controller.

From Eq. (27.68), it is clear that couplings of q- and d-axis voltages exist through the d- and q-axis currents, respectively, and the back emf. During dynamic operation, such coupling effects become undesirable. The coupling effects of d- and q-axis currents and the back emf into q- and d-axis voltages, respectively, can be removed by the feed-forward terms shown in the shaded part of block diagram of Fig. 27.44, which also shows the two current-control loops. The two outputs v_d^* and v_q^* from the decoupled current controllers are transformed to the stator reference frame before being subjected to pulse-width modulators or hysteresis comparators. Note that the current references i_d^* and i_q^* are obtained with due regard for the desired operating and limiting conditions as described in Section 27.4.5.

Under this type of control, which is exercised in the rotor reference frame, the d- and q-axis currents are separately regulated. The purpose of the q-axis current controller is primarily to control the developed torque, especially for the nonsalient-pole motor. For this motor, the d-axis current is normally maintained at zero when the motor is operated below the base speed. The d-axis current may be used to weaken the airgap flux so that the motor operates with a constant-power-like characteristic. It should be noted that field weakening may also be carried out more directly by adjusting the rotor excitation current by using a spillover signal from the speed controller when the base speed is exceeded.

The dynamic response of the drive under the vector control scheme indicated in Fig. 27.44 is the highest possible with a CSI drive. It should also be noted that the dq currents in the rotor reference frame vary only the mechanical dynamics of the rotor. In fact, they are dc quantities when the motor runs at a constant speed. Consequently, the following error (or lag) associated with tracking a sinusoidally time varying current reference, which is the case when current control is exercised in the stator a–b–c reference frame, can be reduced easily by using integral-type current controllers.

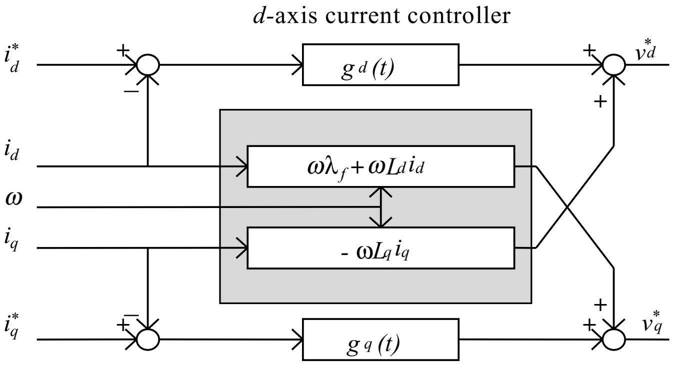

d-axis current controller
i_d^*
+
−
$g_d(t)$
+
+
v_d^*
i_d
$\omega\lambda_f + \omega L_d i_d$
ω
i_q
$-\omega L_q i_q$
i_q^*
+
−
$g_q(t)$
+
+
v_q^*
q-axis current controller

FIGURE 27.44 The d- and q-axis decoupling compensation.

27.4.8 Further Reading

1. W. Leonard, *Control of Electrical Drives.* Springer-Verlag, 1985.
2. J. M. D. Murphy and G. G. Turnbull, *Power Electronic Control of AC Drives.* Pergamon Press, 1988.
3. G. R. Slemon, *Electric Machines and Drives.* Addison-Wesley, 1992.
4. W. W. Novotny and T. A. Lipo, *Vector Control and Dynamics of AC Drives.* Oxford Science Publications, 1996.

27.5 Permanent Magnet ac Synchronous Motor Drives

M. . ah an

27.5.1 Introduction

Since the introduction of samarium–cobalt and neodymium–iron–boron magnetic materials in the 1970s and 1980s, synchronous motors with permanent-magnet excitation in the rotor have been displacing the dc motor in many high-performance applications. The trend is more noticeable in applications requiring high-performance motors of up to a few kilowatts. In low- to medium-power applications, the superior dynamics, smaller size, and higher efficiency of motors with PM excitation in the rotor, compared to all other motors, are well known. Prior to this development, ferrite and alnico magnets were routinely used in small servomotors, with the magnet excitation in the outer stator. Such motors need a brush–commutator assembly to supply power to the armature, which is a problem. Nevertheless, interesting low-inertia, low-armature inductance designs are possible that are desirable for servo applications. One such design is the pancake ironless armature with the commutator–brush assembly directly located on the printed armature. These shortcomings of the commutator–brush are now avoided by locating the magnets in the rotor and by having three-phase windings in the stator that are supplied from an inverter.

The arrangement just mentioned is very similar to a conventional synchronous motor. This is particularly so when the stator windings and the rotor MMF are sinusoidally distributed.

Several rotor configurations of the PM synchronous motor have been developed, of which the important ones are indicated in Figs. 27.45–27.47.

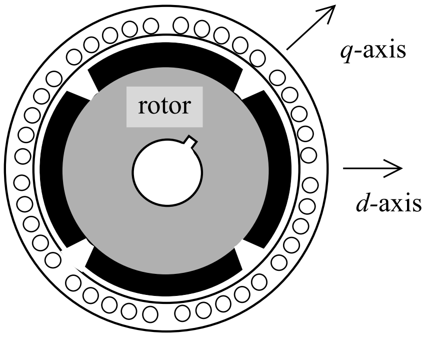


FIGURE 27.45 Schematic of the cross section of a surface-magnet synchronous motor.

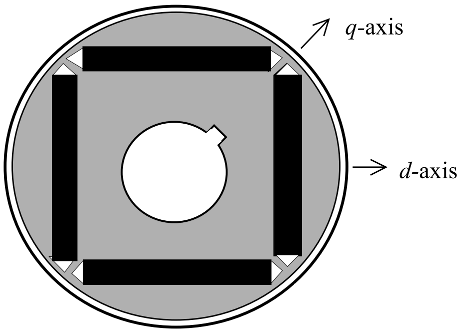


FIGURE 27.46 Schematic of the rotor cross section of an interior-magnet motor.

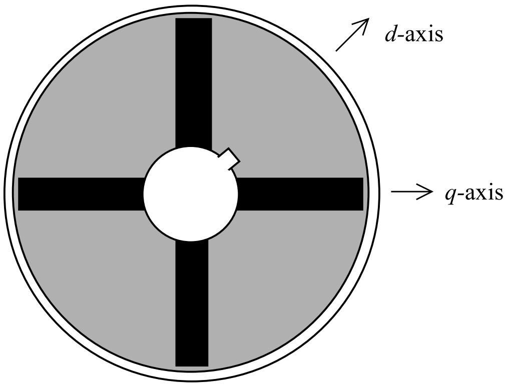


FIGURE 27.47 Schematic of the rotor cross section of a circumferential-magnet motor.

27.5.2 The Surface-Magnet Synchronous Motor

The surface-magnet motor comes with the rotor magnets glued onto the surface of the rotor. An additional stainless steel (i.e., nonmagnetic) cylindrical shell may be used to cover the rotor in order to keep the magnets in place against centrifugal force in high-speed applications. Since the relative permeability of the magnet material is very close to unity, the effective airgap is uniform and large. (The airgap is normally about 8 mm.) Consequently, the synchronous inductances along the rotor d- and q-axes, as indicated in Fig. 27.45, are equal and small (i.e., $L_d = L_q = L_s$). The armature reaction in this type of motor is small.

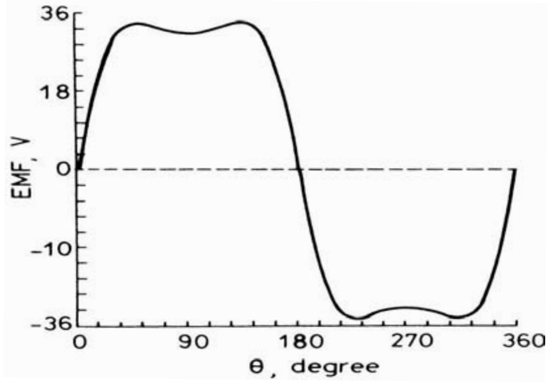


FIGURE 27.48 Back emf of a trapezoidal waveform motor.

The three-phase winding in the stator has sinusoidal distributed windings. In another form, the motor may have trapezoidal distributed winding, and the rotor mmf is also uniformly distributed. Such a motor, often called a brushless dc motor because of its similarity to the inside-out conventional brushed PM dc motor, develops a trapezoidal back-emf waveform as indicated in Fig. 27.48, when it is driven at a constant speed. The back emf waveforms have flat tops for nearly 120° in each half-cycle followed by 60° of transition from positive to negative polarity of voltage and vice versa. These motors are very suitable for variable-speed applications such as spindle drives in machine-tool and disk drives.

27.5.2.1 Control of the Trapezoidal-Wave Motor

Neglecting higher-order harmonic terms, the back emf in the motor phases may be as indicated in Fig. 27.49. Each back emf has a constant amplitude (or flat top) for 120° (electrical) followed by 60° of transition in each half cycle. The developed torque at any instant is given by

$$T = \frac{e_{an} i_a + e_{bn} i_b + e_{cn} i_c}{\omega} \quad \text{Nm} \qquad (27.71)$$

It is readily seen that the ideal current waveform in each phase needs to be a quasi-square waveform of 120° of conduction angle in each half cycle. The conduction of current in each phase winding coincides with the flat part of the back emf waveforms, which guarantees that the developed torque, i.e., $(\sum_{x=a}^{c} e_{xn} \cdot i_{xn}/\omega_r)$, is constant or ripple-free at all times. With such quasi-square current waveforms, a simple set of six opto-couplers or Hall-effect sensors would be required to drive the six inverter switches indicated in Fig. 27.36. The output current waveforms for the three-phase inverter and the switch-

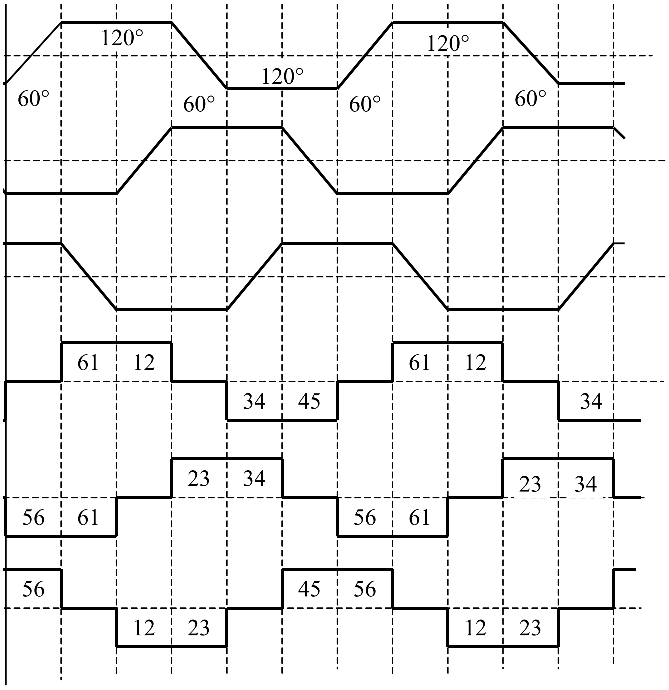


FIGURE 27.49 Back-emf and current waveforms and on states of transistor switches in the trapezoidal-waveform motor.

ing devices that conduct during the six switching intervals per cycle are also indicated in Fig. 27.49. Since only six discrete outputs per electrical cycle are required from the rotor position sensors, the requirement of a high-resolution position sensor is dispensed with. Continuous current control for each phase of the motor, by hysteresis or PWM control, to regulate the amplitude of the motor current in each phase is normally employed. The operation of the brushless dc motor drive is described in detail in Section 27.6.

Even though careful electromagnetic design is employed in order to have perfect trapezoidal back-emf waveforms as indicated in Fig. 27.49, the back-emf waveforms in a practical brushless dc motor exhibit some harmonics, as indicated in Fig. 27.48. If ripples in the back-emf waveforms are significant, then torque ripples will also exist when the motor is driven with quasi-square phase current waveforms. These ripples may become troublesome when the motor is operated at low speed, when the motor–load inertia may not filter out the torque ripples adequately.

A second source of torque ripple in the PM BLDC motor is from the commutation of current in the inverter. Since the actual phase currents cannot have the abrupt rise and fall times as indicated in Fig. 27.49, torque spikes, one for each switching, may exist.

Even though the PM BLDC motor does not have sinusoidal back-emf and inductance variations with rotor angle, the analysis of Section 27.4 in terms of the fundamental quantities will often suffice. The switching of the inverter using the six rotor-position sensors guarantees that the current waveform in each phase always remains in synchronism with the back-emf of the respective phase. Since the quasi-square phase current waveform in each phase coincides with the flat part of the back-emf waveform of the same phase, the angle γ is clearly zero for such operation. Thus, considering fundamental quantities, the motor back-emf and torque characteristics can be expressed by

$$E = K_E \omega \quad \text{volts} \tag{27.72}$$

$$T = K_T I \cos \gamma = K_T I \quad \text{Nm} \tag{27.73}$$

where K_E and K_T are equal in consistent units. Note that E and I are now RMS values of the fundamental components of these quantities.

27.5.2.2 Sensorless Operation of the PM BLDC Motor

In spindle and other variable-speed drive applications, where the lowest speed of operation is not less than a few hundred revs/min, it may be possible to obtain the switching signals for the inverter from the motor back emf, thus dispensing with rotor-position sensors. The method consists of integrating the back emf waveforms, which are the same as the applied phase voltage if the other voltage drops are neglected, and comparing the integrated outputs with a fixed reference. These comparator outputs determine the switching signals for inverter. It may be noted that the amplitude of the back-emf waveforms is proportional to the operating speed, so that the frequency of the comparator outputs increases automatically with speed. In other words, the angle γ and the current waveform relative to the back emf waveform in each phase remains the same regardless of the operating speed. Integrated circuits are available from several suppliers that perform this task of sensorless BLDC operation satisfactorily, covering a reasonable speed range.

27.5.3 The PM Sine-Wave Motor

The PM sine-wave motor, which may also have magnets on the rotor surface or buried inside the rotor (as in the interior-magnet motor of Fig. 27.46), has sinusoidally distributed windings. The airgap flux distribution produced by the rotor magnets is also sinusoidal, arranged through magnet shaping. Consequently, the back-emf waveform of each phase is also a sinusoidal waveform, as indicated in Fig. 27.50, when the motor is driven at a constant speed.

It should be noted, however, that with magnets mounted on the rotor surface, the effective airgap is large and uniform so that $L_d = L_q = L_s$. Because of the large equivalent airgap, these inductances are also small, and consequently the armature reaction is small. As a result, this motor essentially operates with fixed excitation, and there is hardly any scope for altering the operating power factor or the rotor mmf, once the motor and its drive voltage and current ratings have been selected.

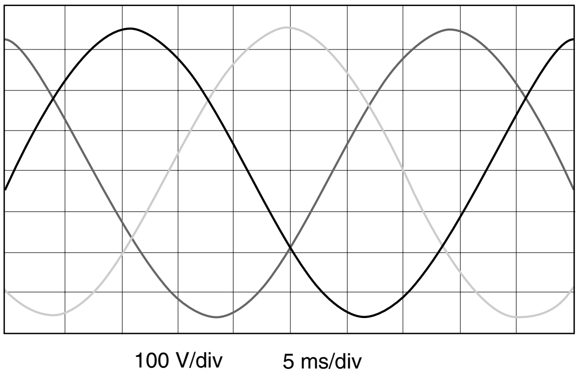


FIGURE 27.50 Back emf waveforms of a sine-wave PM motor. Speed = 1815 rev/min.

The PM sine-wave interior-magnet motor, which comes with magnets buried inside the rotor as indicated in Figs. 27.46 and 27.47, has an easier magnetization path along the rotor q-axis, so that $L_q > L_d$. The small airgap implies that the inductances L_d and L_q may not be small, and hence may allow considerable scope for field weakening.

If the sine-wave motor is supplied from an SPWM inverter, the analyses and vector diagrams of this motor are no different from those in Section 27.4 for the nonsalient-pole and salient-pole synchronous motor drives. The surface-magnet motor is more akin to the nonsalient-pole motor, since $L_d = L_q = L_s$, whereas the interior magnet motor is more akin to the salient-pole motor because of the d- and q-axes inductances being unequal. Thus, the equations in Section 27.4 will apply equally well for this motor, both in the steady state and dynamically and for both voltage- and current-source supply.

27.5.3.1 Control of the PM Sine-Wave Motor

The sinusoidal back-emf waveforms imply that the three-phase motor must be supplied with sinusoidal three-phase currents if a dc-motor-like (or vector-control-like) torque characteristic is desired, as was found in Section 27.4. For such operation, the phase currents must also be synchronized with the respective phase back-emf waveforms, in other words, with the rotor dq-reference frame. This implies operation with a specified γ angle. Two implementations are possible.

In one scheme, the stator currents are regulated in the stator reference frame and the stator current references are produced with reference to the rotor position, as indicated in Fig. 27.51. The rotor position θ is continuously sensed and used to produce three sinusoidal current references of unit amplitude. The phase angle γ of the references relative to the respective back-emf waveforms is usually derived from the speed controller, which defines the field-weakening regime of the drive. The operating power factor of the drive may also be addressed using the γ angle control, as explained in Section 27.4.5. The amplitudes of these references are then multiplied by the error of the speed controller in order to produce the desired torque reference. In this way, both the RMS value I of the phase current and its angle γ with respect to E_f can be adjusted independently (which is equivalent to independent dq-axis current control). Three PWM current controllers are indicated, but two suffice for a balanced motor. Other types of current controllers, such as hysteresis controllers, may also be used.

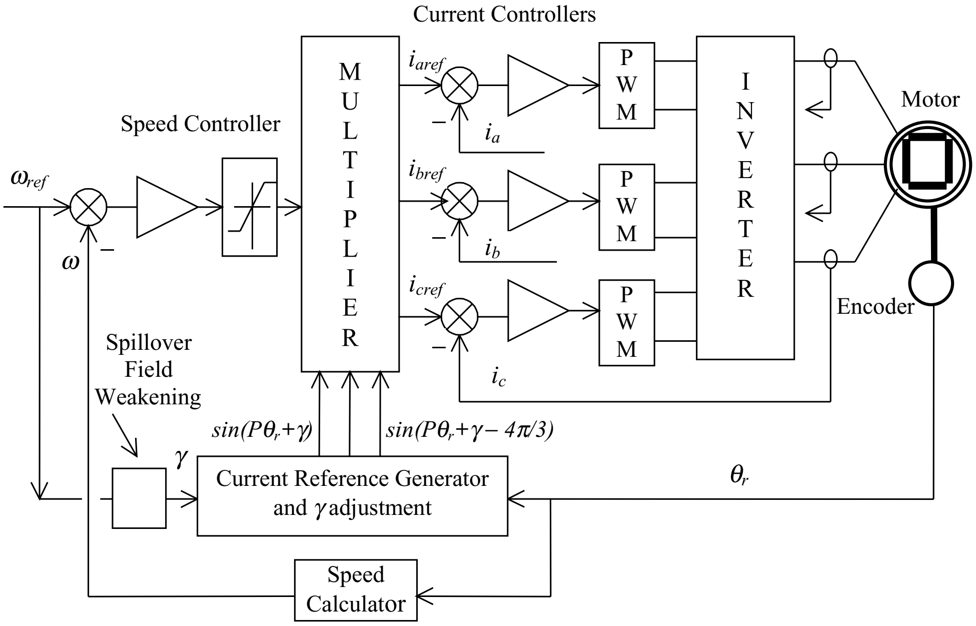


FIGURE 27.51 Speed-controlled drive with the inner torque loop via current control in the stator reference frame.

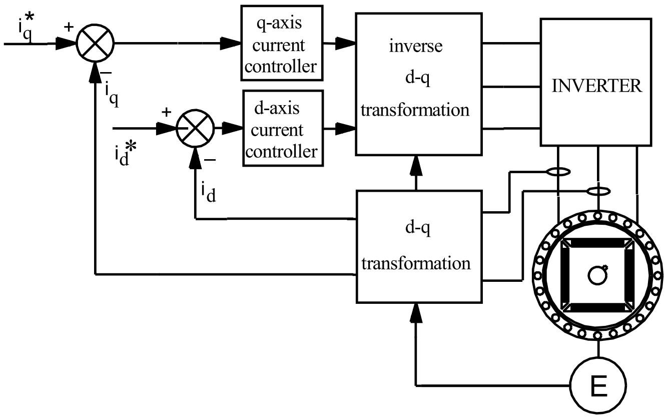

i_q^*
+
−
i_q
+
i_d^*
−
i_d
q-axis current controller
d-axis current controller
inverse d-q transformation
d-q transformation
INVERTER
E

FIGURE 27.52 Block diagram of current-controlled drive.

In the second scheme, the motor currents are first transformed into the rotor *dq*-reference frame using continuous rotor-position feedback, and the measured rotor *d*- and *q*-axis currents are then regulated in the rotor reference frame, as indicated in Fig. 27.52. The main advantage of regulating the stator currents in the rotor reference frame, compared to the stator reference frame as in the first scheme, is that current references now vary more slowly and hence suffer from lower tracking error. At constant speed, the stator current references are in fact dc quantities as opposed to ac quantities, and hence the inevitable tracking errors of the former scheme are easily removed by a integral type controller. The other advantage is that the current references may now include feed-forward decoupling so as to remove the cross coupling of the *d*- and *q*-axis variables as shown in the motor representation of Fig. 27.44. The latter scheme is currently preferred, since it allows more direct control of the currents in the rotor reference frame.

It should be noted that continuous transformations to and from rotor *dq*-axes are required; hence the rotor-position sensor is a mandatory requirement. Rotor-position sensors of 10-to 12-bit accuracy are normally required. This is generally viewed as a weakness for this type of drive.

The general torque relationship of a sine-wave motor supplied from a current-source SPWM inverter is given by Eq. (27.69), which is rewritten here

$$T = \frac{3}{2}P(\phi_f i_q + (L_d - L_q)i_d i_q) \tag{27.74}$$

Precise control of the developed torque control requires that both i_d and i_q be actively controlled in order to regulate it to the level determined by the error of the speed controller. For the surface-magnet synchronous motor, the large effective airgap means that $L_d \approx L_q$, so that i_d should be maintained at zero level. This implies that the i_d current reference in Fig. 27.52 should be kept zero. For the interior magnet motor, $L_q > L_d$, so that i_d and i_q have to be controlled simultaneously to develop the desired torque. A few modes of operation are possible.

27.5.3.2 Operating Modes

. . . . ***Operation with Maximum Torque per Ampere (MTPA) Characteristic*** In this mode of control, the developed torque T per ampere of stator current is the highest for a given rotor excitation. The combination of i_d and i_q that develops the maximum torque per ampere of stator current is indicated in Fig. 27.53. The reference signal for the inner

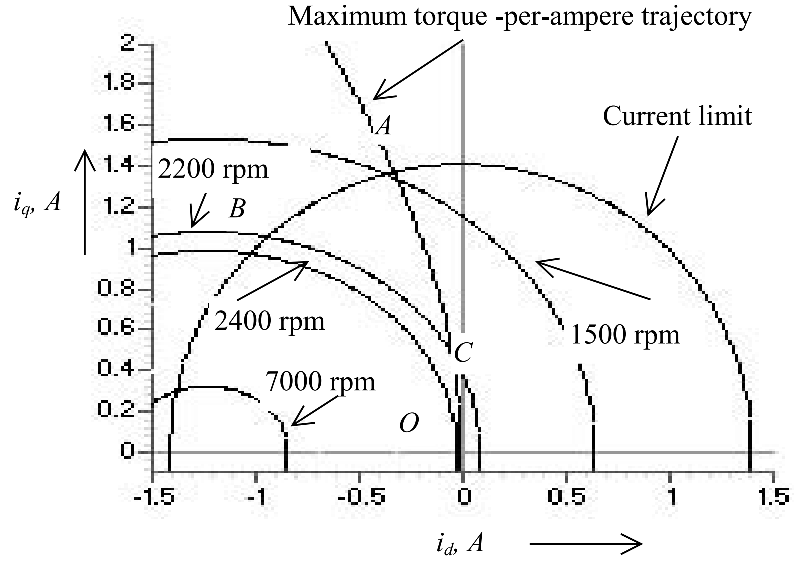


FIGURE 27.53 i_d–i_q trajectories for the maximum torque-per-ampere characteristic and for maximum voltage and current limits of an interior PM motor.

torque loop normally determines the i_q reference; the i_d reference is given by

$$i_d = \frac{\lambda_f}{2(L_q - L_d)} - \sqrt{\frac{\lambda_f^2}{4(L_q - L_d)^2} + i_q^2} \tag{27.75}$$

It should be noted that with $i_d = 0$, this mode of operation is achieved for the surface magnet motor.

. . . . *Operation with Voltage and Current Limits* The maximum current limit of the motor/inverter, I_{smax}, is normally imposed by setting appropriate limits on i_d and i_q such that

$$i_d^2 + i_q^2 \leq I_{smax}^2 \tag{27.76}$$

Equation (27.75) defines a circle around the origin of the i_d–i_q plane.

The available dc-link voltage to the inverter places an upper limit of the motor phase voltage, V_{smax}, given by

$$V^2 = V_d^2 + V_d^2 \leq V_{\max}^2 \tag{27.77}$$

$$(L_q i_q)^2 + (L_d i_d + \lambda_f) \leq \left(\frac{V_{am}}{\omega}\right)^2 \tag{27.78}$$

where the stator voltages v_d and v_q are expressed in the rotor reference frame, as in Eq. (27.68). Equation (27.78) is obtained from the voltage equation of (27.68) when the phase resistance R is neglected. Equation (27.78) defines elliptical trajectories that contract as speed increases. All three modes of operation are included in Fig. 27.53.

. . . . *Operation with Field Weakening* This mode of operation is normally required for operating the motor above the base speed. A constant-power characteristic is normally desired over the full field-weakening range. For a given rotor excitation of λ_f and developed power of P_0, the developed torque T and the net rotor flux linkage required for constant-power operation can be determined. From this, the limiting values for i_d and i_q, which further constrain the allowable i_d–i_q trajectory as is also indicated in Fig. 27.53, can be determined.

The operating modes described in the preceding section are normally included in a trajectory controller that generates the references for i_d and i_q continuously, as indicated in Fig. 27.54.

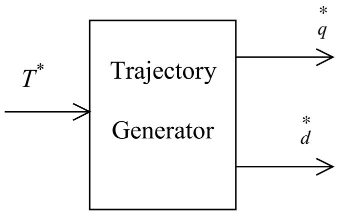


FIGURE 27.54 i_d and i_q trajectory generation satisfying the desired operating modes.

27.5.4 Further Reading

1. T. J. E. Miller, *Brushless Permanent Magnet and Reluctance Motor Drives.* Oxford Science Publications, 1989.
2. "Performance and Design of Permanent Magnet AC Motor Drives", Tutorial course, IEEE IAS Society, 1989.
3. R. M. Crowder, *Electric Drives and Their Controls.* Oxford Science Publications, 1995.

27.6 Permanent-Magnet Brushless dc BLDC Motor Drives

D. Patterson

27.6.1 Machine Background

Anyone studying electric machines would be aware that the classical synchronous machine offers the possibility of the very highest efficiencies. These machines have the power-carrying conductors in the stationary part; therefore, there is no need to transfer high power through a brush system. The field is provided on the rotating part either by an electromagnet, which does require some very low-power brushes, or at best by a permanent magnet with no power requirements at all.

This is clearly better than the traditional dc machine with high-power brushes dand rotating conductors, which also provide a very poor path for heat to get away from the rotor under overload conditions. You might well then ask, "why did we use so many of them?" It was of course because the dc machine offered the ability to control the speed fully and easily, which the synchronous machine, when running from the mains at a fixed frequency, definitely could not do. Thus, for example, all electric trains and trams built up to the 1980s, many of them still in service, use brushed dc motors.

The induction machine, the workhorse of industry, is quite efficient, but because of the need to carry magnetizing current in the stator as well as load current, and the existence of slip, it cannot be as good as the synchronous machine. It also innately has a very limited speed range.

All this changed with the advent of inexpensive, reliable power electronics. Quite suddenly power-electronics engineers had the ability to vary both the frequency and the amplitude of an ac supply and thus to provide the holy grail of variable-speed ac motors. This was first applied to induction machines, with the simplest form of open-loop control. The complexity of control for synchronous machines added substantially to the cost and was not so appealing. Today the thought of putting a digital signal processor (DSP) or a microcontroller in a small motor controller is no longer as daunting as it was 10 years ago, so the distinction between the complexity of a controller for induction machines and synchronous machines has almost disappeared.

Although power electronics radically changed our attitudes towards electric machine design and operation, there was a second very important development that arrived on the scene at almost the same time; the appearance of very powerful rare-earth permanent-magnet materials.

The first rare-earth magnet material was samarium–cobalt, used in very special applications such as space and defense, but it was then, and still is, very expensive. Neodymium–iron–boron (NdFeB) came next with even higher energy product. Energy product is a measure used to quantify the effectiveness of magnets. NdFeB began expensively, but has continued to drop in price at a spectacular rate and recently became cheaper than ferrites in term of dollars per unit of energy product. Thus, all the machines discussed here are permanent magnet (PM) machines, in general using NdFeB magnets.

27.6.1.1 Clarifying Torque vs Speed Control

As is well understood, given a fixed magnetic flux level, the magnitude of the current in a motor determines the magnitude of the torque out of the machine. In a general application if a torque is set, the speed is determined by the load. This is what happens when driving an automobile. The throttle or accelerator varies the torque. The speed can be very slow or very high for the same foot position, depending on the road conditions and vehicle motion history, even if the vehicle is in the same gear. This principle of torque control rather than speed control is fundamental to the operation of electric machines. When speed control is required in PM BLDCMs, it is usual to implement torque control, with an extra outside control loop, like a cruise control in an automobile, to use the torque control to deliver speed control. So from here on the discussion will describe torque control for the variable speed motor.

27.6.1.2 Permanent-Magnet ac Machines

There are two quite different types of permanent-magnet ac machines, actually looking very similar in their physical realization but dramatically different in their electrical characteristics and in the way in which they are controlled.

. . . . ***Permanent-Magnet Synchronous Machines*** These are simple extensions of the classical synchronous machine, where all of the voltages and currents are designed to be sinusoidal functions of time, as they are in the synchronous machine when used as a supply generator. These machines are known as permanent-magnet synchronous machines (PMSMs) or brushless ac machines and are discussed elsewhere in this book. Although the application of sinusoidal waveforms everywhere is comforting to many and does result in less acoustic noise, fewer ‘stray losses,” etc., there is in general a requirement to know the exact rotor angular position at every instant of time, with an accuracy on the order of 1°. This knowledge is then used to shape the current waveforms to be sure that they are in phase with the back emf of the windings. Although much research is going on to run these machines without position sensors, the reality in the workplace today is that a relatively expensive shaft-position encoder is needed with a PMSM in order to control it electronically.

. . . . ***Permanent-Magnet Brushless dc Machines*** A very much simpler possibility has emerged, which also gives the benefits of smooth torque and rapid controllability. This results in smaller minimum machine size, yielding maximum machine power density.

For this variant, the current waveforms and the back emf waveforms are trapezoidal rather than sinusoidal. In this case the machine is known as a permanent-magnet brushless dc machine (PMBDCM), with waveforms as shown in Fig. 27.55.

27.6.1.3 Brief Tutorial on Electric Machine Operation

The operation of electric machines can be explained in a variety of ways. Two possible and different methods are as follows:

1. Using an understanding of the interaction of magnetic fields and the tendency of magnetic fields to align. This tendency to align is what provides the force that makes a compass needle swing around until it aligns with the earth’s magnetic field.
2. Using the physical principle that “a current-carrying conductor in a magnetic field has a force exerted on it.” This force is commonly known as the Lorentz force.

The difference between the two explanations is that the first method gives better “physical pictures.” However, when one gets a little more serious, wanting to put in numbers, the force equations, although not greatly more difficult, are a little more challenging as they involve vector cross products.

With the second method, once the principle is accepted, there is a particularly simple scalar version of the force

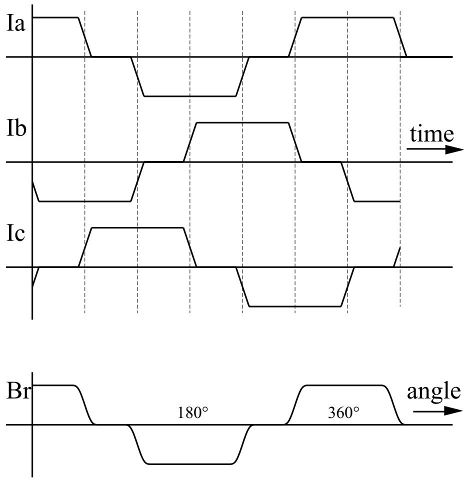


FIGURE 27.55 Phase currents as functions of time and the flux density on the surface of the rotor as a function of angular position for a typical PMBDCM.

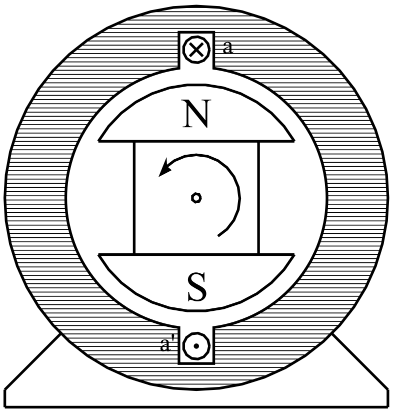


FIGURE 27.56 A simple motor with a single coil in the stator and a permanent-magnet rotor.

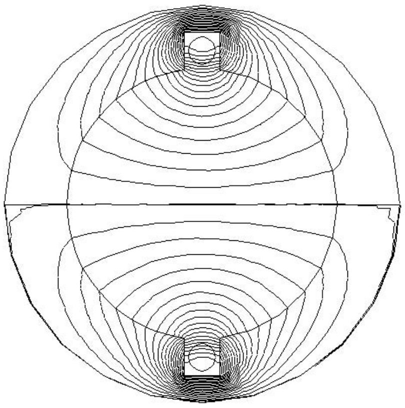


FIGURE 27.57 A computer-generated magnetic field for current in the windings and a stator; the stator is made of electrical steel.

equation that very rapidly and simply gives numeric answers. The directions of the force, current, and motion are all orthogonal, i.e., at right angles, and a formal exposition would again use a vector cross product. The familiar force equation, $F = BLI$, can be used, where F is the force in newtons, B is the flux density in teslas, L is the length of the conductor in meters, and I is the current in amperes.

Consider the simple machine of Fig. 27.56. The rotor is a magnet with a north and a south pole, and there is a coil of wire in the slots in the stator. Current is shown going into the conductor called **a** at the top of the stator and coming out of the conductor called **a**′ at the bottom. To simulate a real machine more closely, one should imagine putting a one-turn "coil" of wire into the slot, with a connection made at the back of the machine to connect the top wire to the bottom, so that when applying a positive voltage is applied to the top wire and a negative voltage to the end of the coil (the bottom wire), current will flow in at the top and out at the bottom as discussed previously.

. . . . ***Method*** If the current is flows into the top and comes out of the bottom as marked, then according to the right-hand rule magnetic flux will be forced to go through the center of the coil from right to left, creating a north pole on the left. The flux will then double back through the iron frame of the motor to arrive back at the south pole on the right.

Figure 27.57 shows a computer-generated magnetic-field plot. This was produced using finite element analysis and modeling the stator as electrical steel, the volume in the center as air, and injecting current into the coil. If the permanent-magnet rotor is then put inside the stator of Fig. 27.57, the rotor will align by rotating 270° counterclockwise.

. . . . ***Method*** In this case, looking at Fig. 27.58, the conductor **a** will be immersed in a quite dense field produced by the magnets, with the flux lines going up the page in the rotor, across the airgap into the steel of the stator, and heading down the stator to jump back across the lower airgap to return to the south pole. If a current is directed into the upper conductor and out of the bottom as before, it will produce forces. Applying the direction rules associated with the Lorentz force, the force on the conductor will be to the right at the top and to the left at the bottom. Invoking Newton's third law, which states that action and reaction are equal and opposite, it is clear that if the wire is fixed, as it is, then there will be a force on the rotor to the left at the top and to the right at the bottom; thus, the rotor will move counterclockwise as before.

27.6.2 Electronic Commutation

If the rotor of Fig. 27.58 moves, then to keep it rotating in the same direction, sooner or later the current in the conductors must be reversed. The time at which that needs to be done is when the rotor has moved to an almost aligned position. Thus, it is not really a matter of time, but rather of rotor position. Since the rotor is a permanent magnet, it is a very simple matter to determine at least where the physical pole edges are, using simple, reliable, and inexpensive Hall-effect (HE) sensors. These are small semiconductor devices that respond to magnetic flux density. (There are many ways to sense the

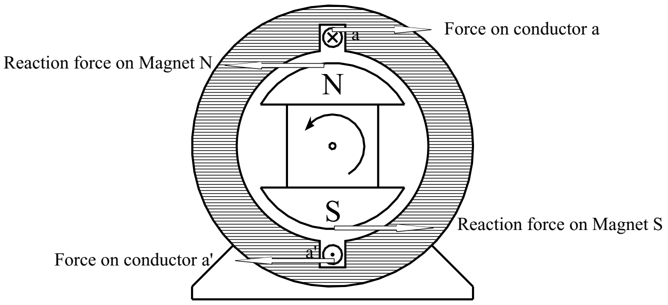


FIGURE 27.58 Lorentz forces on conductor and rotor of a simple machine.

position of the rotor; however, the remainder of this exposition will stay with the HE sensor for simplicity.)

A very simple motor, relying on the inertia of the rotor for continuous rotation, could have a control circuit which sensed when the rotor magnet was horizontal and then reversed the current in **aa**′ of Fig. 27.58.

The traditional "H" bridge switching circuit shown in Fig. 27.59 does that very effectively. Switch drive logic must ensure that either S1 and S4 are on or S2 and S3 are on, and never S1 and S2 simultaneously, or S3 and S4 simultaneously. This simultaneous operation would provide a short circuit. When this happens because of errors in the switch-drive signal it is called "shoot-through." There are generally important parts of the switch drive signal logic, discussed later, that try to make this impossible in normal operation.

In real motors the permanent-magnet rotor field does not change instantaneously from north to south as the rotor rotates, so there would be reasonably large angles over which torque could not be effectively produced. Also, more coils are put in so that the space of the machine frame is used more efficiently.

The use of three "phases," as in Fig. 27.60, is very common. There are many things that balance naturally in a three-phase system, and it is the simplest system with which it is possible to develop constant and unidirectional torque at all times and positions.

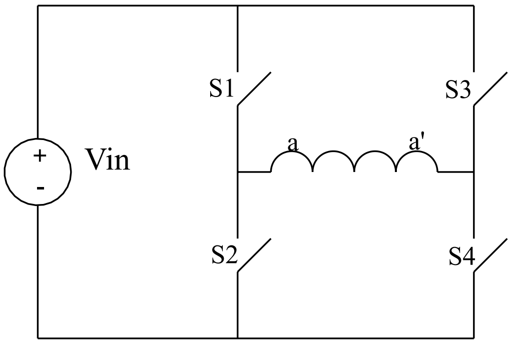


FIGURE 27.59 An "H" bridge circuit that can reverse the current through **aa**′, as drawn with mechanical switches.

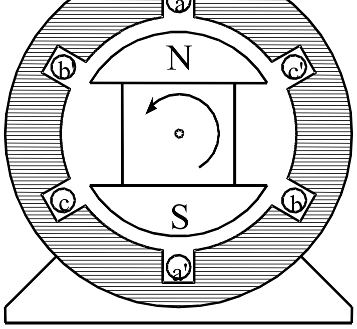


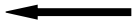
FIGURE 27.60 The physical layout of a three-phase PM BLDC motor.

A very common method has developed, known as "six-step switching". In this system three phases are used, and connected in a star shape. There is a space between each of the magnet poles on the rotor and two phases are activated at any one time, the third "resting" as the space between the magnet poles passes over it.

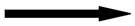
Although the motor in Fig. 27.60 looks just like a three-phase synchronous machine, its operation is rather different. As just stated, the windings are invariably star-connected, as shown in Fig. 27.61.

27.6.2.1 Six-Step Switching Explained

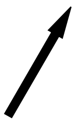
Consider the coil **aa**′, as shown in Fig. 27.60 and also diagrammatically in Fig. 27.61. Current driven into the **a** terminal, coming out of the **a**′ terminal, will produce, as discussed before, flux from left to right, as shown here.



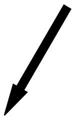
Obviously, if the current direction in **aa**′ is reversed, the flux will be:



Similarly if current is driven into **b** and out of **b**′, flux will result:



And if it is reversed,



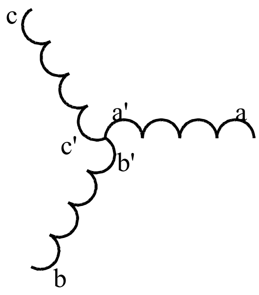
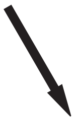
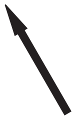


FIGURE 27.61 The schematic connection of the windings shown in Fig. 27.60.

Finally, if current is driven into **c** and out of **c**′, flux will result:

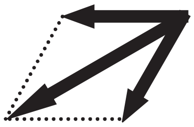


And if it is reversed,



The permanent magnet rotor would tend to align with the flux arrow shown in each of the states just shown, as discussed in Section 27.6.1.3.1.

Now if the motor is wired in a star as shown in Fig. 27.61 and a steady current is driven into **a** and out of **b**, the first and the fourth of the cases just shown occur at the same time. They add to produce a resultant,



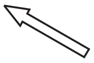
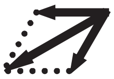
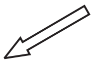
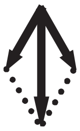
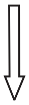
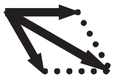
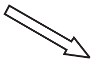
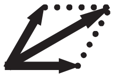
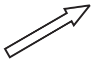
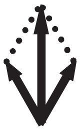
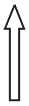
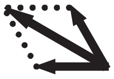
and the rotor will tend to align with this resultant.

The Hall-effect sensors are positioned so that just as the rotor gets to this point, another arrangement of the windings is energized, and the rotor is pulled around another 60°. The rotor never quite achieves its desired position

If a controller has input power from positive and negative of a dc supply and outputs to the terminals **a**, **b**, and **c** only, then the sequence of connections shown in Table 27.2 below will produce the resultant flux directions as shown, providing continuous rotation.

The switching of Table 27.2 is simply achieved by a variant of the "H" bridge, as shown in Fig. 27.62. This process of switching current into different windings is called commutation and is the equivalent of the sliding brush contacts in a traditional brushed dc machine.

TABLE 27.2 Sequence of connections that results in counterclockwise continuous rotation of the rotor of the PM BLDC motor of Fig. 27.60

When Rotor is at This Position, Connections are Made as at Right	Terminal **a**	Terminal **b**	Terminal **c**	Flux Directions
	Current in	Current out	Zero	
	Zero	Current out	Current in	
	Current out	Zero	Current in	
	Current out	Current in	Zero	
	Zero	Current in	Current out	
	Current in	Zero	Current out	

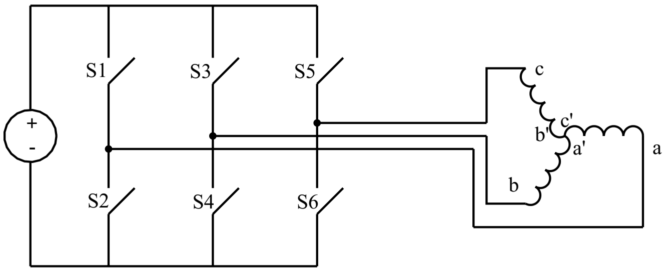


FIGURE 27.62 The switching circuit used for commutation of a PM BLDC motor.

27.6.3 Current/Torque Control

The preceding discussion has been about current in the windings rather than voltage across them. In very simple, very small brushless dc machines, such as the one in the muffin fan in a computer power supply, voltages are connected directly to the windings. For these small motors the resistance of the windings is relatively high, and this helps limit the actual current that flows and swamps inductive effects.

There is an extra difficulty that must be addressed with high-performance, high-efficiency, well-made machines and it adds another layer to the control of the motor. Such machines can easily be designed with very low-resistance windings. It is not uncommon to have windings for a 200-V machine at the 20-kW level with winding resistances of less than 0.1 Ω.

When starting, or at a low speed, the current in a winding is limited only by the very low resistance, and for the machine in this example, by Ohm's law, $I = E/R$ would result in more than 2000 A

The most common requirement is for a steady current in the windings, to provide a steady torque. There is always a back emf generated in the windings whenever the motor is rotating, which is proportional to speed and subtracts from the applied voltage. Thus, currents cannot be determined just by terminal voltage. The winding does, however, have inductance. Whenever copper conductors are put in coils in an iron structure, particularly if there are low-reluctance magnetic paths with only small airgaps, the creation of quite large inductances cannot be avoided. These are used to very good effect.

The nature of inductance is that when a voltage is applied to an inductor, instantaneous current does not result; rather, the current begins to increase and ramps up in a quite controlled fashion. If the voltage across the inductor is reversed, the current does not immediately reverse; rather, it ramps down, will go through zero, and reverses if the reversed voltage is left there long enough. However, if the voltage is alternated by switching rapidly, as can be done with power electronics, the current can be controlled to ramp up and ramp down either side of a desired current, staying within any determined tolerance of that desired current.

Figure 27.63 looks very like the simple H-bridge commutation circuit, but is performing a very different function. It is controlling the current amplitude to stay within a desired band. If S1 and S4 are turned on, then the current will begin to increase from left to right in the winding. The current sensor in the circuit detects when the current reaches a value of half the hysteresis band of the comparator above the desired current level and initiates turn-off of S1 and S4 and turn-on of S2 and S3. (If they were all turned off at once, the inductive nature of the circuit would produce very high voltages, which would cause arcing in mechanical switches, or breakdown and failure of semiconductor switches.) The current then begins to decrease a small amount, down to half the hysteresis band of the comparator below the desired current level, and then the switches reverse again. Thus, a desired current level is achieved, with an arbitrarily small triangular ripple superimposed, as shown in Fig. 27.64.

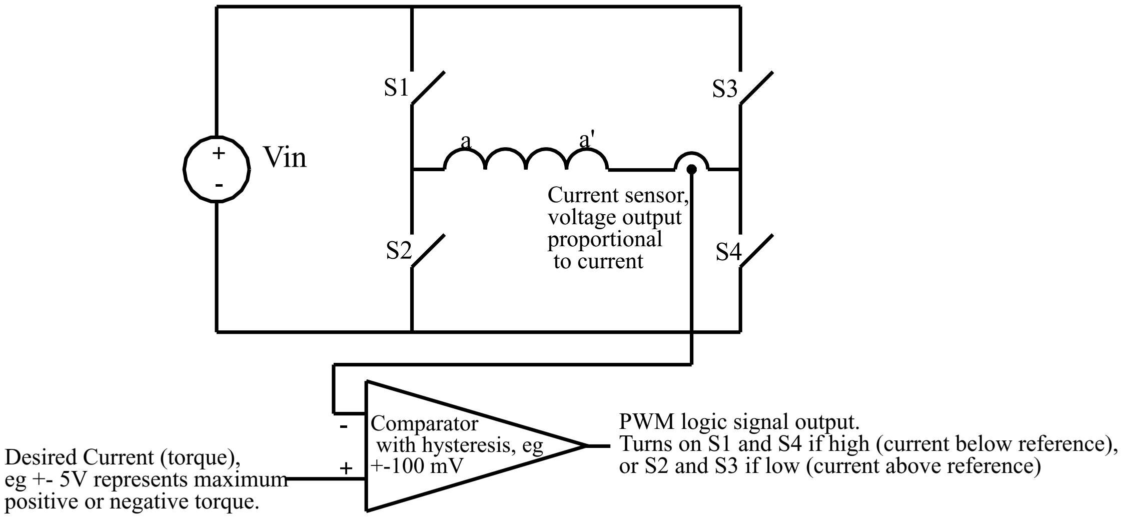

S1
S3
+
-
Vin
a
a'
Current sensor, voltage output proportional to current
S2
S4
-
+
Comparator with hysteresis, eg +-100 mV
Desired Current (torque), eg +- 5V represents maximum positive or negative torque.
PWM logic signal output.
Turns on S1 and S4 if high (current below reference), or S2 and S3 if low (current above reference)

FIGURE 27.63 Hysteresis-band current control using pulse-width modulation (PWM).

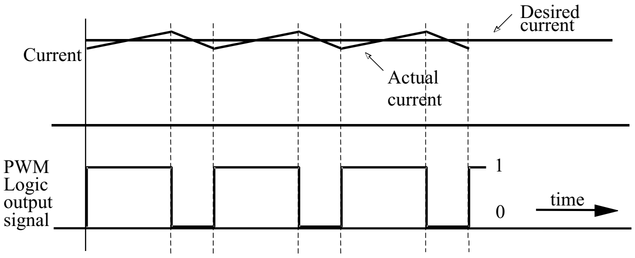


FIGURE 27.64 Hysteresis-band current control and PWM waveforms.

The general process of controlling by switching a voltage fully on or fully off at high speed is called pulse-width modulation (PWM), and the specific method of current control achieved here with PWM is called hysteresis band current control (HBCC). Of course, to keep this current ripple small, the switching may need to be very fast, but with modern semiconductor switches there is no great problem up to 100 kHz for small machines and typically above 15 kHz for acoustic noise reasons, for machines rated up to several hundred kilowatts.

A perceived "drawback" of HBCC is that the switching frequency is determined by circuit inductance, the width of hysteresis band, the back emf, and the applied voltage, ranging very widely in normal operation. It is not difficult, but it is a little more complicated, to use a fixed frequency and a linear analog of the current error to modify the pulse width of the PWM signal.

27.6.3.1 Switching Losses

There is a practical limit to how often semiconductor switches can be operated. At every change of state, if the switch is carrying current as it is opened, then as the voltage rises across the switch and the current through it falls, there is a short pulse of power dissipated in the switch. Similarly, as the switch is closed, the voltage will take some time to fall and the current will take some time to rise, again producing a pulse of power dissipation. This loss is called switching loss. Fairly obviously, it will represent a power loss proportional to the switching frequency, and so the switching frequency is generally set as low as it can be without impinging on the effective operation of the circuit. "Effective operation" might well include criteria for acoustic noise and levels of vibration.

27.6.3.2 igh-Efficiency Method of Managing Switching in the Bridge

A very common way to control the current with the smallest number of switching transitions is to combine HBCC with, for example, alternating only S1 and S2 in Fig. 27.65, leaving S4 on all the time, on the understanding that there will be a back emf in the winding and the current can still be increased or decreased as desired.

Thus, when the motor is rotating and the back emf is somewhere between zero and the rail voltage, alternating two switches rather than four will still allow current control in the coil, using for example HBCC, exactly as before.

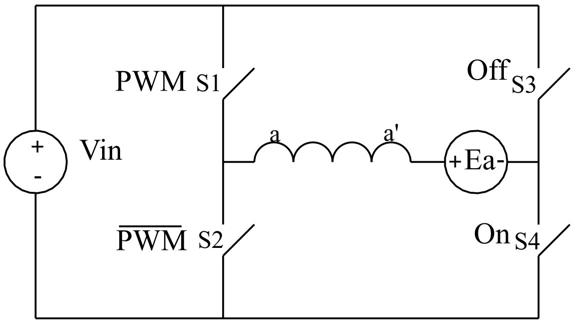


FIGURE 27.65 H-bridge switching with one switch steadily on and a back emf.

This is a very common control scheme and will need some extra logic to reverse the direction of rotation of the motor, by either turning S4 off and S3 on continuously, or by swapping the control signals to the left and right "legs." For full servo operation, normal H-bridge switching can be used and the logic is slightly different, but not significantly more complicated. However, following the discussion above, the switching losses will be higher.

27.6.4 A Complete Controller

27.6.4.1 Combining Commutation and P M Current Control

The real breakthrough is that one set of six switches can be used for both PWM and commutation. That is the clever part, and also the confusing part when one first tries to understand what is going on.

Thus, in a controller there are two control loops. The first is an inner current loop switching at, for example, 15 kHz to control carefully and exactly the current in two of the coils. Then at a much lower rate, for example at 50 times a second at 3000 rpm, the two coils doing the work are changed according to Table 27.2, controlled by an outer commutation loop, using information from the Hall-effect shaft-position sensors.

A complete controller is shown in block diagram form in Fig. 27.66. Various aspects of this block diagram will now be examined and explained in detail.

27.6.4.2 ardware Details

. . . . ***Semiconductor Switches*** The three most likely semiconductor switches for a six-step controller are the bipolar junction transistor (BJT), the metal oxide silicon field-effect transistor (MOSFET), and the insulated-gate bipolar transistor (IGBT). Older controllers used BJTs; however, contemporary controllers tend to use MOSFETs for lower voltages and powers and IGBTs for higher voltages and powers. Both of these devices are controlled by a gate signal

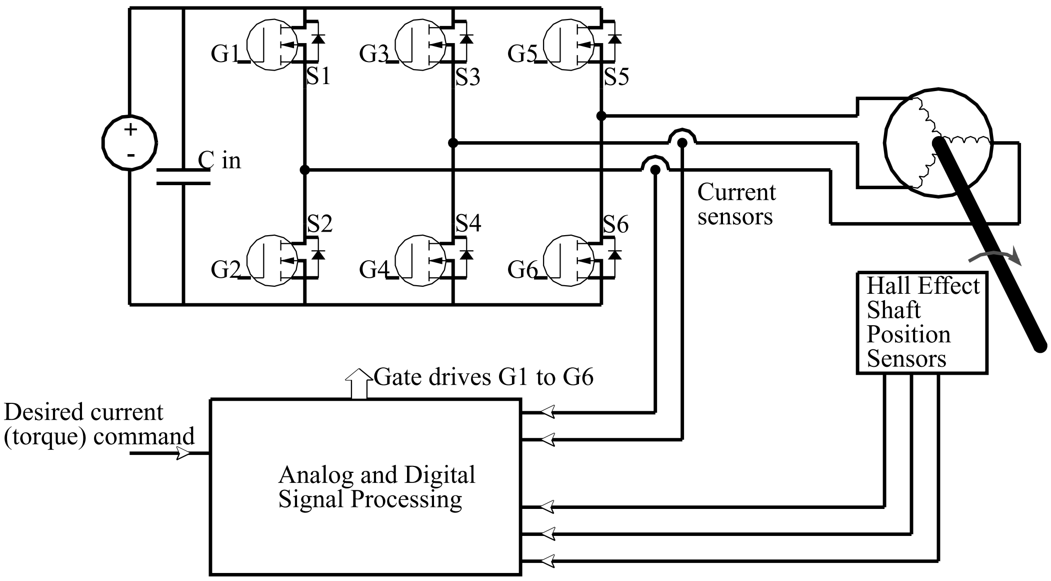


FIGURE 27.66 A complete controller showing the two feedback paths, one for the position sensors and one for the current sensors.

and will turn on when the voltage of the gate above the source or emitter is greater than about 5 V (about 10 V is common) and off when the gate voltage falls below the threshold. Systems typically use zero volts for the off state. The controller of Fig. 27.66 shows MOSFETs used for the six switches.

The trick is that the voltage at terminal **a**, also S1's source, is either ground or the positive potential of the battery, depending on which switches are on. Driving S2, S4, and S6 is easy since the MOSFET sources are all at the potential of the negative rail and the lower gate drive signals are referred to this rail.

There is a range of dedicated integrated circuits that can drive the switches S1, S3, and S5 and that use a "charge pump" principle to generate the drive signal and the drive power internally, all related to the MOSFET source potential. Various approaches to this technical challenge of providing a floating gate drive are commonly discussed under the generic heading of "high-side drives."

For the most sophisticated drives, a transformer coupling is used to provide a tiny power supply especially for the isolated gate drive and to send the control signals through either an opto coupler or a separate transformer coupling. The high-side drive problems here are exactly the same as those encountered in the traditional buck converter, or in drives for induction motors and PMSMs.

. . . . ***Dead Time and Flyback Diodes*** Two issues have been mentioned that must be addressed when using high-speed electronic switches in inductive circuits.

The first, in Section 27.6.2, "*Electronic Commutation*," was that care should be taken to ensure that the upper and lower switches in the same "leg," (e.g., S1 and S2) are never turned on at the same time. If the controller attempts to turn one off and the other on at the same instant and switch turn-off is slower than turn-on (as it is with BJTs and IGBTs), then a short circuit will result for a brief time. The bus capacitor is usually very large to provide ripple current (see later) and usually of very high quality, being fabricated especially for power electronic applications, and can easily provide thousands of amperes for a few microseconds, which is enough to destroy the semiconductor switches.

The second issue, discussed in Section 27.6.3, "*Current/Torque Control*," is that one cannot turn off both switches in a leg at the same time, even for a few nanoseconds, since the voltages resulting from attempting to interrupt current in an inductor will cause avalanche breakdown and failure of the semiconductors. This sounds like quite a dilemma.

There is actually a very simple and effective solution. At any transition the control circuitry ensures that the active switches are all turned off before any switch is turned on, usually for a few microseconds. This is known as "dead time," and its provision is an essential part of most of the dedicated integrated circuits in use. Then a "flyback"/"freewheel" diode is put in antiparallel with each semiconductor switch, and this provides the current path during dead time. These diodes are shown in Fig. 27.66.

The diode has a little more loss than the switch, since the diode forward drop is more than the switch drop. This is significant in a low-voltage controller. However, as stated earlier, for a low-voltage controller MOSFETs are the device of choice. They have a lesser-known property: When gated on, they can carry current in both directions. Intriguingly, the "on"-state resistance is lower in reverse than in the forward direction Thus, for low-voltage controllers, when the switch forward drop represents a significant contribution to losses, the MOSFET is turned on after dead time for both current

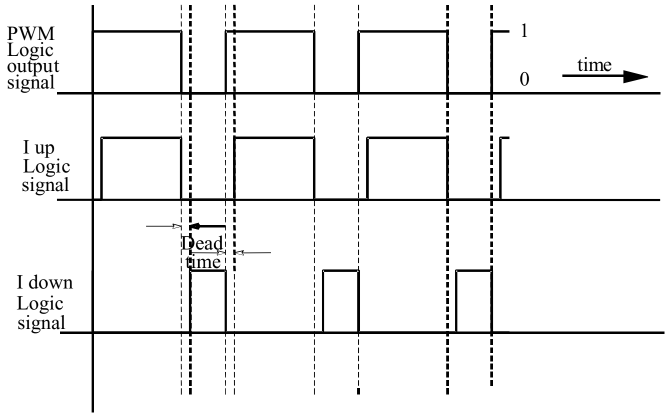


FIGURE 27.67 Dead time introduced into the PWM logic signal, for switch drive.

directions. Thus, the higher loss in the diode is only for a few microseconds.

It is not difficult to produce from the PWM signal an "*I* up" logic signal that is used to cause the current to increase and an "*I* down" logic signal used to decrease it, with the timing as shown in Fig. 27.67. The function can be executed in sequential logic, or with simple analog timing circuits.

. . . . ***Semiconductor Detail*** In MOSFETs and most IGBTs, there is a diode already within the device; it is unavoidable and results from the fabrication processes. In modern power semiconductors, this intrinsic diode is optimized to be a good switching diode. The serious designer, however, will check the specifications for reverse recovery of this diode, since in highly optimized controller designs, reverse recovery losses in the intrinsic diode can be significant and are very difficult to control. In low-voltage controllers one can put a Schottky diode in parallel with the intrinsic body diode. The Schottky diode, with its lower forward voltage drop will tend to take the current and has no reverse recovery problems, but the current must commutate to it from the semiconductor die, and the inductance of the connections is critical.

. . . . ***The Smoothing Capacitor on the Input to the Controller*** This is a substantial capacitor, often very expensive (it is shown in Fig. 27.66 as C in), and its design is quite challenging. The issue of smoothing is quite serious. If there are high-frequency or sudden current changes in the leads from the dc supply to the controller, they will radiate electromagnetic energy. Good design will limit the length of conductors in which current is changing rapidly. Thus, a very large capacitor is placed physically as close to the positive bus of the switches as possible, aiming to have steady current in the longer conductors from the dc supply up to the capacitor. When the motor is running at, say, half speed and providing large torques, a very high level of ripple current is carried by this capacitor. Kirchhoff's current law (KCL) must be applied at node A, as shown in Fig. 27.68. Good capacitors have a maximum ripple-current rating buried in their specification sheets. It turns out that in general, the size of the capacitor in a given design has very little to do with how much voltage ripple one can tolerate at the bus but rather is determined by the ability to carry the ripple current without the capacitor heating up and failing. It has been known that small electrolytics in prototype controllers mysteriously explode. On searching it is found that they are in parallel with the main capacitor and quite close to it, so they carry a lot of ripple current, then heat up and explode

27.6.4.3 The Signal-Processing Block for Producing Switch-Drive Signals from Hall-Effect Sensors and Current Sensors

. . . . ***Operation of the Hall Sensors*** The flux density directly under a magnet pole can be any where from 500 to 800 mT with NdFeB magnets. Hall effect (HE) sensors with a digital output, called Hall-effect switches, change state at very close to zero flux density. Thus, they will change state when the north and south pole are equidistant from them, so that for example, in Fig. 27.69, the switch HE1 is just changing state with the rotor as shown.

In practice a motor designer needs to consider what magnetomotive force comes from the current in the windings

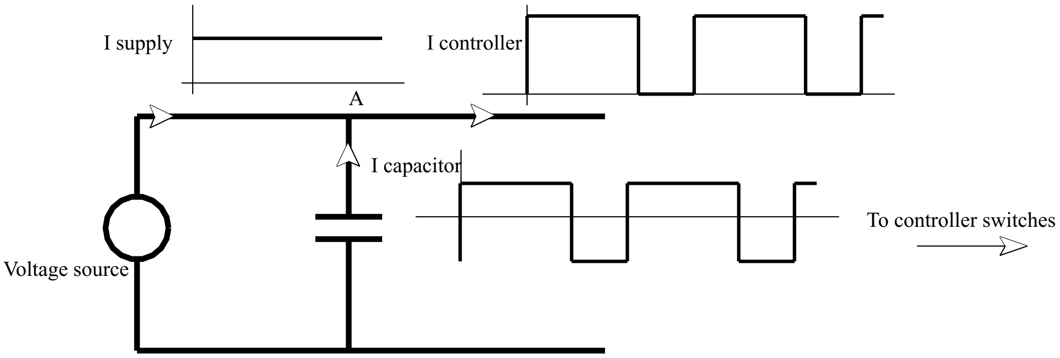


FIGURE 27.68 Kirchhoff's current law at node A.

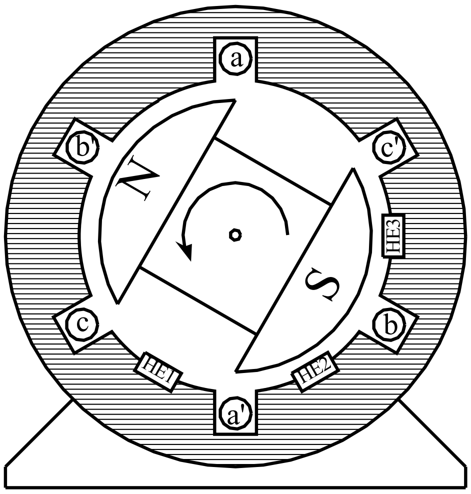


FIGURE 27.69 Possible Hall-effect switch positions in a three-phase machine.

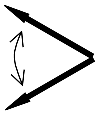
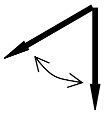
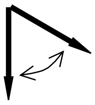
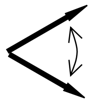
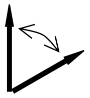
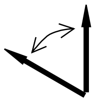
that might result in flux which would trip the HE sensor at a slightly different time. If you follow all the preceding logic about six-step switching, you will see that you only need the magnet poles to have a span of a bit more than 120°. Using 180° magnet poles can add considerably to the cost, as well as having an impact on such things as cogging torque. Actual designs often add extra "sense" magnets to cover 180° just at the circumferential strip where the HE switches are located, adding minimally to the magnet mass and ensuring good and accurate triggering. However, if the switches operate as shown earlier, then Table 27.3 will result for the HE switches located as shown in Fig. 27.69.

Figure 27.66 shows two current sensors. In the most sophisticated systems there are two current sensors, one in each of two motor phases. The current sensing is done at the winding and isolated with either an HE sensor in a soft ferromagnetic magnetic core surrounding the conductor (commercial items are available), or by using a resistive shunt sensor and some accurate analog signal isolation/coupling through transformers or opto couplers. The isolation is necessary since the potential at points **a**, **b**, and **c** is either the dc bus voltage or zero, depending on which switches are on, so that any current measure such as the small voltage across a shunt is superimposed on these very large voltage changes. This is a very similar problem to that for the high-side gate drives discussed earlier. The current in the third winding is determined by the algebraic application of KCL, given the other two readings.

. . . . *Sensing the Current in the Motor Windings*

Simple controllers sometimes avoid the complexities of isolated current measurement and instead measure the current in the return negative supply, for example from the bottom of the three lower switches to the bottom of the supply-smoothing capacitor. This arrangement senses current when an upper and a lower switch is on, but not when the current is being carried in flyback diodes or by two lower switches. Although it is inexpensive, it does not provide fully accurate control. The system works because the current should be decreasing when a measure is not available, heading toward zero, so switch or system failure due to overcurrent should not occur.

TABLE 27.3 Hall-effect switch outputs for rotor positions as shown, HE switches placed as in Fig. 27.69

When the Center of the Rotor North Pole is in This Sector	HE1 Outputs	HE2 Outputs	HE3 Outputs
	1	0	0
	1	1	0
	1	1	1
	0	1	1
	0	0	1
	0	0	0

. . . . *Detail of Management of Current Sensing*

The controller must select the right current to increase or decrease, dependent on rotor position. The following convention is adopted. Positive current provides torque in the counterclockwise direction and therefore goes into winding **a**, **b**, or **c**.

All systems are capable of regeneration, which implies that negative torque can be commanded (without reversing the direction of rotation) to make the machine operate as a generator, developing retarding torque.

Thus, for the preceding sequence of sector determinations, referring back to Table 27.2, the output of current sensors should be directed to the current controller as shown in Table 27.4.

The addition and negation required can be carried out with standard operational amplifier circuitry. The three required analog measures are then fed to a three-to-one analog multi-

TABLE 27.4 Current sensors to use as input to the current controller for each of the six rotor position sectors

Hall-Effect Switch Outputs (HE1, HE2, HE3)	Monitor Current as Read by
100	Sensor a
110	Negative of (sensor a + sensor b)
111	Negative of (sensor a + sensor b)
011	Sensor b
001	Sensor b
000	Sensor a

plexer, gated from the HE switch signals suitably processed in combinational logic. The resulting single analog output is fed to the current comparator.

. . . . ***Details of Logic for Directing Control Signals to the Right Switches*** Given that dead time is introduced elsewhere in sequential logic, or with timing circuits, it is a simple matter to develop the combinational logic for directing, or steering, the switching signals to the right switches. A typical scheme for a specific controller is shown in Table 27.5.

It is usual also to include some shut-down logic from dedicated protection circuits, for example sensing overcurrent, over bus voltage, undervoltage for gate drive, and over temperature both in the motor and in the controller power stage. For simplicity, this is not shown in the table.

27.6.5 Summary

27.6.5.1 What Has Been Discussed

The physical principles of the operation of a PM BLDC motor have been discussed, which led to the development of the necessary parts of a power electronic controller. One specific type of current control, Hysteresis band current control, was explained in detail, and one specific type of switch logic pattern was developed. The exposition has included many of the issues that can cause difficulties for controller designers if they are not careful.

TABLE 27.5 Summary of logic used to steer *I* up and *I* down signals to the correct switches and to turn on the correct lower switch, for the scheme discussed in section 27.6.2

HE States (1, 2, 3)	S1	S2	S3	S4	S5	S6
100	*I* up	*I* down	0	1	0	0
011	0	0	0	1	*I* up	*I* down
011	0	1	0	0	*I* up	*I* down
000	0	1	*I* up	*I* down	0	0
100	0	0	*I* up	*I* down	0	1
110	*I* up	*I* down	0	0	0	1

27.6.5.2 What Has Not Been Discussed

Many PM BLDC motors have more than one pair of poles. The foregoing arguments can all be extended to higher pole-count machines by taking any mention of degrees to be electrical degrees rather than mechanical degrees. The controller discussed in detail only manages one direction of rotation. It is an excellent exercise, and straightforward, but not trivial, to repeat the preceding steps, preparing the tables for clockwise rotation of the simple machine discussed earlier. Then, following the discussion in the first part of Section 27.6.3, "*Current/Torque Control*," about H-bridge switching, prepare the logic tables again for full bidirectional control, using the *I* up and *I* down logic signals exactly as before, but applying them to both "legs" determined by the rotor position. Only one form of current sensing was discussed in detail. There are many simpler schemes in use that do not have quite the flexibility and accuracy of the foregoing, but that can suit certain applications. Similarly, there are other forms of current control, such as the constant frequency linear method briefly discussed. Shaft-position sensors take many forms. Adherence to the HE sensor was for simplicity, and to reinforce the magnetic-field aspects of the machine operation.

27.6.6 Further Reading

Apart from power electronics texts, which usually cover this area very sketchily, there are three small books that are specifically about machines, but have more detail on the range of controllers used.

1. Timothy J. E. Miller, *Brushless Permanent-Magnet and Reluctance Motor Drives*. Oxford University press, 1989. For square-wave brushless dc motors.
2. T. Kenjo and S. Nagamori, *Permanent-Magnet and Brushless DC Motors*. Oxford University Press, 1985. For small machines used particularly in consumer electronics.
3. Duane C. Hanselman, *Brushless Permanent Magnet Motor Design*. McGraw-Hill, 1994. For the possible range of controllers in the last chapter.
4. Application notes from the various integrated circuit companies, particularly those that specialize in motor control.

27.7 Servo Drives

M. . ah an

27.7.1 Introduction

Servo drives are motor drives that operate with high dynamic response. Historically, servo drives have implied motion-control systems in which sophisticated motor design, drive, and control techniques have been employed to obtain very much shorter positioning times than is possible with conventional drive systems. Examples are in machine tool drives, robotic actuators, computer disk drives, and so on. The power range for these drives has typically been in the range of a few kilowatts or less. This range has steadily increased in recent years as a result of advances in magnetic materials, machine design, power and signal electronic devices, and sensors.

Apart from the fast positioning times, "high dynamic response" also means that the drive operates with the following:

1. Very smooth torque up to a very low speed
2. Very high reliability and little maintenance
3. Immunity from load disturbances

The last of the foregoing items is brought about by robust and intelligent control algorithms; the first two items are brought about by innovative and often costly motor and controller designs. As a result of these, the cost of a servo motor drive is usually much higher than equivalent power rated industrial drives.

The distinctions just mentioned may be easily recognized by noting, for example, that the drives that bring material in a mill may not require high performance, but the drives that take part in shaping, milling, or reducing the material should have high dynamic response in order to increase throughput and meet the accuracy requirements of the final product.

27.7.2 Servo-Drive Performance Criteria

The performance of a servo drive can be expressed in terms of a number or factors such as servo bandwidth, accuracy, percentage regulation, and stiffness. While servo bandwidth indicates the ability of the drive to track a moving or cyclic reference, the percentage regulation and stiffness stipulates the drive's static holding performance for speed or position, in the face of disturbances from the load and in the supply conditions. The servo bandwidth, given as a frequency in hertz, is often found from the system frequency response plot, such as the Bode diagram.

The percentage regulation of a speed-controlled system often refers to the percentage change in speed from no load to full load. In a type-zero system this figure will have a finite value. Many systems are type zero, albeit with a high gain so that the regulation is acceptably low. For such systems, the regulation is often necessary for operational reasons. In some applications, zero percentage error is required, which calls for type 1 or integral type control system.

The servo stiffness is similar to the percentage error mentioned earlier, but it applies mainly for the position servo. It specifies the deflection of the load from its reference position when full load torque is applied. Its is usually the slope of the deflection versus the applied load torque in rad/Nm around the reference position.

27.7.3 Servo Motors, Shaft Sensors, and Coupling

Servo drives use motors that allow the desired goals of high dynamic response to be achieved. The following are the important parameters/attributes of a servo motor:

1. High torque-to-inertia ratio
2. High torque-to-volume ratio
3. Low inductance of the motor windings
4. Low cogging torque at low speed
5. Efficient heat dissipation
6. Low coefficient of shaft compliance
7. Direct coupled, high-resolution, shaft-mounted sensors for position and speed

High torque-to-inertia ratio allows fast acceleration or deceleration of the drive when motion references are changed. This is often achieved through innovative low-inertia rotor design and low inductance in the stator winding. One example of a dc servo motor is the pancake printed armature dc motor with no iron in the rotor, as indicated in Fig. 27.70. The rotor is sandwiched between axially mounted stator poles. The commutator is also on the printed armature. Another example is the disk rotor stepping motor, also without iron in the rotor, as indicated in Fig. 27.71.

PM ac synchronous motors with modern high-energy-density magnets in the rotor, as described in Section 27.6, are also examples where the motor designer strives to minimize the rotor inertia. Modern permanent magnets allow the required airgap flux to be developed with a much-reduced volume of the magnets, consequently reducing the diameter of

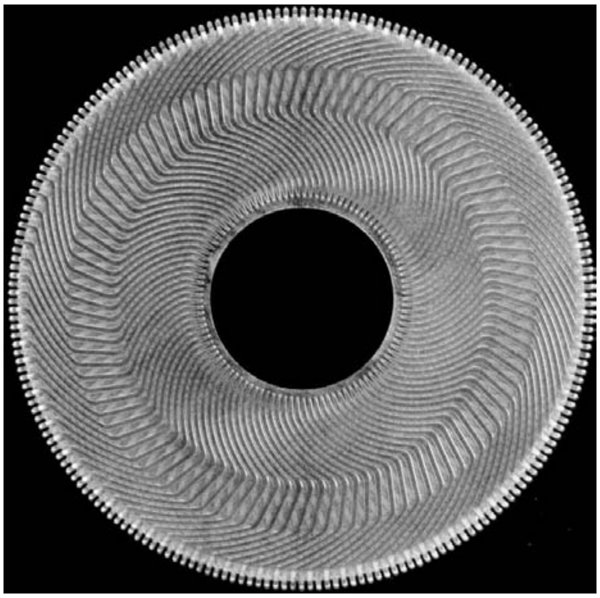


FIGURE 27.70 Pancake armature of a dc servo motor. Courtesy: Printed Motors Ltd., UK.

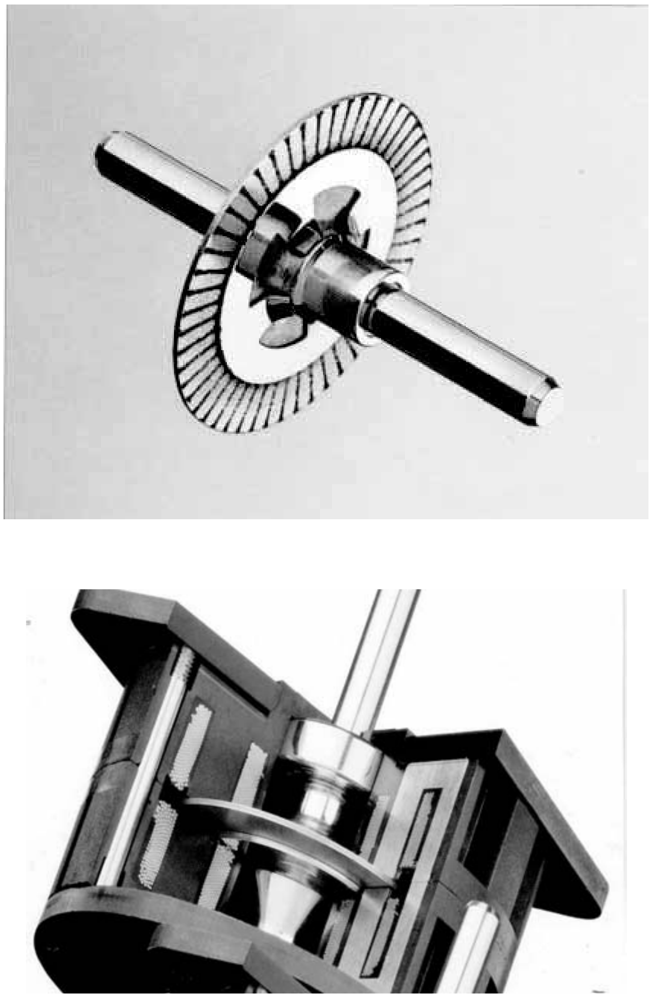


FIGURE 27.71 A disk rotor stepping motor with ironless rotor for low inertia and inductance. Courtesy: Escap Motors.

the rotor. It is well known that the moment of inertia of a motor increases as the fourth power of its outer radius

Another benefit of the modern permanent magnet material is that the motor volume is also reduced. Servo motors often have to be located in a very confined space, and this reduction is volume is an important attribute.

The ironless designs mentioned earlier bring other benefits in the form of reduced inductance and cogging torque. Brushed pancake ironless motors are available with armature inductance as low as 100 μH.

From Section 27.2.2, the mechanical and electrical time constants of a brushed dc motor are given by

$$\tau_m = \text{mechanical time constant} = \frac{R_a J}{K_E K_T} \quad \text{s}$$

and

$$\tau_a = \text{electrical time constant} = \frac{L_a}{R_a} \quad \text{s}$$

It is well known that for the highest load acceleration, the load inertia referred to the motor should be equal to the rotor inertia. Thus, in a matched system, the total inertia the motor accelerates is twice its own inertia. In other words, the motor inertia should also be minimized.

For a good servo motor, the ratio between the mechanical and the electrical time constants is often of the order of five or more. This allows the speed and the current-control loops to be decoupled and noninteracting. The electrical time constant of a motor determines how quickly the motor current may be changed and hence how quickly torque can be developed. As also mentioned in Section 27.2, drives with a reasonable dynamic performance should have an inner torque loop. This torque loop is built around current loops, for the armature for the brushed dc motor, or for the d- and q-axis currents for the induction and synchronous motor drives. Having a low inductance in the winding allows these currents to be followed dynamically changing current or torque references with higher accuracy and bandwidth.

The cogging torque, if appreciable, causes the rotor to have preferential positions. As a result, the position accuracy of the motor may suffer. Another problem is the ripple in speed as the motor is operated at low speed. At high speed, these ripples due to cogging torque may be filtered out by the motor inertia; however, the extra loss due to cogging remains. The ironless or toothless rotor obviously produce very small cogging torque because of the absence of preferential paths for the airgap flux to establish through the rotor iron of the brushed dc motor. The surface magnet synchronous motor also has this feature. The interior magnet motor normally has skewed stator slots to avoid production of cogging torque.

Servo motors often operate with frequent start-and-stop duty, with fastest allowable acceleration and deceleration during which the motor current is allowed to reach about 2 to 3 times the continuously rated current. The increased I^2R loss in such duty must be dissipated. This calls for adequate cooling measures to be incorporated in the motor housing. With such operation, it is sometimes possible to excite mechanical resonance due to shaft compliance. This is avoided through proper arrangement of the shaft position/speed sensor and the coupling between the motor and the sensor. A belt-driven speed sensor may be acceptable for an industrial drive; however; for servo applications, a rigid, direct-coupled sensor mounted as close as possible to the motor armature is preferable. Additionally, the speed sensor is also required to have negligible noise. Speed signal from analog tachogenerators, which were used for speed sensing until recently, invariably needed to be filtered to remove the cyclic ripple/noise that existed. Such filtering often limits the maximum speed-control bandwidth of a drive.

27.7.4 The Inner Current/Torque Loop

The inner current loop(s) in a servo motor drive play a more important role than just limiting the current in case of overload. These loops operate continuously to regulate the motor-developed torque so as to meet the load demand, and for meeting the speed trajectory specified by the motion controller. Motor drives of high dynamic response currently employ PWM current sources. These sources use MOSFET or IGBT switching devices that allow the modulator to be operated with a switching frequency between 10 and 25 kHz. At these frequencies, the inherent switching delay, which is equivalent to half of the PWM switching period, is made rather small for the bandwidth of the torque control loop. The bandwidth of the current control loops closely represents the bandwidth of torque control. This because the motor-developed torque generally proportional to these currents. Servo drives up to a few kilowatts presently have torque/current control-loop bandwidths in excess of 1 kHz.

For higher power, fast-response drives, such as those used in the metal-processing industries, thyristor converters have been used for many years. The switching frequencies of these converters are rather low, being some multiple of the mains frequency, according to the converter chosen. Fortunately, the larger mechanical time constant of the larger power motor and the nature of the applications have allowed the 300-Hz (360-Hz in the United States) switch frequency of the three-phase thyristor bridge converter to be used satisfactorily in many applications requiring high dynamic response. The growing availability of faster and higher power IGBT devices is continually enhancing the dynamic performance of larger drives.

Fast-response, inner torque-control loops have in recent years been extended to ac induction and synchronous motors. These motors were hitherto considered only for industrial drives. The vector methods described in Sections 27.3 and 27.4, which employ inner quadrature axis current controllers in the synchronous (for the induction motor) or the rotor (for the synchronous motor) reference frame, have transformed the prospects of ac motor drives in servo applications.

Because of the fast dynamic response requirement of servo drives, the servo motor is nearly always driven with the maximum torque per ampere (MTPA) characteristic. Field weakening is normally not used. In other words, field control either directly for a brushed dc motor or a synchronous motor or indirectly through armature reaction (i.e., through i_d current control) for induction or PM ac synchronous motors is not used for field weakening. It is nevertheless used for regulating the field at the desired level. Field weakening is mainly used for drives where operation at higher than base speed with constant-power characteristic is desirable.

27.7.5 Sensors for Servo Drives

Servo drives require high-bandwidth current sensors for the inner torque loop and high-accuracy, noise-free speed and position sensors for the outer loops. The current sensor is often a Hall device with an amplifier, which can have bandwidths as high as 100 kHz. The inner current loop both limits and continuously regulates the motor current in all operating modes of the drive, including acceleration and deceleration. About 2–3 times the continuous rated current of the motor is tolerated during acceleration and deceleration. This entails limiting the speed controller output to the level corresponding to the current sensor output for the limiting values of motor currents.

The current-sensor output has to be filtered to adequately remove the switching frequency noise. Otherwise, certain switching devices in converter may be overloaded. This task is more important for the thyristor converters for dc drives for which the switching frequency is rather low. This filtering of the current sensor output limits the bandwidth of the current-control system, i.e., the inner torque-control loop.

Performance of servo-motor drives depends critically on the noise and accuracy of the speed and position sensors. Synchro-resolvers with 12-bit or higher digital accuracy were used in many servo-drive systems until recently. The advent of cheaper incremental and absolute optical encoders has altered this situation completely. These digital sensors are actually position sensors. The speed information is derived from positions measured by discrete differentiation. Such differentiation is not feasible with analog position sensors, because of the noise.

Analog tachogenerators are also avoided for speed servo systems. This is because of the tachogenerator ripples inherent in the sensor.

Modern discrete position sensors provide for virtually noise-free speed and position sensing. This allows very fast dynamic response to be achieved if the switching frequency of the converter allows it.

27.7.6 Servo Control-Loop Design Issues

27.7.6.1 Typical Controllers

. . . . ***Proportional Controller*** A proportional controller provides for a straight gain to amplify the error signal. It has no discriminatory properties. With the input and feed resistance values indicated in Fig. 27.72, the total gain of the controller is $K+1$.

For this controller,

$$v_c = (K+1)(\theta_i - \theta) \qquad (27.79)$$

. . . . ***Transient Velocity Feedback Controller*** It is well known that a following error will exist in the preceding system when a moving or ramp reference is tracked. If a rate feedback,

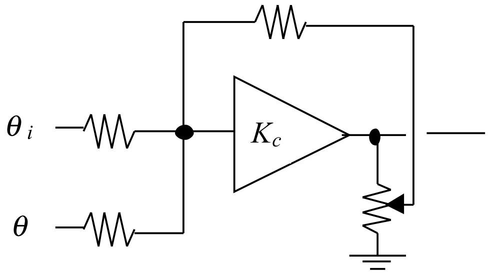


FIGURE 27.72 Proportional controller.

such as the speed feedback in a position-control system, is used to damp the system, this error is further increased. To overcome this following error due to velocity feedback, transient velocity feedback can be used as indicated in Fig. 27.73.

The speed (velocity) signal is passed through an RC circuit at the input of the amplifier circuit. An input current occurs only when the speed signal changes. In the steady state, the capacitor is fully charged, so that no following error in the steady state due to the velocity feedback can exist.

In the steady state when the velocities are equal, the output may lag or lead depending on the relative values of R_1 and R_2. It can be shown that in the absence of frictional load torque, as is often the case in servo applications, no following error is introduced if $R_1 = R_2$.

. . . . ***Integral Controller*** In the transient-velocity and error-rate feedback schemes, a following error will exist if viscous friction and load torque are present. If such loads are present, the system gain has to infinity to have zero error. Very large gains will make any physical systems unstable, unless bandwidth limitations exist. One way to employ infinite gain in the steady state is to use an integrator. This amplifies the steady-state error until it is eliminated.

Normally, a proportional plus integral (PI) action is used. A derivative term is normally not used in the control system of a drive system, since the drive feedback signals are very noisy. Instead, derivative signals are obtained through sensors such as tachogenerators. The structure of a PI controller is indicated in Fig. 27.74. It can be shown that there will be no steady-state error even in the presence of frictional or other load torque.

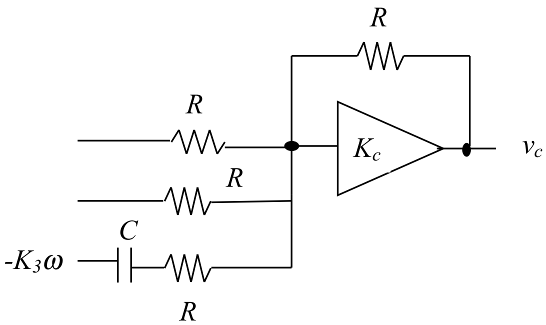


FIGURE 27.73 Transient-velocity controller.

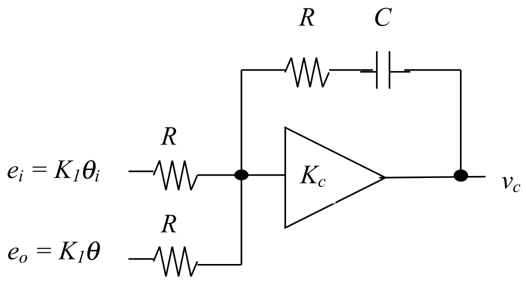


FIGURE 27.74 Integral-type controller.

Many types of more complex controllers are available, such as the variable-structure controller. Drives with fuzzy controllers have also been in the marketplace for some years.

The controller circuits just described are usually implemented in analog circuits using operational amplifiers. Digital implementations are also being gradually introduced using embedded microcontrollers and digital signal processors.

27.7.6.2 Simplified Drive Representations and Control

Consider the block diagram of Fig. 27.75 in which individual elements (blocks) are represented in terms of their transfer functions in terms of the Laplace operators.

Here, $G_A(s)$, $G_C(s)$, $G_L(s)$, $H_T(s)$, and $H_F(s)$ represent the transfer functions of the power converter plus the motor, the controller, the load, the sensor (of speed in this example), and the filter following the sensor, respectively. The reference input for speed and the feedback signal are connected to a summing junction of an operational amplifier through resistors R_i and R_f, respectively.

The preceding system can be simplified to that shown in Fig. 27.76, and further to that in Fig. 27.77.

In general, if the individual control blocks are approximated as first-order systems and are mutually decoupled, meaning that each block operates in a frequency band that is far outside

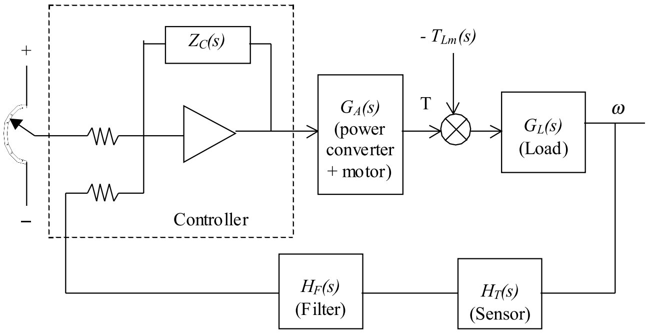


FIGURE 27.75 Block-diagram of a speed-control system.

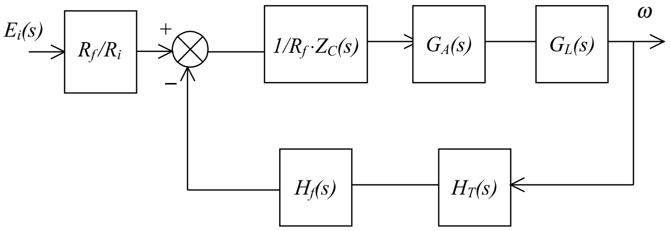


FIGURE 27.76 Simplified representation of Fig. 27.75.

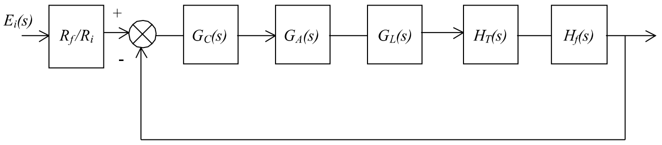


FIGURE 27.77 Further simplified representation of Fig. 27.75.

the frequency bands of all other blocks, then the foregoing systems can be represented by a transfer function of the form

$$G_1(s) = \frac{K}{(1+sT_1)(1+sT_2)(1+sT_3)(1+sT_4)\cdots} \tag{27.80}$$

When T_3 and T_4 are much smaller time constants than T_1 and T_2, the preceding may be approximated by

$$G_1(s) = \frac{K}{(1+sT_1)(1+sT_2)(1+sT_s)} \tag{27.81}$$

where $T_s = T_3 + T_4 + \cdots$, etc. A dc-motor speed-control system with current and speed sensors falls in this category. For such a system there exist two dominant time constants (poles).

For such a system, a proportional plus integral controller is of the form

$$G_c(s) = \frac{(1+s\tau_1)(1+s\tau_2)}{s\tau_o(1+s\tau_{F1})(1+s\tau_{F2})} \tag{27.82}$$

One optimization criterion (Kessler's) stipulates that $\tau_1 \approx T_1$, $\tau_2 \approx T_2$, and $\tau_o = 2KT_s$. With this stipulation, the transfer function of the complete system is given by

$$G(s) = G_1(s)G_c(s) = \frac{1}{2sT_s(1+T_s)} \tag{27.83}$$

and

$$\frac{V(s)}{V_i(s)} = \frac{G}{1+G} = \frac{1}{1+2sT_s+2s^2T_s} \tag{27.84}$$

Note that two filter time constants τ_{F1} and τ_{F2} are included in $G_c(s)$ for the sake of its realizability. These can be relegated to frequencies far higher than the range of interest and can be ignored for further analysis of the system. For an unit step input of v_i, the output v is given by

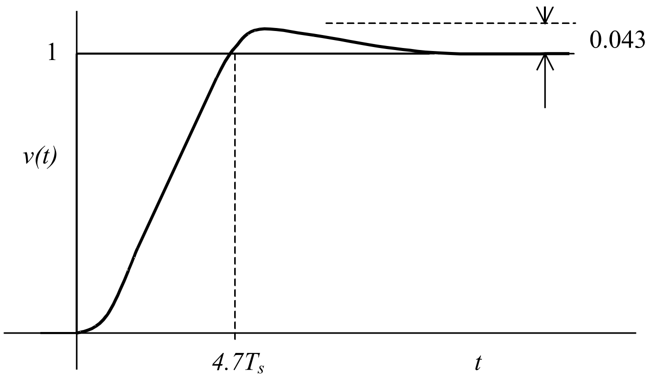


FIGURE 27.78 Response of the optimized system of Fig. 27.75.

$$v(t) = 1 - \sqrt{2}e^{-1/2T_s}\sin\left(\frac{t}{2T_s} + \frac{\pi}{4}\right) \qquad \text{for} \quad t \geq 0. \tag{27.85}$$

A typical output is sketched in Fig. 27.78.

If the transfer function $G_1(s)$ has one dominant time constant $T_1(s)$, as for the field current control of a dc motor, a suitable controller is the form

$$G_c(s) = \frac{(1+sT_1)}{s\tau_o(1+sT_F)} \tag{27.86}$$

In some cases, the transfer function $G_1(s)$ is of the form

$$G_1(s) = \frac{K}{sT_1(1+sT_2)(1+sT_s)} \tag{27.87}$$

where T_s is the sum of a number of short time constants, associated with sensors, switching frequency, and so on. The current controller of the dc motor with back emf has such a characteristic. A suitable PI controller for this system is

$$G_c(s) = \frac{(1+s\tau_1)(1+s\tau_2)}{s\tau_o(1+s\tau_{F1})(1+s\tau_{F2})} \tag{27.88}$$

For this system, Kessler's optimization criterion stipulates that

$$\tau_1 = 4T_s,\ \tau_2 = T_2, \quad \text{and} \quad \tau_o = \frac{8KT_s}{T_1}$$

The transfer function of the complete system is then

$$\frac{V(s)}{V_i(s)} = \frac{1+4sT_s}{1+4sT_s+8s^2T_s^2+8s^3T_s^3} \tag{27.89}$$

The peak overshoot of this system to a unit step unit is usually unacceptable, as indicated by the response of Fig. 27.80. This

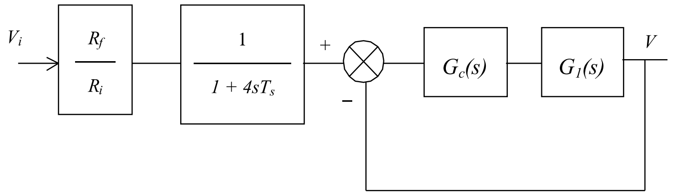


FIGURE 27.79 Block diagram representation of a typical current controller.

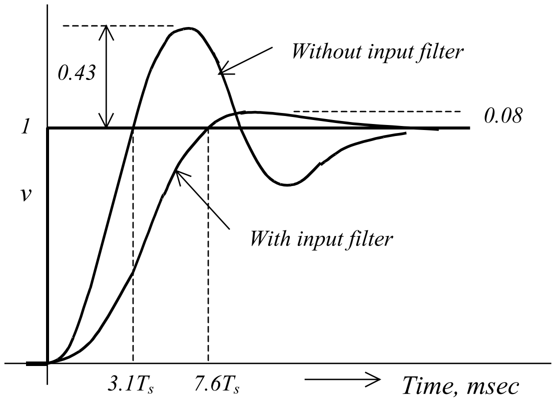


FIGURE 27.80 Optimized response of the system of Fig. 27.79.

overshoot is usually reduced by inserting a first-order filter in the reference circuit. The filter network and the responses are given in Fig. 27.79.

27.7.7 Further Reading

1. George W. Younkin, *Industrial Servo Control Systems: Fundamentals and Applications*. Marcel Dekker, 1996.
2. B. C. Kuo and J. Tal, *Incremental Motion Control 1: DC Motors and Systems*. SRL Publishing, 1978.
3. D. Shetty and R. Kolk, *Mechatronics Systems Design*. PWS Publishing, 1997.
4. A. Fransua and R. Magureanu, *Electric Machines and Drive Systems*. Techical Press, Oxford, 1984.

27.8 Stepper Motor Drives

M. . ah an

27.8.1 Introduction

A stepper motor is a positioning device that increments its shaft position in direct proportion to the number of current pulses supplied to its windings. A digital positioning system without any position or speed feedback is thus easily implemented at a much lower cost than with other types of motors, simply by delivering a counted number of switching signals to the motor. Typically, a 200-steps-per-revolution stepper motor with 5 stepping accuracy will be equivalent to a dc motor with a 12-bit (or 4000 counts/rev) encoder plus the closed-loop speed and position controllers for obtaining similar positioning resolution. This advantage, however, is obtained at a cost of increased complexity of the drive circuits. A disadvantage of the motor is perhaps its inability to reach an absolute position, since the final position reached is only relative to its arbitrary initial position. Nevertheless, the true digital nature of this motor makes it a very suitable candidate for digital positioning systems in many manufacturing, automation, and indexing systems.

The working principle of stepper motors is based on the tendency of the rotor to align with the position where the stator flux becomes maximum (i.e., seeking of the minimum-reluctance position, also called the detent position). The rotor and the stator are both toothed structures, and the stator normally has more than two windings to step the rotor in the desired direction when they are energized in certain combinations with current. Some motors additionally have permanent magnets embedded in the rotor that accentuate an already existing, zero-excitation detent torque. These motors hold their positions even when the stator excitations are removed completely, a feature desirable for some applications.

In addition to the point-to-point stepping action, these motors can also be operated at high slewing speed, simply by increasing the pulsing rate of phase currents. Since the motor is inherently a synchronous actuator, the pulsing rate has to be increased and decreased properly, so that the rotor may follow it. At the end of a complete run, the motor always stops at the desired incremental position or angle without any accumulated error. The only error that may be encountered is mainly due to the machining accuracy of the teeth in the stator and rotor. This error is of the order of about 5 of one step position/angle and it is nonaccumulative.

27.8.2 Motor Types and Characteristics

27.8.2.1 Single-Stack Variable-Reluctance Stepper Motor

Single-stack motors are normally of the variable-reluctance type with no excitation in the rotor. The cross section of a three-phase motor with two stator poles/phase and four rotor poles are indicated in Fig. 27.81. The motor can be stepped clock or anticlockwise by energizing the phase winding in the ABCA or ACBA sequence, respectively. The step angle, i.e., the angle moved by rotor for each change in excitation sequence, of the motor is given by

$$\theta_s = \frac{360^\circ}{Np} \tag{27.90}$$

where N is the number of phases in the stator and p is the number of poles in the stator. Single-stack motors typically has larger step angles than other types because of limitations of

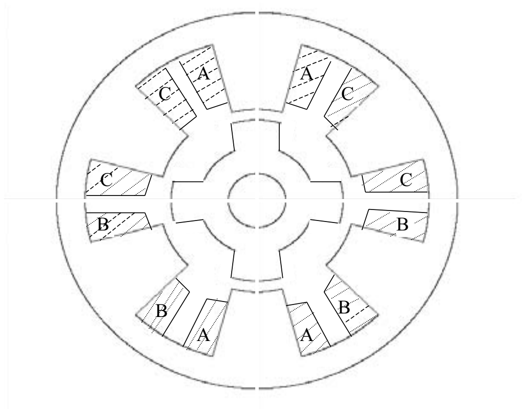


FIGURE 27.81 Cross section of a single-stack variable-reluctance stepper motor.

space for the windings. The step angle of these motor tend to be larger than the multistack and hybrid stepper motors.

For each excited winding, the motor develops a torque–angle (T–θ) characteristic as indicated in Fig. 27.82. Note there are two equilibrium positions of the rotor, namely, X and Y, where the motor develops zero torque.

The position X is referred to as the stable detent position, around which the rotor develops a restoring torque when displaced. The restoring torque increases as the rotor is moved from its detent position, becoming a maximum $T_{\max}$ on either side of this position. The slope of the T–θ characteristic around this detent position and the maximum torque, both of which depend on the level of excitation, indicate how far the rotor will be displaced under load torque. This means that the level of excitation also affects the position holding accuracy of the motor.

The motor may also be excited in the sequence: AB–BC–CA or AB–CA–BC for forward and reverse stepping, respectively. The two phases-on scheme develops more torque around the detent positions at the expense of twice the resistive losses.

Yet another excitation scheme is AB–B–BC–C–CA–A–AB for forward stepping and AB–A–AC–C–BC–B–AB for reverse stepping. In this scheme, the step size is halved as opposed to the full-step size of the previous sequences. Two different levels of torque is produced for alternate detent positions. However, the reduced step size and the more damped nature of each step may outweigh this disadvantage.

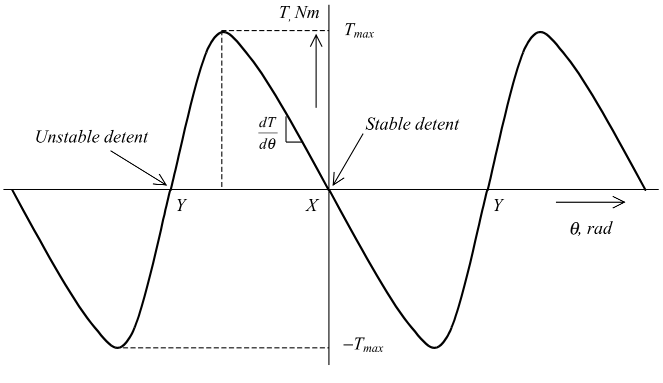


FIGURE 27.82 Static torque characteristic of a stepper motor.

27.8.2.2 Multistack Variable-Reluctance Stepper Motor

In a multistack variable-reluctance motor, the stator windings are stacked along the shaft. Each stack section now has the same number of poles in the stator and the rotor. Normally each stator stack is staggered with respect to its neighbor by one Nth of a pole pitch, where N is the number of stator/rotor phases or sections. The cutout view of Fig. 27.83 shows some internal details of a six-phase multistack motor, in which each stack has a phase winding between two rings, each with 32 stator and rotor poles. The step size of this motor is

$$\theta_s = \frac{360^\circ}{Np} = \frac{360^\circ}{6 \times 32} = 1.875^\circ \tag{27.91}$$

The excitation sequence of this motor is similar to the ones mentioned in Section 27.8.2.1, except that more excitation sequences are available. When a stator winding is energized, the rotor poles of that section tend to align with those defined by the stator excitation. The stator and rotor teeth in the other sections are not aligned. By changing the combination of excited phases to the next in sequence, the rotor is made to move by one step angle.

27.8.2.3 ybrid Stepper Motor

A hybrid stepper motor has an axially oriented permanent magnet sandwiched between two sections of the stator and rotor, as indicated in Fig. 27.84. The magnet flux distributes radially through the two stator and rotor sections, both of which are toothed, and axially through the back iron of the stator and the shaft. The stator has two phase windings, each of which creates alternate polarities of magnetic poles in both

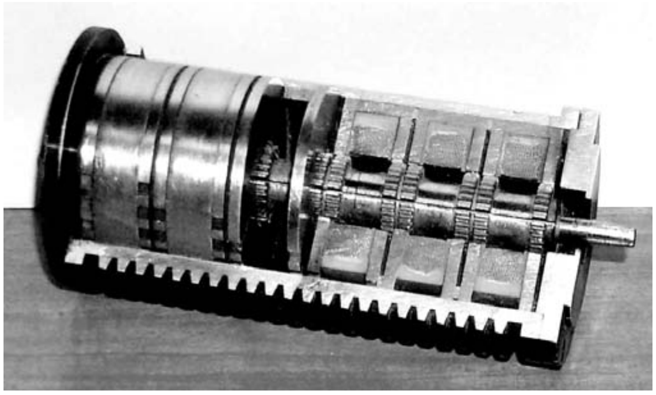


FIGURE 27.83 Cutout view of a six-phase, multistack, variable-reluctance stepper motor. Courtesy: Pratt Hydraulics, UK.

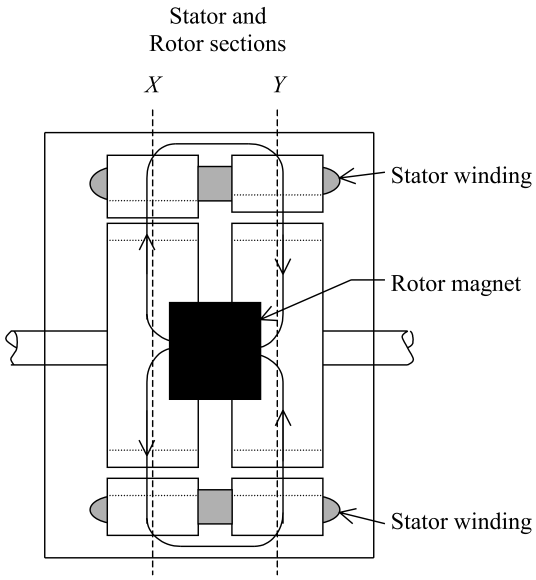


FIGURE 27.84 Axial section of the hybrid motor.

sections of the stator. Stator windings are excited with bipolar currents, as opposed to the unipolar currents in the variable-reluctance motors of the two preceding sections. The magnetic flux produced by the stator windings is circumferential in each stator and rotor section, but also crosses the airgap radially. It does not, however, pass through the rotor magnet. The two rotor sections are offset by half its tooth pitch.

The rotor magnet causes to the stator and rotor teeth to settle at the minimum reluctance position with a modest amount of detent torque to keep the rotor in position when the stator windings are not energized. The rotor magnet flux distributes outward through stator poles 3 and 7 in section X and inward through poles 1 and 5 in section Y, as shown in Fig. 27.85a and 27.85b. When stator windings A and B (indicated as dark and faint shaded, respectively) are energized with positive and negative currents, respectively, the resulting stator flux also distributes through these same poles, so that the rotor then develops a much higher detent torque (T–θ) characteristic. The motor can be stepped forward or backward by energizing windings in sequence $A\bar{B}$–AB–$\bar{A}B$–$\bar{A}\bar{B}$ or $A\bar{B}$–$\bar{A}\bar{B}$–$\bar{A}B$–$A\bar{B}$, respectively, where the overbar indicates the polarity of currents in phases A and B.

The stepping angle of a hybrid stepper motor is given by

$$\theta_s = \frac{90^\circ}{p} \tag{27.92}$$

where p is the number of rotor poles.

27.8.2.4 Permanent-Magnet Stepper Motor

Permanent-magnet stepper motors have alternate polarities of permanent magnets on the rotor surface while the rotor iron, if it is used, has no teeth. In one type of construction, the rotor has no iron, and the stator consists of two windings that set up alternate poles when energized, just as in the case of the hybrid motor. The rotor consists of permanent magnets, alternately polarized, attached to the surface of a nonmagnetic disk, as shown in Fig. 27.86. The stator and rotor fluxes cross the airgap, one on either side of the disk, axially.

27.8.3 Mechanism of Torque Production

27.8.3.1 Variable-Reluctance Motor

If it is assumed that the current in the excited winding remains constant, the production of static torque of a variable reluctance motor around a detent position is given by

$$T = \frac{dW_m}{d\theta} \tag{27.93}$$

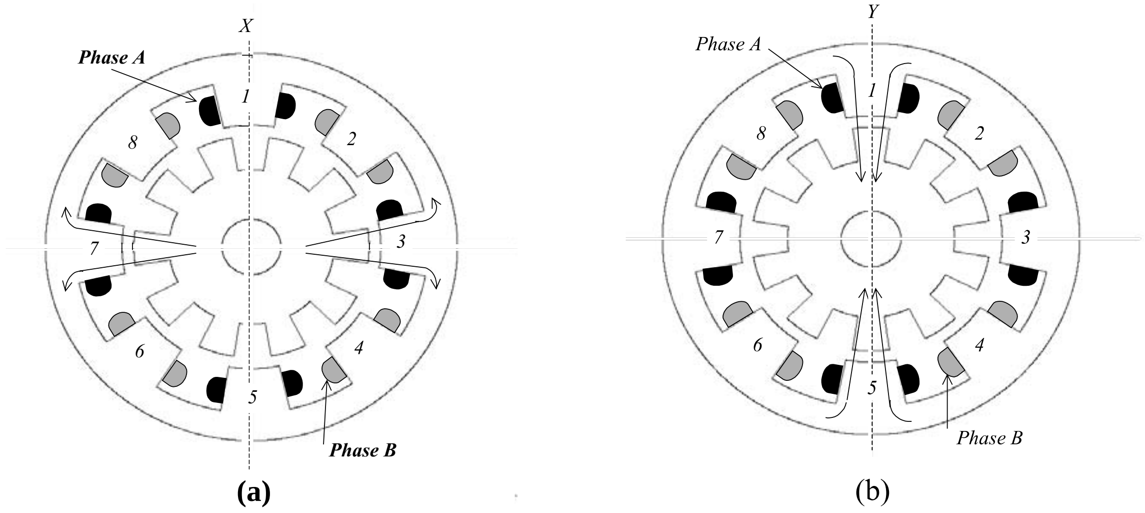


FIGURE 27.85 Cross section of the hybrid motor. (a) Section X; (b) section Y.

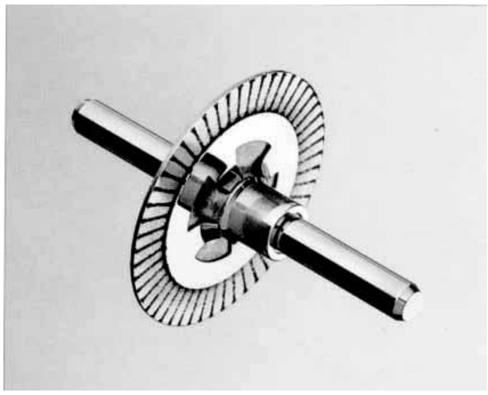


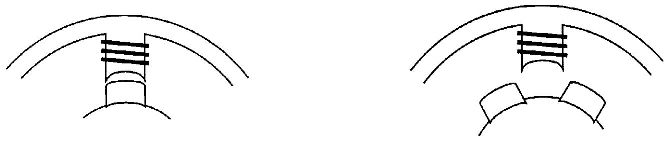
FIGURE 27.86 Rotor of a PM stepper motor. Courtesy: Escap Motors.

This torque expression may also be expressed as in (27.94) when it is further assumed that the inductance of the excited winding at any given position remains constant for all currents

$$T = \frac{1}{2} i^2 \frac{dL}{d\theta} \tag{27.94}$$

The developed torque is due to the variation of inductance (or reluctance) with position. Note that the direction of current has no bearing on the developed torque. When the stator and rotor poles are perfectly aligned, as indicated in Fig. 27.87a, the inductance L changes little with a small change in θ. The developed torque is thus very small around this position, corresponding to the position X in Fig. 27.82. When the stator and rotor teeth are unaligned, as in Fig. 27.87b, L changes more significantly with θ, and the restoring torque becomes much larger. As θ increases, $dL/d\theta$ goes through a maximum, producing $T_{\max}$. It should be noted that around a stable detent, L reduces as θ increases, so that the slope of the T–θ characteristic is negative at the origin. Beyond the position where $T_{\max}$ is developed, L increases as a result of the next set of rotor teeth coming under the stator teeth. This explains the drop in $T_{\max}$ and the positive slope of the T–θ characteristic in the region between where $T_{\max}$ is developed and Y in Fig. 27.82.

If stepper motors are operated in magnetically linear region where L remains constant with current for a given angular position, the developed torque per unit volume is small. Because of this, steppers motors are normally driven far into saturation. Equation (27.94) then does not represent the torque characteristic adequately.



(a) (b)

FIGURE 27.87 Stator and rotor teeth alignment. (a) Aligned position, $\theta = X$; (b) unaligned position, $\theta = Y$.

For a saturated stepper motor, the calculation of the T–θ characteristic for any given current involves complex computation of stored energy, or coenergy, for each position of the rotor. This requires the magnetization characteristics of the motor for different levels of stator currents and rotor positions to be known. Reference [1] at the end of this section may be consulted for further reading on this.

27.8.3.2 ybrid and PM Motors

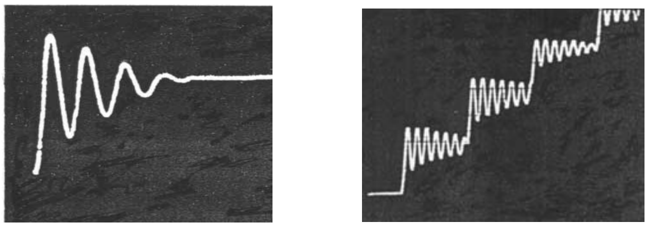
In hybrid stepper motors, most of the developed torque is contributed by the variable-reluctance principle explained earlier. The rest is developed by the rotor magnet in striving to find the minimum-reluctance position. It should be noted that the alternate polarities of the magnetic poles created by each winding may be reversed by the direction of its current. Consequently, the polarity of the winding currents also determine the direction in which the developed torque increases positively around a detent position.

27.8.4 Single- and Multistep Responses

When the rotor is at a detent position and phase currents are changed to a new value, the detent position is moved and the rotor proceeds towards it and settles down at the new detent position. The movement of the rotor is influenced by shape of the T–θ characteristic and the load friction. The rotor stepping is normally quite underdamped. The final positioning error is also determined largely by the load torque. For instance, if the T–θ characteristic is assumed to be a sinusoidal function of θ, the error in stepping is given by Eq. (27.95), where $T_{\max}$ is the peak of the T–θ characteristic and T_L is the load friction torque

$$\theta_e = \left| \sin^{-1}\left(\frac{T_L}{T_{\max}}\right) \right| \tag{27.95}$$

However, this error does not accumulate as further stepping is performed. If the phase currents are switched in succession, the rotor makes multiple steps. Typical single and multistep responses are as indicated in Fig. 27.88.



(a) (b)

FIGURE 27.88 Typical step responses of a stepper motor: (a) single-step response; (b) multistep response.

The maximum rate at which the rotor can be moved depends on several factors. The rise and fall times of the winding currents, which are largely determined by the electrical parameters of the windings and the type of drive circuits used, and the combined inertia and friction parameters of the motor and load are important factors.

The discrete signals to step the motor in the forward or reverse direction are translated into current-switching signals for the drive circuits. This translator is a simple logical operation that is embedded in most of the integrated circuits available for driving stepper motors.

In many applications, the stepper motor is operated at far higher speeds than it can start/stop from. The performance of a stepper motor at high speed is normally given in terms of its pull-out torque–speed (T–ω) characteristic. This characteristic indicates the maximum average torque the motor may develop while stepping continuously at a given rate. This torque is also largely determined by parameters of the motor and its drive circuits. Figure 27.89 indicates the typical shape of the pull-out T–ω characteristic of a stepper motor drive.

At low speed, the pull-out torque is roughly equal to the average value of the positive half-cycle of the T–θ waveforms of Fig. 27.82. At high speed, the finite but fixed rise and fall times of currents and the back emf of the winding reduces the extent to which the windings are energized during each switching period. Consequently, the pull-out torque of the motors falls as the stepping rate (speed) increases.

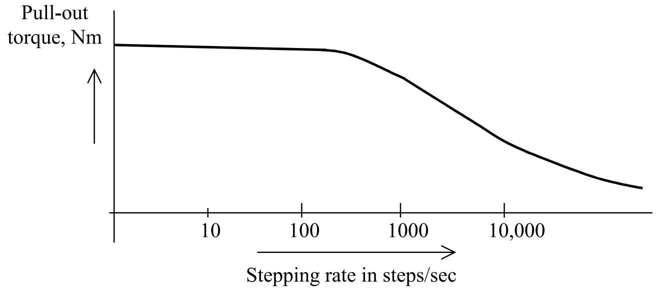


FIGURE 27.89 Typical pull-out torque characteristic of a stepper motor.

For operation at high speed, the stepping rate is gradually increased and decreased from one speed to another. Without careful acceleration and deceleration to and from a high speed, the motor will not be able to follow the stepping commands and will lose its synchronism with the stepping pulses or winding excitations. The acceleration and deceleration rates of a stepper motor are also determined largely by the pull-out torque characteristic.

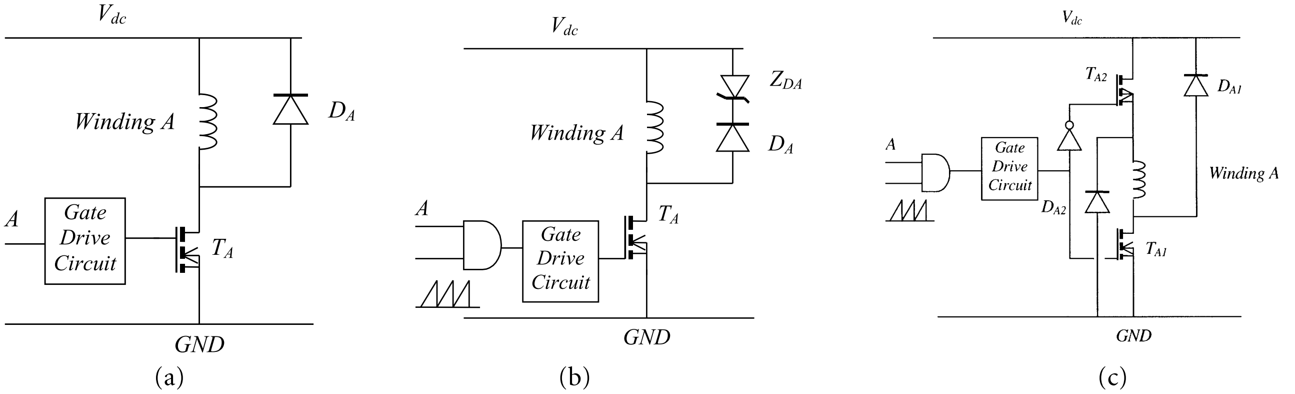
Stepper motors are known to suffer from mechanically induced resonance and consequent misstepping when its switching rate falls within certain bands, which are largely determined by the way the developed torque varies with time as the motor steps. Careful selection of stepping rate is normally employed to overcome the problem. Some shaft-mounted external damping measures may also be used when the stepping rate needs to be continuously varied, such as in the case of machine-tool profile following.

27.8.5 Drive Circuits

Two types of drive circuits are in general use for stepper motors. The unipolar drive is suitable for variable-reluctance stepper motors, for which the developed torque is determined by the level of current, not its polarity. For hybrid and permanent-magnet motors, the direction of current is also important, so that bipolar drive circuits are more suitable.

27.8.5.1 Unipolar Drive Circuits

In its simplest form, the unipolar drive circuits, one for each winding, are as indicated in Fig. 27.90. The transistor (MOSFET) is turned on to energize the winding, with a current that is limited either by the winding resistance or by hysteresis or PWM current controllers. The free-wheeling diode allows the winding current a circulating path when the transistor is turned off.



(a) (b) (c)

FIGURE 27.90 Three commonly used unipolar drive circuits: (a) the basic unipolar drive; (b) unipolar drive with PWM current limiting and Zener diode turn-off; (c) unipolar drive with regenerative turn-off.

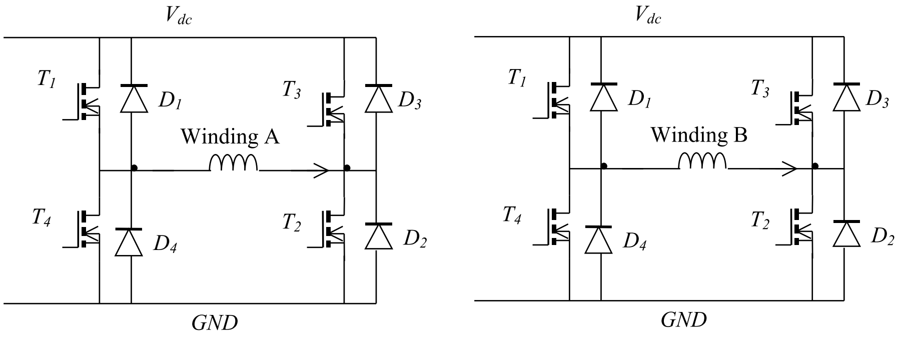


FIGURE 27.91 Bipolar drive circuit (gate-drive circuits omitted).

The drive circuit of Fig. 27.90a is a basic one. A better drive circuit is shown in Fig. 27.90b, which includes a zener diode in the freewheeling path. A pulse-width modulator is also included in the gate driving circuit. The pulse-width modulator allows a higher dc supply voltage (typically 5–10 times the voltage for the resistance-limited drive) to be used, thereby reducing the rise time of current at switch-on by 5 to 10 times. The zener diode allows a fast fall time for the current when the transistor is turned off by dissipating the trapped energy of the winding at switch-off faster. Yet another scheme is shown in Fig. 27.90c, which allows the trapped energy of the winding at switch-off to be returned to the dc source when the transistor is turned off, rather than being dissipated in the winding or the freewheeling circuits. This circuit is by far the most efficient, and at the same time gives the fastest possible rise and fall times for the winding currents.

27.8.5.2 Bipolar Drive Circuits

The bipolar drive allows the motor windings to driven with bidirectional currents. The four-transistor bridge drive circuit of Fig. 27.91; one for each winding, is the most popular. The circuit can cater to the required rise and fall times of the winding by properly selecting the dc supply voltage V_{dc}, the pulse-width modulator, and the current controller gains.

Some hybrid and PM motors come with four windings, two for each phase. These may be connected in series or parallel, depending on the torque characteristics desired. In any case, only two drive circuits of the type indicated in Fig. 27.91 are required.

27.8.5.3 Drive Circuits for Bifilar ound Motors

Hybrid stepping motors may also come with bifilar windings, which allow the simpler unipolar drive circuits to be used. These motors have two tightly coupled windings for each phase. Figure 27.92 illustrates two bifilar windings on stator pole and their unipolar drives. The two windings on each pole have opposite sense, so that the magnetic polarity is reversed by simply switching the other winding. Since only unidirectional current is involved, the unipolar drive circuits of Fig. 27.90a or 27.90b may be used at a considerable savings in terms of the drive circuits. This benefit, is however, derived at the cost of extra winding space, and hence larger volume, for the same torque.

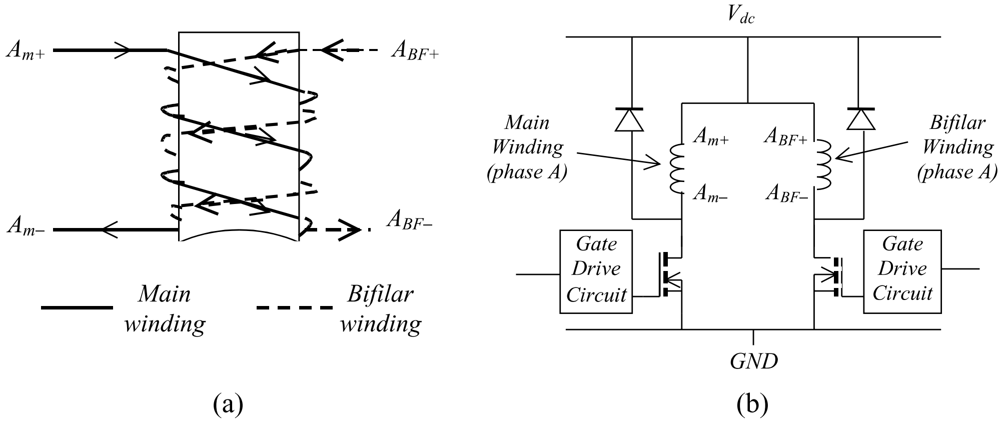
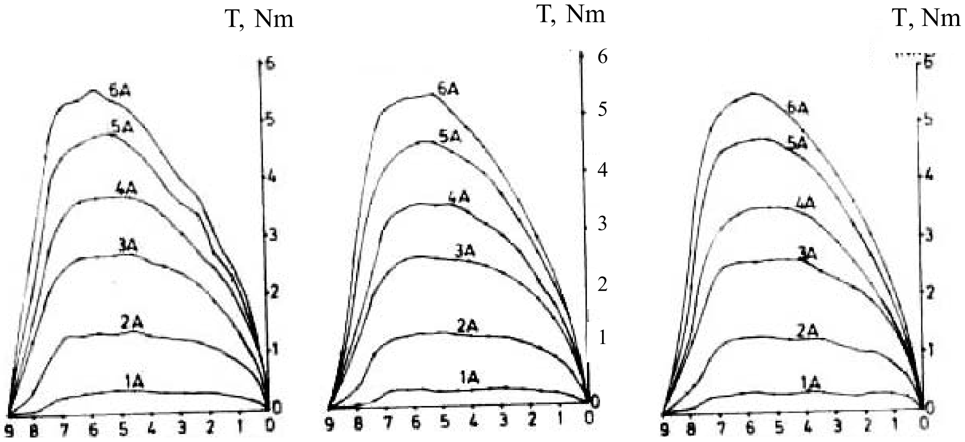


FIGURE 27.92 Drive circuits for one phase of a bifilar-wound motor. (a) Bifilar pole windings; (b) drive circuits.



Phase A Phase B Phase C

FIGURE 27.93 T–θ characteristics of a three-phase variable-reluctance motor.

27.8.6 Microstepping

The drive sequences mentioned in Section 27.8.2 normally switch rated current through the motor windings. These produce regular step angles. The half-stepping operation also uses rated motor currents. Halving of the step angle is arranged mainly through the selection of the windings switched. In microstepping, the regular step angle of the motor is subdivided further by a factor, typically from 10 to 100, by energizing the winding partially, with combinations of currents ranging from zero to full rated value in more than one winding simultaneously. This does not lead to any sacrifice of the developed torque, since the phase currents are so selected that the peak of total torque contributed by two partially energized windings is not lower than the peak detent torque $T_{\max}$ obtained in regular stepping.

The idea behind microstepping is readily understood when it is considered that by increasing the current in phase A of a two-phase hybrid in 10 equal steps to full value and decreasing the current in phase B in a similar manner, the motor step size may be divided by a factor of 10. If closed-loop current controllers are added to the two drive circuits of Fig. 27.91 and distinct current references are obtained from a reference generator, a complete microstepping drive is realized.

In microstepping, the two current references must have values such that the motor does the following:

1. Develops the same $T_{\max}$ for every combination of winding currents
2. Develops the same torque slope, i.e., $dT/d\theta$ at every microstepping detent position
3. Dissipates no more than the rated power loss (I^2R) for every combination of winding currents

The preceding conditions are necessary if the motor is to retain its static accuracy, maximum torque, and power dissipation characteristics.

The static torque characteristics (Fig. 27.92) of stepper motors are close to but not exactly sinusoidal functions of angle θ. The required current references for all windings of a stepper motor, including the variable reluctance motor of three or more phases, can easily be calculated from the data of the T–θ characteristics of the motor for each phase for various currents and rotor positions. A typical set of T–θ data for a three-phase variable-reluctance motor is shown in Fig. 27.93. The application of the three conditions mentioned earlier leads to an unique set of current references for each phase of the motor for each microstep. Figure 27.94 shows the current references for this motor for microstepping.

In multistepping operation, these microstepping current references have to be issued to the current controllers for each phase, at a rate determined by the commanded stepping rate.

Care has to be taken in designing the phase current controllers so that actual winding currents match the current references in both single and multistepping operation up to the maximum stepping rate desired. Since the current references are time varying, high-bandwidth current controllers are normally required to cover the desired speed range.

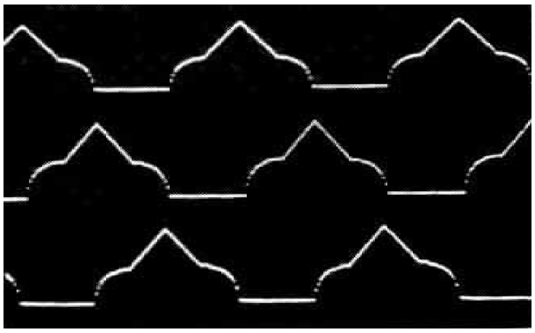


FIGURE 27.94 Microstepping current references for the VR motor of Fig. 27.93. Stepping rate: 28,800 steps/s, $I = 6$ A (maximum).

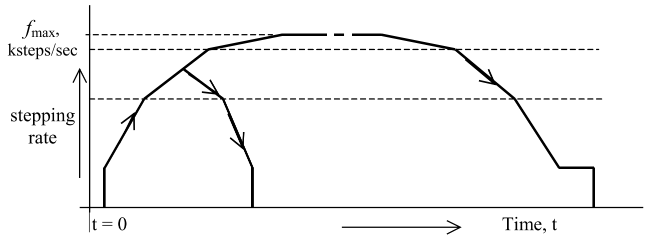


FIGURE 27.95 Typical acceleration/deceleration profiles.

27.8.7 Open-Loop Acceleration Deceleration Profiles

As mentioned in Section 27.8.4, many applications require the stepper motors to be driven far above the stepping rates to and from which the motor can start and stop abruptly without losing or gaining any step. This calls for carefully designed acceleration/deceleration profiles that the stepping pulse rate must not exceed.

The number of steps the motor is to be stepped and its direction are normally under the control of the motion controller. Once this reference is known, a digital timer/counter circuit can be used in the controller to progressively adjust the time between the stepping pulses such that a prescribed acceleration/deceleration profile, as indicated in Fig. 27.95, is followed. The timer/counter and the pulsing sequence controller (the translator) need to be managed in real time to execute the motion-control task at hand.

The fastest acceleration–deceleration profile a stepper motor is capable of is largely determined by its pull-out (T–ω) characteristic, which in turn is determined by the motor winding parameters and the drive circuit. An optimized stepping profile to and from the top speed may have a number of segments, as indicated in Fig. 27.95. These profiles are easily computed from the pull-out (T–ω) characteristic by integrating the dynamic torque balance equation of the drive. For a large positioning angle, the entire profile, including some constant-speed running at the top speed, may be used. For short positioning angles, only part of the profile may be traversed. In general, a single-segment acceleration–deceleration profile is used in commercial stepper motor controllers, so as to avoid a great deal of realtime number crunching by the profile controller.

The overall stepper motor controller thus consists of the blocks depicted in Fig. 27.96.

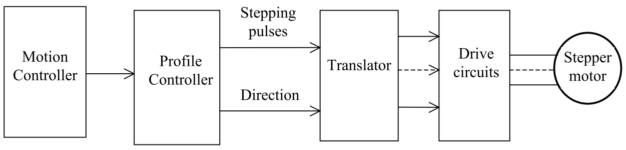


FIGURE 27.96 Structure of an open-loop motion controller for a stepper motor.

27.7.8 urther Reading

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27. Switched-Reluctance Motor Drives

Adrian Cheo

27. .1 Introduction

The switched-reluctance (SR) motor is a doubly salient electric machine with salient poles on both the stator and rotor. The machine is operated by switching current pulses to each stator winding on and off in a continuous switching sequence. The rotor poles have no excitation. Figure 27.97 shows the physical topology of a typical SR motor. The diagram illustrates a motor with eight salient stator poles (numbered A1 to D2) and six salient rotor poles (numbered 1 to 6). Although many combinations of the number of stator and rotor poles are possible, this particular type has found widespread use.

The phase windings on the stator of the SR motor consist of concentrated windings wrapped around the stator poles. In the conventional arrangement each stator pole winding is connected with that of the diametrically opposite pole to

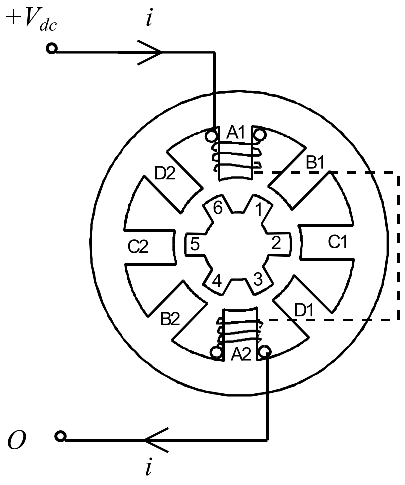


FIGURE 27.97 Four-phase SR motor topology.

form a stator phase. In Fig. 27.97, the connected stator pole pairs are indicated by the same prefix letter.

The general principle of operation of the SR motor is the same as all types of reluctance machines, i.e., the stator and the rotor poles seek the minimum-reluctance position, so that the stator excited flux becomes maximum. Hence, when current flows in an SR motor stator phase and produces a magnetic field, the nearest rotor pole will tend to position itself with the direction of the developed magnetic field. This position, which is termed the *aligned position*, is reached when the rotor pole center axis is aligned with the stator pole center axis (assuming symmetrical poles). The aligned position also corresponds to the position of minimum reluctance, and hence the position of maximum inductance.

It should be noted that the *unaligned* position is defined as the position when the *interpole axis*, or the axis of the center of the interpolar space in the rotor, is aligned with a stator pole axis. This position corresponds to the position of minimum inductance. These rotor axis positions are illustrated in Fig. 27.98.

To achieve continuous rotation, the stator phase currents are switched on and off in each phase in a sequence according to the position of the rotor. Consider the motor schematic illustrated in Fig. 27.97. If coils A1 and A2 of phase A are excited and produce a magnetic field in a vertical direction, then poles 1 and 4 on the rotor will align themselves with the stator poles of phase A. If the coils of phase A now have their current switched off, and coils B1 and B2 of phase B are now excited, then in a similar fashion the rotor will move so that poles 2 and 5 are aligned with stator poles B1 and B2. Exciting phases A, B, C, and D in sequence will produce rotor rotation in the counterclockwise direction.

From the preceding discussion, one may see that the switching on and off of excitation current to the motor phases is related to the rotor pole positions. This means that some form of position sensor is essential for the effective operation of the SR motor.

27. .2 Advantages and Disadvantages of Switched-Reluctance Motors

The SR motor has a number of inherent advantages that makes it suitable for use in certain variable-speed drive applications. Nevertheless, the motor also has some inherent disadvantages that must be considered before choosing the motor for a particular application. In Table 27.6, the main advantages and disadvantages of the SR motor drive are summarized.

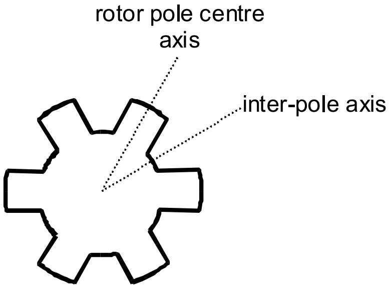


FIGURE 27.98 Rotor pole axis positions.

TABLE 27.6 Advantages and disadvantages of SR drives

Advantages	Disadvantages
Low-cost motor	Need for position measurement
Robust motor construction	Higher torque ripple than other machine types
Absence of brushes	
No motor short-circuit fault	Higher noise than other machine types
No shoot-through faults	
Ability to operate with faulted phase	Nonlinear and complex characteristics
High torque-to-inertia ratio	
Unidirectional currents	
High efficiency	

27. .3 Switched-Reluctance Motor Variable-Speed Drive Applications

The main application for SR motors is in variable-speed drive systems. One application area has been general-purpose industrial drives where speed, acceleration, and torque control are desired. SR-motor-based industrial drives provide the advantages of a very wide range of operating speeds as well as high efficiency and robustness. Other applications of the SR drive include automotive applications, where the SR motor has advantages of robustness and fault tolerance. The SR motor in this application can also be easily controlled for acceleration, steady speed, and regenerative braking.

The SR motor is also well suited to aerospace applications where the ability to operate under faulted conditions and its suitability for operation under harsh environments are critical. Additionally, the very high speed capability and high power density also make these motors well suited in the aerospace field. There are also many domestic appliances where cost is of primary concern. In these products, the SR motor can provide a low-cost solution for a brushless fully controllable motor drive. In addition, the motor can be used in battery-powered applications, where the motor's high efficiency and ability to use a dc supply are important.

27. .4 SR Motor and Drive Design Options

The main components of the drive system are shown in Fig. 27.99. It is important to design the motor and drive together in an integrated manner. The main criteria that need to be considered in designing the components of the SR drive system will be discussed later. It will be seen that certain design choices, which may be advantageous for one component of the drive system, may bring about disadvantages in another component. This highlights the need for a careful, integrated system approach to be taken when designing the drive system.

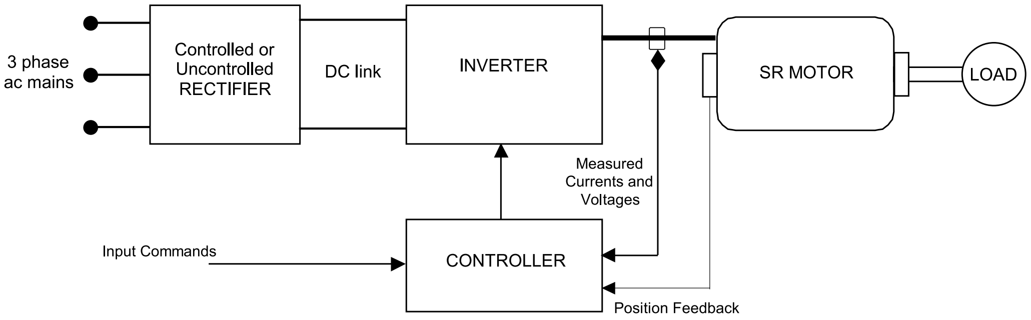


FIGURE 27.99 Main components of an SR drive.

27. .4.1 Number of Motor Phases

There are many possibilities in choosing the number of stator phases and rotor poles in SR motors. The simplest SR motor may consist of only one phase; however, to operate the motor in four quadrants (motoring or generating in both forward or reverse directions), at least three phases are required. The most common configuration to date has been the four-phase SR motor, which has eight rotor poles and six stator poles, as was shown in Fig. 27.97.

27. .4.2 Maximum Speed

The SR motor is capable of operating at very high speeds because of its robust rotor construction, and in most applications the maximum speed is limited by the inverter switching speed and not limited by the motor itself. The maximum speed of the SR motor is itself normally greater than 15,000 rpm for a standard SR motor.

However, to determine the maximum drive speed, the controller and motor must be considered together. This is because the power electronic device switching speed is directly proportional to the commutation frequency, which is in turn proportional to the motor speed. The maximum switching frequency of the power devices must therefore be taken into account in the SR drive design.

27. .4.3 Number of Power Devices

In general, the number of switches per phase in SR motor drives will vary according to the inverter topology. A wide range of different SR drive circuits are available for SR drives, and these are detailed below. Circuits with only one switch per phase are possible; however, these have various disadvantages such as control restrictions, a need for extra windings, or higher switch voltages. However, with two switches per phase the motor is fully controllable in four quadrants and has completely independent motor phase control. Therefore, the maximum number of power switches required for the motor operation is normally $2q$, where q is the number of phases.

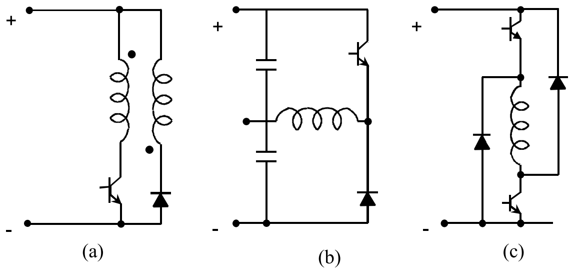
27. .4.4 Inverter Topology Types for SR Motors

As was mentioned, the torque produced in the SR motor is independent of the direction of current flow in each motor phase. This means the inverter is only required to supply unidirectional currents into the stator windings. The three major circuit topology types that have been used each winding of an SR motor drives are shown in Fig. 27.100. As indicated in this figure, these are commonly termed the *bifilar*, *split dc supply*, and *two-switch* type inverter circuits.

In the circuits shown in Fig. 27.100, only one or two switching components per phase are required. Other circuit topology types that use shared components between the motor phases have limitations in control flexibility.

. . . . *Bifilar-Type Inverter Circuit* In Fig. 27.100a, a drive circuit for a bifilar-wound SR motor is shown. The bifilar windings are closely coupled, with one winding being connected to a switching device while the other is connected to a freewheeling diode. Current is increased in the winding when the switching device closes. At turn-off, the current transfers to the secondary winding through transformer action, and the inductive energy flows back into the supply via the freewheeling diode. If perfect coupling is assumed, then the voltage across the switching device will rise to twice the dc supply voltage during turn-off. However, in practice this would be higher. This is because there will be some uncoupled inductance in the primary that will cause high induced voltages when the current in the winding collapses to zero. Thus, snubbing circuits would almost certainly be required to protect the switching components from overvoltage.

The advantage of the bifilar circuit is that it requires only one switching device per phase. However, with the advent of



(a) (b) (c)

FIGURE 27.100 Major SR inverter topology types: (a) bifilar type; (b) split dc supply type; (c) two-switch type.

modern power electronic devices, which have both low cost and low losses, this advantage quickly disappears.

. . . . ***Split dc Supply Inverter Circuit*** The split dc supply type inverter circuit shown is shown in Fig. 27.100b. As in the bifilar circuit, this configuration also uses only one switching device and one diode per phase. However, a center-tapped dc source is required. When the switching device is turned on, current increases in the phase winding because of the positive capacitor voltage being applied. At turn-off, the current is forced to flow through the diode and thus decays to zero more quickly because of the connection to the negative voltage. It is usual for the dc center tap to be implemented using a split capacitor in the dc link. The voltages across each capacitor must remain balanced, which means that there can be no significant power-flow difference between the two capacitors.

Upon examination of the circuit, it can be seen that because of the split capacitor bank, only half the available dc voltage can be switched across the phase winding. Thus, for the same voltage across the motor phases that is supplied by the bifilar circuit earlier, the dc supply voltage must be doubled with respect to the bifilar circuit supply. This means that the voltage rating of the devices would effectively be the same as in the bifilar circuit. This is inherently inefficient. The configuration also has the need for balanced split capacitive components. In addition, it will be seen that the *soft-chopping* form of control described in Section 27.9.7 is not available in this drive.

. . . . ***Two-Switch Inverter Circuit*** The two-switch inverter type circuit, which is shown in Fig. 27.100c, uses two switching devices and two diodes per phase. Unlike the previous two circuits, three modes of operation are possible:

Mode 1: Positive phase voltage. A positive phase voltage can be applied by turning both switching devices on. This will cause current to increase in the phase winding.

Mode 2: Zero phase voltage. A zero voltage loop can be imposed on the motor phases when one of the two switches is turned off while current is flowing through the phase winding. This results in current flow through a freewheeling loop consisting of one switching device and one diode, with no energy being supplied by or returned to the dc supply. The current will decay slowly because of the small resistance of the semiconductors and connections, which leads to small conduction losses. This mode of operation is used in soft chopping control, as described in Section 27.9.7.

Mode 3: Negative phase voltage. When both switches in a motor phase leg are turned off, the third mode of operation occurs. In this mode, the motor phase current will transfer to both of the freewheeling diodes and return energy to the supply. When both of the diodes in the phase circuit are conducting, a negative voltage with amplitude equal to the dc supply voltage level is imposed on the phase windings.

In this circuit the switching devices and diodes must be able to block the dc supply voltage amplitude when they are turned off, in addition to any switching transient voltages. However, because the circuit contains two devices in series, the blocking voltage is essentially half the value seen in the previous two circuit types for the same applied motor phase voltage amplitude. Another advantage of the two-switch inverter circuit is that it offers greater control flexibility with its three modes of voltage control.

A disadvantage of this inverter type, as compared to the bifilar and split dc supply types, is that it contains twice as many switching components per phase. However, with the current wide availability and economy of power semiconductors, in most applications the advantages of the two-switch circuit outweigh the cost of an extra switching device per phase.

27. .5 Operating Theory of the Switched-Reluctance Motor Linear Model

If a linear magnetic circuit is assumed, the flux linkage is proportional to phase current for any rotor position θ. This is demonstrated in Fig. 27.101, where the magnetization curves for the linear SR motor for various rotor positions and currents are shown. In this linear case, the inductance L at

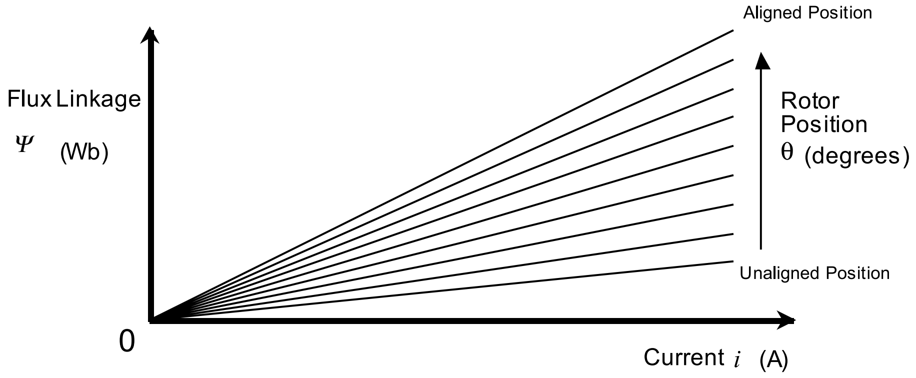


FIGURE 27.101 Magnetization characteristics of linear SR motor.

any position θ, which is the slope of these curves, is *constant* and independent of current.

As the motor rotates, each stator phase undergoes a cyclic variation of inductance. As can be seen in Fig. 27.101, in the fully aligned position (when a rotor pole axis is directly aligned with the stator pole axis) the reluctance of the magnetic circuit through the stator and rotor poles will be at a minimum, and thus the inductance of the stator winding will be at a maximum. The opposite will occur in the fully unaligned position (when the rotor interpole axis is aligned with the stator pole). Thus, the inductance becomes a function of position only and is not related to the current level. If it is also assumed that mutual inductance between the phases is zero, then a typical inductance variation $L(\theta)$ with respect to rotor position similar to that shown in Fig. 27.102 arises. Although this is an idealized inductance variation, it is helpful in the understanding of key operating principles of the machine. One should note that in the idealized inductance variation there are sharp corners, which can only arise if flux fringing is completely ignored.

Four distinct regions can be identified in the plot of the linear inductance variation shown in Fig. 27.102. These distinct regions correspond to a ranges of rotor pole positions relative to the stator pole positions as be described below:

Region A. This region begins at rotor angle θ_1, where the first edge of the rotor, with respect to the direction of rotation, just meets the first edge of the stator pole. The inductance will then rise in a linear fashion until the poles of the stator and rotor are completely overlapped at angle θ_2. At this point, the magnetic reluctance is at a minimum and the phase inductance is at a maximum. These rotor positions are illustrated in Figs. 27.103a and 27.103b for an example four-phase motor with rotor pole 1 approaching the stator pole of phase A.

Region B. This region spans from rotor positions θ_2 to θ_3. In this region, the inductance remains constant because the rotor pole is completely overlapped by the stator pole (i.e., the overlap area of the poles remains constant). At rotor angle θ_3 the edge of the rotor pole leaves the stator pole overlap region, and thus the area of overlap will again begin to decrease. The position at which this occurs is illustrated in Fig. 27.103c.

Region C. When the rotor moves past θ_3, the rotor pole leading edge begins to leave the pole overlap region, and region C begins. At this point, the inductance begins to linearly decrease, until at θ_4, the rotor pole has completely left the stator pole face overlap region. At this point the inductance is at its minimum once more. The rotor

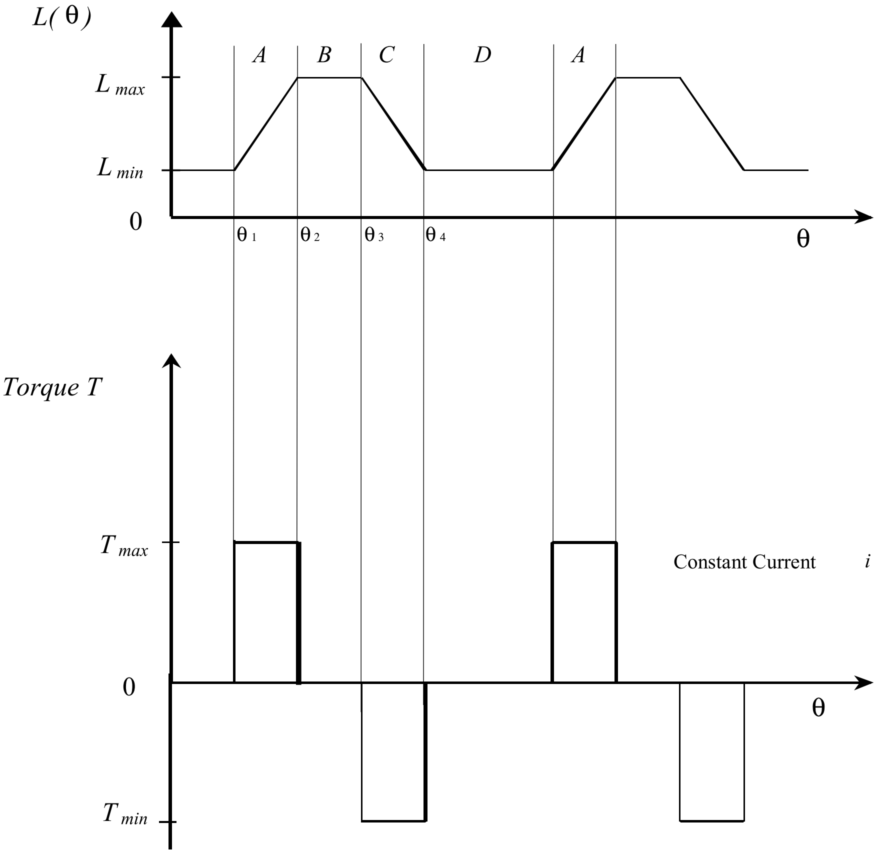


FIGURE 27.102 Typical linear inductance variations and corresponding torque variations for constant-phase current.

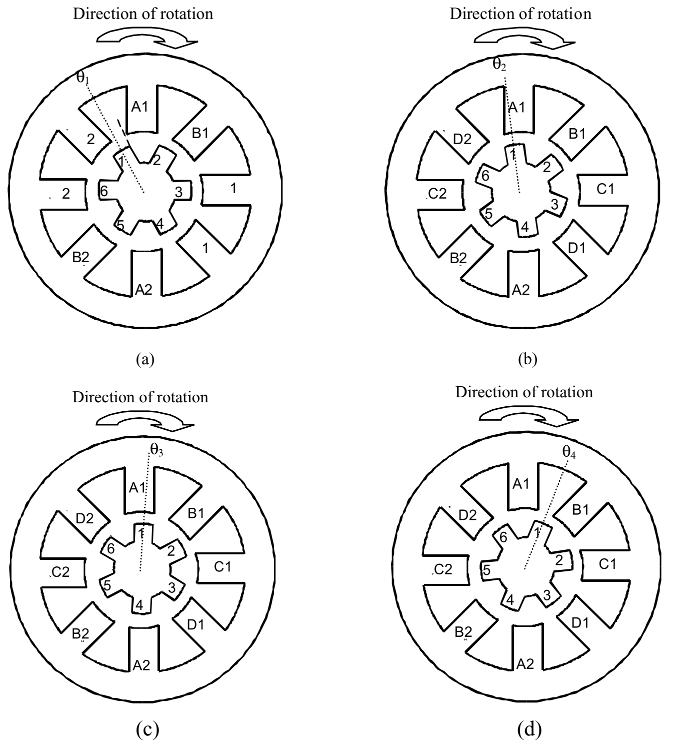


FIGURE 27.103 Rotor pole 1 positions. (a) Meeting edge of stator pole A. (b) Overlapped by stator pole A. (c) Edge of rotor pole leaving overlap region. (d) Rotor pole completely leaving overlap region. (Note: Airgap space is exaggerated for clarity.)

position at which the rotor pole has completely left the overlap is indicated in Fig. 27.103d.

Region D. In this region the rotor and stator have no overlap, and thus the inductance remains constant, at the minimum level, until region A is reached once again.

It was mentioned earlier that when a stator phase is excited, the rotor poles will tend to move toward the maximum-inductance region. Thus, a motoring torque is produced when a stator phase is provided with a current pulse during the angles when the inductance is rising (assuming motoring rotation is in the direction of increasing θ in Fig. 27.102. This means that if positive torque is desired, excitation should be arranged such that current flows between the appropriate rotor angles when the inductance is rising.

Conversely, if current flows during the decreasing inductance region, a negative torque would result. This is because the rotor will be attracted to the stator pole in such a way that it rotates in the opposite direction to the motoring rotation, or in other words, the rotor experiences a torque opposite to the direction of rotation.

It should be noted that this reluctance machine torque always acts to decrease the reluctance. The direction of current flowing into the stator winding is irrelevant. This signifies that unidirectional current excitation is possible in the SR motor drive.

The variation of torque with rotor angle for a constant phase winding current is as shown in Fig. 27.102. It can be seen that the torque is constant in the increasing and decreasing inductance regions, and is zero when the inductance remains constant.

The preceding physical explanation of the developed torque is also given by the familiar torque equation (27.96) for a variable-reluctance machine

$$T = \frac{1}{2} i^2 \frac{dL(\theta)}{d\theta} \tag{27.96}$$

From (27.96) it is evident that the magnitude of the instantaneous torque developed in the SR motor is proportional to both i_2 and $dL/d\theta$. If the inductance is increasing with respect to the angle, and current flows in the phase winding, then the torque will be positive and the machine will operate in motoring mode. Hence, from Eq. (27.96) it can be seen that when the motor phase is excited during a rising inductance region, part of the energy from the supply is converted to mechanical energy to produce the torque, and another part is stored in the magnetic field. If the supply is turned off during this region, then any stored magnetic energy is partly converted to mechanical energy and partly returned to the supply.

However, a negative or braking torque will be developed by the motor if the inductance is decreasing with respect to the rotor angle and current flows in the phase winding. In this case energy flows back to the supply from both the stored magnetic energy and the mechanical load, which acts as a generator.

It can also be seen from Eq. (27.96) that the sign (or direction) of the torque is independent of the direction of the current and is only dependent on the sign of $dL/d\theta$. This explains the torque waveforms that were seen in Fig. 27.102, where for constant current (and constant $dL/d\theta$ magnitude), the magnitude of the torque was constant in the rising or decreasing inductance regions. However, it was seen that the torque changes from positive to negative according to the sign of $dL/d\theta$.

Hence, the ideal waveform for the production of motoring torque would be a square-wave pulse of current (with magnitude equal to the maximum possible supply current) flowing only during the increasing inductance period. This current waveform is illustrated in Fig. 27.104b. However, in practice this type of current waveform is difficult to produce in a motor phase. This is because the motor phase current is supplied from a finite dc voltage source, and thus inductance of the stator phase winding would delay the rise and fall of current at the pulse edges. Instead, a more practical current waveform is normally used as is illustrated in Fig. 27.104c. It can be seen that in this waveform the ideal square waveform is

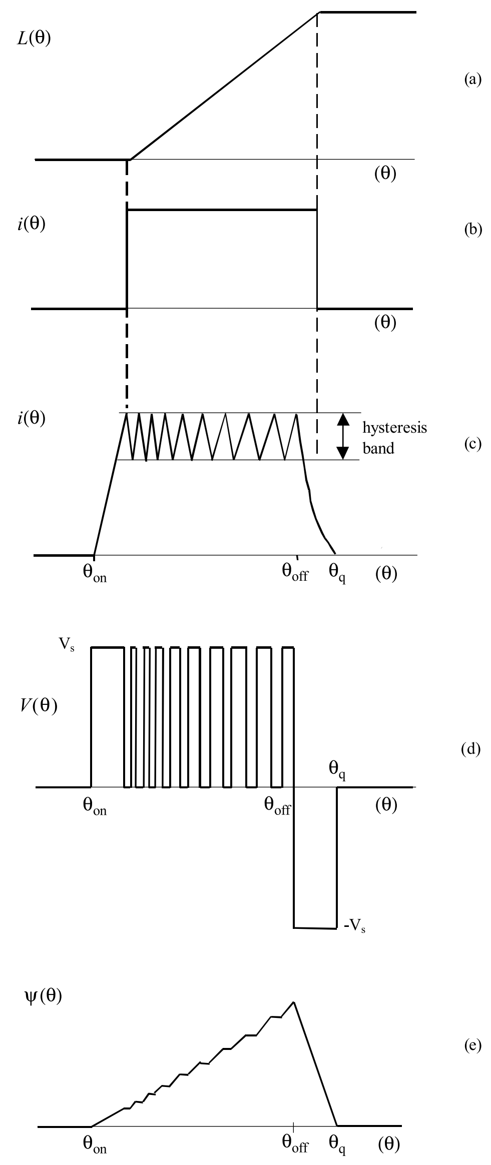


FIGURE 27.104 (a) Linear phase inductance variation. (b) Ideal square-wave phase current. (c) Chopping-mode phase current. (d) Chopping-mode phase voltage. (e) Flux linkage waveform corresponding to chopping-mode current.

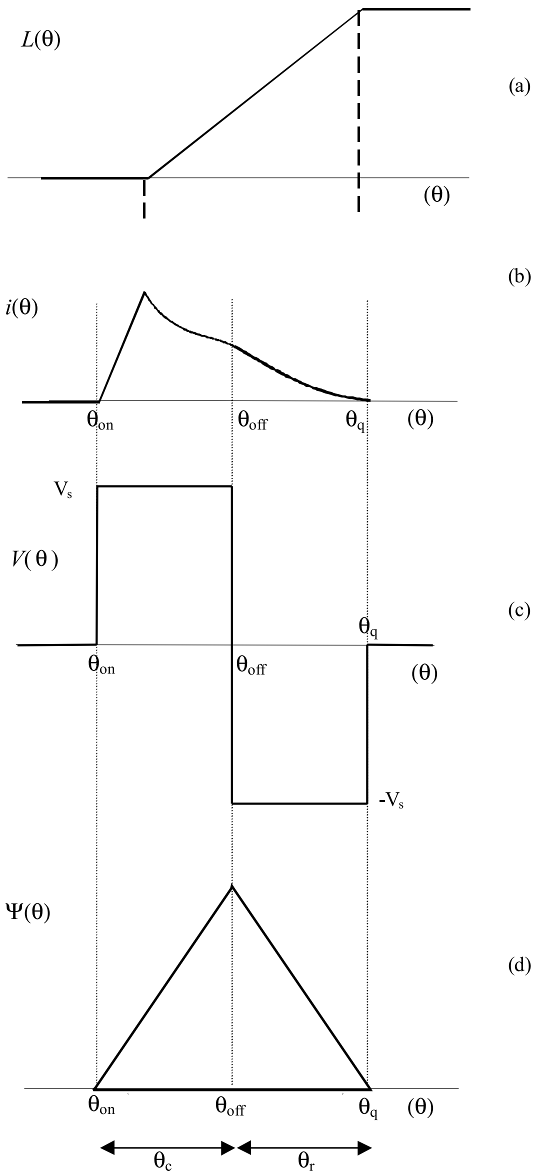


FIGURE 27.105 (a) Linear phase inductance variation. (b) Single-pulse-mode phase current. (c) Single-pulse-mode phase voltage. (d) Flux linkage waveform corresponding to single-pulse-mode current.

closely approximated by the use of hysteresis current control. At higher speeds hysteresis current control can no longer be used and a current waveform similar to that shown in Fig. 27.105b is seen in the phase winding. These two types of practical current waveforms, which approximate the ideal square-pulse waveform (a) at *low to medium speeds* and (b) at *high speeds*, will be discussed next.

27. .5.1 Low- to Medium-Speed Approximation to Square-Pulse Current Waveform

At low to medium motor speeds, the ideal square-pulse current waveform is approximated in the practical motor drive using hysteresis current control, as is shown in Fig. 27.104c. The hysteresis method of controlling the current is termed the *chopping-mode control* method in SR motor drives. During the time of conduction (between the turn-on and turn-off angles), the current is maintained within the hysteresis band by the switching off and on of the phase voltage by the inverter when the phase current reaches the maximum and minimum hysteresis band. An example of the voltage waveform used for the hysteresis current control is shown in Fig. 27.104d, where a constant inverter dc supply voltage of magnitude V_s is used. It can be seen that the switching frequency of the voltage waveform decreases as the angle increases. This is due to the fact that the phase inductance is linearly increasing with angle, which has the effect of increasing the current rise and fall time within the hysteresis band.

In the chopping-mode control method, the *turn-on region* is defined as the angle between the *turn-on angle* θ_{on} and the *turn-off angle* θ_{off}, and is chosen to occur during the rising inductance region for motoring torque. In the practical chopping current waveform, the current turn-on angle θ_{on} is placed somewhat before the rising inductance region. This is to ensure that the current can quickly rise to the maximum level in the minimum-inductance region before the rising-inductance, or torque-producing, region. Similarly, the turn-off angle θ_{off} is placed a little before the maximum inductance region so that the current has time to decay before the negative-torque, or decreasing-inductance, region. The angle at which the current decays to zero after turn-off is labeled as θ_q in Fig. 27.104c.

27. .5.2 High-Speed Approximation to Square-Pulse Current Waveform

The chopping mode of operation cannot be used at higher speeds, as at these speeds the hysteresis band current level will not be reached. This is because at high speeds the back emf of the motor becomes equal to or larger than the voltage supply in the rising-inductance region, which limits the increase of the motor phase current. In addition, the rise time of the current will correspond to an ever-increasing angle as the speed is increased. Eventually, at high speeds, the rise-time angle will be so large that the turn-off angle θ_{off} will be reached before the hysteresis current level has been exceeded. Thus, at high speeds the current is switched on and off only once per cycle. In SR motor drive control, this is called the *single-pulse mode* of operation. An example of the single-pulse mode current is illustrated in Fig. 27.105b.

In the single pulse mode of operation, the inverter power switches turn on at rotor angle θ_{on}, which places the dc voltage supply V_s across the phase winding, as is shown for the example single-pulse voltage waveform in Fig. 27.105c.

As for the chopping-mode case, in order to maximize torque θ_{on} must usually be located prior to the rising inductance region. This is so that, while the inductance is low, the current has a chance to rise rapidly to a substantial value before the torque-producing region begins and the motor back emf increases. At rotor angle θ_{off}, the power switches are turned off, and the phase will have a negative voltage (typically $-V_s$) thrown across it. The current will then decay until it becomes zero at rotor angle θ_q.

27. .6 Operating Theory of the SR Motor II Magnetic Saturation and Nonlinear Model

In the linear model described earlier, it was assumed that the inductance of a phase winding is independent of current. However, in a real SR motor significant saturation of the magnetic circuit normally occurs as the phase current increases, and thus the phase inductance is related to both the phase current level and position. Because of the magnetic saturation effect, the actual phase inductances at a given rotor position can be reduced significantly compared to the inductance given by linear magnetization characteristics. In addition, the effect of magnetic saturation becomes larger as the motor current level increases.

The effects of saturation in an SR motor can be observed in a plot of its magnetization curves. This shows the relationship of flux linkage versus current, at rotor positions varying between the fully aligned and unaligned angles. A typical set of SR motor magnetization curves is shown in Fig. 27.106, where it can be seen that there is a nonlinear relationship between the flux linkage and current for each curve.

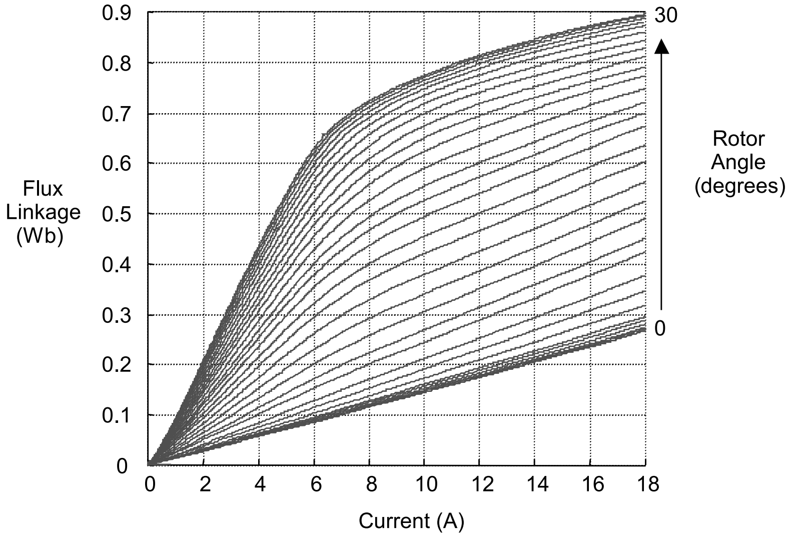


FIGURE 27.106 Measured four-phase SR motor magnetization characteristics (each curve represents a constant rotor position).

Because of the magnetic saturation effect discussed earlier, the instantaneous torque equation (27.96), which was derived assuming linear conditions, will not be generally valid for calculating the torque in SR motors. Therefore, for accurate calculations, the torque must take into account the dependence of phase inductance with current and position.

If one considers the phase inductance saturation, the expression for instantaneous torque production of an SR motor phase can be written as

$$T = \left[\frac{\partial W'}{\partial \theta}\right]_{i=constant} \tag{27.97}$$

where the coenergy W' is defined as

$$W' = \int_0^i \Psi \, di \tag{27.98}$$

27. .7 Control Parameters of the SR Motor

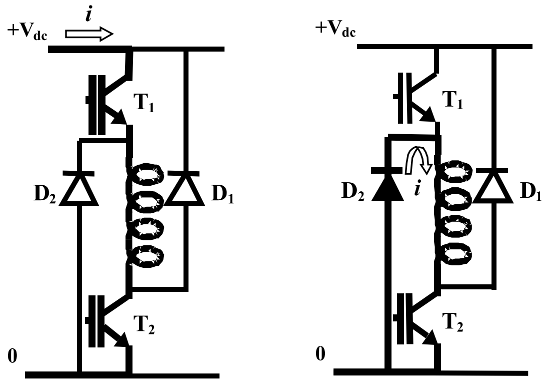
A variety of performance characteristics can be obtained in the SR motor by controlling various parameters. These parameters include the chopping-mode control hysteresis level at low to medium speeds, and the turn-on and turn-off angles θ_{on} and θ_{off} at all motor speeds. By controlling these parameters it is possible to produce any desired characteristic such as constant torque, constant power, or some other particular characteristic in between.

As discussed in Section 27.9.5, two distinct modes of operation apply in the SR motor depending on the nature of the current waveform. These modes are the chopping-mode control, which can be used at low to medium motor speeds, and the single-pulse mode of control, which is used at high speeds. Both of these modes of operation will be further detailed hereafter, with an explanation of the corresponding inverter switching operation.

27. .7.1 Chopping-Mode Control

In the chopping-mode control region, the turn-on and turn-off angles are controlled together with the current level. As described in Section 27.9.5, the turn-on angle and turn-off angle are controlled so that current flows during the rising-inductance or positive torque-producing region. This normally means that the turn-on angle is placed shortly before the place where the rising inductance angle begins, and the turn-off angle is placed shortly before this region ends.

In the chopping mode, the current level is controlled to remain below the maximum allowable level. This involves switching the voltage across the phase on and off in such a manner that the current is maintained between some chosen upper and lower hysteresis current levels. An example of this form of current chopping control was shown in Fig. 27.104c.



(a) (b)

FIGURE 27.107 Soft chopping mode conduction paths: (a) both devices on positive voltage applied to motor phase; (b) T1 turned off zero-voltage freewheeling loop applied to motor phase.

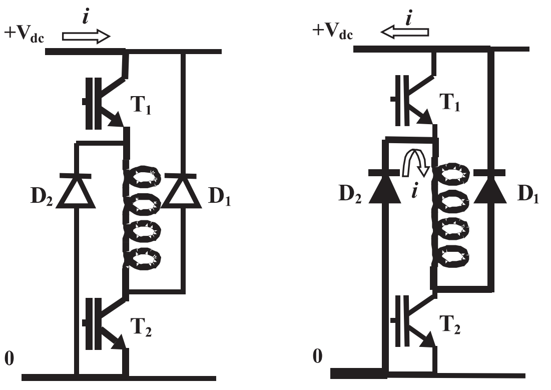
The actual torque production of the motor in the chopping mode is set by the control turn-on and turn-off angles and the current hysteresis level. Within the chopping mode of operation, two current hysteresis control schemes can be used. These are termed *soft* and *hard* chopping. Soft chopping can only be used in some circuit configurations, such as that shown in Fig. 27.107. For soft chopping control one switching device remains on during the entire conduction period while the other is switched on and off to maintain the desired current level. This can be seen in Figs. 27.107a and 27.107b, where the two conduction modes during chopping are shown. When both switches are on, the phase winding receives the full positive supply, whereas when only one switching device is on, the phase experiences a zero-voltage freewheeling loop that will decrease the current.

In the hard-chopping scheme, both devices are switched simultaneously and have the same switching state at all times. If both switching devices are turned on, the phase winding sees the full positive supply. To decrease the current, the full negative supply is applied by turning both devices off as shown in Fig. 27.108. In circuit configurations with fewer than two switches per phase, only hard chopping can be used.

Soft chopping is more advantageous than hard chopping. This is because of a smaller dc ripple current in the supply, which can substantially minimize the ripple-current rating of the dc link capacitor, as well as lower the hysteresis loss in the motor. It has also been found that soft chopping lowers acoustic noise and electromagnetic radiation.

27. .7.2 Single-Pulse Mode Control

At higher speeds, the back emf of the SR motor eventually becomes greater than or equal to the supply voltage during the rising-inductance region. This means that even if a phase is excited, the current in the motor phase will not increase in the rising inductance region. Therefore, at higher speeds the turn-



(a) (b)

FIGURE 27.108 Hard chopping mode conduction paths: (a) both devices on positive voltage applied to motor phase; (b) T1 and T2 turned off negative voltage applied to motor phase.

on angle must be placed before the beginning of the increasing inductance region, so that the phase current will have an adequate time to increase before the back emf becomes high.

In addition, the time available for the current to rise after turn-on becomes less and less as the speed of the motor increases. This is due to the fact that the available conduction time is lower for constant switching angles as the speed of rotation increases. This can be seen by considering that speed is the time rate of change of angle. Thus, as the speed increases, there will be a point when the current level never rises to the chopping level. At this point, the single-pulse mode of operation will come into effect and the current will decrease or remain constant throughout the increasing inductance zone. An example of a single-pulse-mode current waveform was seen in Fig. 27.105b.

As the current is not commutated in the single-pulse mode, the control in this mode consists only of controlling the on and off angles. The turn-on angle θ_{on} can be placed at some point in advance of the rising-inductance region where the phase inductance is low, so that current can increase at a faster rate before the increasing-inductance region. The angle can be advanced up until maximum allowable current occurs at the peak of the waveform (this may even mean switching on in the previous decreasing inductance zone). The actual control turn-on and turn-off angles for the single-pulse mode, for a given load torque and speed, can be determined by simulating the motor equations.

The speed at which changeover between single-pulse and chopping mode occurs is called the *base speed.* Base speed is defined as the highest speed at which chopping mode can be maintained at the rated voltage and with fixed on and off angles. Below the base speed, the current increases during the rising-inductance region, unless it is maintained at the maximum or a lower level by chopping.

Therefore, it can be seen that at lower speeds that are below the base speed, the motor is controlled using chopping-mode control, whereas at speeds above the base speed the single pulse mode of control is used. In both control modes the control turn-on and turn-off angles are chosen so that the motor provides the required load torque.

27. .8 Position Sensing

It can be seen from the preceding discussion that to control the SR motor satisfactorily, the motor phases are excited at the rotor angles determined by the control method. It is therefore essential to have knowledge of the rotor position. Furthermore, the rotor angle information must be accurate and have high resolution to allow implementation of the more sophisticated nonlinear control schemes that can minimize torque ripple and optimize the motor performance.

This means that the performance of an SR drive depends on accurate position sensing. The efficiency of the drive and its torque output can be greatly decreased by inaccurate position sensing, and corresponding inaccurate excitation angles. It has been demonstrated that at high motor speeds an error of only 1° may decrease the torque production by almost 8 of the maximum torque output.

Traditionally, rotor-position information has been measured using some form of mechanical angle transducer or encoder. The position-sensing requirements are in fact similar to those for brushless PM motors. However, although position sensing is required for the motor operation, position-measurement sensors are often undesirable. The disadvantages of the electromechanical sensors include the following:

(a) The position sensors have a tendency to be unreliable because of environmental factors such as dust, high temperature, humidity, and vibration.
(b) The cost of the sensors rises with the position resolution. Hence, if high-performance control is required, an expensive high-resolution encoder needs to be employed.
(c) There is an additional manufacturing expense and inconvenience due to the sensor installation on the motor shaft. In addition, consideration must be given to maintenance of the motor because of the mechanical mounting of the sensors, which also adds to the design time and cost.
(d) Mechanical position sensors entail extra electrical connections to the motor. This increases the quantity of electrical wiring between the motor and the motor drive. This wire normally needs to be shielded from electromagnetic noise and thus further adds to the expense of the drive system.
(e) The allocation of space for the mounting of the position sensor may be a problem for small applications (such as for motors used in consumer products).

Hence, to overcome the problems induced by rotor-position transducers, researchers have developed a number of methods to eliminate the electromechanical sensor for deriving position information. This is achieved by indirectly determining the rotor position. Such methods are commonly termed *sensorless* rotor-position estimation methods. The term sensorless seems to imply that there are no sensors at all. However, there must be some form of sensor used to measure the rotor position. In fact, the term sensorless position estimation in reality implies that there are no additional sensors required to determine position apart from those that measure the motor electrical parameters to control the motor. These are normally current- or voltage-measuring circuits.

Hence, all sensorless position estimation methods for the SR motor use some form of processing on electrical waveforms of the motor windings. In essence, the major difference between sensorless position detection, and the electromechanical sensors mentioned above, is that there is no mechanical connection of the sensor to the motor shaft. Therefore, the sensorless position detection involves electrical measurements only.

27. . urther Reading

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27.1 Synchronous Reluctance Motor Drives

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27.1 .1 Introduction

In recent years there has been a revival of interest in reluctance machines. Two main machines have been the focus of this interest the switched-reluctance machine (SRM) and the synchronous reluctance machine (Syncrel). The SRM is a machine that does not have sine-wave spatial distributed windings, but instead has concentrated coils and a doubly salient rotor and stator structure. The operation of this machine is highly nonlinear in character, and normal ac machine modeling techniques cannot be applied in a straightforward manner to describe its operation. The SRM drive has been considered in detail in an earlier section.

The Syncrel, on the other hand, has conventional three-phase sinusoidally distributed windings on the stator. The word "synchronous" in the machine's name emphasizes the fact that the stator windings generate a spatial sinusoidally distributed magnetomotive force (mmf) in the airgap between the stator and the rotor, and under steady-state conditions the rotor rotates in synchronism with this field. Therefore, the stator winding configuration of this machine is virtually exactly the same as that of the induction machine or the conventional synchronous machine. The major difference between the Syncrel and conventional synchronous and induction machines is in the rotor structure. In both the induction machine and the synchronous machine, there is a source of flux in the rotor itself. In the case of the induction machine, this flux is produced by currents resulting from an induction mechanism, and for the synchronous machine there is a field winding wound on the rotor that is fed with dc current to produce flux. The permanent magnet synchronous machine replaces the wound field on the rotor with a permanent magnet. The Syncrel, on the other hand, does not have any source of flux on the rotor, but instead the rotor is designed to distort the flux density distribution produced by the sinusoidally distributed mmf.

Sinusoidally wound reluctance machines were traditionally used in the fiber-spinning industry because of their synchronous nature. This made it simple to keep a large number of machines running at the same speed using just the frequency of the supply to the machines. These machines were direct-on-line-start machines. This was facilitated by the presence of an induction machine starting cage on the rotor. This cage was also essential to damp out oscillations in the rotor speed when running at synchronous speed. It should be pointed out that these machines are not considered to be Syncrels *a Syncrel does not have an induction machine cage on the rotor.* A Syncrel is absolutely dependent on an intelligent inverter drive in order to start the machine and to stabilize it when running. The lack of a requirement for a starting cage means that the rotor design can be optimized for best torque and power performance.

The revival of interest in the Syncrel in the early 1980s was motivated by the development of low-cost microprocessors and reliable power electronics, coupled with the perception that the Syncrel may be more efficient and simpler to control in variable-speed applications compared to the induction machine. The control simplicity is achieved in practice mainly because one does not have to locate the flux vector in order to implement vector control. The potential for improved efficiency and torque density compared to the induction machine is very dependent on the rotor design. The Syncrel has the advantage over the switched-reluctance machine in that it produces relatively smooth torque naturally, and it uses a conventional three-phase inverter. Therefore, inverter technology developed for the induction machine can be applied directly.

27.1 .2 Basic Principles

Reluctance machines are one of the oldest electric machine structures, since they are based on the basic physical fact that a magnet attracts a piece of iron. In fact, Syncrel structures were being published in the early 1920s [1]. The essential idea behind the operation of all reluctance machines is that the windings of the machine produce magnetic poles that are used to attract the reluctance rotor. If the magnetic poles are moved around the periphery of the machine at the rate at which the rotor is moving, then sustained torque and rotation can be achieved.

A conceptual diagram of a Syncrel is shown in Fig. 27.109. In this figure the rotor is represented as a simple “dumbbell”-type rotor. The axes of the three-phase sinusoidally distributed windings are indicated by the dashed lines. If these windings are being fed with currents, then a spatial sinusoidally distributed mmf results. Because this mmf is sinusoidally distributed it can be represented by a “space vector” (similar to sinusoidal time-varying quantities being represented by a time phasor). In Fig. 27.109, this resultant space vector is indicated by $\underline{F} \cdot \underline{F}_d$ and $\underline{F}_q$ are the components of this vector that lie along the high-permeance and low-permeance axes of the machine, respectively.

If one considers the situation shown in Fig. 27.109, then the rotor would tend to rotate in the direction indicated. This rotation would continue until the high-permeance d_r axis (i.e., the least-reluctance axis) of the machine aligns with the mmf vector. When this alignment occurs, the flux produced by the stator mmf vector would be maximized. If the $\underline{F}$ vector also rotates as the rotor rotates, then as mentioned previously, the angle between $\underline{F}$ and d_r will remain constant and the rotor will continue to chase the $\underline{F}$ vector, continuous rotation being the result.

One can ask even more fundamental questions, such as, “why does the rotor rotate to the position that maximizes the flux density?” This is essentially asking, why does a magnet attract a piece of iron? To completely answer this question one

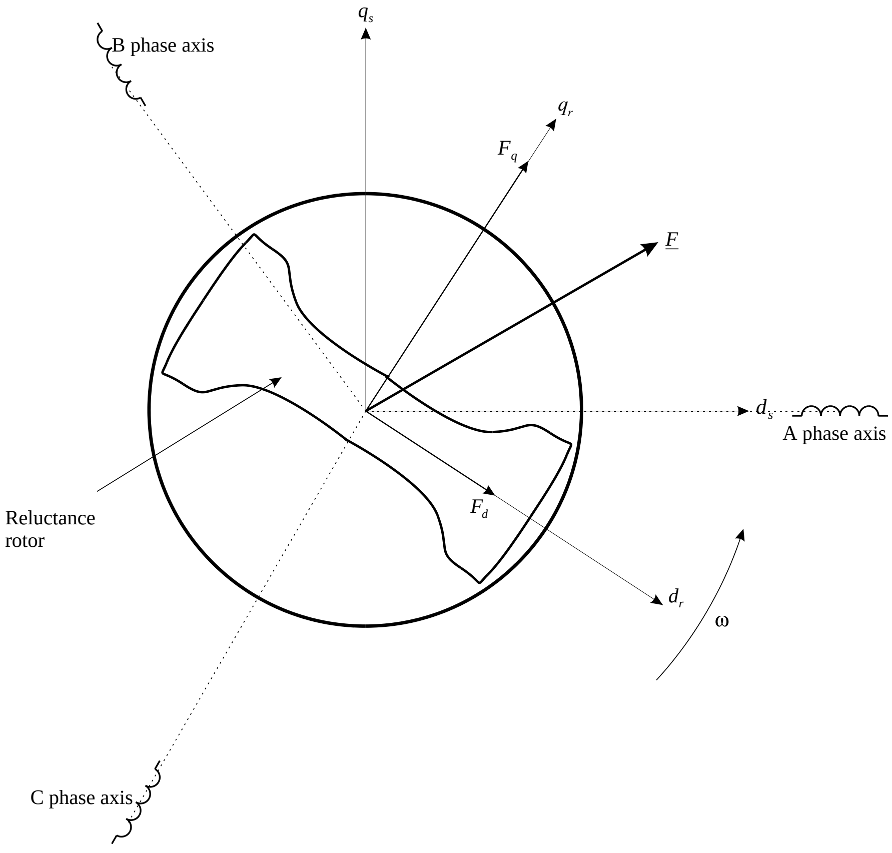

FIGURE 27.109 Conceptual diagram of a synchronous reluctance machine.

has to delve into the field of quantum physics, which is beyond the scope of this presentation. A less complicated explanation is based on the fact that the stator flux density tends to align the domains in the ferromagnetic rotor material, which produces an effect similar to having a current-carrying winding wrapped around the rotor. This effective current then interacts with the stator flux density to produce a force that has a component that is oriented radially around the periphery of the machine. It is this component that produces the torque on the rotor that causes the alignment with the stator mmf vector.

It was mentioned previously that in order to have continuous motion, the mmf vector $\underline{F}$ must rotate at the same angular velocity as the rotor so that the angle between the mmf vector and the d_r axis of the rotor is kept at a constant value. The rotation of the mmf vector is achieved by feeding the three-phase windings of the machine with time-varying currents. It can be shown that if these form a balanced 120° temporally phase-shifted set of sinusoidal currents, then the resultant mmf vector will rotate at a constant velocity related to the frequency of the input current waveforms and the number of pole pairs in the machine.

In order to get a more precise figure for the torque produced by a Syncrel, one has to develop techniques of modeling the machine. Because the Syncrel is a reluctance machine, the coenergy technique for developing the torque expressions can be used [2,3]. The coenergy technique is a very accurate way of determining the torque as it explicitly takes into account the saturation nonlinearities in the iron of the machine. However, the technique does not lend itself to mathematical analysis and is not a good way of understanding the basic dynamic properties of the machine. The coenergy approach will not be pursued any further in this presentation.

27.1 .3 Machine Structure

The essential difference between the Syncrel and, say, the induction machine is the design of the rotor. Most experimental Syncrel systems that have been built use the stator of an induction machine, including the same windings. The rotor designs can take on a number of different forms, from the very simple and basic dumbbell-shaped rotor (such as that sketched in Fig. 27.109) to more complex designs. Unfortunately, the designs that are simple to manufacture (such as the dumbbell design) do not give good performance; therefore, one is forced into more complex designs. The design of the rotor in a Syncrel is the key to whether it is economic to manufacture and has competitive performance with similar machines.

The design of Syncrel rotors fall into four main categories of increasing manufacturing complexity and performance: dumbbell or higher pole-number equivalent designs, flux-barrier designs, radially laminated flux-barrier designs, and axially laminated designs. The first two of these design methodologies are old and lead to designs with poor to modest performance. Therefore, they will not be considered any further. The latter two, however, lead to machine designs with performance comparable to that of the induction machine.

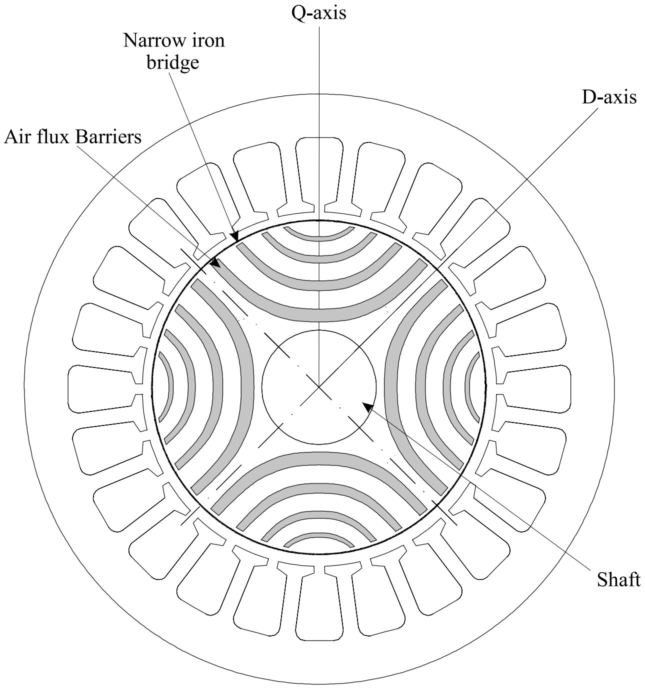

FIGURE 27.110 Cross section of a radially laminated Syncrel.

Figures 27.110 and 27.111 show the cross section of a four-pole machine with a radial lamination flux-barrier designed

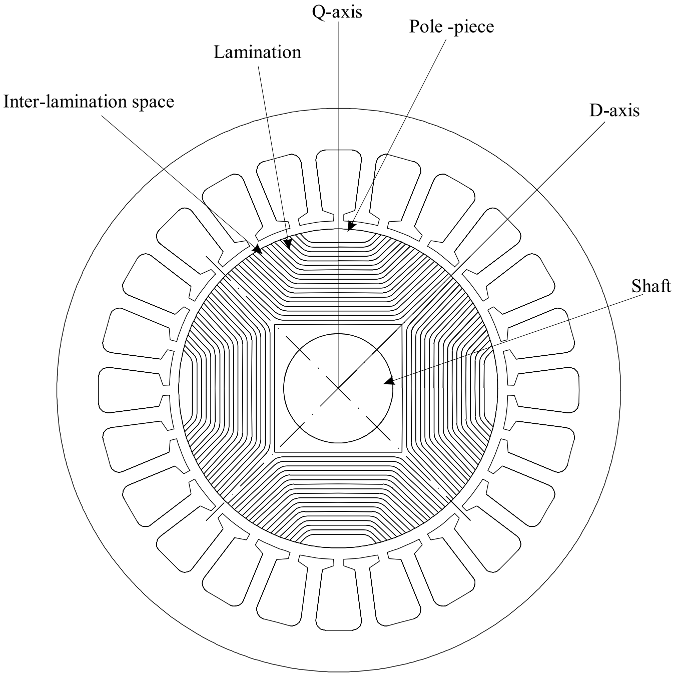

FIGURE 27.111 Cross section of an axially laminated Syncrel.

rotor and an axially laminated rotor. The radial lamination design allows the rotor to be built using similar techniques to standard radial laminations for other machines. The flux barriers can be punched for mass production, or wire eroded for low production numbers. These laminations are simply stacked onto the shaft to form the rotor. The punched areas can be filled with plastic or epoxy materials for extra strength if required. The iron bridges at the outside of the rotor are designed to saturate under normal flux levels and therefore do not adversely affect the performance of the machine. They are there to provide mechanical strength.

The axially laminated rotor is constructed with laminations running the length of the rotor (i.e., into the page on Fig. 27.111). In between the laminations a nonmagnetic packing material is used. This can be aluminum or bronze, for example, but a nonconductive material such as slot insulation is better since eddy currents can be induced in conductive materials. The ratio of the steel laminations to nonmagnetic material is usually about 1 : 1. The axial laminations are all stacked on top of each other, and a nonmagnetic pole piece is bolted on top of the stack to hold the laminations to the shaft. The strength of these bolts is usually the main limitation on the mechanical strength and hence speed of rotation of this rotor. If more or thicker bolts are used to increase strength, the magnetic properties of the rotor are compromised because of the amount of lamination that has to be cut out to make room for them.

Radial and axial laminated rotors are usually limited to four-pole or higher machines because of the difficulty of accommodating the shaft in two-pole designs. An axially laminated two-pole rotor has been built with the shafts effectively bonded onto the end of the rotor. Another design was constructed of a block of alternating steel and bronze laminations, the whole structure being brazed together and the resultant stack then being machined into a round rotor and shafts (this rotor was used for high-speed generator applications).

Of the two rotor designs, the radially laminated one has the best potential for economic production. The axially laminated rotor in general gives the best performance, but the mass production difficulties with folding and assembling the laminations make its adoption by industry unlikely. On the other hand, improved designs for radially laminated rotors mean that they can now produce performance very close to that of the axial laminated designs, and the ease of manufacture would indicate that these rotors are the future of Syncrel rotors.

27.1 .4 Basic Mathematical Modeling

In order to give a more quantitative understanding of the machine, a basic mathematical dynamic model of the machine will be introduced.[1] This model will assume that the iron material in the machine does not saturate. This means that the flux density and flux linkage of the windings in the machine are linear functions of the currents in the machine.

To derive the electrical dynamic model of a machine, one usually uses Faraday's flux-linkage expressions. In the case of the Syncrel, the self and mutual flux linkage between the phases is obviously a function of the angular position of the rotor; therefore, one needs to have expressions for these inductances in terms of rotor position. The fundamental assumption used to make this mathematically tractable is that the inductances vary as a sinusoidal function of the rotor position.[2] The other major part of the modeling process is the conversion from a three-phase model to a two-phase model. This is a process that is carried out for most sinusoidally wound machines, since it allows a variety of machines to be represented by very similar models.

A further complication in this process is that the two-phase model is derived in a "rotating reference frame," as opposed to a stationary reference frame. Developing the equations in a rotating reference frame has the advantage that the normal sinusoidal currents feeding the machine are transformed into dc currents in steady state, and the angular dependence of the machine's inductances disappear.

One way of heuristically understanding the effect of the rotating-frame transformation is to imagine that we are observing the machine's behavior from the vantage point of the rotor. Because the sinusoidal flux density waveform is rotating around the machine in synchronism with the rotor, it appears from the rotor that the flux density is not changing with time i.e., it is a flux density created by dc currents flowing in a single sinusoidally distributed winding. This single sinusoidal winding is effectively rotating with the rotor. It should be noted that the transformation process of the fluxes, currents, voltages, and machine parameters to the two-phase rotating frame is an invertible process; therefore, one can apply the inverse transformation to ascertain what is happening in the original three-phase machine.

The models derived using the three-phase to two-phase transformations are known as *dq* models, the *d* and *q* referring to the two axes of the machine in the two-phase model (both stationary and rotating frame *dq* axes are shown in Fig. 27.109). The linear[3] *dq* equations for the Syncrel can be derived as [4]

$$v_d = Ri_d + L_d \frac{di_d}{dt} - \omega L_q i_q \tag{27.99}$$

$$v_q = Ri_q + L_q \frac{di_q}{dt} + \omega L_d i_d \tag{27.100}$$

---

[1] Note that the model is not derived but instead just stated. The structure of the model will be heuristically explained.

[2] The sinusoidal variation of inductance with rotor position turns out to be very accurate because the stator windings are sinusoidally wound. This forces the flux linkage to behave in a sinusoidal fashion.

[3] Linear refers to the fact that the equations are derived assuming that the iron circuit behaves linearly in relation to applied mmf and the flux produced.

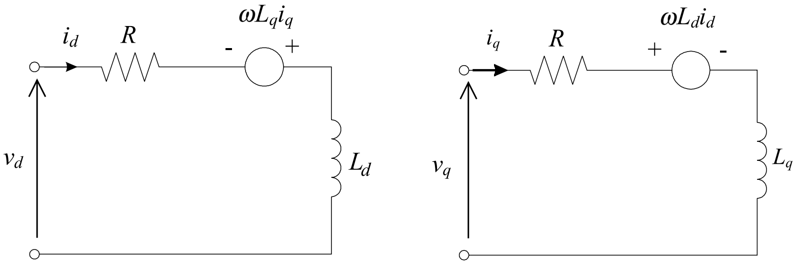

FIGURE 27.112 Two-phase equivalent circuit of the Syncrel in a rotating frame.

where

v_d, i_d ≡ the d-axis voltage and current
v_q, i_q ≡ the d-axis voltage and current
L_d, L_q ≡ the d- and q-axis inductances, respectively
ω ≡ the electrical angular velocity of the rotor

Thus far we have concentrated on the electrical dynamics of the machine. The other very important aspect is the torque produced by the machine. It is possible to derive the torque of the Syncrel using the principle of virtual work based on coenergy as

$$T_e = \frac{3}{2} p_p (L_d - L_q) i_d i_q \tag{27.101}$$

The 3/2 factor is to account for the fact that the two-phase machine produces two-thirds the torque of the three-phase machine.[4]

The only other remaining equation is the mechanical equation for the system:

$$J\dot{\omega}_r + D\omega_r + T_F = T_e \tag{27.102}$$

where

J ≡ the rotational inertia of the rotor/load
D ≡ the friction coefficient for the load
T_F ≡ the fixed load torque of the load
ω_r ≡ the rotor mechanical angular velocity ($= \omega / p_p$)

REMARK. *Equation (27.101) shows that the machine must be designed so that $L_d - L_q$ is as large as possible. This will maximize the torque that is produced by the machine for given d- and q-axis currents. To lower L_q one must design the q-axis so that it has as much air obstructing the flow of flux as possible, and the d-axis must be designed so that it has as much iron as possible. In practice these quantities cannot be varied independently.*

Figure 27.112 shows the equivalent circuit for the Syncrel corresponding to Eqs. (27.99) and (27.100). One can see that the dynamic equations for the Syncrel are intrinsically simple. In contrast, the induction machine electrical equations consist of a set of four complex coupled differential equations.

27.1 .5 Control Strategies and Important Parameters

The dq model captured in Eqs. (27.99)–(27.101) can be used to explain a number of control strategies for the Syncrel. It is beyond the scope of this section to present the derivation of these. The interested reader should consult references [4–6] cited at the end of this section.

One of the most common control strategies for any electrical machine is to maximize the torque per ampere of input current. The following discussion should be considered in conjunction with Fig. 27.113, which shows the relationship of the various vectors in the machine to the $d_r q_r$ and $d_s q_s$ axes.

It turns out that one of the critical parameters for the control of the Syncrel is the angle of the resultant current

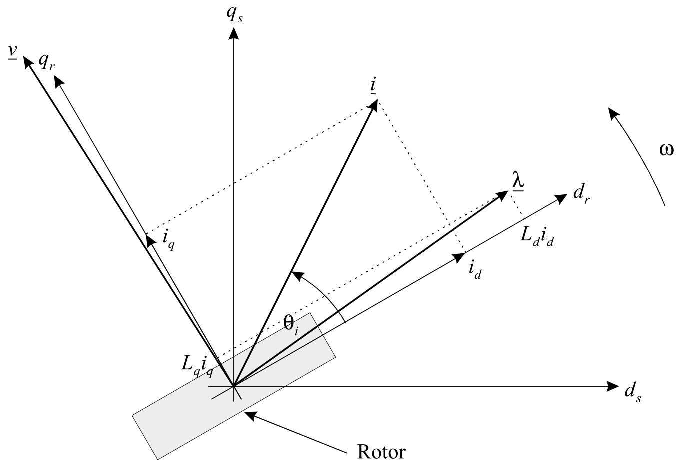

FIGURE 27.113 Space phasor diagram of a Syncrel.

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[4] The 3/2 conversion factor is required if the transformations are power-variant transformations, as opposed to the power-invariant transformations. The power-variant transformations are the most common ones used because the single-phase machine parameters can be used directly in the resultant models, and the two-phase voltages and currents are identical in magnitude to their three-phase counterparts.

vector in the machine in relation to the d-axis of the machine. It is possible to write the torque expression for the Syncrel in terms of this as

$$T_e = \frac{3}{2}p(L_d - L_q)|i|^2 \sin 2\delta \tag{27.103}$$

It is obvious that this expression is maximized for a given value of i if $\delta = \pi/4$. Therefore, one should control the currents so that δ stays at this angle if maximum torque per ampere is desired.

Another control objective for the Syncrel is to maximize the power factor for the machine. This is important to minimize the kVA for the inverter. It can be shown that the current angle to maximize the power factor is [4]

$$\delta = \tan^{-1}\sqrt{\xi} \tag{27.104}$$

where

$$\xi = L_d/L_q \qquad \text{(the inductance ratio)}$$

REMARK. *Equation (27.104) indicates that ξ is the important parameter in relation to power factor. In order to obtain a power factor of 0.8, one requires an inductance ratio of approximately 10.*

Finally, we shall consider another control objective maximize the rate of change of torque with a fixed-current-angle control strategy. In effect this means that one is maximizing the rate of change of the currents in the machine for a given voltage applied to it. The analysis of this requirement results in [4]

$$\delta = \tan^{-1}\xi \tag{27.105}$$

REMARK. *As with the maximum-power-factor case, ξ is the most important parameter in relation to the rate of change of torque. Because this control effectively optimizes the current into the machine for a given voltage and angular velocity, this angle also corresponds to that required to maximize the field-weakening range of the machine.*

Other control strategies for the machine can be devised, as well as the current angles required to obtain the maximum power from the machine during field-weakening operation.

REMARK. *If one carries out a thorough analysis of all the control properties of the Syncrel, then it emerges that all performance measures for the machine are enhanced by a large value of the ξ ratio.*

27.1 .6 Practical Considerations

The control strategies discussed in the previous section were all derived assuming that the machine does not exhibit saturation and there are no iron losses. The q-axis of the machine does not have any saturation, as the flux path on this axis is dominated by air. However, the d-axis of the machine does exhibit substantial saturation under operational flux levels, and this effect must be accounted for to optimize the drive's performance.

The effect that saturation has on the ideal current angles is to increase them. This increase is most pronounced for the maximum torque per ampere control strategy, since this strategy results in a larger component of current in the d-axis, and consequently more saturation. Maximum power factor and maximum rate of change of torque are not affected as much. In order to get the correct current angle for maximum torque per ampere, a lookup table of the saturation characteristic of the machine must be stored in the controller, which is consulted in order to calculate the desired current angle [7].

It has been found that iron losses in the stator and the rotor also affect the optimal current angles. However, usually saturation effects dominate, and the effects of iron losses can be ignored.

27.1 .7 A Syncrel Drive System

The basic structure of a variable speed drive system based on using the Syncrel is shown in Fig. 27.114. Many components of this drive are very similar to those found in an induction machine drive system. One notable exception is the L_d lookup table block and the current reference generator. The L_d lookup stores the current vs d-axis inductance table for the machine, thereby allowing the inductance to be determined for various current levels. This table is also used to generate the incremental d-axis inductance. The inductance values generated from this table are used in the state feedback block and the torque estimator.

The state feedback block effectively generates an offset voltage to the PWM generator so that the voltage it produces is at least enough to counter the back emf. This technique effectively eliminates the back emf disturbance from the current-control loops.

The current reference generator takes the desired torque as an input and generates the required d- and q-axis currents at the output. This block uses a lookup-table technique together with an inverse of the torque equation to generate these currents and takes into account the saturation characteristics of the machine.

The three-to-two-phase block converts the currents from a three-phase stationary frame to a two-phase rotating frame. This is a standard block in induction machine drives, and as with induction-machine drives, this means that the Syncrel control algorithm is implemented in a rotating reference frame. The conversion from this frame back to the stationary frame occurs implicitly in the space vector PWM generator.

The Syncrel control algorithm is essentially a simplified vector controller, and consequently the computational requirements are not high. This means that a Syncrel controller can be implemented on a modest microprocessor. As far as

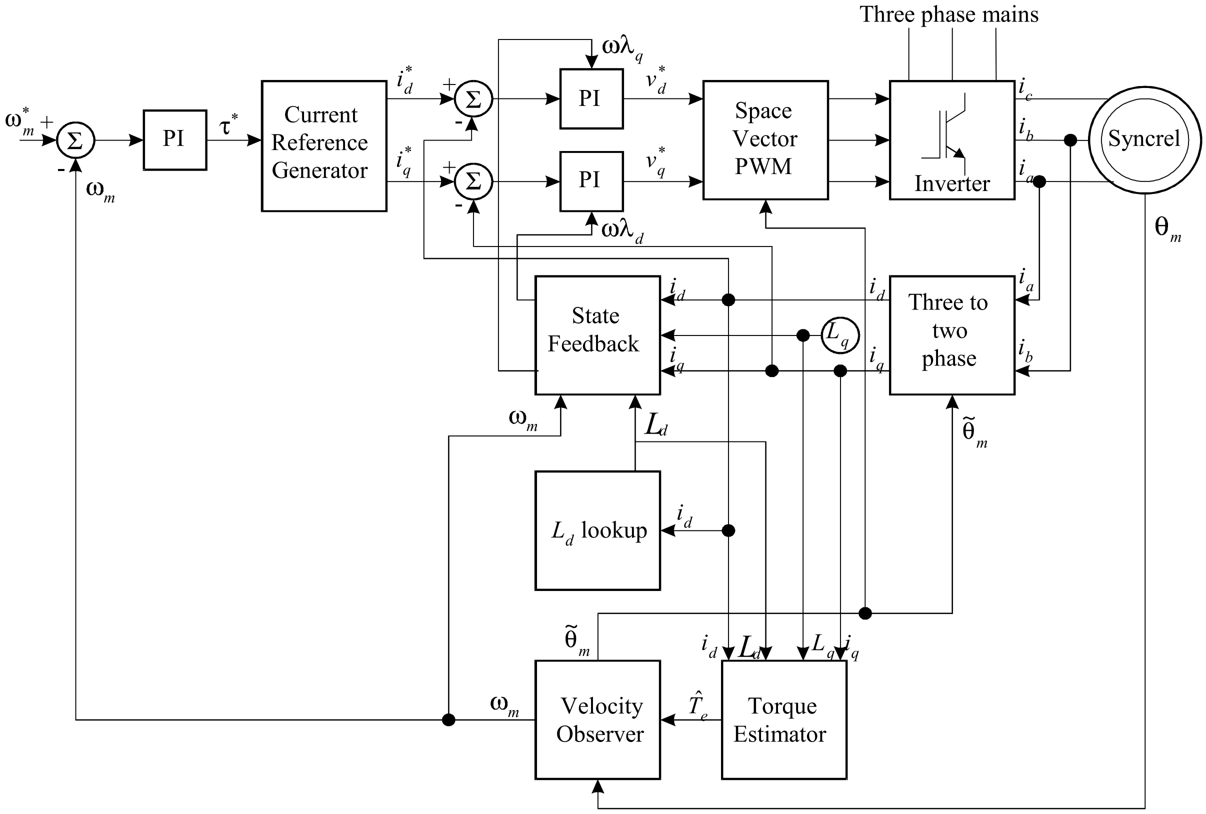

FIGURE 27.114 Block diagram of a Syncrel drive system.

input and output hardware is concerned, the requirements are basically the same as those for an induction machine system i.e., sample two of the phase currents, the link voltage, and the rotor position.

27.1 .8 Conclusions

The Syncrel-based drive system offers simplicity in control, excellent performance for variable-speed and position-control applications, good torque and power density, and efficiency that is more than competitive with that of induction-machine drive systems. To date very few commercial drive systems are available using Syncrels, this being mainly due to the slow emergence of easy-to-manufacture rotors that give good performance, and the conservatism of the motor-drive industry. One commercial application that has emerged is ac servo applications, where the Syncrel offers low torque ripple (with appropriate rotor design) together with a small moment of inertia. Other applications under consideration are in the area of drives for electric vehicles and generators for flywheel energy storage systems. It remains to be seen whether the Syncrel can ever challenge the supremacy of the vector-controlled induction machine in mainstream industrial applications.

The interested reader who wishes to pursue Syncrel drives in more detail can find a good coverage of the control and motor design issues in [8].

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28

Sensorless Vector and Direct Torque Controlled Drives

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28.1 General

Variable-speed drives are continuously innovated. Their development is characterized by the progress made in various areas including power and microelectronics, control systems, magnetic materials, modern communication technologies (e.g. for ultra-fast bus communications), etc. In the past, dc motors were used extensively in areas where variable-speed operation was required, since their flux and torque could be controlled easily by controlling the field and armature current respectively. However, dc motors have certain disadvantages, which are mainly due to the existence of the commutator and the brushes. However, these problems can be overcome by the application of ac motors, which can have simple and rugged structure, high maintainability and economy; they are also robust and immune to heavy overloading.

The rapid advancements made in the field of microprocessors and DSPs has contributed significantly to the development of various high-performance ac drives, since it has become possible to introduce relatively complicated control systems in these drives. One of the main developers of motion control DPS is Texas Instruments (see also Section 28.3).

Among the various ac drive systems, those which contain the squirrel cage induction motor have a particular cost advantage. At present the cage induction motor is the most frequently used motor in industry. This is due to the fact that it is simple, rugged, requires only low maintenance and is one of the cheapest machines available at all power ratings. However, permanent magnet synchronous motors are also becoming increasingly used. Owing to their excellent control capabilities, variable speed drives incorporating ac motors and employing modern static converters and torque control can compete well with high-performance four-quadrant dc drives.

In recent years various speed and position sensorless control schemes have been developed for variable-speed ac drives. The main reasons for the development of these "sensorless" drives are [35]: reduction of hardware complexity and cost; increased mechanical robustness and overall ruggedness; operation in hostile environments; higher reliability; decreased maintenance requirements; increased noise immunity; unaffected machine inertia; improvement of the vibration behaviour, elimination of sensor cables etc. The terminology "sensorless" refers to the fact that no conventional speed or position monitoring (e.g. tachometer based speed sensors, optical incremental sensors or electromechanical resolvers) are used in these drives. In "sensorless" drives, the speed and/or the position signal is obtained by using monitored voltages and/or currents and by utilizing mathematical models or artificial-intelligence-based systems [35, 36]. In addition to these techniques, it is also possible to replace a conventional speed or position sensor in a variable-speed drive by using integrated sensor ball bearings (e.g. by using sensor bearings manufactured by SKF [39, 40, 41].

Commercially available sensorless induction motor drives incorporate speed estimators (not position estimators). These drives operate in the speed range of 1 and 100 rated speed, and having speed control accuracy as high as ±5 of base

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[1] [DTC Direct Torque Control is the registered trade mark of DTC, owned by ABB Industry Oy].

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speed. The performance of sensorless drives mainly depends on the torque control capabilities and also on the speed (and position) estimation accuracy and bandwidth. The dynamic performance of first generation sensorless drives approaches those of standard vector drives, at least at speeds higher than 3–5 of the rated speed. First generation sensorless drives are not suitable to control the rotor position, (since that would require an absolute rotor position estimation with 12–16 bit accuracy and a high bandwidth, in addition to full torque control capability at zero speed). The state-of-the-art research in the field of sensorless ac drives is related to speed and position sensorless drives operating in the very low speed range [43]. In many applications, cranes, hoists, traction drives, etc., it is very important to maintain the required torque down to zero speed [43]. Second generation sensorless ac drives will compete with standard vector drives, and will have full torque control at zero speed and at least 12 bit absolute position accuracy.

28.2 Basic Types of Torque-Controlled Drive Schemes Vector Drives, Direct-Torque-Controlled Drives

At present there exist basically two different types of instantaneous electromagnetic-torque-controlled ac drives (briefly torque-controlled drives) for high-performance applications: these are vector-controlled (VC) and direct-torque-controlled (DTC) drives. However, a new type of high-performance ac drive is under development at Aberdeen University and Heriot-Watt University, this is based on a joint research work.

Vector-controlled drives were introduced more than 20 years ago in Germany by Blaschke, Hasse and Leonhard. It is less known that Jonsson in Sweden [18] had also developed sensorless vector-controlled drives, under the name NFO (natural field-oriented control) drives, almost 20 years ago, but the results were not published for a long time. Vector drives have achieved a high degree of maturity and have become increasingly popular in a wide range of applications. They have established a substantial and continuously increasing worldwide market. It is an important feature of various types of vector-controlled drives that they allow the dynamic performance of ac drives to match or sometimes even to surpass that of the dc drive. By using vector control, similar to the torque control of a separately excited dc motor, it is possible to control separately the flux and torque producing current components. At present, the main trend is to use sensorless vector drives, where the speed and position information is obtained by utilizing monitored voltages and/or currents.

Direct-torque-controlled drives were introduced in Japan by Takahashi [28] and also in Germany by Depenbrock [9] more than 10 years ago. However, the first industrial direct-torque-controlled drive was introduced by ABB a few years ago [31] and this is a very significant industrial contribution. DTC technology was first introduced by ABB in 1994, and the first DTC product, the ACS600, was introduced in 1995. It is a main feature of the ABB DTC drive that the flux and torque are controlled directly and independently by the selection of optimal inverter switching modes (e.g. these are optimal switching voltages in a voltage-source-inverter-fed (VSI) drive). The ABB drive is a sensorless induction motor drive, which does not incorporate any mechanical transducers (for position and/or speed monitoring). In general, a DTC drive is simpler than a VC drive (see Section 28.2.2) and gives very fast torque response. ABB DTC implementation data is not available and is the property of ABB [35].

28.2.1 Fundamentals of Vector Drives

In the present section a brief description is given of the fundamentals of vector- and direct-torque-controlled drives.

28.2.1.1 Dc Machine Torque Control

Due to the stationary orthogonal field axes, the control structure of dc machines is relatively simple, but their mechanical construction is complicated. In a separately excited dc machine, the instantaneous electromagnetic torque, t_e, is proportional to the product of the field current, i_f (flux producing current) and the armature current, i_a (torque producing current),

$$t_e = c i_f i_a = c_1 \psi_f i_a \tag{28.1}$$

In Eqn. (28.1), c and c_1 are constants, ψ_f is the field flux. The field flux can be established either by a stationary dc excited field winding, or by permanent magnets. Torque control can be achieved by varying the armature current, and quick torque response is obtained if the armature current is changed quickly and the field current (field flux) is constant. However, this principle can also be used for the instantaneous torque control of ac machines (both induction and synchronous: the latter can be of the electrically excited, reluctance or the permanent magnet excited type), as discussed below.

28.2.1.2 Induction Machine Vector Control

Vector control techniques incorporating fast microprocessor and DSPs have made possible the application of ac drives for high-performance applications, where traditionally only dc drives were employed. In the past such control techniques would have been not possible because of the complex hardware and software required to solve the complex control problem. As for dc machines, torque control in ac machines can also be achieved by controlling the motor currents (e.g. stator currents of an induction machine). However, in contrast to a dc machine (see the previous section), in an ac machine, both the phase angle and the modulus of the current has to be controlled, or in other words, the current vector has to be controlled. This is the reason for the terminology "vector control". Furthermore, in dc machines, the orientation of the field flux and the armature mmf is fixed by the commutator, while in ac machines, the field flux and the spatial angle of the armature mmf require external control. In the absence of this control, the spatial angles between the various fields in ac machines vary with the load and yield unwanted oscillating dynamic response. When vector control is used, the torque- and flux-producing current components are decoupled and the transient response characteristics are similar to those of a separately excited dc machine (see details below).

The mechanism of torque production in an ac machine and also in a dc machine is similar. Unfortunately this similarity has not been emphasized before the 1970s, and this is one of the reasons why the technique of vector control did not emerge earlier. The formulae given for the electromagnetic torque in many well-known textbooks on electrical machine theory (which do not discuss space vector theory) have also implied that, for the monitoring of the instantaneous electromagnetic torque of an induction machine, it is also necessary to monitor the rotor currents and the rotor position. Even in the 1980s some publications seemed to strengthen this false conception, which only arose because the complicated formulae derived for the expression of the instantaneous electromagnetic torque had not been simplified. However, by using fundamental physical laws and/or space vector theory, it is easy to show that, similar to the expression of the electromagnetic torque of a separately excited dc machine, the instantaneous electromagnetic torque of an induction machine can be expressed as the product of a flux-producing current and a torque-producing current, if a special, flux-oriented reference frame is used, i.e. if flux-oriented control is employed. In this case, the stator current components (which are expressed in the stationary reference frame) are transformed into a new rotating reference frame, which rotates together with a selected flux linkage space vector. In general, there are three main possibilities for the selection of the flux linkage vector, so the chosen flux linkage vector can be either the stator flux linkage vector, rotor flux linkage vector or magnetizing flux linkage vector. Hence the terminology: stator-flux-, rotor-flux- and magnetizing-flux-oriented control. In these three cases the instantaneous electromagnetic torque can be expressed as follows [35]:

$$t_e = c_{1s}|\bar{\psi}_s| i_{sy}^{s} \quad \text{for stator-flux-oriented control} \tag{28.2}$$

$$t_e = c_{1r}|\bar{\psi}_r| i_{sy}^{r} \quad \text{for rotor-flux-oriented control} \tag{28.3}$$

$$t_e = c_{1m}|\bar{\psi}_s| i_{sy}^{m} \quad \text{for magnetizing-flux-oriented control} \tag{28.4}$$

It is important to note that these expressions are similar to Eqn. (28.1), and for linear magnetic conditions c_{1s}, c_{1r}, c_{1m} are constants, $|\bar{\psi}_s|$, $|\bar{\psi}_r|$ and $|\bar{\psi}_m|$ are the modulus of the stator-, rotor- and magnetizing-flux-linkage space vectors, respectively. Furthermore, the torque-producing stator currents in the stator-, rotor- and magnetizing-flux-oriented reference frame are denoted by i_{ys}^{s}, i_{sy}^{r} and i_{sy}^{m} respectively (the superscript indicates the special reference frame used). It should be noted that the real and imaginary axes of a rotating reference frame fixed to a flux linkage space vector are denoted by x and y, respectively. The torque producing stator currents in Eqns. (28.2)–(28.4) take the role of the armature current in Eqn. (28.1). The application of Eqn. (28.3) will be shown in the drive scheme of Fig. 28.1(a) below. Equations (28.2)–(28.4) can be derived from a single equation, according to which the instantaneous electromagnetic torque of an induction machine can be expressed as the cross vectorial product of the stator flux linkage and current space vectors (in every reference frame) [32]. It follows from Eqn. (28.2) that when the stator flux linkage modulus is constant ($|\bar{\psi}_s| = \text{const.}$), and the torque-producing stator current is changed quickly, quick torque response is obtained. Similar considerations hold for Eqns. (28.3) and (28.4). This simple physical picture forms the basis of vector-controlled drives. It is important to note that the $t_e = c|\bar{\psi}|i_{sy}$ type of expression for the instantaneous electromagnetic torque also holds for smooth-air-gap synchronous motors as discussed below, and this equation is utilized in the vector control implementations of smooth-air-gap synchronous motors.

Since the expression of the electromagnetic torque contains the transformed stator currents, it is obvious that, in a vector-

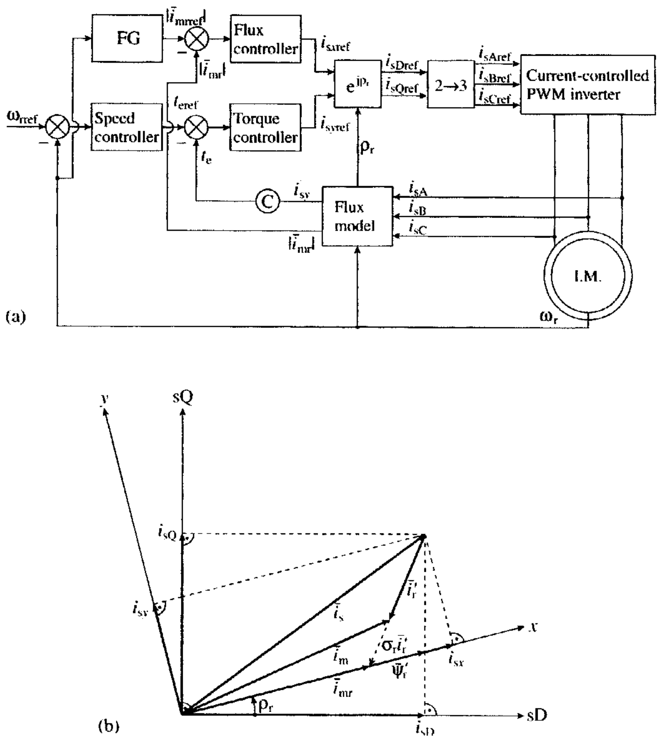


FIGURE 28.1 Direct rotor-flux-oriented vector control scheme of an induction motor with impressed stator currents. (a) Drive scheme, and (b) vector diagram.

controlled drive, the stator currents must be transformed into the required special reference frame (e.g. for a stator-flux-oriented controlled drive, the stator current components in the stationary reference frame must be transformed into the stator current components in the stator-flux-oriented reference frame). It is a common feature of all vector-controlled drives that the modulus and phase angle of the ac excitation are controlled. However, since the reference frame is aligned with the selected flux linkage space vector (e.g. stator flux linkage space vector), the transformation contains the angle of the flux linkage space vector (e.g. stator flux angle, with respect to the real axis of the stationary reference frame). Thus, the implementation of vector control requires the flux angle and also the flux linkage modulus and a major task for an implementation is to have an accurate flux linkage estimation. However, this is also a major task in a drive employing direct torque control.

When the selected flux linkage is the stator flux linkage, in principle, it can be easily obtained by using terminal voltages and currents. This follows directly from physical considerations, since in the stationary reference frame, the stator flux linkage is the integral of the terminal voltage minus the ohmic stator loss, $\bar{\psi}_s = \int(\bar{u}_s - R_s\bar{i}_s)dt$ (where $\bar{\psi}_s$, $\bar{u}_s$ and $\bar{i}_s$ are the space vectors of the stator flux linkage, stator voltage and stator current, respectively, and they are expressed in the stationary reference frame). However, at low stator frequencies some problems arise when this technique is applied [43], since the stator voltages become very small and the ohmic voltage drops become dominant, requiring very accurate knowledge of the stator resistance and very accurate integration. The stator resistance can vary due to temperature changes; and this effect can also be considered by using a thermal model of the machine. Drifts and offsets can greatly influence the precision of integration. The overall accuracy of the estimated flux linkage vector will also depend on the accuracy of the monitored voltages and currents. At low frequencies more sophisticated techniques must be used to obtain the stator flux linkages. The monitoring of the stator voltages can be eliminated in a voltage-source inverter-fed machine, since they can be reconstructed by using the monitored value of the dc link voltage and also the switching states of the switching devices (of the inverter). As shown in Section 28.2.3.2, the components of the stator flux linkage space vector can also be used to obtain the rotor speed signal in a speed sensorless drive, i.e. by utilizing the speed of the stator flux linkage space vector (which is equal to the rate of change of the angle of the stator flux linkage space vector).

When the selected flux linkage space vector is the rotor flux linkage vector ($\bar{\psi}'_r$), it is also possible to obtain it from the terminal quantities by first obtaining the stator flux linkage vector ($\bar{\psi}_s$), and then by applying the appropriate modifications, $\bar{\psi}'_r = (L_r/L_m)(\bar{\psi}_s - L'_s\bar{i}_s)$, where L_r, L_m and L'_s are the rotor, magnetizing and stator transient inductances respectively and $\bar{i}_s$ is the space vector of the stator currents expressed in the stationary reference frame. This follows directly from the fact that the stator and rotor flux linkage space vectors can be expressed as $\bar{\psi}_s = L_s\bar{i}_s + L_m\bar{i}'_r$ and $\bar{\psi}'_r = L_r\bar{i}_r + L_m\bar{i}_s$, where $\bar{i}'_r$ is the rotor current space vector in the stationary reference frame. Thus an accurate knowledge of the machine inductances is required and this is a difficult problem, since they can vary with the saturation level, and the conventional tests (no-load and blocked rotor tests) do not give accurate values for an induction machine with closed rotor slots. Furthermore, at low frequencies the same problems arise as with the stator flux linkage estimation, and to avoid these, various rotor flux models can be used. Some of these models also use the rotor speed (or rotor position), which can be monitored, but in "sensorless" applications, the speed or position is not monitored directly, but is estimated by using advanced control (observers, intelligent systems, etc.) or other techniques.

There are basically two different types of vector control techniques: direct and indirect techniques [35]. The direct implementation relies on the direct measurement or estimation of the rotor-, stator- or magnetizing flux linkage vector amplitude and position. The indirect method uses a machine model, e.g. for rotor-flux-oriented control it utilizes the inherent slip relation. In contrast to direct methods, the indirect methods are highly dependent on machine parameters. Traditional direct vector control schemes use search coils, tapped stator windings or Hall effect sensors for flux sensing. This introduces limitations due to machine structural and thermal requirements. Many applications use indirect schemes, since these have relatively simpler hardware and better overall performance at low frequencies, but since these contain various machine parameters, which may vary with temperature, saturation level and frequency, various parameter adaptation schemes have been developed. These include self-tuning controller applications, Model Reference Adaptive System (MRAS) applications, applications of observers, applications of intelligent controllers (fuzzy, neuro, fuzzy-neuro controllers), etc. If incorrect modulus and angle of the flux linkage space vector are used in a vector control scheme, then flux and torque decoupling is lost and the transient and steady-state responses are degraded. Low frequency response, speed oscillations, loss of input–output torque linearity are major consequences of detuned operation together with decreased drive efficiency.

To illustrate a simple vector-controlled drive, Fig. 28.1(a) shows the schematic drive scheme of an induction motor with impressed stator currents employing direct rotor-flux-oriented control.

In the drive scheme of Fig. 28.1(a), the expression of the electromagnetic torque given by Eqn. (28.3) has been used, but for simplicity, the notation has been simplified, thus $c = c_{1r}$, $i_{sy} = i^r_{sy}$ and hence $t_e = c_{1r}|\bar{\psi}_r|i_{sy}$. Furthermore, the modulus of the rotor flux linkage space vector can be expressed as $|\bar{\psi}_r| = L_m|\bar{i}_{mr}|$, where L_m is the magnetizing inductance of the induction machine and $|\bar{i}_{mr}|$ is the modulus of the rotor magnetizing current space vector shown in Fig. 28.1(b). The flux-producing and torque-producing stator current references (i_{sxref}, i_{syref}) are obtained on the outputs of the flux and torque controllers respectively (which can, e.g., be PI controllers), and are then transformed to the stator currents in the stationary reference frame (i_{sDref}, i_{sQref}), where all the current components are also shown in Fig. 28.1(b). For this purpose $\bar{i}_{\text{sref}} = i_{\text{sDref}} + j i_{\text{sQref}} = (i_{\text{sxref}} + j i_{\text{syref}}) \exp(j\rho_{\text{r}})$ is used, where ρ_{r} is the position of the rotor flux linkage space vector (with respect to the real axis of the stationary reference frame). For illustration purposes Fig. 28.1(b) shows all the stator current components and also the angle ρ_{r}. In the drive scheme of Fig. 28.1(a), the torque-producing stator current (i_{sy}) and the modulus of the rotor magnetizing current are obtained on the output of a rotor flux linkage model. In the simple case shown, the rotor flux linkage model uses the monitored rotor speed and also the monitored stator currents as inputs. Such a model can be obtained by considering the rotor space vector voltage equation of the induction motor [32]. This yields the modulus and angle of the rotor flux linkage space vector (hence the name flux model), but since the rotor flux modulus is the product of L_{m} and $|\bar{i}_{\text{mr}}|$, thus $|\bar{i}_{\text{mr}}|$ can also be obtained. Furthermore, since the position of the rotor flux linkage space vector (ρ_{r}) is also determined in the flux model, and since the stator currents are also inputs to the flux model (in practice only two stator currents are required), the torque-producing stator current i_{sy} can also be obtained. For this purpose the relationship between the stator current space vector expressed in the rotor-flux-oriented reference frame ($\bar{i}'_{\text{s}}$) and the stator current space vector expressed in the stationary reference frame ($\bar{i}_{\text{s}}$) is considered; thus $\bar{i}'_{\text{s}} = i_{\text{sx}} + j i_{\text{sy}} = \bar{i}_{\text{s}} \exp(-j\rho_{\text{r}})$, where $\bar{i}_{\text{s}}$ is the space vector of the stator currents in the stationary reference frame $\bar{i}_{\text{s}} = (\frac{2}{3})(i_{\text{sA}} + a i_{\text{sB}} + a^2 i_{\text{sC}})$. In Fig. 28.1(a), FG is a function generator, on the output of which the modulus of the rotor magnetizing current reference ($|\bar{i}_{\text{mrref}}|$) is obtained, and its input is the monitored speed. This can be used for field-weakening purposes. When the conventional field weakening technique is used, then below base speed $|\bar{i}_{\text{mrref}}|$ is constant, but above base speed it is reduced, i.e. it is inversely proportional to the rotor speed. In Fig. 28.1(a), the electromagnetic torque reference is obtained on the output of the speed controller. This can be a conventional PI controller, a fuzzy logic controller, etc. It can be seen that the drive scheme shown in Fig. 28.1(a) also contains two current controllers and i_{sy} is obtained (in the flux model) by utilizing the transformation $\exp(-j\rho_{\text{r}})$, but the transformation $\exp(j\rho_{\text{r}})$ is also used (to obtain i_{sDref}, i_{sQref}). However, it will be shown below that the current controllers and these transformations are eliminated when direct torque control is used.

Figure 28.2 shows the schematic drive scheme of an induction motor with impressed stator currents employing indirect rotor-flux-oriented control. In Fig. 28.2(a) the torque and flux producing stator current references (i_{sxref}, i_{syref}) and also the angular slip frequency reference (ω_{slref}) are generated from the reference electromagnetic torque (t_{eref}) and reference rotor magnetizing current modulus ($|\bar{i}_{\text{mrref}}|$). The rotor position (θ_{r}) is monitored and is added to the reference value of the slip angle (θ_{slref}), to yield the position of the rotor magnetizing current space vector (or rotor flux linkage space vector). These angles are also shown in Fig. 28.2(b). The transformation of i_{sxref} and i_{syref} into the three-phase stator reference currents is similar to that shown in the direct scheme above (see Fig. 28.1(a)). The expressions used for the estimation of i_{sxref} and ω_{slref} follow from the rotor voltage equation of the induction machine [35], and these expressions are $\omega_{\text{slref}} = i_{\text{syref}}/(T_{\text{r}} i_{\text{sxref}})$ and $i_{\text{sxref}} = (1 + T_{\text{r}} p)|\bar{i}_{\text{mrref}}|$, where T_{r} is the rotor time constant and p is the differential operator, $p = d/dt$.

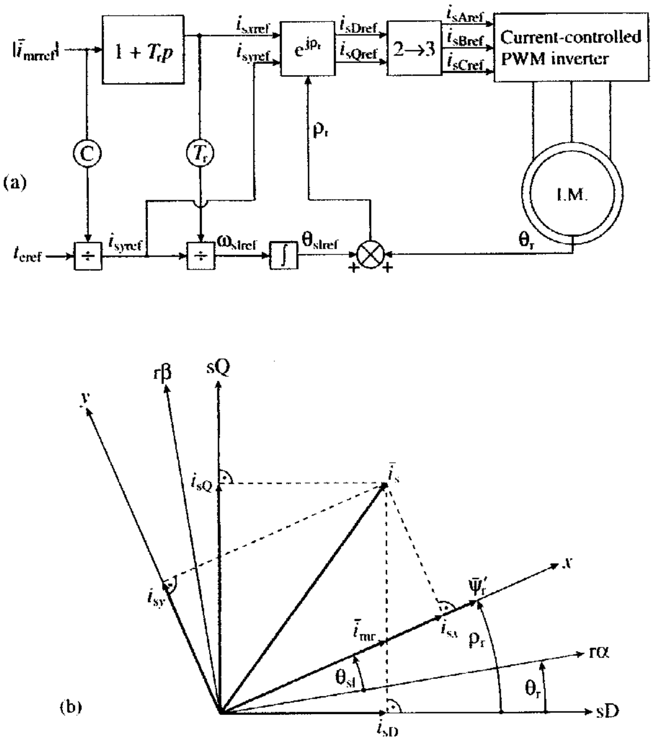


FIGURE 28.2 Indirect rotor-flux-oriented vector control scheme of induction motor with impressed stator currents. (a) Drive scheme and (b) vector diagram.

28.2.1.3 Permanent Magnet Synchronous Machine and Synchronous Reluctance Machine Vector Control

Inverter-fed synchronous motors are widely used in high-performance variable-speed drive systems. If the synchronous machine is supplied by a current-controlled voltage-source PWM inverter, then the stator currents are decided by the reference speed or reference electromagnetic torque and the inverter drives the synchronous motor so that the instantaneous stator currents follow their reference values. For high-performance drives it is possible to use various rotor configurations: rotors with permanent magnets, reluctance type, and electrically excited rotors.

There are basically three types of permanent magnet synchronous machines (the permanent magnets are on the rotor). In the permanent magnet synchronous machine with surface-mounted magnets, the (polar) magnets are located on the surface of the rotor and the machine behaves like a smooth-air-gap machine (the direct and quadrature-axis synchronous inductances are equal, $L_{sd} = L_{sq}$) and there is only magnet torque produced. In the permanent magnet synchronous machine with inset magnets, the (subpolar) magnets are inset into the rotor (directly under the rotor surface), and this is a salient-pole machine ($L_{sd} \neq L_{sq}$) and both magnet torque and reluctance torque are produced. In the permanent magnet synchronous machine with buried magnets (interior magnets), the magnets are buried in the rotor ($L_{sd} \neq L_{sq}$) and again both magnet and reluctance torques are produced. There are basically three types of permanent magnet machines with buried magnets, depending on how the magnets are buried in the rotor: the magnets can be radially placed, axially placed or they can be inclined.

A synchronous machine with reluctance rotor (SYRM) can have various rotor configurations. In earlier constructions, rotor saliency was achieved by removing certain teeth from the rotor of a conventional squirrel cage. Such synchronous reluctance machines with low output power have been used for a long time and their inferior performance, combined with their relatively high price, have resulted in their limited use. However, as a result of recent developments, more reliable and robust new constructions exist; these have basically three types of rotors: segmential, flux barrier and axially laminated rotors. In the SYRM with segmental rotor, saliency ratios (L_{sd}/L_{sq}) of 6–7 have been obtained. If the number of rotor segments is very large, then a distributed anisotropic structure is obtained, which is similar to the various axially laminated structures used in the past. By using multiple segmental structures, the saliency ratio can be increased. In the SYRM with axially laminated rotor, the rotor is made of conventional axial laminations bent into U or V shapes and stacked in the radial direction. With this structure it is possible to produce very high saliency ratios, and saliency ratios of 9–12 have been obtained. This also leads to fast torque responses. A synchronous reluctance machine is a salient-pole machine which produces reluctance torque.

. . . . ***Permanent Magnet Machines*** In a permanent magnet synchronous motor with surface-mounted magnets, torque control can be achieved very simply, since the instantaneous electromagnetic torque can be expressed similarly to that of the dc machine given by Eqn. (28.1):

$$t_e = c_F \psi_F i_{sq} \tag{28.5}$$

where c_F is a constant, ψ_F is the magnet flux (rotor flux in the rotor reference frame), and i_{sq} is the torque-producing stator current component (quadrature-axis stator current in the rotor reference frame). Both ψ_F and i_{sq} are shown in Fig. 28.3(b). Equation (28.5) can be obtained in many ways. However, according to simple physical considerations, the electromagnetic torque must be maximum when the torque angle (δ) is 90°, and the torque varies with the sine of the torque angle, which is the angle between the space vector of the stator currents and the magnet flux (it is also shown in Fig. 28.3(b)). It follows from Fig. 28.3(b) that the quadrature-axis stator current is $|\bar{i}_s| \sin\delta$. The expression of the torque is also similar to those shown in Eqns. (28.2)–(28.4) for the induction motor, and this is an expected physical feature. It can also be seen that the electromagnetic torque can be controlled by controlling the stator currents. The torque expression also follows directly from the fact that for all singly salient electrical machines the instantaneous electromagnetic torque can be considered to be equal to the cross vectorial product of the stator flux linkage space vector and stator current space vector:

$$t_e = c_F(\bar{\psi}'_s \times \bar{i}'_s) = c_F(L_s \bar{i}'_s + \psi_F) \times \bar{i}'_s = c_F \psi_F \times \bar{i}'_s = c\psi_F i_{sq} \tag{28.6}$$

where the cross-vectorial product is denoted by ×, and $\bar{\psi}'_s$ and $\bar{i}'_s$ are the space vectors of the stator flux linkage and stator current space vectors, respectively, in the rotor reference frame and L_s is the stator inductance (ψ_F is the magnet flux). It can be seen that the electromagnetic torque is proportional to the magnet flux (rotor flux) and the quadrature-axis stator current (torque producing stator current). If the magnet flux is constant, and the quadrature-axis current is changed rapidly (e.g. by a current-controlled PWM inverter), a quick torque response is obtained.

In contrast to the vector control scheme of the induction motor, the vector control scheme of the permanent magnet induction motor is simpler. This follows from the fact that the magnet flux is fixed to the direct axis of the rotor reference frame and the space angle between the magnet flux and the direct axis of the stator reference frame is equal to the rotor angle, θ_r, which can be monitored by using a position sensor (in a "sensored" drive). In contrast to this, in the induction motor, e.g. if rotor-flux-oriented control is performed, it is also necessary to know the position of the rotor flux linkage space vector with respect to the direct axis of the stator reference frame, and in general this angle is not equal to the rotor angle and its determination requires the use of a flux model. In the vector control scheme for the pm synchronous motor the quadrature-axis stator current (in the rotor reference frame) can be obtained simply by considering that, when the stator current vector is expressed in the rotor reference frame, then $\bar{i}'_s = \bar{i}_s \exp(-j\theta_r)$. In this expression the rectangular form of the stator current vector in the rotor reference

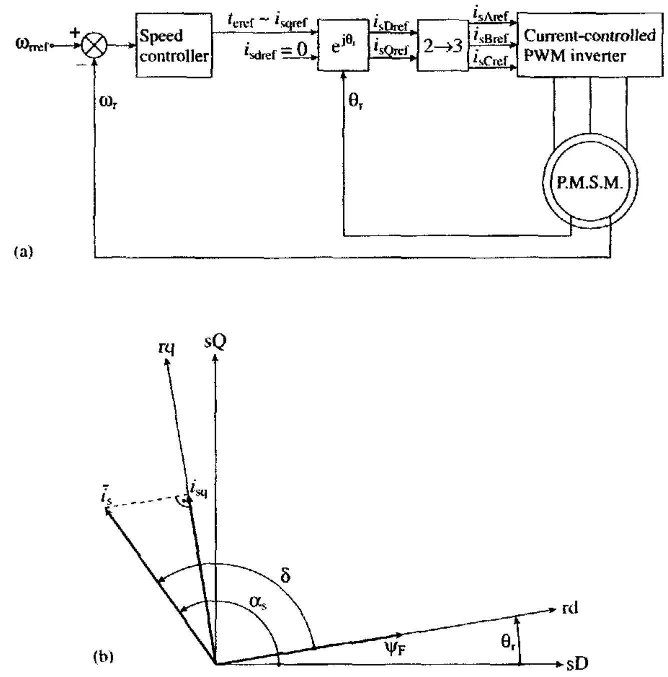


FIGURE 28.3 Rotor-oriented vector control scheme of a permanent magnet synchronous motor with surface mounted magnets supplied by a current-controlled PWM inverter. (a) Drive scheme and (b) vector diagram.

frame is $\bar{i}_s' = i_{sd} + j i_{sq}$, and the stator current vector in the stator (stationary) reference frame is $\bar{i}_s = i_{sD} + j i_{sQ} = |\bar{i}_s| \exp(j\alpha_s)$, where as shown in Fig. 28.3(b), α_s is the angle of the stator current vector (with respect to the direct axis of the stationary reference frame). Thus finally $\bar{i}_s' = i_{sd} + j i_{sq} = |\bar{i}_s| \exp[j(\alpha_s - \theta_r)]$ is obtained, yielding

$$i_{sq} = |\bar{i}_s| \sin(\alpha_s - \theta_r) = |\bar{i}_s| \sin(\delta) \qquad (28.7)$$

in agreement with that discussed above, and hence the electromagnetic torque can be expressed as

$$t_e = c_F \psi_F |\bar{i}_s| \sin(\alpha_s - \theta_r) = c_F \psi_F i_{sq} \qquad (28.8)$$

It follows that, if the stator current modulus and angle are known (e.g. by using a rectangular-to-polar conversion of the measured direct- and quadrature-axis stator current components i_{sD}, i_{sQ}) and the rotor angle (θ_r) is measured (e.g. by a suitable position sensor), then the quadrature-axis stator current can be simply determined according to Eqn. (28.7). As stated above, Eqn. (28.8) is physically expected, since it shows that the electromagnetic torque varies with the sine of the torque angle (torque angle $\delta = \alpha_s - \theta_r$). It also follows that maximum torque per stator current is obtained when the torque angle is ninety degrees.

Equation (28.8) forms the basis of rotor-oriented vector control schemes, which use a position sensor. Figure 28.3(a) shows a possible implementation of a vector-controlled (rotor-oriented controlled) permanent magnet synchronous machine with surface mounted magnets, where the machine is supplied by a current-controlled PWM inverter.

In Fig. 28.3(a) the electromagnetic torque reference (t_{eref}) is proportional to i_{sqref}, since $t_{\text{eref}} = c\psi_F i_{\text{sqref}}$. Below base speed, $i_{\text{sdref}} = 0$, since in this case the torque angle is 90° and maximum torque/ampere is obtained. However, above base speed, in the field-weakening range, where the inverter voltage limit is reached, a negative value of i_{sdref} is used and in this case the torque angle is larger than 90°. Since the stator current modulus $|\bar{i}_s|$ cannot exceed its maximum value (i_{smax}), thus $|\bar{i}_s| = \sqrt{(i_{sd}^2 + i_{sq}^2)} \leq i_{\text{smax}}$, the quadrature-axis stator current i_{sq} may have to be reduced, thus t_{eref} may also have to be limited. The stator current components in the stationary reference frame (i_{sDref}, i_{sQref}) are obtained by using the transformation $\exp(j\theta_r)$, and this is followed by the application of the two-phase-to-three-phase transformation. This scheme is similar to that shown in Fig. 28.2(a). However, for the permanent magnet synchronous motor, in Fig. 28.3(a) the rotor position (θ_r) is used (rotor-oriented control) instead of the position (ρ_r) of the rotor flux linkage space vector (rotor-flux-oriented control) and the angular slip frequency reference is zero. Furthermore below base speed, $i_{\text{sdref}} = 0$.

It is also possible to have a speed-sensorless implementation, where the rotor speed is obtained by utilizing the speed of the stator flux linkage space vector (rate of change of the angle of the stator flux linkage space vector). Although such a drive can be used in a wide speed range, it will not give fully controlled torque operation down to zero speed.

One main difference between the vector control of a synchronous machine and the vector control of an induction machine is their cross-magnetizing behavior. In an electrically excited synchronous machine, the stator currents produce a rotor flux which is in space quadrature to the flux produced by the field winding. Thus, similar to the cross-magnetizing armature reaction of a dc machine, a reduction of the field flux can be caused at high values of torque. In a synchronous machine with surface mounted magnets, normally this demagnetization effect is small, due to the large air-gap associated with the magnets, but at high currents it can cause magnet demagnetization. This effect must be considered when designing the motor. However, in an induction machine subjected to vector control (e.g. rotor-flux-oriented control), the quadrature-axis rotor flux linkage (in the rotor-flux-oriented reference frame) is zero. Thus there is no demagnetization effect caused by the torque producing stator current.

The $i_{sd} = 0$ control method has been a popular technique for a long time and has been used to avoid the demagnetization of the magnet material. In general, in a permanent magnet synchronous motor, where the direct- and quadrature-axis stator inductances (L_{sd}, L_{sq}) are not equal, e.g. for a machine with interior magnets, independent control of i_{sd} (flux-producing current) and i_{sq} (torque-producing current) is possible by considering that the direct-axis stator flux linkage is $\psi_{sd} = \mathrm{Re}(\bar{\psi}'_s) = \psi_F + L_{sd} i_{sd}$ (see also the definition used in Eqn. (28.6) and the expression of the electromagnetic torque is $t_e = c[\psi_F i_{sq} + (L_{sd} - L_{sq}) i_{sd} i_{sq}]$. This last equation follows from the fact that, in general, $t_e = c\bar{\psi}'_s \times \bar{i}'_s$ holds, where $\bar{\psi}'_s = \psi_{sd} + j\psi_{sq}$, $\psi_{sd} = \psi_F + L_{sd} i_{sd}$, $\psi_{sq} = L_{sq} i_{sq}$.

. . . . ***Synchronous Reluctance Machines*** Due to the low cost, simplicity of control, absence of rotor losses and field-weakening capability, recently increased research efforts has focused at varioius industrial and automotive applications of synchronous reluctance motors. The synchronous reluctance motor (SYRM) is a greatly robust singly salient machine (similar to the stator of an induction machine, the stator bore is smooth but slotted and there is a symmetrical three-phase stator winding carrying balanced three-phase currents; however, there is a salient-pole rotor). In a high-performance synchronous reluctance motor the rotor is axially laminated; this results in high saliency ratios (high L_{sd}/L_{sq} where L_{sd} and L_{sq} are the direct- and quadrature-axis synchronous inductances, respectively). The high saliency ratio results in high power density, increased torque, high power factor and increased efficiency. Reluctance torque is created by the alignment of the minimum reluctance path of the rotor with the rotating magnetizing mmf which is produced by the stator currents (there are no rotor currents in a cageless design).

The electromagnetic torque of a SYRM can also be expressed similarly to that of the induction motor or permanent magnet synchronous motor. In general, the electromagnetic torque is developed by the interaction of the stator flux linkage space vector and stator current space vector, thus $t_e = \frac{3}{2} P \bar{\psi}'_s \times \bar{i}'_s$, where P is the number of pole pairs and the stator flux linkage and current space vectors in the rotor reference frame are $\bar{\psi}'_s = \psi_{sd} + j\psi_{sq}$ and $\bar{i}'_s = i_{sd} + ji_{sq}$, respectively. The subscripts d and q denote the direct- and quadrature-axis quantities, respectively, in the rotor (synchronous) reference frame. Due to the absence of rotor currents, the stator flux linkages are established by the stator currents, thus $\psi_{sd} = L_{sd} i_{sd}$, and $\psi_{sq} = L_{sq} i_{sq}$, where L_{sd} and L_{sq} are the direct- and quadrature-axis synchronous inductances, respectively. It follows that

$$t_e = \tfrac{3}{2} P \bar{\psi}'_s \times \bar{i}'_s = \tfrac{3}{2} P(\psi_{sd} i_{sq} - \psi_{sd} i_{sd}) = \tfrac{3}{2} P(L_{sd} - L_{sq}) i_{sd} i_{sq}. \tag{28.9}$$

It is important to note that in Eqn. (28.9) the stator current components (i_{sd}, i_{sq}) are expressed in the rotor reference frame, and can be obtained from the stator currents in the stationary reference (i_{sD}, i_{sQ}) as

$$\bar{i}'_s = i_{sd} + ji_{sq} = \bar{i}_s \exp(-j\theta_r) = (i_{sD} + ji_{sQ}) \exp(-j\theta_r) \tag{28.10}$$

where θ_r is the rotor angle, and this is why in general, the rotor position is required (e.g. in a control scheme using rotor-oriented control) for the transformation of the measured stator currents (i_{sD}, i_{sQ}). For better understanding, Fig. 28.4(b) shows the stator current vector, the stator flux linkage vector and also the various reference frames.

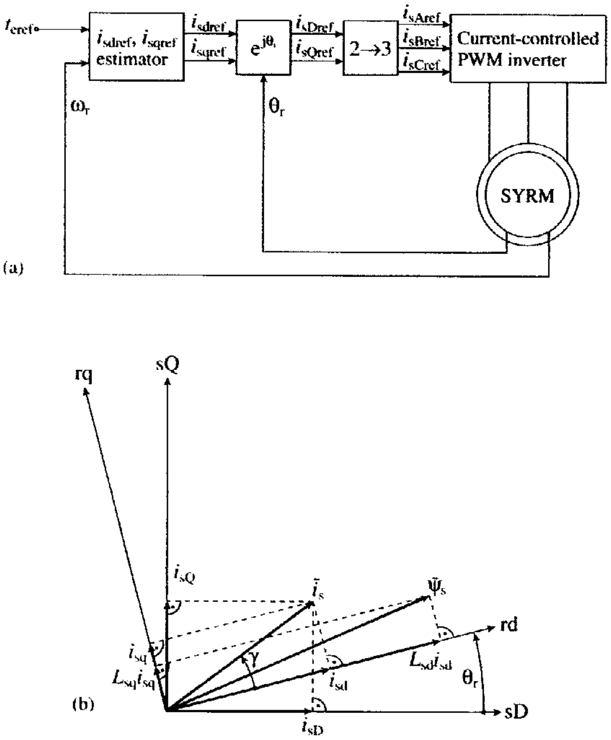


FIGURE 28.4 Rotor-oriented vector control scheme of a synchronous reluctance motor supplied by a current-controlled PWM inverter. (a) Drive scheme and (b) vector diagram.

Equations (28.9) and (28.10) can be used for the implementation of the rotor-oriented control of the synchronous reluctance motor. However, Eqn. (28.9) can also be arranged into the following form, if $\psi_{sd} = L_{sd} i_{sd}$ is utilized:

$$t_e = \tfrac{3}{2} P(L_{sd} - L_{sq}) i_{sd} i_{sq} = [\tfrac{3}{2} P(1 - L_{sq}/L_{sd})] \psi_{sd} i_{sq} = c\psi_{sd} i_{sq} \tag{28.11}$$

where $c = \frac{3}{2} P(1 - L_{sq}/L_{sd})$ and it should be noted that in general it is saturation dependent. Equation (28.11) resembles the torque expression of a separately excited dc motor, to that of a vector-controlled induction motor and also to that of a permanent magnet synchronous motor with surface magnets; see Eqns. (28.1), (28.2), (28.3) and (28.5). In a vector-controlled synchronous reluctance motor drive, where the motor is supplied by a current-controlled PWM inverter, and where rotor-oriented control is performed, independent control of the torque and flux (torque-producing stator current and flux-producing stator current) can be achieved as shown in Fig. 28.4(a).

In Fig. 28.4 the gating signals of the six inverter switching devices are obtained on the output of hysteresis current controllers. On the inputs of these the difference between the actual (measured) and reference stator line currents are present. The three-phase stator current references are obtained from their two-axis components (i_{sD}, i_{sQ}) by the application of the two-phase-to-three-phase ($2 \rightarrow 3$) transformation, and these are obtained from the reference values of i_{sd}, i_{sq} by the application of the $\exp(j\theta_r)$ transformation. These reference values are obtained in the appropriate estimation block from the reference value of the torque (t_{eref}) and the monitored rotor speed (ω_r). This estimation block can be implemented in various ways, according to the required control strategy. In general there are three different constant angle control strategies: fastest torque control, maximum torque/ampere control and maximum power factor control. It can be shown [35] that, for example, the fastest torque response can be obtained by a controller, where $\gamma = \tan^{-1}(L_{sd}/L_{sq})$ where γ is the angle of the stator current space vector with respect to the real-axis of the rotor reference frame (d axis), as shown in Fig. 28.4(b). The rotor-oriented control scheme of the synchronous reluctance machine shown in Fig. 28.4(a) is very similar to the rotor-oriented control scheme of the permanent magnet synchronous machine shown in Fig. 28.3(a).

It should be noted that in a recent book [35] more than 20 types of sensorless vector drives have been discussed in detail.

28.2.2 Fundamentals of Direct-Torque-Controlled Drives

In addition to vector control systems, instantaneous torque control yielding very fast torque response can be obtained by employing direct torque control. Drives with direct torque control (DTC) are finding great interest, since ABB recently introduced the first industrial direct-torque-controlled induction motor drive, which according to ABB can work even at zero speed. This is a very significant industrial contribution, and it has been stated by ABB that "direct torque control (DTC) is the latest ac motor control method developed by ABB" [31, 35].

ABB has recently introduced a DTC based medium voltage drive called the ACS1000 equipped with Sinus Filter, thus feeding pure sinusoidal voltages and currents to the motor. This is ideal for pumps and fans, particularly for retrofits.

ABB has also recently introduced a DTC based current excited synchronous machine drive called the ACS6000 SD. This is particularly suitable for medium voltage metal rolling mill applications.

In a DTC drive, flux linkage and electromagnetic torque are controlled directly and independently by the selection of optimum inverter switching modes. The selection is made to restrict the flux linkage and electromagnetic torque errors within the respective flux and torque hysteresis bands, to obtain fast torque response, low inverter switching frequency and low harmonic losses. The required optimal switching voltage vectors can be selected by using a so-called optimum switching voltage vector look-up table. This can be obtained by simple physical considerations involving the position of the stator flux linkage space vector, the available switching vectors and the required torque and flux linkage.

Figure 28.5 shows the schematic of one simple form of a DTC induction motor drive, which uses the stator flux linkages. Thus it will be referred to as a stator-flux-based DTC induction motor drive, but other forms of DTC drives are also possible, which are based on the rotor flux linkages or magnetizing flux linkages.

In Fig. 28.5 the induction motor is supplied by a VSI inverter and the stator flux linkage and electromagnetic torque errors are restricted within their respective hysteresis bands. For this purpose a two-level flux hysteresis comparator and a three-level torque hysteresis comparator are used respectively. The outputs of the flux and torque comparators ($d\psi$, dt_e) are used in the inverter optimal switching table, which also uses information on the position (ρ_s) of the stator flux linkage space vector. It should be noted that it is not the actual flux linkage vector position which has to be determined, but only the sector where the flux linkage vector is located. It can be seen that the DTC drive scheme requires stator flux linkage and electromagnetic torque estimators. In principle, the stator flux linkages can be estimated by integrating the terminal voltage reduced by the ohmic losses. However, at low frequencies large errors can occur due to the variation of the stator resistance, integrator drift and noise. Therefore, instead of using open-loop flux linkage estimators, other techniques should be used (e.g. flux observer). Observers have reduced sensitivity to parameter variations, but the accuracy of a stator flux linkage observer can be increased by also using online parameter estimators (e.g. for the estimation of the stator resistance), or a thermal model of the machine whose outputs can be used for accurate stator resistance estimation. However, it is also possible to use a joint state and parameter observer which estimates the stator flux linkages, the stator resistance or temperature (required to estimate the "hot" value of the stator resistance), and also the rotor speed (in a "sensorless" drive).

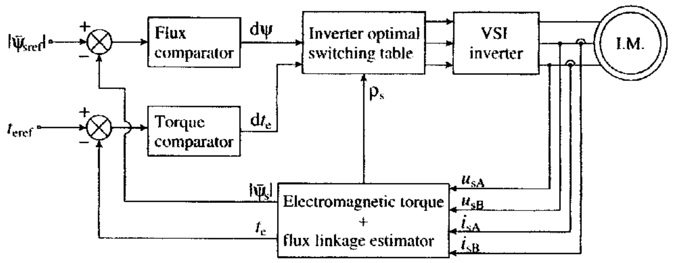


FIGURE 28.5 Schematic of stator-flux-based DTC induction motor drive.

For stator flux linkage estimation it is not necessary to monitor the stator voltages since they can be reconstructed by using the inverter switching functions and the monitored dc link voltage (see also Section 28.2.3.2).

The main features of the DTC can be summarized as: direct control of stator flux and electromagnetic torque; indirect control of stator currents and voltages; approximately sinusoidal stator stator fluxes and stator currents; reduced torque oscillations; excellent torque dynamics; inverter switching frequency depends on flux and torque hysteresis bands. The main advantages of a conventional DTC are: absence of coordinate transformations (which are required in most of the vector-controlled drive implementations); absence of separate voltage modulation block (required in vector drives); absence of voltage decoupling circuits (required in voltage-source inverter-fed vector drives), reduced number of controllers (e.g. only a speed controller is required if the drive contains a speed loop), the actual flux linkage vector position does not have to be determined, but only the sector where the flux linkage is located, etc. However, in general, the main disadvantages of a conventional DTC can be: large torque and flux ripples and variable switching frequency. Measurements on ABB ACS600 DTC drives prove that in ABB's DTC implementation these problems are solved. In general, these problems can be overcome by using suitable techniques: DTCs exist with torque and flux ripple minimization schemes [35, 41], and although the variable switching frequency is caused by the hysteresis control of the electromagnetic torque and stator flux linkage, smaller torque and flux hysteresis widths result in a smoother harmonic spectra.

In the ABB DTC induction motor drive, torque response times typically better than 2 ms are obtained together with high torque control linearity even down to low frequencies including zero speed. According to ABB, the new ac drive technology rests chiefly on a new motor model which enables the computation of motor states without using a speed or position sensor. There is only limited information on the ABB ACS600 motor model. The ABB DTC induction motor drive contains the ACS 600 frequency converter (inverter), shown in Fig. 28.6. The inverter switchings directly control the motor flux linkages and electromagnetic torque.

The ACS 600 product family suits many applications and operating environments, with a large selection of ac voltage, power and enclosure ratings, combined with highly flexible communication capabilities. For illustration purposes Fig. 28.7 shows some measured responses obtained in the ABB sensorless DTC induction motor drive (see also Section 28.2.3, which discusses various speed-sensorless implementation techniques, including the sensorless technique used by ABB).

ABB has also developed a DTC induction motor drive, which combines accurate speed control and direct torque control with line braking for regenerative applications, such as cranes, centrifuges and winding machines in the range 11–50 kW. The ACS 611 incorporates two inverters in one frame. An active inverter replaces the usual diode rectifier (at the input side), thus reducing time harmonics and ensuring an almost perfectly sinusoidal supply. The extra inverter also enables full four-quadrant operation and two-way energy flow, which means that the drive can divert excess energy from a braking motor back into the electrical system, when it is not required by the motor. The DTC technology allows the drive to switch between maximum motoring and maximum generating power in less than five milliseconds, allowing the drive to adapt to highly dynamic changes of the motor load.

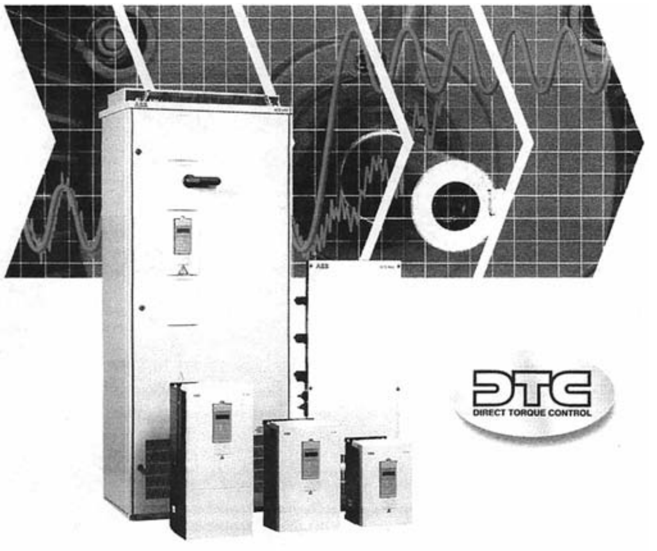


FIGURE 28.6 ACS 600 frequency converter (Courtesy of ABB Industry, Oy, Helsinki).

Regenerative DTC based ACS600 Multidrive is also available from 200 kVA to 4000 kVA.

It should be noted that basically there are two types of DTC drives: conventional DTC drives, where the switching frequency is changing, and DTC drives, with constant switching frequency [35]. It can be shown [40, 41] that in this second type of DTC drive it is relatively easy to ensure reduced torque ripples. For the ACS600 the average switching frequency is controlled.

Other types of DTC drives utilize similar principles to those discussed above, i.e. direct-torque-controlled permanent magnet synchronous machine drives, direct-torque-controlled synchronous reluctance motor drives and direct-torque-controlled electrically excited synchronous motor drives. A recent book [35] discusses 10 types of induction motor and synchronous motor DTC drives, and for this purpose both the voltage-source and current-source inverter-fed drives (VSI, CSI) are considered.

It is important to emphasize some differences between the direct torque control of an induction motor and that of a permanent magnet synchronous motor. For permanent magnet synchronous motors the initial values of the stator flux linkages (in the stationary reference frame) are not zero.

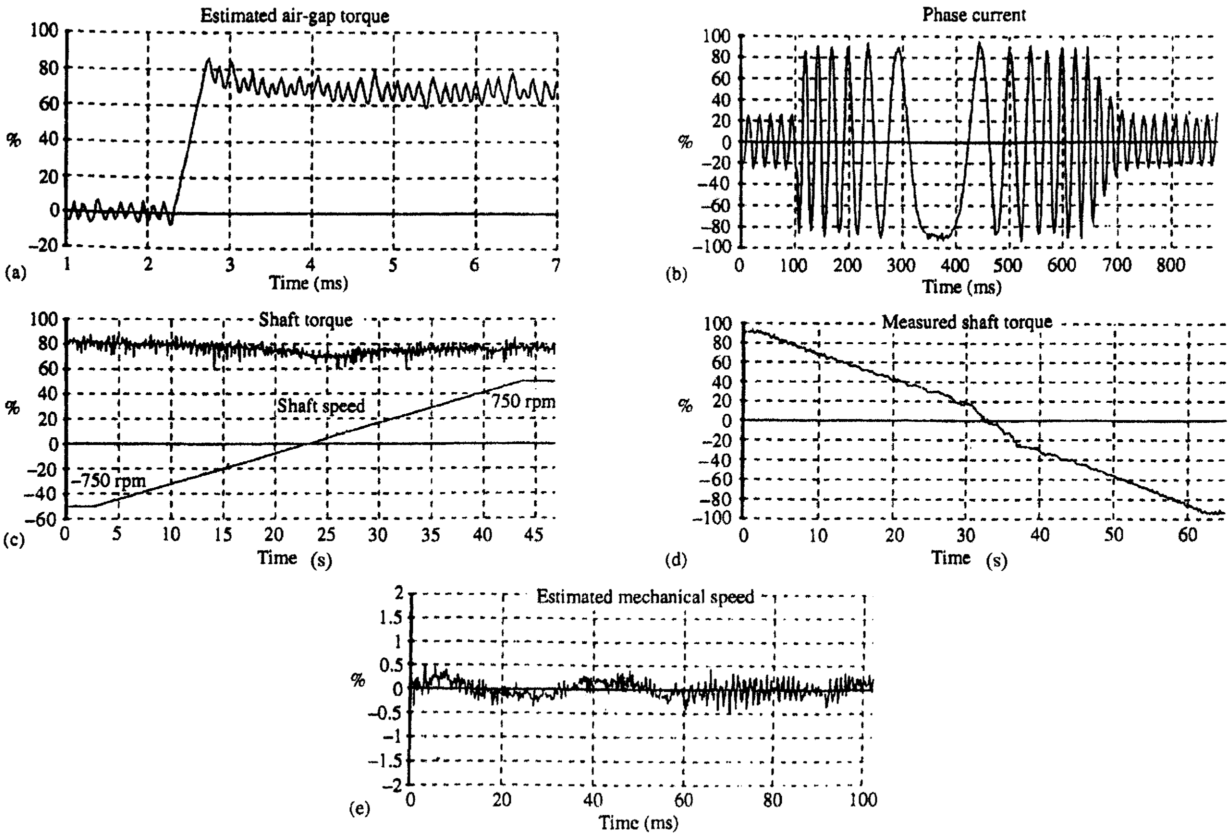


FIGURE 28.7 ABB sensorless DTC drive responses.

Furthermore, in a permanent magnet synchronous motor, the stator flux linkage space vector will change even when zero voltage vectors are applied, since the magnets rotate with the rotor. In addition, it follows from Eqn. (28.5) that, e.g., for the permanent magnet synchronous motor with surface-mounted magnets the electromagnetic torque is proportional to the load angle and not to the slip frequency as in induction motors (the load angle is defined as the angle between the stator and rotor flux linkage space vectors, when the stator resistance is neglected). This is why for controlling the amplitude of the stator flux linkage space vector and for changing the electromagnetic torque (or torque angle) quickly, zero voltage vectors are not used in the direct-torque-controlled permanent magnet synchronous motor drive. The fastest torque response in the permanent magnet synchronous motor drive employing DTC can be obtained by increasing the rotating speed of the stator flux linkage space vector.

28.2.3 Speed and Position Sensorless ac Drive Implementations

In the present subsection, the general aspects of sensorless drives are first discussed. This is followed by discussing the main types of sensorless high-performance ac drive schemes.

28.2.3.1 General, Objectives, Main Types of Sensorless Schemes

In the past few years great efforts have been made to introduce speed and/or shaft position sensorless torque-controlled (vector- and direct-torque-controlled) ac drives. These high-performance drives are usually referred to as "sensorless" drives, although the terminology "sensorless" refers only to the speed and shaft sensors, and there are still other sensors in the drive system (e.g. current sensors), since closed-loop operation cannot be performed without them.

Sensorless vector drives have become the norm for industry and almost every large manufacturer. However, it is a main feature of almost all of these industrial drives that they cannot operate at very low frequencies without speed or position sensors. In general, to solve the problems at low frequencies, a number of special techniques can be used, e.g. which deliberately introduce asymmetries in the machine, or where extra signals are injected into the stator in order to detect various types of anisotropies (due to slots, saturation, etc.). However, so far these techniques have not been accepted by industry, due to the undesirable side effects and other problems [43].

To reduce total hardware complexity and costs, to increase the mechanical robustness and reliability of the drive, to have increased noise immunity, to eliminate cables connecting the mechanical sensors to other parts of the drive, to reduce the overall size, etc., it is desirable to eliminate the conventionally used mechanical (speed, position) sensors in high-performance drives. Furthermore, an electromechanical sensor increases system inertia, which is undesirable in high-performance drives. It also increases the maintenance requirements. In very small motors it is impossible to use electromechanical sensors. In a low-power torque-controlled drive the cost of such a sensor can be almost equal to all the other costs. In drives operating in hostile environments, or in high-speed drives, speed sensors cannot be mounted. As realtime computation (DSP) costs are continuously and radically decreasing (see also Section 28.3 on low-cost Texas Instruments motion control DSPs), speed and position estimation can be performed by using software-based state-estimation techniques where stator voltage and/or current measurements are performed.

The main techniques of sensorless control for induction motor drives [35, 43], which can be used for both vector-controlled and direct-torque-controlled drives are:

1. open-loop estimators using monitored stator voltages/currents
2. estimators using spatial saturation stator phase third harmonic voltage
3. estimators using saliency (geometrical, saturation, etc.) effects
4. model reference adaptive systems (MRAS)
5. observers (Kalman, Luenberger)
6. estimators using artificial intelligence (artificial neural network and fuzzy-logic-based estimators, fuzzy-neural estimators, genetic-algorithm-assisted neural networks, etc.).

The main techniques of sensorless control of vector-controlled and direct-torque-controlled permanent magnet synchronous motor drives are [35, 43]:

1. open-loop estimators using monitored stator voltages/currents
2. stator phase third harmonic voltage-based position estimator
3. back emf-based position estimators
4. observer-based (Kalman, Luenberger) position estimators
5. estimators based on inductance variation due to geometrical and saturation effects
6. estimators using artificial intelligence (artificial neural networks, fuzzy-logic-based systems, fuzzy-neural networks, etc.).

The main techniques for sensorless control of synchronous reluctance motors are [35]:

1. estimators using stator voltages and currents, utilizing speed of stator flux linkage space vector
2. estimators using spatial saturation third harmonic voltage component
3. estimators based on inductance variation due to geometrical effects:
    - indirect position estimation using the measured rate of change of the stator current (no test voltage vector used)
    - indirect flux detection by using measured rate of change of the stator current and applying test voltage vectors/on-line reactance measurement (INFORM) method/low-speed application
    - indirect position estimation using the rate of change of the measured stator current vector by using zero test voltage vector (stator is short-circuited) high speed application
4. estimators using observers (e.g. extended Kalman filter)
5. estimators using artificial intelligence (neural networks, fuzzy-logic-based systems, fuzzy-neural networks, etc.).

In addition to the "sensorless" techniques shown above, it is also possible to implement quasi-sensorless (encoderless) drives, which do not contain conventional speed or position sensors, but where the speed and position information is obtained by using a sensor bearing. For this purpose SKF has developed a family of sensor bearings, and it has been shown [39, 40] that these can also be used in high-performance drives.

The latest field of research in sensorless drives is related to the sensorless position control of induction motors at very low and zero speed. This involves zero speed operation at a predetermined rotor position. In this case the control algorithm must rely on some anisotropic effects (e.g. rotor slotting).

28.2.3.2 Sensorless Drive Schemes

In the present section, various sensorless ac drive schemes are discussed together with encoderless (quasi-sensorless) drive schemes.

. . . . ***Mathematical-Model-Based Schemes*** Due to page restrictions only some of the main principles will be discussed briefly.

Open-Loop Flux Estimators Using Monitored Stator Voltages/Currents, Voltage Reconstruction, Drift Compensation Many types of open-loop and closed-loop flux linkage, position and speed estimators have been discussed in detail in a recent book [35]. The position-sensorless estimators discussed first are open-loop estimators. If the open-loop estimator is a stator flux linkage estimator, then it will also yield the angle of the stator flux linkage space vector with respect to the real axis of the stator reference frame (ρ_s), together with the modulus of the flux space vector. In general, for a synchronous machine, in the steady state, the first time derivative of this angle gives exactly the rotor speed, $\omega_r = d\rho_s/dt$, so accurate estimation of the stator flux vector also yields the rotor speed, and this concept can be used in speed-sensorless synchronous motor drives. However, in the transient state, in a drive where there is a change in the reference electromagnetic torque, the stator flux linkage space vector moves relative to the rotor (to produce a new torque level), and this influences the rotor speed. This effect can be neglected if the rate of change of the electromagnetic torque is limited.

Open-loop flux estimators can use either a voltage model or a current model: these two cases are now discussed. If a *voltage model* is used, in general, the stator flux linkage space vector can be obtained by the integration of the terminal voltage minus the stator ohmic drop:

$$\bar{\psi}_s = \int (\bar{u}_s - R_s \bar{i}_s) dt. \tag{28.12}$$

The voltage space vector ($\bar{u}_s$) and the current space vector ($\bar{i}_s$) are obtained from measurements of the stator voltages and stator currents. Thus the direct- and quadrature-axis stator flux linkage components in the stator reference frame are obtained as

$$\psi_{sD} = \int (u_{sD} - R_s i_{sD}) dt \tag{28.13}$$

$$\psi_{sQ} = \int (u_{sQ} - R_s i_{sQ}) dt \tag{28.14}$$

where the stator voltages and currents can be obtained from the measured line voltages and currents as follows:

$$u_{sD} = \tfrac{1}{3}(u_{BA} - u_{AC}) \tag{28.15}$$

$$u_{sQ} = (-1/\sqrt{3})(u_{AC} - u_{BA}) \tag{28.16}$$

$$i_{sD} = i_{sA} \tag{28.17}$$

$$i_{sQ} = (1/\sqrt{3})(i_{sA} + 2i_{sB}) \tag{28.18}$$

If the stator flux linkage components are known, e.g. they have been obtained by using Eqns. (28.13), and (28.14), then it is also possible to estimate the components of the rotor flux linkage space vector by considering $\bar{\psi}'_r = (L_r/L_m)(\bar{\psi}_s - L'_s\bar{i}_s)$, where $\bar{\psi}'_r$ is the space vector of the rotor flux linkages expressed in the stationary reference frame, $\bar{\psi}'_r = \psi_{rd} + j\psi_{rq}$, L_m and L_r are the magnetizing inductance and rotor self-inductance respectively, and L'_s is the stator transient inductance, $L'_s = \sigma L_s$, where the leakage factor is $\sigma = [1 - L_m^2/(L_s L_r)]$, where L_s is the stator self-inductance. Thus in component form, $\psi_{rd} = (L_r/L_m)(\psi_{sD} - L'_s i_{sD})$ and $\psi_{rq} = (L_r/L_m)(\psi_{sQ} - L'_s i_{sQ})$. It can be seen that the estimation of the stator flux linkage space vector requires integration, and also the stator resistance. The presence of the integrator and the temperature dependency of the stator resistance makes this open-loop estimator impractical at very low stator frequencies (see also below), if some modifications are not made to the estimator.

If the so-called *current model* is used for the estimation of the various flux linkages, then, e.g., for an induction motor the rotor voltage equation is utilized for the estimation of the rotor flux linkage space vector. It then follows from the rotor voltage space vector equation of the induction motor and also by using the defining equations for the stator and rotor flux linkage space vectors that

$$d\bar{\psi}'_r/dt = -(1/T'_r)\bar{\psi}'_r + (L_m/T_r)\bar{i}_s + j\omega_r\bar{\psi}'_r \tag{28.19}$$

where T'_r is the rotor transient time constant ($T'_r = \sigma T_r$, where $T_r = L_r/R_r$ is the rotor time constant). However, it can be seen that this estimator also requires the speed signal (or a position signal), so this is not a sensorless solution. On the other hand, it also follows that this estimator even works at zero frequency, but is sensitive to the detuning of the machine parameters L_m and T_r, which can change due to main flux saturation and temperature effects. To get higher accuracy, parameter adaptation must be used (where the parameters are adapted in realtime).

In comparison, the voltage-model-based flux estimator performs better at higher speeds, since in this case the stator resistance has reduced effects (since the ohmic voltage drop is small). However, at lower speeds, the current-model-based flux estimator performs better, since it can work even at zero frequency, but as mentioned above, it requires a speed or position estimator and is also sensitive to various machine parameters. It follows that a hybrid observer (*hybrid model*), which uses both the voltage-model-based and current-model-based estimators could be used for flux estimation in the entire speed range, but this is not a sensorless solution.

The angle of the stator flux linkage space vector can be obtained from the stator flux linkage components as

$$\rho_s = \tan^{-1}(\psi_{sQ}/\psi_{sD}). \tag{28.20}$$

It is important to note that, e.g., in a vector-controlled induction motor drive using stator flux-oriented control, or in a direct-torque-controlled induction motor drive, and also in a vector-controlled PMSM drive with surface magnets, or in a direct-torque controlled PMSM drive using Eqn. (28.30), depends greatly on the accuracy of the estimated stator flux linkage components and these depend on the accuracy of the monitored voltages and currents, and also on an accurate integration technique. Errors may occur in the monitored voltages and currents due to the following factors: phase shift in the measured values (because of the sensors used), magnitude errors because of conversion factors and gain, offset in the measurement system, quantization errors in the digital system, etc. Furthermore, an accurate value has to be used for the stator resistance, especially if the drive operates at low stator frequency. In general, for accurate flux linkage estimation, the stator resistance must be adapted to temperature changes [43]. The integration can become problematic at low frequencies, where the stator voltages become very small and are dominated by the ohmic voltage drops. At low frequencies the voltage drop of the inverter must also be considered [43]. This is a typical problem associated with voltage-model-based open-loop flux estimators used in all ac drives, which utilize monitored terminal voltages and currents.

Drift compensation is also an important factor in a practical implementation of the integration, since drift can cause large errors of the position of the stator flux linkage space vector. In an analog implementation the source of drift is the thermal drift of analog integrators. However, a transient offset also arises from the dc components which result after a transient change. An incorrect flux angle will cause phase modulation in the control of the currents at fundamental frequency, which, however, will produce an unwanted fundamental frequency oscillation in the electromagnetic torque of the machine. Furthermore, since in the open-loop speed estimator which utilizes the stator flux linkage components, the rotor speed is determined from the position of the stator flux linkage space vector, thus a drift in the stator flux linkage vector will cause incorrect and oscillatory speed values. In a speed control loop, this drift error, will cause an undesirable fundamental frequency modulation of the modulus of the reference stator current space vector ($|\bar{i}_{\mathrm{sref}}|$). The open-loop stator flux linkage estimator can work well down to 1–2 Hz, but not below this, unless special techniques are used. In addition to the stator flux estimation based on Eqns. (28.13) and (28.14), and which is shown in Fig. 28.8(a), it is also possible to construct other stator flux linkage estimators, where the integration drifts are reduced at low frequency. For this purpose, instead of open-loop integrators, closed-loop integrators can be used [35].

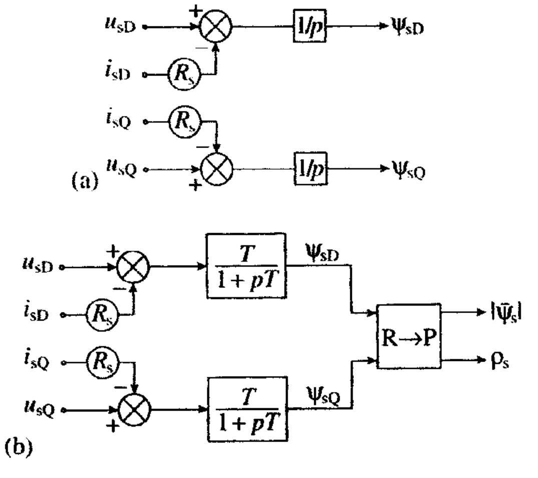
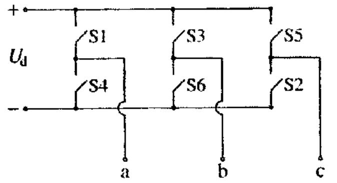


FIGURE 28.8 Stator flux linkage estimators. (a) Estimation in the stationary reference frame, (b) estimation in the stationary reference frame using quasi-integrators.

It is also possible to estimate the stator flux linkage components by using low-pass filters instead of pure integrators. In this case $1/p$ is replaced by $T/(1+pT)$ where T is a suitable time constant. Such a flux linkage estimation scheme is shown in Fig. 28.8(b). To obtain accurate flux estimates at low stator frequency, the time constant T has to be large and the variation of the stator resistance with temperature also has to be considered. It is an advantage of using the flux linkage estimation scheme shown in Fig. 28.8(b) that the effects of initial conditions are damped by the time constant T. Obviously there will be a phase shift between the actual and estimated flux linkages, but increased T decreases the phase shift. However, an increased T decreases the damping.

In vector-controlled and DTC drives it is also possible to use such improved low-pass-filter-based flux estimators, where the magnitude and phase errors introduced by the low-pass-filter are reduced. For example, in a DTC voltage-source inverter-fed induction motor drive the inaccurate flux estimation can lead to incorrect voltage switching vector selection, but the application of an improved low-pass-filter-based flux estimator can lead to reduced current harmonics, reduced torque ripples in the steady state and also to an improved stator flux locus. For this purpose, in the improved flux estimator, in addition to the low-pass filter (which acts on the stator voltage minus ohmic drops), there is an extra compensator circuit, which is connected to the output of the low-pass filter. This compensator adds to the direct-axis stator flux the extra value (ω_c/ω_e) times the quadrature-axis stator flux (which is the first output of the low-pass filter), and it adds to the quadrature-axis stator flux the value (ω_c/ω_e) times the direct-axis stator flux (which is on the second output of the low-pass filter), where (ω_c/ω_e) is the ratio of the cutoff frequency of the low-pass filter and the synchronous frequency. The synchronous frequency can be obtained by using the monitored (or reconstructed) stator voltage, stator current and by also knowing the stator resistance.

The estimation of the stator flux linkage components described above requires the stator terminal voltages. However, it is possible to have a scheme, where these voltages are not monitored, but they are reconstructed from the dc link voltage (U_d) and the switching states (S_A, S_B, S_C) of the six switching devices of a six-step voltage-source inverter [35, 36]. Figure 28.9 shows the schematic of the six switches of the voltage-source inverter and the values of the switching func-



$S_A=1$	S_1 ON	S_4 OFF
$S_A=0$	S_1 OFF	S_4 ON
$S_B=1$	S_3 ON	S_6 OFF
$S_B=0$	S_3 OFF	S_6 ON
$S_C=1$	S_5 ON	S_2 OFF
$S_C=0$	S_5 OFF	S_2 ON

FIGURE 28.9 Inverter switches and the switching functions.

tions are also shown together with the appropriate switch positions.

The stator voltage space vector (expressed in the stationary reference frame) can be obtained by using the switching states and the dc link voltage U_d as

$$\bar{u}_s = \tfrac{2}{3} U_d (S_A + aS_B + a^2 S_C). \tag{28.21}$$

Thus

$$u_{sA} = \mathrm{Re}(\bar{u}_s) = \tfrac{1}{3} U_d (2S_A - S_B - S_C) \tag{28.22}$$

$$u_{sB} = \mathrm{Re}(a^2 \bar{u}_s) = \tfrac{1}{3} U_d (-S_A + 2S_B - S_C) \tag{28.23}$$

$$u_{sC} = \mathrm{Re}(a \bar{u}_s) = \tfrac{1}{3} U_d (-S_A - S_B + 2S_C) \tag{28.24}$$

Hence by the substitution of Eqn. (28.21) into (28.12), the stator flux linkage space vector can be obtained as follows for a digital implementation. The kth sampled value of the estimated stator flux linkage space vector (in the stationary reference frame) can be obtained as

$$\begin{aligned}\bar{\psi}_s(k) = \psi_s(k-1) + \tfrac{2}{3} U_d T[S_A(k-1) + aS_B(k-1) \\ + a^2 S_C(k-1)] - R_s T \bar{i}_s(k-1)\end{aligned} \tag{28.25}$$

where T is the sampling time (flux control period), i_s is the stator current space vector. Resolution of Eqn. (28.25) into its real and imaginary axis components gives ψ_{sD} and ψ_{sQ}. However, it is important to note [43] that Eqn. (28.25) is sensitive to:

- voltage errors caused by dead time effects (e.g. at low speeds, the pulsewidths become very small and the deadtime of the inverter switches must be considered)
- the voltage drop in the power electronic devices
- the fluctuation of the dc link voltage
- the variation of the stator resistance (but this resistance variation sensitivity is also a feature of the method using monitored stator voltages).

Due to the finite turnoff times of the switching devices (power transistors) used in a three-phase PWM VSI, there is a need to insert a time delay (dead time, t_{dead}) after switching a switching device off and the other device on in one inverter leg. This prevents the short-circuit across both switches in the inverter leg and the dc link. Due to the presence of the dead-time, in a voltage controlled drive system, the amplitude of the output voltages of the inverter (stator voltages of the machine) will be reduced and will be distorted. This effect is very significant at low speeds. In space vector terms this means that at very low speeds, the stator voltage space vector locus produced by the inverter, without using any dead-time effect compensation scheme, becomes distorted and the amplitude of the stator voltage space vector is unacceptably small. Due to the presence of the dead time, the output voltage space vector of the inverter is not equal to the desired (reference) voltage space vector, but it is equal to the sum of the desired voltage space vector and an error voltage space vector ($\Delta \bar{u}_k$). The error voltage space vector can be estimated by utilizing information available on the switching times of the power transistors. Various dead-time compensation schemes have been discussed in [35] and, for example, it is possible to implement such dead-time compensation schemes where the existing space vector PWM strategy is not changed but only the reference stator voltage space vector ($\bar{u}_{\mathrm{sref}}$) is modified by adding the error stator voltage space vector.

Recent trends are such, that in position-sensorless drives, the stator voltage sensors are also eliminated and only current sensors are used, but the dc link voltage is also monitored. It is possible to have a position-sensorless drive implementation based on Eqn. (28.25) where the dead-time effects are also considered and the thermal variation of the stator resistance is also incorporated into the control scheme, which will even work at very low speeds. Obviously there are other possibilities as well to solve the problem of integration at low frequencies, e.g. cascaded low-pass filters can be used with programmable time constants, etc. Sometimes it is also possible to use appropriate voltage references instead of actual voltages if the switching frequency of the inverter is high compared to the electrical time constant of the motor. In this case the appropriate reference voltages force the actual currents to follow their references. Such a solution has the additional advantage of further reducing the required number of sensors, and since no filtering of the voltages is required, no delay is introduced due to filtering. In general, a delay introduced by a low-pass filter (acting on the voltages) is a function of the motor speed (since the modulus of the voltage is a direct function of the speed, e.g. at low speeds it is small), thus in a vector-controlled drive it is not possible to keep the stator current in the desired position, as speed changes. This adversely affects the torque/ampere capability and motor efficiency, unless filter-delay compensation is introduced (e.g. by using a lead-lag network).

Open-Loop Speed Estimators In the previous subsection, open-loop flux estimators have been discussed for both induction motors and synchronous motors. In the present subsection it is shown that, if the stator flux linkages are known, then the rotor speed of the induction or synchronous motor can be simply obtained by utilizing the information on the speed of the stator flux linkage space vector.

For the synchronous machine (e.g. permanent magnet synchronous machine), the rate of change of the stator flux position angle, i.e. the first derivative of the angle ρ_s, is equal to the rotor speed (rotor speed is equal to stator flux vector speed), see also Eqn. (28.16):

$$\omega_r = d\rho_s/dt. \tag{28.26}$$

Thus, for example, in the speed control loop of a permanent magnet synchronous motor drive, this relationship can be directly utilized. The estimation of the rotor speed based on the derivative of the position of the stator flux linkage space vector can be slightly modified by considering that the analytical differentiation, $d\rho_s/dt$, where $\rho_s = \tan^{-1}(\psi_{sQ}/\rho_{SD})$, gives

$$\omega_r = (\psi_{sD} d\psi_{sD}/dt - \psi_{sQ} d\psi_{sQ}/dt)/(\psi_{sD}^2 + \psi_{sQ}^2). \quad (28.27)$$

In Eqn. (28.27) the derivatives of the flux linkage components can be eliminated, since they are equal to the respective terminal voltage minus the corresponding ohmic drop; thus:

$$\omega_r = [\psi_{sD}(u_{sD} - R_s i_{sD}) - \psi_{sQ}(u_{sQ} - R_s i_{sQ})]/(\psi_{sD}^2 + \psi_{sQ}^2). \quad (28.28)$$

is obtained. In Eqn. (28.28) the stator flux linkage components can be obtained by using Eqns. (28.13) and (28.14). For digital implementation, Eqn. (28.28) can be transformed into

$$\omega_r(k) = [\psi_{sD}(k-1)\psi_{sQ}(k) - \psi_{sQ}(k-1)\psi_{sD}(k)]/[T_s(\psi_{sD}(k)^2 + \psi_{sQ}(k)^2)] \quad (28.29)$$

where $\omega_r(k)$ is the value of the speed at the kth sampling time, and T_s is the sampling time.

The rotor speed estimation based on the position of the stator flux linkage space vector can also be conveniently used in other schemes, i.e. stator-flux-oriented control of the permanent magnet synchronous machine or in vector-controlled or direct-torque-controlled induction motor drives (e.g. in the case of the induction motor see below). However, in all of these applications, for operation at low speeds, the same limitations hold as above. Furthermore, for the induction motor, $d\rho_s/dt$ will not give the rotor speed, but will only give the speed of the stator mmfs, which is the synchronous speed (ω_s), and the rotor speed is the difference between the synchronous speed and the slip speed ($\omega_r = \omega_s - \omega_{s1}$).

In an induction motor drive, e.g. in the DTC induction motor drive, the speed signal can be required due to two reasons. One reason is that it can be used for stator flux linkage estimation, if the stator flux linkage estimator requires the rotor speed signal (e.g. when a hybrid stator flux linkage estimator is used, which uses both the stator voltage equation, and also the rotor voltage equation, and the rotor voltage equation contains the rotor speed). The other reason is that a rotor speed signal is required if the drive contains a speed control loop (in this case the speed controller outputs the torque reference, and the input to the speed controller is the difference between the reference speed and the estimated speed). In many variable-speed drive applications torque control is required, but speed control is not necessary. An example of an application where the electromagnetic torque is controlled, without precise speed control, is traction drives. In traction applications (diesel-electric locomotives, electrical cars, etc.) the electromagnetic torque is directly controlled, i.e. the electromagnetic torque is the commanded signal, and it is not the result of a speed error signal.

The key to the success of simple open-loop speed estimation schemes is the accurate estimation of the stator (or rotor) flux linkage components. If the flux linkages are accurately known, then it is possible to estimate the rotor speed by simple means, which utilizes the speed of the estimated flux linkage space vector. This technique is used in various commercially available induction motor drives; thus this is now briefly discussed. In these commercial implementations the stator voltages are not monitored but are reconstructed from the dc link voltage and switching states of the inverter (see above).

In an induction motor the rotor speed can be expressed as

$$\omega_r = \omega_{mr} - \omega_{s1} \quad (28.30)$$

where ω_{mr} is the angular speed of the rotor flux (relative to the stator), $\omega_{mr} = d\rho_r/dt$, and ω_{s1} is the angular slip frequency. It follows from the induction motor equations [35] that

$$\omega_{s1} = [L_m/(T_r|\bar{\psi}_r|^2)](-\psi_{rq} i_{sD} + \psi_{rd} i_{sQ}) \quad (28.31)$$

or in terms of the electromagnetic torque

$$\omega_{s1} = (2t_e R_r)/(3P|\bar{\psi}_r|^2) \quad (28.32)$$

where L_m is the magnetizing inductance, T_r is the rotor time constant, t_e is the electromagnetic torque, R_r is the rotor resistance, P is the number of pole pairs, ψ_{rd} and ψ_{rq} are the rotor flux linkage components (in the stationary reference frame), $|\bar{\psi}_r|$ is the modulus of the rotor flux linkage space vector, $|\bar{\psi}_r| = \sqrt{(\psi_{rd}^2 + \psi_{rq}^2)}$, and i_{sD} and i_{sQ} are the stator direct and quadrature axis currents (in the stationary reference frame). Physically, ω_{s1} is the speed of the rotor flux linkage space vector with respect to the rotor. It is possible to obtain an expression of ω_{mr} in terms of the rotor flux linkage components by expanding the expression for the derivative $d\rho_r/dt$. Since the rotor flux linkage space vector expressed in the stationary reference frame is $\bar{\psi}_r' = \psi_{rd} + j\psi_{rq} = |\bar{\psi}_r| \exp(j\rho_r)$, thus $\rho_r = \tan^{-1}(\psi_{rq}/\psi_{rd})$, it follows that

$$\begin{aligned}\omega_{mr} &= d\bar{\psi}_r/dt = d[\tan^{-1}(\psi_{rq}/\psi_{rd})]/dt \\ &= (\psi_{rd} d\psi_{rq}/dt - \psi_{rq} d\psi_{rd}/dt)/(\psi_{rd}^2 + \psi_{rq}^2). \quad (28.33)\end{aligned}$$

Substitution of Eqn. (28.33) into Eqn. (28.30) and by also considering Eqns. (28.31) or (28.32), gives

$$\begin{aligned}\omega_r = {} & (\psi_{rd} d\psi_{rq}/dt - \psi_{rq} d\psi_{rd}/dt)/|\bar{\psi}_r|^2 \\ & - [L_m/T_r|\psi_r|^2](\psi_{rd} i_{sQ} - \psi_{rq} i_{sD}) \quad (28.34)\end{aligned}$$

and

$$\omega_{\mathrm{r}} = (\psi_{\mathrm{rd}} d\psi_{\mathrm{rq}}/dt - \psi_{\mathrm{rq}} d\psi_{\mathrm{rd}}/dt)/|\bar{\psi}_{\mathrm{r}}|^2 - (2t_{\mathrm{e}}R_{\mathrm{r}})/(3P|\bar{\psi}_{\mathrm{r}}|^2) \tag{28.35}$$

where the electromagnetic torque can be obtained from

$$t_{\mathrm{e}} = \tfrac{3}{2}P(\psi_{\mathrm{sD}} i_{\mathrm{sQ}} - \psi_{\mathrm{sQ}} i_{\mathrm{sD}}) \tag{28.36}$$

or

$$t_{\mathrm{e}} = \tfrac{3}{2}P(L_{\mathrm{m}}/L_{\mathrm{r}})(\psi_{\mathrm{rd}} i_{\mathrm{sQ}} - \psi_{\mathrm{rq}} i_{\mathrm{sD}}). \tag{28.37}$$

When a rotor speed estimator is based on Eqn. (28.34) or (28.35), it uses the monitored stator currents and, e.g., the rotor flux components, which, however, can be obtained from the stator flux linkages by considering

$$\psi_{\mathrm{rd}} = (L_{\mathrm{r}}/L_{\mathrm{m}})(\psi_{\mathrm{sD}} - L'_{\mathrm{s}} i_{\mathrm{sD}}) \tag{28.38}$$

$$\psi_{\mathrm{rq}} = (L_{\mathrm{r}}/L_{\mathrm{m}})(\psi_{\mathrm{sQ}} - L'_{\mathrm{s}} i_{\mathrm{sQ}}) \tag{28.39}$$

where L_{r} is the rotor self-inductance and L'_{s} is the stator self-inductance. In Eqns. (28.36) and (28.37) the stator flux linkages can be obtained by using monitored stator currents and monitored or reconstructed stator voltages as discussed above, see Eqn. (28.25).

In summary it should be noted that the speed estimators discussed above depend heavily on the accuracy of the flux linkage components used. If the stator voltages and currents are used to obtain the flux estimates, then by considering the thermal variations of the stator resistance, (e.g. by using a thermal model), and also by using appropriate saturated inductances, the estimation accuracy can be greatly improved. However, a speed-sensorless high-performance direct-torque-controlled drive using this type of speed estimator will only work successfully at ultra low speeds (including zero speed), if the flux estimator is some type of a closed-loop observer.

Closed-Loop Observer-Based Flux and Speed Estimation in Vector and DTC Induction Motor Drives, Full-Order Adaptive State Observers, Luenberger and Kalman Observers In general, an estimator is defined as a dynamic system whose state variables are estimates of some other system (e.g. electrical machine). There are basically two types of estimator: open loop and closed loop, the distinction between the two being whether or not a correction term, involving the estimation error, is used to adjust the response of the estimator. A closed-loop estimator is referred to as an observer. As discussed above, in open-loop estimators, especially at low speeds, parameter deviations have a significant influence on the performance of the drive both in the steady state and transient state. However, it is possible to improve the robustness against parameter mismatch and also signal noise by using closed-loop observers.

An observer can be classified according to the type of representation used for the plant to be observed. If the plant is considered to be deterministic, then the observer is a deterministic observer, otherwise it is a stochastic observer. The most commonly used observers are Luenberger and Kalman types [35]. The Luenberger observer (LO) is of the deterministic type and the Kalman filter (KF) is of the stochastic type (of optimal oberserver). The basic Kalman filter is only applicable to linear stochastic systems, and for non-linear systems the extended Kalman filter (EKF) can be used, which can provide estimates of the states of a system or both the states and parameters (joint state and parameter estimation). The EKF is a recursive filter (based on the knowledge of the statistics of both the state and noise created by measurement and system modelling) which can be applied to a non-linear time-varying stochastic system. The basic Luenberger observer is applicable to a linear, time-invariant deterministic system. The extended Luenberger observer (ELO) is applicable to a non-linear time-varying deterministic system. The simple algorithm and the ease of tuning of the ELO may give some advantages over the conventional extended Kalman filter [35].

In high-performance induction machine drives it is possible to use various types of speed and flux observers. These include a full-order (fourth-order) adaptive state observer (Luenberger observer) which is constructed by using the equations of the induction machine in the stationary reference frame by adding an error compensator. This is a system which is also used in some commercial drives. Furthermore, the Extended Kalman Filter (EKF) and the Extended Luenberger Observer (ELO) could also be used [35], but at present, due to the large computational burden, these systems are not used in commercial drives. However, it should be noted that it is also possible to use reduced-order observers, where there is some reduction in computations. An EKF-based sensorless induction motor drive can also work at zero frequency [25].

In the full-order adaptive state observer the rotor speed is considered as a parameter, but in the EKF and ELO the rotor speed is considered as a state variable. Furthermore, as discussed above, whilst the ELO is a deterministic observer, the EKF is a stochastic observer which also uses the noise properties of measurement and system noise. When the appropriate observers are used in high-performance speed-sensorless torque-controlled induction motor drives (vector-controlled drives, direct-torque-controlled drives), stable operation can be obtained over a wide speed range. Various industrial ac drives already incorporate observers and it is expected that, in the future, observers will have an increased role in industrial high-performance vector and direct-torque-controlled drives.

Since at present, the adaptive state observer is the simplest observer used in high-performance drives, this is now described briefly. However, for better understanding, first, a state estimator is described which can be used to estimate the rotor flux linkages of an induction machine. This estimator is then modified so it can also yield the speed estimate, and thus an adaptive speed estimator is derived (to be precise, a speed adaptive flux observer is obtained). To obtain a stable system, the adaptation mechanism can be derived by using the state error dynamic equations together with Lyapunov's stability theorem [35]. In an inverter-fed drive system, the observer uses the monitored stator currents together with the monitored (or reconstructed) stator voltages, or reference stator voltages. However, when the reconstructed stator voltages or reference voltages are used, some error compensation schemes must also be used.

A state observer is a model-based state estimator, which can be used for the state (and/or parameter) estimation of a non-linear dynamic system in realtime. In the calculations, the states are predicted by using a mathematical model (the estimated states are denoted by $\hat{x}$), but the predicted states are continuously corrected by using a feedback correction scheme. This scheme makes use of actual measured states (x) by adding a correction term to the predicted states. This correction term contains the weighted difference of some of the measured and estimated output signals (the difference is multiplied by the observer feedback gain, G). Based on the deviation from the estimated value, the state observer provides an optimum estimated output value ($\hat{x}$) at the next input instant. In an induction motor drive a state observer can also be used for the realtime estimation of the rotor speed and some of the machine parameters, e.g. stator resistance. This is possible since a mathematical dynamic model of the induction machine is sufficiently well known. For this purpose the stator voltages and currents are monitored on-line and for example, the speed and stator resistance of the induction machine can be obtained by the observer quickly and precisely. The accuracy of the state observer also depends on the model parameters used. By using a DSP, it is possible to conveniently implement the adaptive state observer in real time. The state observer is simpler than the Kalman observer, since no attempt is made to minimize a stochastic cost criterion.

To obtain the full-order non-linear speed observer, first the model of the induction machine is considered in the stationary reference frame and then an error compensation term is added to this. The simplest derivation uses the stator and rotor space vector equations of the induction machine [35]. These yield the state variable equations in the stationary reference frame if the space vectors of the stator currents ($\bar{i}_s$) and rotor flux linkages ($\bar{\psi}'_r$) are selected as state variables:

$$dx/dt = Ax + Bu \qquad (28.40)$$

where the input matrix is $B = [I_2/L'_s, 0_2]^T$. Furthermore, the output equation is defined as

$$i_s = Cx. \qquad (28.41)$$

In Eqn. (28.40) $x = [i_s, \psi'_r]$ is the state vector, which contains the stator current column vector, $i_s = [i_{sD}, i_{sQ}]^T$ and also the rotor flux linkage column vector, $\psi'_r = [\psi_{rd}, \psi_{rq}]^T$. Furthermore, u is the input column vector, which contains the direct and quadrature axis stator voltages $u = u_s = [u_{sD}, u_{sQ}]^T$. The state matrix A is a 4×4 matrix and is dependent on the angular rotor speed (ω_r), I_2 is a second-order identity matrix, $I_2 = \mathrm{diag}(1, 1)$, and 0_2 is a two-by-two zero matrix. In Eqn. (28.41) C is the output matrix, $C = [I_2, 0_2]^T$. Equation (28.40) can be used to design the observer and for this purpose the correction term described above is added (this contains the difference of actual and estimated states). Thus a full-order state observer, which estimates the stator currents and rotor flux linkages can be described as

$$d\hat{x}/dt = \hat{A}\hat{x} + Bu + G(i_s - \hat{i}_s)$$
$$\hat{A} = \begin{bmatrix} -[1/T'_s + (1-\sigma)/T'_r]I_2 & [L_m/(L'_s L_r)][I_2/T_r - \hat{\omega}_r J] \\ L_m I_2/T_r & -I_2/T_r + \hat{\omega}_r J \end{bmatrix} \qquad (28.42)$$

where L_m and L_r are the magnetizing inductance and rotor self-inductance, respectively, L'_s is the stator transient inductance, $T'_s = L'_s/R_s$ and $T'_r = L'_r/R_r$ are the stator and rotor transient time constants, respectively, and $\sigma = 1 - L_m^2/(L_s L_r)$ is the leakage factor. Furthermore

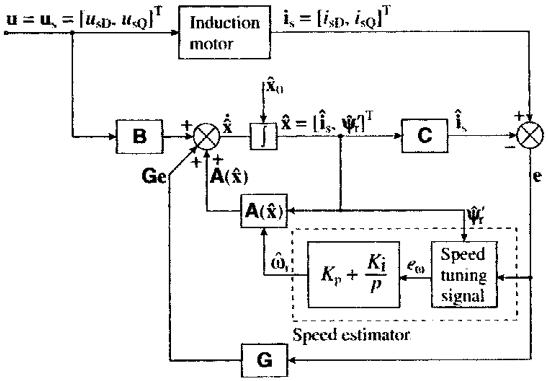
$$J = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}.$$

In Eqn. (28.42) the output vector is

$$\hat{i}_s = C\hat{x} \qquad (28.43)$$

where ^ denotes estimated values. It can be seen that the state matrix of the observer ($\hat{A}$) is a function of the rotor speed, and in a speed-sensorless drive the rotor speed must also be estimated. The estimated rotor speed is denoted by $\hat{\omega}_r$, and in general $\hat{A}$ is a function of $\hat{\omega}_r$. It is important to note that the estimated speed is considered as a parameter in $\hat{A}$; however, in some other types of observers (e.g. extended Kalman filter), the estimated speed is not considered as a parameter, but it is a state variable. In Eqns. (28.42) and (28.43) the estimated state variables are $\hat{x} = [\hat{i}_s, \hat{\psi}'_r]^T$ and G is the observer gain matrix, which is selected so that the system will be stable. In Eqn. (28.42) the gain matrix is multiplied by the error vector $e = i_s - \hat{i}_s$ where i_s and $\hat{i}_s$ are the actual and estimated stator current column vectors respectively, $i_s = [i_{sD}, i_{sQ}]^T$, $\hat{i}_s = [\hat{i}_{sD}, \hat{i}_{sQ}]^T$. By using Eqns. (28.42) and (28.43) it is possible to implement a speed estimator which estimates the rotor speed of an induction machine by using the adaptive state observer shown in Fig. 28.10.

In Fig. 28.10 the estimated rotor flux linkage components and the stator current error components are used to obtain the


$\mathbf{u} = \mathbf{u}_s = [u_{sD}, u_{sQ}]^T$
Induction motor
$\mathbf{i}_s = [i_{sD}, i_{sQ}]^T$
$\hat{\mathbf{x}}_0$
B
+
$\dot{\hat{\mathbf{x}}}$
∫
$\hat{\mathbf{x}} = [\hat{\mathbf{i}}_s, \hat{\boldsymbol{\psi}}_r']^T$
C
$\hat{\mathbf{i}}_s$
+
−
Ge
+
+
$\hat{\mathbf{A}}(\hat{\mathbf{x}})$
e
$\mathbf{A}(\hat{\mathbf{x}})$
$\hat{\boldsymbol{\psi}}_r'$
$\hat{\omega}_r$
$K_p + \frac{K_i}{p}$
e_ω
Speed tuning signal
Speed estimator
G

Speed tuning signal
using space vector notation:
$e_\omega = \mathrm{Im}(\hat{\bar{\psi}}_r' \bar{e}^*)$

FIGURE 28.10 Adaptive speed observer (speed adaptive flux observer) in an induction motor drive.

error speed-tuning signal, which can be put into a very compact, simple form when the space vector notation is used: $e_\omega = \mathrm{Im}(\hat{\bar{\psi}}_r' \bar{e}^*)$, where $\hat{\bar{\psi}}_r' = \psi_{rd} + j\psi_{rq}$ and $\bar{e} = e_{sD} + je_{sQ}$. The estimated speed is obtained from the speed-tuning signal by using a PI controller [35], thus:

$$\hat{\omega}_r = K_p(\hat{\psi}_{rq}e_{sD} - \hat{\psi}_{rd}e_{sQ}) + K_i\int(\hat{\psi}_{rq}e_{sD} - \hat{\psi}_{rd}e_{sQ})dt \quad (28.44)$$

where K_p and K_i are proportional and integral gain constants respectively, $e_{sD} = i_{sD} - \hat{i}_{sD}$ and $e_{sQ} = i_{sQ} - \hat{i}_{sQ}$ are the direct and quadrature axis stator current errors, respectively.

In summary it can be seen that an adaptive observer can be used to obtain the rotor flux estimates $(\hat{\psi}_{rq}, \hat{\psi}_{rd})$ and the rotor speed is estimated by using the estimated rotor flux linkages and using the stator current errors (e_{sD}, e_{sQ}). This is why the precise name of this speed observer is "speed adaptive flux observer". The rigorous proof can be obtained by using Lyapunov's stability theory or by applying Popov's hiperstability theorem [35].

If the chosen PI constants K_p and K_i are large, then the convergence of the rotor speed estimation will be fast. However, in a PWM inverter-fed induction machine, the estimated speed will be rich in higher harmonics, due to the PWM inverter. Thus the PI gains must be limited when the stator voltages and currents are obtained asynchronously with the PWM pattern. To ensure stability (at all speeds), the conventional procedure is to select observer poles which are proportional to the motor poles (the proportionality factor is k). This makes the observer dynamically faster than the induction machine. However, to make the sensitivity to noise small, the proportionality constant is usually small. The scheme can give accurate results above 1–2 Hz. However, in a discrete implementation of the speed observer, for small sampling time and low speed, accurate computation is required; otherwise, due to computational errors, stability problems can occur (roots are close to the stability limit). For this purpose, another pole placement procedure could be used, which ensures that the low speed roots are moved away from the stability limit [35].

For DSP implementation the discretized form of the observer and the adaptation mechanism have to be used. Thus the discretized observer is described by $\hat{x}(k+1) = A_d\hat{x}(k) + B_d u(k) + G_d[i_s(k) - \hat{i}_s(k)]$, where G_d is the discretized observer gain matrix, $A_d = \exp(AT) \approx I_4 + AT + (AT)^2/2$ is the discretized system matrix, where T is the sampling time, and $B_d = \int[\exp(AT)]B_d\tau \approx BT + ABT^2/2$.

The speed observer discussed above will only give correct speed estimates if correct machine parameters are used in the system matrix and in the input matrix. However, these also contain the stator and rotor transient time constants, T_s' and T_r', which also vary with temperature (since they depend on the temperature-dependent stator and rotor resistances, respectively. The variation of the stator resistance has significant influence on the estimated speed, especially at low speeds. On the other hand, in a high dynamic performance induction motor drive, where the rotor flux is constant, the influence of the rotor resistance variation is constant, independent of the speed, since the speed estimation error and the rotor resistance error cannot be separated from the stator variables. The influence of the stator resistance variation on the speed estimation can be removed by using an adaptive stator resistance estimation scheme [35] and in this case, a drive using this scheme can be operated in a stable manner in a very wide speed range, including extremely low speeds as well. However, it should be noted that the speed observer discussed above uses the monitored stator voltages. In a PWM inverter-fed induction machine the stator voltages contain harmonics due to the inverter and also the degree of voltage measurement deteriorates at low speeds. These problems can be overcome in various ways, e.g. by reconstructing the stator voltages from the inverter switching states by using the monitored dc link voltage (see above). Alternatively, in a drive system, instead of the measured stator voltages it is also possible to use the reference voltages, e.g. these are the inputs to a space-vector PWM modulator. If this technique is used for the induction machine, to obtain high accuracy, it is necessary to compensate for the error between the reference and actual stator voltages by the estimation of the voltage error. For this purpose the adaptive observer shown in Fig. 28.10 must be complemented by a voltage error estimator block. This voltage error contains both a dc and an ac component, corresponding to a constant bias error between the real and reference voltage and also to an amplitude error. These errors are present due to the dead time which is required to prevent the short circuits of the inverter arms, errors caused by A/D quantization, voltage drops of the switching devices, etc. The modified observer with stator voltage error compensator is simple to implement and significantly improves the system behavior. The extra parts of this observer scheme contain a stator voltage error estimator. It can be shown by simple considerations that this voltage error estimator outputs the integral of $G(i_s - \hat{i}_s)$ and this signal is manipulated into other signals which are then added to the reference voltages to obtain the correct stator voltages.

MRAS-Based Flux and Speed Estimation in Vector and DTC Drives For an induction machine, the open-loop speed and flux linkage estimators discussed above have utilized the stator and rotor voltage equations of the induction machine. However, the accuracy of these open-loop observers depends strongly on the machine parameters. In closed-loop estimators the accuracy can be increased. For induction motor drives five rotor speed observers using Model Reference Adaptive System (MRAS) have been described in [35]: the first four schemes are mathematical-model-based schemes, but the fifth scheme is an artificial-intelligence-assisted MRAS scheme. In a mathematical-model-based model reference adaptive system, two estimators are used. One of these is the so-called reference model, which does not include the rotor speed and the other is the so-called adjustable model, which contains the rotor speed. The outputs of the two estimators are then compared, and the error is used to obtain the adaptation mechanism (adaptation model, e.g. expression of the estimated speed).

In general, in a MRAS system, some state variables, x_d, x_q (e.g. rotor flux linkage components, ψ_{rd}, ψ_{rq}, or back emf components, e_d, e_q, etc.) of the machine (which are obtained by using measured quantities, e.g. stator voltages and currents) are estimated in a reference model and are then compared with state variables $\hat{x}_d$, $\hat{x}_q$ estimated by using an adaptive model. The difference between these state variables is then used in an adaptation mechanism, which outputs the estimated value of the rotor speed ($\hat{\omega}_r$) and adjusts the adaptive model until satisfactory performance is obtained. Such a scheme is shown in Fig. 28.11(a) for an induction machine, where the compact space vector notation is used. However, Fig. 28.11(b) corresponds to an actual implementation, and here the components of the space vectors are shown.

The appropriate adaptation mechanism (expression of the estimated rotor speed) can be derived, e.g. by using Popov's criterion of hyperstability. This results in a stable and quick response system, where the differences between the state variables of the reference model and adaptive model (state errors) are manipulated into a speed-tuning signal (ε), which is then an input into a PI-type of controller (shown in Fig. 28.11(c)), which outputs the estimated rotor speed. Four mathematical-model-based schemes have been discussed in [35]: these use the speed-tuning signals $\varepsilon_\omega = \mathrm{Im}(\bar{\psi}'_r \hat{\bar{\psi}}'^*_r)$, $\varepsilon_e = \mathrm{Im}(\bar{e}\hat{\bar{e}}^*)$, $\varepsilon_{\Delta e} = \mathrm{Im}(\Delta\bar{e}\bar{i}_s^*)$ and $\varepsilon_{\Delta e'} = \mathrm{Im}(\Delta\bar{p}\bar{i}_s^*)$, respectively. In these expressions $\bar{\psi}'_r$ and $\bar{i}_s$ denote the rotor flux linkage and stator current space vectors, respectively, in the stationary reference frame, $\bar{e}$ denotes the back emf space vector also in the stationary reference frame $\bar{e} = (L_m/L_r)d\bar{\psi}'_r/dt$ and finally the error back emf space vector is defined as $\Delta\bar{e} = \bar{e} - \hat{\bar{e}}$. The symbol ^ denotes the quantities estimated by the adaptive model.

To improve the performance of the observers described, pure integrators are not used in these schemes. Scheme 3 is robust to stator resistance and rotor resistance variations, and can even be used at very low speeds, e.g. 0.3 Hz (but not zero speed). All the MRAS observers use monitored stator currents and stator voltages (or reconstructed voltages). However, an artificial-intelligence-based MRAS speed estimator seems to offer the most satisfactory performance, even at very low speeds (see also Chapter 29).

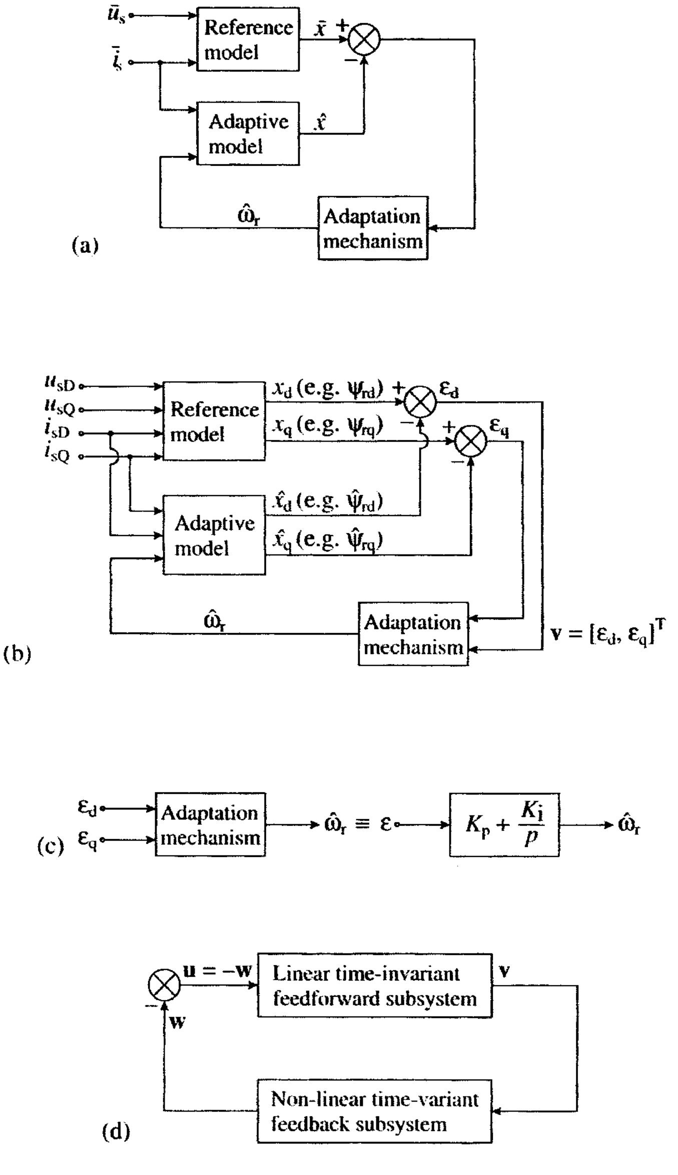

$\bar{u}_s$
$\bar{i}_s$
Reference model
$\bar{x}$
+
−
Adaptive model
$\hat{\bar{x}}$
$\hat{\omega}_r$
Adaptation mechanism
(a)
u_{sD}
u_{sQ}
i_{sD}
i_{sQ}
Reference model
x_d (e.g. ψ_{rd})
x_q (e.g. ψ_{rq})
ε_d
ε_q
Adaptive model
$\hat{x}_d$ (e.g. $\hat{\psi}_{rd}$)
$\hat{x}_q$ (e.g. $\hat{\psi}_{rq}$)
$\hat{\omega}_r$
Adaptation mechanism
$\mathbf{v} = [\varepsilon_d, \varepsilon_q]^T$
(b)
ε_d
ε_q
Adaptation mechanism
$\hat{\omega}_r \equiv \varepsilon$
$K_p + \frac{K_i}{p}$
$\hat{\omega}_r$
(c)
u = −w
Linear time-invariant feedforward subsystem
v
w
Non-linear time-variant feedback subsystem
(d)

FIGURE 28.11 MRAS-based speed estimator scheme. (a) Basic scheme (using space vector notation), (b) basic scheme (using space vector components), (c) adaptation mechanism, (d) equivalent non-linear feedback system.

Estimators Using Saliency Effects In general, in induction motor drives it is possible to estimate the rotor speed, rotor position and various flux linkages of a squirrel-cage induction motor by utilizing different types of saliency effects (rotor slotting, inherent air-gap asymmetry, intentional rotor magnetic saliency created by spatial modulation of rotor slot leakage inductance and other saliency effects, e.g. saliency created by saturation). These techniques are discussed below.

Estimators using rotor slot harmonics

The rotor speed and slip frequency of a cage induction motor can also be estimated by utilizing rotor slot harmonics or eccentricity harmonics. Namely, due to slotting (slot openings), there are slot harmonics produced by the variation of the reluctance due to stator and rotor slots. The rotor slot harmonics cause stator voltage and current harmonics, which can be filtered to obtain the rotor speed signal. In a speed-sensorless high-performance drive, up to now, due to the measurement bandwidth limitation, such an estimator has not been directly used for rotor speed estimation, but it has only been used indirectly to help the tuning of MRAS speed estimators. However, it is possible to use this technique for low-performance applications. It is a major advantage of this technique that variations in the motor parameters do not influence the accuracy of the estimation and the technique can also be used for all loads. The rotor slot harmonics can be detected by using various techniques: utilizing monitored stator voltages or by utilizing monitored stator currents. It should be noted that the technique cannot be used at zero speed, since the slot-harmonic voltages are very small.

Using Monitored Stator Voltages

When stator voltages are monitored the following physical picture is utilized. Since the air-gap mmf contains slot harmonics, slot harmonic voltages are induced in the stator windings when the rotor rotates. Both the amplitude and frequency of these depend on the rotor speed. However, it is difficult to extract information on the rotor speed from the magnitude, because it depends not only on the rotor speed but also on the magnitude of the flux level and the loading conditions. Thus the rotor speed and the slip frequency is obtained from the frequency of these slot harmonic voltages. In a stator phase of an induction machine the magnitude of the induced slot harmonic voltages is small and thus to separate these from the dominating fundamental voltage, the stator phase voltages are added. Thus the resulting voltage, $u_s = u_{sA} + u_{sB} + u_{sC}$, will contain a slot harmonic component u_{sh}, due to the fundamental mmf wave, but due to main flux saturation it will also contain a third harmonic component u_{s3}. Furthermore, when an inverter supplies the induction machine, the stator voltage (u_s), will also contain extra time harmonic voltages, u_{shk}, where k is the time harmonic order. Hence in general $u_s = u_{sh} + u_{s3} + u_{shk}$. The frequency of the slot harmonic voltage components (u_{sh}, u_{shk}) is related to the stator frequency and rotor speed (and the number of rotor slots, which is assumed to be known). If the mmf distribution is assumed to be sinusoidal, then the resulting stator voltage $u = u_{sA} + u_{sB} + u_{sC}$ will contain the rotor slot harmonic voltages (u_{sh}) and the frequency of their dominant component (fundamental slot harmonic frequency) is $f_{sh} = N_r f_r \pm f_1 = 3Nf_1 - N_r f_{s1}$ where $N_r = 3N \pm 1$. In this expression f_r is the rotational frequency of the rotor, $f_r = \omega_r/2\pi$, where ω_r is the angular rotor speed. Furthermore, f_1 is the stator frequency ($f_1 = \omega_1/2\pi$, where ω_1 is the angular stator frequency) and f_{s1} is the slip frequency, $f_{s1} = f_1 - f_r = (\omega_1 - \omega_r)/2\pi = \omega_{s1}/2\pi$, where ω_{s1} is the angular slip frequency and N_r is the number of rotor slots per pole-pair ($N_r = Z_r/P$) (Z_r is the number of rotor slots and P is the number of pole pairs). It follows that the rotor slot harmonic frequency only depends on f_1, f_r and N_r. By considering $\omega_r = \omega_1(1-s)$, where s is the slip, it is also possible to express f_{sh} as $f_{sh} = [Z_2(1-s)/P \pm 1]f_1$.

When the induction machine is supplied by a three-phase inverter, in general, the output currents and voltages of the inverter contain time harmonics (u_{sk}, i_{sk}). Since in the output voltage of the three-phase inverter, there are no harmonic voltages with harmonic orders $3k$, where $k = 1, 2, \ldots$, the voltage (u_s) which is obtained by adding the three stator phase voltages (u_{sA}, u_{sB}, u_{sC}) does not contain time harmonics if the induction motor is symmetrical. However, slot harmonic voltages are present in the stator winding, due to the time harmonic fluxes produced by the time harmonic currents. The slot harmonic frequency due to the kth time harmonic can be expressed as

$$f_{shk} = \begin{cases} N_r f_r \pm kf_1 = 3Nf_1 \pm 6mf_1 - N_r f_{s1} & k = 6m - 1 \\ N_r f_r \pm kf_1 = 3Nf_1 \pm 6mf_1 - N_r f_{s1} & k = 6m + 1 \end{cases}$$

where $N_r = 3N + 1,\ m = 1, 2, \ldots$.

If saturation of the main flux paths occurs, a third-harmonic voltage (u_3) is produced in each stator phase voltage. These third harmonic voltages are in phase with each other and therefore are present in the sum of the phase voltages. In general the magnitude of the third-harmonic voltage in a stator phase is smaller than the magnitude of the fundamental voltage in the corresponding stator phase, but the slot harmonic voltage is also small and thus u_3 cannot be ignored even if the motor operates at rated voltage. The third harmonic voltage is approximately one fifth of the slot harmonic component.

If an induction motor with star-connected stator windings is assumed with the neutral point accessible, then the summation of the stator voltages can be performed by using three potential transformers, whose secondary winding are connected in series. It is also possible to use operational amplifiers to add the three stator voltages, but in a DSP controlled drive the addition can be simply done numerically. Thus u_s is obtained. It follows from above, that u_{sh} can be obtained by removing the voltage components u_{s3} and u_{shk}. This can be achieved by using various circuits [34, 35] and then the frequency of the rotor slot harmonic (f_{sh}) can be obtained from u_{sh}. By subtracting the stator frequency, $f_{sh} - f_1 = N_r f_r$ is obtained and multiplication of this by $2\pi/N_r$ gives the angular rotor speed $\omega_r = 2\pi(f_{sh} - f_1)/N_r$. The slip frequency can be obtained by using $f_{s1} = f_1 - f_r$, where $f_r = \omega_r/2\pi$. However, special considerations are required in the low-speed range, because at low speeds the amplitude of the slot harmonic voltages decrease.

Using Monitored Stator Currents
By utilizing rotor slot harmonics, the rotor speed can also be estimated by using the monitored stator line currents and performing harmonic spectral estimation. This is the preferred technique, since in speed-sensorless drives there is always the need for current monitoring, and it is useful to reduce the number of sensors required (by eliminating the voltage sensors). The stator current slot harmonics can be similarly obtained as given above: thus, if a stator line current of a PWM inverter-fed induction motor is monitored, then $f_{shk} = N_r f_r \pm k f_1$ holds, where $f_r = f_1(1 - s)$.

For the purpose of speed estimation, in a PWM inverter-fed induction motor drive, a line current is monitored, scaled and low-pass filtered (to eliminate high frequency PWM harmonics) and, e.g., digital FFT can be used to detect the speed dependent rotor slot harmonic (f_{sh}). When f_{sh} is known, by using the expression given above for the fundamental slot harmonic frequency, the angular rotor speed can be obtained as $\omega_r = 2\pi f_r = 2\pi(f_{sh} \pm f_1)/N_r$. It follows that the accuracy of the estimated rotor speed depends on the accuracy of the measurement of f_{sh} and f_1.

Estimators using eccentricity
In practice, the air-gap mmf also contains space harmonics due to various types of asymmetries, e.g. eccentricity [35], by neglecting the effects of magnetic saturation, and assuming sinusoidally distributed stator windings, the stator current contain harmonics with the frequencies $f = [(cZ_2 \pm n_d)(1 - s)/P \pm k]f_1$, where f_1 is the fundamental stator frequency, c is any integer, Z_2 is the number of rotor slots, and n_d is the eccentricity order number, which for static eccentricity is zero and for dynamic eccentricity is 1. Furthermore, s is the slip, P is the number of pole pairs and k is the order of the time harmonics ($k = 1, 3, 5, 7$, etc.). It should be noted that, if $c = 1$, and $k = 1$ and $n_d = 0$, the expression reduces to that given above for the dominant slot harmonic frequency. It also follows that for "pure" dynamic eccentricity ($c = 0$, $n_d = 1$, $k = 1$), the current harmonics due to eccentricity are $f = [1 \pm (1 - s)/P]\,f_1$ and this expression is independent of Z_2 and only requires knowledge on the pole-pair number, which can however be obtained by simple measurement. Thus if the pole-pair number is known, and in an initial test the harmonics associated with "pure" dynamic eccentricity are first detected by FFT from the measured stator current, then it is possible to estimate the slip (and also the speed). Although the harmonics caused by pure eccentricity enable Z_2-independent speed and slip estimation, they provide much lower slip resolution than the slot harmonics for a given sampling time. Thus the slot harmonics can be used to provide the accurate speed estimation and the eccentricity harmonics are only used to give extra information for initialization of the slot harmonic estimator. By using the estimated slip and also the expression of the eccentricity harmonics given above, it is then possible to use a search algorithm to obtain Z_2, n_d and k from a table containing possible values of these parameters. When these are known, these parameters can be used in a speed-sensorless induction motor drive using current harmonic spectral estimation. However, this technique cannot be used at zero speed.

Estimation using other techniques which are suitable for low-frequency operation

General
It is possible to estimate flux linkage space vector position (and using this information, the rotor position) by using flux linkage detection based upon saturation induced inductance variations, where test voltages are applied to the stator terminals of the machine and the flux linkage space vector position is detected from measured current responses. Furthermore, in the presence of injected high frequency stator voltages, for the estimation of flux linkage space vector position and the rotor position, it is also possible to use saliency effects, which are due to magnetic saturation (main flux or leakage flux saturation) or saliency effects intentionally created by using special rotor construction, where spatial modulation of the rotor leakage inductance is created (e.g. by periodically varying the rotor slot opening widths or by varying the depths of the rotor slot openings, etc.). In addition, it is also possible to extract the rotor position by using the fact that, in a cage induction motor, the motor leakage inductance varies with the rotor position. Some of these techniques are discussed briefly below.

When an induction motor operates at extremely low frequency, the signal-to-noise ratio of the stator voltage measurement is very poor and the stator ohmic drop is dominant (see also the discussion above on open-loop estimators). Thus it is difficult to obtain an accurate value of the stator (or rotor) flux linkages and the rotor speed by any of the mathematical-model-based speed estimators discussed above. When the conventional mathematical model of the induction machine is used, at zero stator frequency the machine fluxes and the rotor speed are not observable, since in essence the induction motor behaves like a resistance (stator resistance). However, various types of anisotropies (saliency due to saturation, rotor slotting, etc) can be utilized in smooth-air-gap machines for flux, speed and position estimation. For this purpose several techniques exist, but it is a common feature of most of these that they also use injection schemes (voltage or current injection). These allow low-speed operation, but for high-speed operation other schemes must be used. Furthermore, so far, for smooth-air-gap induction machines with closed rotor slots (e.g. for many low- and medium-power induction motors) these techniques have not given satisfactory solutions. This is mainly due to the fact that these algorithms rely on the variation of the rotor leakage inductance with the level of the main flux (there is main flux saturation dependency), but in motors with closed rotor slots, there is also saturation of the leakage fluxes. However, there is one type of algorithm, which can be effectively used even at very low stator (and also zero) stator frequency, but instead of relying on saturation effects, it utilizes the position dependency of the leakage inductance (transient inductance) of a squirrel-cage induction motor. This technique requires voltage sensors and also some modifications to the conventional PWM technique used (see Section 5.3.2).

Estimation Utilizing Saturation Induced Saliencies

Various techniques are described below which utilize saturation induced saliencies. These can be used to obtain the rotor position, rotor speed, flux position, etc.

Estimation using the INFORM technique

A simple technique is described below which in principle can be used for the rotor position estimation of permanent magnet synchronous machines and also synchronous reluctance machines [27, 35, 36]. This technique (the INFORM method) can be well used for motors where there is physical saliency (e.g. permanent magnet motor with interior magnets). This is based on the fact that, in the induction motor, due to saturation of the stator and rotor teeth, the stator inductances depend not only on the level of saturation but also on the position of the main flux. It follows from the stator voltage equation of the saturated induction machine that at standstill the rate of change of the stator currents can be approximated as $di_s/dt = u_s/L$. In this equation L is the complex stator transient inductance of the induction machine, whose magnitude and angle depend on the magnetic operating point and the direction of the magnetizing flux linkage space vector. By applying appropriate stator voltage test vectors (u_s), the rate of change of the stator current space vector (di_s/dt) can be measured. The angle of the magnetizing flux linkage space vector can then be obtained since the locus of the modulus of the complex transient inductance is an ellipse and the minimum of this ellipse is in the direction of the magnetizing flux linkage space vector. The INFORM technique has to be complemented by a Kalman filter or another state observer and needs the use of other sensorless techniques for higher speeds.

Estimation using high-frequency magnetic saliency

It is also possible to estimate flux linkage space vector position in an induction machine by tracking of high-frequency magnetic saliency created by magnetic saturation (main flux or leakage flux saturation) at zero or low rotor speeds [3, 16, 35]. For this purpose high-frequency voltages or currents are injected in the stator of the induction machine. In a VSI-fed drive, the injected voltages can also be produced by the PWM VSI used in the drive scheme (thus no extra injection circuit is required). It will be shown below that this technique is only possible in a saturated smooth air-gap machine, due to the physically existing cross-saturation effect (which effect is due to the saliency caused by saturation).

It is well known [33] that, as a consequence of magnetic saturation, saliency is created and the stator direct and quadrature axis inductances become asymmetrical ($L_{sD} \neq L_{sQ}$) and also coupling will exist between the two axes (cross-saturation effect, $L_{DQ} \neq 0$). It has been shown [33] that, due to saturation, all the inductances are functions of the saliency position (μ), and $L_{sD} = L_1 + \Delta L \cos(2\mu)$, $L_{sQ} = L_1 \Delta L \cos(2\mu)$, $L_{DQ} = L_{QD} = \Delta L \sin(2\mu)$. It then follows that, due to saturation, the stator transient inductances in the direct and quadrature axis (of the stationary reference frame) are also asymmetrical. The direct and quadrature axis stator transient inductances (L'_{sD}, L'_{sQ}) and also the cross-coupling transient inductances ($L'_{DQ} = L'_{QD}$) are functions of the angle μ, and $L'_{sD} = L'_1 + \Delta L' \cos(2\mu)$, $L'_{sQ} = L_1 - \Delta L' \cos(2\mu)$, $L'_{DQ} = L'_{QD} = \Delta L' \sin(2\mu)$, where $L'_1 = (L'_{sd} + L'_{sq})/2$ and $\Delta L' = (L_{sd} - L'_{sq})/2$. In these expressions L'_{sd} and L'_{sq} are the direct and quadrature axis transient stator inductances in the direct and quadrature axes of the existing saliency, respectively. As expected, the cross-saturation coupling and inductance asymmetry disappear when $L'_{sd} = L'_{sq}$.

When high-frequency stator voltages are injected into the stator windings the measured stator currents can be used to obtain information on the position of the saliency. For high stator frequencies, the stator equations of the saturated induction machine in the stationary reference frame can be well approximated by the voltages across the appropriate stator transient inductances. Thus when a symmetrical three-phase high-frequency stator voltage system with amplitude U_{si}, angular frequency ω_i (ω_i is high), is injected into the stator, in the steady state, the stator currents will be displaced from the stator voltages by 90° (since the stator transient inductances are dominant), and it follows from the stator voltage equations (in the stationary reference frame), that the space vector of the stator currents in the stationary reference frame can be expressed as $i_{si} = I_{si0} \exp(j\omega_i t) + I_{si1} \exp[j(2\mu - \omega_i t)]$. This current response can be measured. It can be seen that the first term in the current response is independent of the angle μ; thus, in practice the second term can be used to estimate μ (which is the saliency position). For completeness it should be noted that the amplitudes of the two current components are $I_{si0} = (U_{si}/\omega_i)L'_1/(L'^2_1 - \Delta L'^2)$ and $I_{si1} = (U_{si}/\omega_i)\Delta L'/(L'^2_1 - L'^2)$. It follows that in the absence of cross-saturation (no saliency) $\Delta L' = 0$ and it is not possible to estimate the second term in the expression of the currents (since $I_{si1} = 0$). Furthermore, the first term is a direct measure of the saliency present: it characterizes the average stator transient inductance. By resolving the stator current space vector (i_{si}) into its real and imaginary axis components, i_{sDi} and i_{sQi} are obtained. The angle μ, which is present in the stator current components, can then be extracted in a number of ways. One possibility is to use a demodulation scheme involving heterodyning [16], where the direct axis stator current (i_{sDi}) is multiplied by $\sin(2\hat{\mu} - \omega_i t)$, and the quadrature axis stator current (i_{sQi}) is multiplied by $\cos(2\hat{\mu} - \omega_i t)$, where $\hat{\mu}$ is the estimated saliency angle (in electrical radians) and then the difference of these two signals is obtained: $\varepsilon = i_{sQi}\cos(2\hat{\mu} - \omega_i t) - i_{sDi}\sin(2\hat{\mu} - \omega_i t)$, where ε is the position error signal. When the expressions of the direct and quadrature axis stator currents are substituted into this expression, then the newly obtained expression becomes $\varepsilon = I_{si0}\sin[2(\omega_i t - \hat{\mu})] + I_{si1}\sin[2(\mu - \hat{\mu})]$. The second term of this contains the spatial position information and approaches zero as $\hat{\mu} \to \mu$ (where $\hat{\mu}$ is the estimated and μ is the actual saliency position). The first term can be removed by a low-pass filter. The remaining second part (heterodyned and filtered signal, ε_f) is in the form of a linear position error (as $\hat{\mu} \to \mu$), $\varepsilon_f = I_{si1}\sin[2(\mu - \hat{\mu})] \approx 2I_{si1}(\mu - \hat{\mu})$. This signal can then be used to drive a controller, described by $K_1 + K_2/p$, where K_1 and K_2 are gains of the controller. It follows that the saliency position is obtained as $\hat{\mu} = \int \hat{\omega} dt$, where $\hat{\omega} = (K_1 + K_2/p)\varepsilon_f$. By using the saliency position, it is also possible to obtain estimates of the rotor flux linkages. For this purpose a flux model can be used, thus the measured stator current components of the induction machine are first transformed into the reference frame rotating with the saliency, by using the transformation $\exp(-j\hat{\mu})$, and the obtained transformed stator currents are then used as inputs into the flux model of the machine. The obtained flux linkage components can then be transformed into their stationary axis components ($\hat{\psi}_{rd}$, $\hat{\psi}_{rq}$), by using the transformation $\exp(j\hat{\mu})$. It should be noted that, so far, experimental proof of this saturation-induced saliency technique has not been given for induction motors. The best machine configurations for saturation-induced saliency tracking are those with open or semi-closed rotor slots and are designed so that main flux saturation has a much greater impact on the stator transient inductance than localized leakage saturation. It is important to note that robust tracking of saturation induced saliency may require operation at flux levels which are considerably higher than normal or rated. The maximum operational speed is then limited by core loss and/or stator voltage. Field-weakening greatly beyond base speed may then be not possible.

Another technique has been described recently [4, 36], which allows sensorless vector control at zero flux frequency. With this scheme it is possible to hold a load stationary for a long time, even at zero frequency. For this purpose, saturation effects are again utilized to obtain the position of the rotor flux linkage space vector. However, in this scheme both the stator voltages and currents have to be measured. For estimation purposes a special test current space vector (Δi_s) is added to the reference stator current space vector (i_{sref}), where the test current space vector is pulsating in parallel with the direction of the estimated rotor flux vector axis. It is a very important feature of the scheme that, due to magnetic saturation, the rotor current space vector produced by the test stator current space vector ($-\Delta i_{r\psi}$) is displaced by an angle (γ) with respect to the test current space vector. This follows from the fact that, by assuming fast and small variations of the stator currents, it can be shown that $\Delta i_{r\psi} = \Delta i_{rx} + j\Delta i_{ry}$ where $\Delta i_{rx} = -[1/(1 + L_{rl}/L)]\Delta i_{sx} = k_1\Delta i_{sx}$ and $\Delta i_{ry} = -[1/(1 + L_{rl}/L_m)]\Delta i_{sy} = k_2\Delta i_{sy}$ where k_1 and k_2 are saturation dependent gains, L_{rl} is the rotor leakage inductance, and L and L_m are the dynamic and static inductances, respectively (L is the tangent slope and L_m is the static (chord) slope of the magnetising curve). Under saturated conditions $L < L_m$, and thus $k_2 > k_1$, and therefore the test motion of the stator current space vector (Δi_s) is transferred into the motion of the rotor current space vector without any delay and the current transfer in the x axis (axis coaxial with the rotor flux linkage space vector) takes place with smaller gain than the current transfer in the y axis (axis in space quadrature to rotor flux linkage space vector). In other words, under saturated conditions the space vector $-\Delta i_{r\psi}$ is displaced from the space vector Δi_s by the shifting angle γ. In a saturated machine, it is this effect which causes the shifting angle γ to be different from zero when the estimated rotor flux position ($\hat{\rho}_r$) is different from the actual rotor flux position (ρ_r), i.e. when the error angle is $\delta = \rho_r - \hat{\rho}_r \neq 0$. It is the angle γ which is used to obtain the position of the rotor flux linkage space vector. It is important to note that, if $\rho_r = \hat{\rho}_r$ ($\delta = 0$) then $\gamma = 0$ and, when the shifting angle is not zero, in general it has an opposite direction to the error angle. It follows from the above that, to obtain the shifting angle, the negative rotor current components $-\Delta\hat{i}_{rx}$, $-\Delta\hat{i}_{ry}$ due to the test stator current space vector have also to be known in the estimated-rotor-flux-oriented reference frame.

Another high-frequency injection technique was presented recently [14], where, for the purpose of sensorless rotor flux estimation, a high-frequency signal is injected in the stator of an induction motor. However, this signal is not a rotating signal, but a signal which fluctuates at a synchronous frequency with the fundamental stator frequency. The difference between the direct axis (flux axis) and quadrature axis terminal impedances is used for estimation of the angle of the rotor flux linkage space vector. This difference is small only at fundamental stator frequency, but becomes larger when a high-frequency signal is injected in the stator. The technique makes use of saturation and skin effects. Since the injection signal is independent of the stator frequency, the scheme can work even at very low frequency, but there is a strong dependence on the machine design. When this is also considered, the drive can work with all loads. However, at higher speeds, another sensorless scheme must be used. Another injection scheme was used in an EKF-based sensorless induction motor drive [25], but no experiment results have been shown.

Estimation utilizing saliency introduced by special rotor construction

For the estimation of the rotor position and rotor speed, even at zero and low speeds, it is also possible to use saliency effects, which are intentionally created in an induction motor by using special rotor cage construction, where spatial modulation of the rotor leakage inductance is created. This can be achieved, e.g., by periodically varying the rotor slot opening widths or by varying the depths of the rotor slot openings, etc. In the first case, when the widths of the rotor slot openings are varied, the physical picture is simple: the wider slot openings produce flux paths of high magnetic reluctance, and thus locally low inductance, but the narrow slot openings create low reluctance flux paths and high local inductance. Although it would appear that fully closed or semi-closed rotor slot bridges could increase the amplitude of the reluctance variation, however, it is not useful to extend the spatial modulation depth to these type of slot bridges, since they would magnetically saturate and such saturation would introduce a field dependent variation of the local inductance (but the goal is to have a rotor position dependent inductance variation). It is also possible to create saliency in a cage rotor by having identical rotor slot geometry, but where the height of the conductors in the slot openings is different.

The saliency-based estimation technique resembles the one described in the previous subsection, but the main difference is that in the present case there exists a deliberately introduced saliency due to physical asymmetry, whilst in the previous subsection magnetic saliency existed due to saturation. It should, however, be noted that the introduced rotor saliency is symmetric about each pole, i.e. it is ninety mechanical degrees for a four-pole machine. In order to be able to track the saliency, similarly to that discussed in the previous subsection, symmetrical three-phase high-frequency voltages are injected into the stator, (the amplitude and angular frequency of these are U_{si} and ω_i, respectively). It is shown below that when special (asymmetrical) rotor constructions are used, the stator transient inductances due to asymmetry are position dependent. It is this position dependency of the inductances which causes position-dependent current responses, when the stator is supplied by high-frequency voltages. By measuring these stator currents, it is then possible to extract the information on the rotor position.

When high-frequency stator voltages ($\hat{u}_{si}$) are injected into the stator of the induction machine, it follows from the stator voltage equation of the induction machine in the stationary reference frame that $\hat{u}_{si} \approx d\hat{\psi}_s/dt$, where the stator flux linkage component is mainly a leakage flux component. This contains the appropriate stator transient inductances (sum of stator and rotor leakage inductances). It follows that the stator currents due to the injected stator voltages can be formally expressed in the same way as for the previous scheme. Thus the current response to the injected stator voltages is obtained as $\hat{i}_{si} = I_{si0}\exp(j\omega_i t) + I_{si1}\exp[j(2\theta_r - \omega_i t)]$, which contains a positive-sequence and a negative-sequence stator current component, where $I_{si0} = (U_{si}/\omega_i)(L_{s1} + L'_1)/[(L_{s1} + L'_1)^2 - \Delta L'^2]$ and $I_{si1} = (U_{si}/\omega_i)\Delta L'/[(L_{s1} + L'_1)^2 - \Delta L'^2]$. Mathematically, the expression for i_{si} given above follows directly from the analytical solution of the voltage differential equations. The positive-sequence component rotates at the speed of the injected angular frequency, the negative-sequence component rotates at a speed $2\omega_r - \omega_i$ and the locus of the space vector current i_{si} is an ellipse. This current can be obtained from the measured stator currents by using a bandpass filter (BPF). Although i_{si} contains the rotor position (the angular inclination of the ellipse is equal to the rotor position angle), it is difficult to extract it directly from i_{si}. However, the second component of the stator current contains the rotor angle, and this can be used to estimate the rotor position, by using the same technique as discussed in the previous subsection. It follows that, by using bandpass filtering, $\hat{i}_{si} = i_{sDi} + j i_{sQi}$ is obtained, and by using the direct and quadrature axis currents (i_{sDi}, i_{sQi}) the angular position error signal $\varepsilon = (i_{sQi})\cos(2\hat{\theta}_r - \omega_i t) - (i_{sDi})\sin(2\hat{\theta}_r - \omega_i t)$ is first obtained which can be expressed as $\varepsilon = I_{si0}\sin[2(\omega_i t - \hat{\theta}_r)] + I_{si1}\sin[2(\theta_r - \hat{\theta}_r)]$. The second term contains the rotor position information, and approaches zero as $\hat{\theta}_r \to \theta_r$ (where $\hat{\theta}_r$ is the estimated and θ_r is the actual rotor position). The first term can be removed by a low-pass filter. The remaining second part (heterodyned and filtered signal) is in the form of a linear position error (as $\hat{\theta}_r \to \theta_r$); thus the filtered angular position error signal is $\varepsilon_f = I_{si1}\sin[2(\theta_r - \hat{\theta}_r)] \approx 2I_{si1}(\theta - \hat{\theta}_r)$. This can then be used to drive a PI type of controller, described by $K_1 + K_2/p$, where K_1 and K_2 are gains of the controller: thus, the rotor position is obtained as $\hat{\theta}_r = \int \hat{\omega}_r dt$ where $\hat{\omega}_r = (K_1 + K_2/p)\varepsilon_f$ is the estimated rotor speed. It should be noted that in this scheme the output is $\hat{\theta}_r$, and when this is multiplied by 2 and by using ω_i, $\omega_i t$ is obtained by using an integrator, and thus $(2\hat{\theta}_r - \omega_i t)$ can be obtained. This is then used to get $\cos(2\hat{\theta}_r - \omega_i t)$ and $\sin(2\hat{\theta}_r - \omega_i t)$, which is required in the scheme to get ε. Finally, a low-pass filter is used to obtain ε_f, which is input to a PI controller, which outputs the estimated rotor speed $\hat{\omega}_r$, which is integrated to give the estimated rotor position signal.

In this high-frequency injection scheme, the selection of the injection frequency involves various aspects. The interaction of the injected wave with rotor saliency takes place just below the rotor surface. Thus the injection frequency must be high enough to create a deep bar effect that prevents the high-frequency flux wave from substantially linking with the rotor bars. On the other hand, it must be low enough to ensure that the skin effect in the rotor laminations does not repel the flux from penetrating below the rotor surface. The skin effect restricts the injection frequency to the lower frequency bound of 100 Hz, but the lamination skin effect determines the upper frequency bound, which starts beyond 400 Hz, depending on the thickness of the lamination. The close frequency bounds on either side of the injected signal contribute to a weak position signal.

Finally it should be noted that in practice the various types of saliencies (slot effects, saturation-induced magnetic saliency, deliberately introduced rotor saliency, saliency caused by manufacturing, etc.) can be simultaneously present and they can make the saliency-based estimation task very difficult. In any case, it would appear that, at present, industry is reluctant to employ such sensorless estimation techniques for induction machines which, instead of a conventional cage induction motor, use an induction motor with special rotor cages. On the other hand, for machines which have inherent rotor saliency (e.g. interior permanent magnet motor, synchronous reluctance motor), high-frequency injection and saturation-based techniques could provide simple sensorless solutions for low and zero-speed operation. However, in induction machines problems occur when saturation-induced saliency techniques are used in sensorless drives for the flux estimation, due to the movement of the saturation-based saliencies due to changing flux and torque levels. Thus the position variation of the flux also depends on the operating conditions (torque, flux). This effect becomes even more pronounced in induction motors with closed rotor slots, and the saturation-based sensorless implementation becomes difficult. With regard to the application of high-frequency injection techniques, it should be noted that for machines, with real physical saliency, this can be an attractive sensorless solution. For example, for a synchronous reluctance motor (where due to the physical construction of the rotor saliency exists since $L_{\mathrm{d}} \neq L_{\mathrm{q}}$), if high-frequency sinusoidal stator voltages are injected, then by using the measured high-frequency components of the stator currents it is possible to estimate the rotor position (e.g. by using the demodulation technique described above). This allows low-cost implementations and the sensorless speed/position estimator does not require the use of any machine parameters. However, for high-speed operation, a switchover to other sensorless schemes must be made.

Estimation using the rotor position dependency of the leakage inductance

A rotor position estimation technique has been proposed [17], where the rotor position is estimated in a cage induction motor with a conventional cage rotor (whose rotor is not modified as in the previous scheme described). The estimator requires the monitoring of the phase voltages and utilizes the physical fact that, in a cage induction motor, the total leakage inductances are position dependent. The scheme can work even at zero stator frequency and provides a very accurate position signal. First, it is shown below that the total stator leakage inductances of a cage induction motor are position dependent. This is followed by explaining a position estimation scheme which uses the position dependency of the stator leakage inductance and for this purpose appropriately formed zero-sequence voltages will be used, which can be obtained by using measured stator voltages.

It is well known that the conventional stator transient inductance (total leakage inductance) of an induction motor can be expressed as $L_{\mathrm{s}}' = \sigma L_{\mathrm{s}} = L_{\mathrm{s}} - L_{\mathrm{m}}^2/L_{\mathrm{r}}$. This is based on a machine model, where the flux density distribution is assumed to be sinusoidal. However, in practice, this assumption does not hold, and in general the stator leakage inductance is position dependent because the stator–rotor mutual inductances are position dependent (since the flux density distribution is not sinusoidal). The physical proof is simple and the mathematical proof can be obtained by considering the voltage equations of the motor. For a cage induction motor, where there are N rotor bars, and if only stator winding sA is energized, the expression of the total leakage inductance depends on the rotor angle:

$$L_{\mathrm{s1A}}(\theta_{\mathrm{r}}) = \det L(\theta_{\mathrm{r}})/\det(L_{\mathrm{r}}) \qquad (28.45)$$

where L is an $(N+1) \times (N+1)$ matrix which depends on the rotor position, and L_{r} is the $N \times N$ rotor inductance matrix. Equation (28.45) is very important and allows us to conclude that the total leakage inductance of the cage induction motor varies with the rotor position, and this variation is periodic with $1/N$ revolutions of the rotor. It will now be discussed how the position dependency of the total stator leakage inductances can be used for position estimation in a cage induction motor even at very low (and zero) rotor speed. For this purpose the three stator voltages (u_{sA}, u_{sB}, u_{sC}) are measured when a certain voltage switching vector is applied in the PWM-inverter-fed machine and these voltages are then added to form the corresponding zero-sequence stator voltages. Such a zero-sequence voltage will contain the position information and also induced voltage terms, but by using a combination of two appropriate (opposing) switching voltage vectors and the corresponding zero-sequence voltages, the difference of the two zero-sequence voltages will not contain the ohmic voltage drops and the induced emfs, but they will depend only on the rotor position. This technique is described below whereby the position information is extracted from the difference of the estimated zero-sequence voltages, which apply during the application of the two opposing switching voltage vectors.

In a six-pulse voltage-source inverter (VSI) there are eight switching states (two zero switching states, and six non-zero switching states). The zero switching states occur when all the upper switches of the inverter are connected to the positive dc link rail and the negative switching states occur when the bottom switches of the inverter are connected to the negative dc link rail. However, there are six active switching states, where the six non-zero switching vectors $\bar{u}_1, \bar{u}_2, \ldots, \bar{u}_6$

are produced, and in terms of the dc link voltage, U_d, these switching vectors can be expressed as $\bar{u}_k = \frac{2}{3} U_\mathrm{d} \exp[\, j(k-1)\pi/3]$, where $k = 1, 2, \ldots, 6$. Thus, e.g., in a VSI-fed cage induction motor drive, when the voltage switching vector u_1 is applied by the PWM inverter which supplies the motor and the speed is zero, then it follows from physical considerations that the stator voltages are $u_\mathrm{sA} = U_\mathrm{d}/2$, $u_\mathrm{sB} = -U_\mathrm{d}/2$ and $u_\mathrm{sC} = -U_\mathrm{d}/2$, where U_d is the dc link voltage of the inverter. Thus, if each conducting stator phase is represented by the voltage across its ohmic drop and also its total leakage inductance and the corresponding induced voltage, then by considering that $u_\mathrm{sA} = R_\mathrm{s} i_\mathrm{sA} + L_\mathrm{s1A} di_\mathrm{sA}/dt + u_\mathrm{iA}$, $u_\mathrm{sB} = R_\mathrm{s} i_\mathrm{sB} + L_\mathrm{s1B} di_\mathrm{sB}/dt + u_\mathrm{iB}$ and $u_\mathrm{sC} = R_\mathrm{s} i_\mathrm{sC} + L_\mathrm{s1C} di_\mathrm{sC}/dt + u_\mathrm{iC}$, if the stator voltages are measured and are added (in this way the zero-sequence stator voltage is obtained when the first voltage switching vector u_1 is applied), then by considering that $i_\mathrm{sA} + i_\mathrm{sB} + i_\mathrm{sC} = 0$ and $u_\mathrm{iA} + u_\mathrm{iB} + u_\mathrm{iC} = 0$,

$$\begin{aligned} u_{01} = u_\mathrm{sA} + u_\mathrm{sB} + u_\mathrm{sC} &= (L_\mathrm{s1A} - L_\mathrm{s1C}) di_\mathrm{sA}/dt \\ &\quad + (L_\mathrm{s1B} - L_\mathrm{s1C}) di_\mathrm{sB}/dt \end{aligned} \tag{28.46}$$

is obtained. It can be seen that this zero-sequence voltage contains the total stator leakage inductances (which are position dependent). The goal is to extract the position information by utilizing this zero-sequence stator voltage. However, for this purpose, first, the derivates of the stator currents are removed from Eqn. (28.46). This can be conveniently performed by considering that, when u_1 is applied, and thus the appropriate inverter switches are activated (as discussed above), the induction motor can be described by the following two equations (which are obtained by physical considerations from the resulting connection diagram, where each conducting stator phase is represented by the voltage across its total leakage inductance and the corresponding induced voltage):

$$\begin{aligned} U_\mathrm{d} &= u_\mathrm{sA} - u_\mathrm{sB} \approx L_\mathrm{s1A} di_\mathrm{sA}/dt + u_\mathrm{iA} - L_\mathrm{s1B} di_\mathrm{sB}/dt - u_\mathrm{iB} \\ U_\mathrm{d} &= u_\mathrm{sA} - u_\mathrm{sC} \approx L_\mathrm{s1A} di_\mathrm{sA}/dt + u_\mathrm{iA} - L_\mathrm{s1C} di_\mathrm{sC}/dt - u_\mathrm{iC}. \end{aligned} \tag{28.47}$$

Thus the derivates of the two stator currents can be obtained in terms of the dc link voltage, the various total leakage inductances and the induced emfs, and these can be substituted into the expression of the zero-sequence voltage, Eqn. (28.46). However, although the resulting expression for the zero-sequence voltage will not contain any currents, and will contain the various total stator leakage inductances, in addition to the dc link voltage it will still contain the induced voltages u_iA, u_iB and u_iC. Thus it is not possible to estimate the position directly from this zero-sequence expression, and another expression must be obtained where the induced voltages are not present. The switching state u_1 will occur periodically during normal operation of the PWM inverter-fed VSI drive, and when this occurs, the voltages u_sA, u_sB and u_sC are sampled and summed to give $u_{01} = u_\mathrm{sA} + u_\mathrm{sB} + u_\mathrm{sC}$, which value is temporarily stored. To complete the voltage measurement procedure, the original duration of $\bar{u}_1$ is extended for a very short additional time interval Δt (thus the conventional PWM technique is modified). Thus a flux linkage error is introduced, which is $\Delta\bar{\psi}_1 = \bar{u}_1 \Delta t$, but which is compensated by an additional change of the flux linkage $\Delta\bar{\psi}_4 = \bar{u}_4 \Delta t$, where $\bar{u}_4 = -\bar{u}_1$, i.e. the respective opposed switching vector $\bar{u}_4$ is switched on for the short time Δt. However, if it is considered that, when the switching vector u_4 is applied by the inverter (thus, when $u_\mathrm{sA} = -U_\mathrm{d}/2$, $u_\mathrm{sB} = U_\mathrm{d}/2$ and $u_\mathrm{sC} = U_\mathrm{d}/2$), and if the zero-sequence stator voltage is obtained when u_4 is applied, then the expression of this zero-sequence voltage, u_{04}, can be obtained similarly to that described for u_{01} above. If the difference of the first and fourth zero-sequence voltages is obtained, then the following very important result is obtained:

$$\begin{aligned} P_\mathrm{A} = u_{01} - u_{04} = f_\mathrm{A}(N\theta_\mathrm{r}) &= 2U_\mathrm{d}(L_\mathrm{s1A} L_\mathrm{s1B} + L_\mathrm{s1A} L_\mathrm{s1C} \\ &\quad - 2L_\mathrm{s1B} L_\mathrm{s1C})/(L_\mathrm{s1A} L_\mathrm{s1B} + L_\mathrm{s1A} L_\mathrm{s1C} + L_\mathrm{s1B} L_\mathrm{s1C}). \end{aligned} \tag{28.48}$$

As expected, this difference signal does not contain the stator currents and the induced voltages. Furthermore, in addition to the dc link voltage (which can be assumed to be constant), it only contains the various total stator leakage inductances, which are position dependent. Thus the difference signal will be a function of the rotor position, denoted by $f_\mathrm{A}(N\theta_\mathrm{r})$, and it is the sA axis position signal. The amplitude of this signal does not depend on the speed and it is almost sinusoidal in time: a full cycle represents $1/N$ revolutions of the induction machine. In the practical implementation of the position estimator, the sA axis position signal can be obtained when the inverter switching states $\bar{u}_1$ and $\bar{u}_4$ ($\bar{u}_4 = -\bar{u}_1$) become active. In general, other two position signals (differences of appropriate zero-sequence voltages) can be obtained when a specific switching voltage vector is applied, which is then followed by a second subsequent switching vector, which is the opposing switching vector. In a six-pulse voltage-source inverter, there exist a total of three independent switching states ($\bar{u}_1$, $\bar{u}_4$); ($\bar{u}_3$, $\bar{u}_6$); ($\bar{u}_5$, $\bar{u}_2$) which can be used for this purpose. It can be shown that, by using a similar derivation to that described above, the sB and sC position signals are as follows:

$$\begin{aligned} P_\mathrm{B} = u_{03} - u_{06} = f_\mathrm{B}(N\theta_\mathrm{r}) &= 2U_\mathrm{d}(L_\mathrm{s1A} L_\mathrm{s1B} + L_\mathrm{s1A} L_\mathrm{s1C} \\ &\quad - 2L_\mathrm{s1B} L_\mathrm{s1C})/(L_\mathrm{s1A} L_\mathrm{s1B} + L_\mathrm{s1A} L_\mathrm{s1C} + L_\mathrm{s1B} L_\mathrm{s1C}) \end{aligned} \tag{28.49}$$

and

$$\begin{aligned} P_\mathrm{C} = u_{05} - u_{02} = f_\mathrm{C}(N\theta_\mathrm{r}) &= 2U_\mathrm{d}(L_\mathrm{s1A} L_\mathrm{s1C} + L_\mathrm{s1B} L_\mathrm{s1C} \\ &\quad - 2L_\mathrm{s1A} L_\mathrm{s1C})/(L_\mathrm{s1A} L_\mathrm{s1B} + L_\mathrm{s1A} L_\mathrm{s1C} + L_\mathrm{s1B} L_\mathrm{s1C}). \end{aligned} \tag{28.50}$$

The smoothness of the position signals allows high accuracy position estimation. In summary the following four main steps are made for the estimation of the rotor position:

1. The phase voltages (u_{sA}, u_{sB}, u_{sC}) are measured during the application of a particular pair of opposing switching vectors (e.g. when u_1 is applied and when $\bar{u}_4 = -\bar{u}_1$ is applied).
2. The corresponding zero-sequence voltages are obtained (e.g. these are u_{01} and u_{41}).
3. The position signals f_A, f_B, f_C are estimated: these use the differences of the appropriate zero-sequence voltages which are obtained by measuring the zero-sequence voltages for the opposing switching voltage vectors $f_A(N\theta_r) = u_{01} - u_{04}$, $f_B(N\theta_r) = u_{03} - u_{06}$, and $f_C(N\theta_r) = u_{05} - u_{02}$.
4. The three position signals form a symmetrical three-phase system, if the number of rotor bars (N) is not a multiple of 3 (which holds for almost all rotor cages). Thus a position space vector can be introduced:

$$\bar{f}(N\theta_r)c(f_A + af_B + a^2 f_C) = f_{SD} + j f_{SQ} = |\bar{f}|\exp(jN\theta_r) \tag{28.51}$$

where c is a constant and a is the usual spatial operator, $a = \exp(j2\pi/3)$. From the angle of this space vector it is possible to obtain the position signal $\theta_N = N\theta_r$, as referred to $1/N$ of a mechanical revolution. The rotor position θ_r within a full revolution can then be obtained by incrementing (or decrementing for reversed rotation) a modulo-N counter whenever a complete cycle of $N\theta_r$ is completed. Thus, within a complete revolution, the incremental rotor position is

$$\theta_r = (2_\theta + \theta_N)/N \tag{28.52}$$

where c_θ is the state of the counter.

This position estimator can work at very low frequencies, even at zero frequency. The estimator can estimate the rotor position with high accuracy. It is quasiinstantaneous since an appropriate pair of zero-sequence voltage samples is taken within a few microseconds. The position sampling frequency is approximately 1 kHz, and this ensures high dynamic bandwidth of the position signal, thus enabling fast sensorless control of both the speed and position (since the speed signal can be obtained from the position signal). The estimator described can be used in high-performance drives, e.g. in vector drives and also in such types of direct-torque-controlled drives which use a PWM modulator (e.g. DTC drives with torque ripple reduction techniques [36]. Extreme speed accuracy and high positional accuracy can be maintained even at high loads in the full operating range. The estimator described above requires the use of monitored stator voltages, but another scheme is under development by one of the authors, where the stator voltages do not have to be measured.

Two recent publications [43, 44] have described the details of a new family of sensorless high-performance induction and permanent magnet synchronous motor drives (vector, DTC and natural-field-oriented drives). These can also be operated at low speed and give excellent performance for sustained zero frequency operation as well. They can form the basis of the next generation of commercial sensorless high-performance ac drives. The new family of sensorless drives can be used for traction, domestic, military, automotive, etc. applications. It is a main feature that they use standard, off-the-shelf motors, and do not rely on saturation effects, and do not use high-frequency injection techniques. Some other important features are [43]

- There is a self-commissioning stage (to obtain various motor, inverter parameters).
- There is no integration involved.
- There is no complicated mathematical model of the motor used (in contrast to some industrial sensorless drives).
- There is no stator voltage measurement, only dc link voltage is measured and stator voltages are reconstructed by also using the switching states of the inverter.
- Only two stator currents are monitored (in real-time).
- There is a real-time parameter estimation block, since several motor parameters are changing during operation (e.g. due to thermal effects and skin effect). This enhances the stability and dynamic performance and is a crucial part of the drive schemes developed.
- There is an inverter model (this can be set-up during the self-commissioning stage). This contains dead-time compensation plus the appropriate voltage drop of the inverter switching devices, etc. No hardware is used for dead-time compensation (in contrast to some other sensorless drives discussed in the literature).
- They can be used for low-speed operation and sustained zero frequency operation, although they do not utilize any artificially created saliency (it uses a standard off-the-shelf) three-phase cage induction motor. The new drives can form the basis of the first industrial drives in the world, which can also work at zero frequency.
- They can be used with high and low loads.
- There is precise flux control.
- There is efficient and fast torque control.
- Implementation can be done by using a low-cost DSP (e.g. a fixed point DSP).
- There is no instability phenomena (in contrast to low-speed instabilities in various other sensorless drives).

A very extensive set of industrial standard of experiments have been performed; these prove the excellent features of the new drives. These tests include:

- Fast and slow reversals at low and extremely low speeds (also involving regenerative braking).
- Zero frequency operation for a long period (sustained operation at zero frequency).
- Testing the robustness of the drive against parameter variations
  - using a 2kW heater and a blower (e.g. to cause changes of the stator resistance)
  - adding external stator resistors
  - internally deliberately changing some parameters in the software, etc. (to prove that the drive can work well, since the estimation algorithm will ensure that the parameters will quickly converge to the correct values)
- Operating the drive at very low speed and suddenly applying various loads to confirm that the drive still works well.

A large number of plots have been obtained, examples of these are:

- speed versus load for different speed references
- torque against torque reference (to show the linearity)
- slow and fast transient speed changes (reversals)
- shock load test (motor runs at no load at a specific speed then load is suddenly applied and then removed)

To illustrate the robustness of the new sensorless drives against parameter deviations, and also the successful sustained zero frequency operation. Figures 28.12, 28.13 and 28.14 show experimental results for a sensorless vector controlled induction motor drive, which contains a 2.2kW induction motor. For this purpose the stator resistance of the induction motor was changed by switching on and off a 2 kW heater and blower mentioned above. Figure 28.12 shows the estimated and actual rotor speed in a sensorless vector controlled induction motor drive [44]. The actual speed was monitored by a speed transducer, but this speed signal was not used in the control loops (only the estimated speed was used). The corresponding Fig. 28.13 shows the variation of the estimated stator resistance. At the start of the plot, the motor was under a cooling phase and after that it is heated (by using the 2 kW heater) and then the cooling phase starts again. Figure 28.14 shows the rotor flux speed obtained by the experiments. It can be seen that sustained zero frequency operation has been achieved for a period of more than 15 minutes. This is an important result and opens the way for many sensorless applications where existing commercial sensorless drives cannot be used.

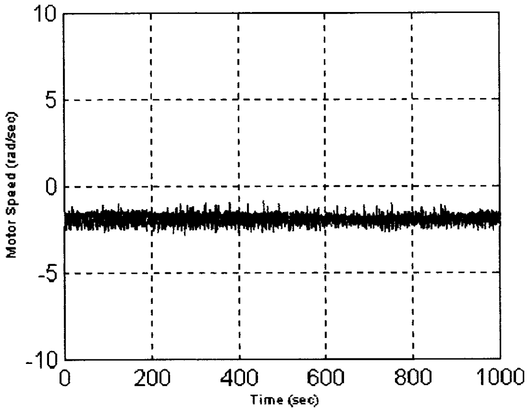


FIGURE 28.12. New sensorless induction motor drive estimated and actual rotor speed.

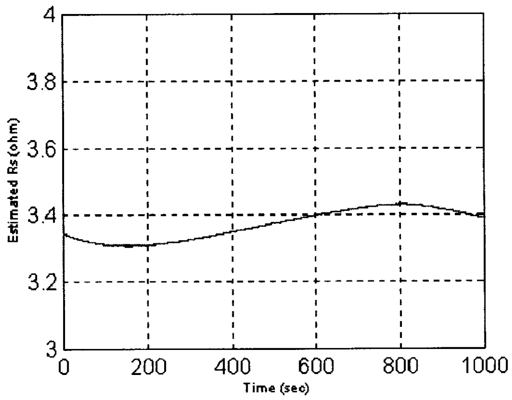


FIGURE 28.13. New sensorless induction motor drive estimated stator resistance.

Experimental results have been also shown for a crane drive using an induction motor and also the new sensorless technology [43, 44]. These results also prove that the new sensorless drive technology can also be used for cranes, elevators, hoists, etc., where so far sensorless drives have not been used (due to stability and other problems).

The new sensorless technology plays a key role in the activities of the recently formed European Sensorless Drives Consortium (ESDC) [43], which involves several multinational and other companies (e.g. Texas Instruments, SKF, Baldor, etc). It is possible to implement the new technology by using low-cost DSPs (e.g. fixed-point DSPs manufactured by Texas Instruments).

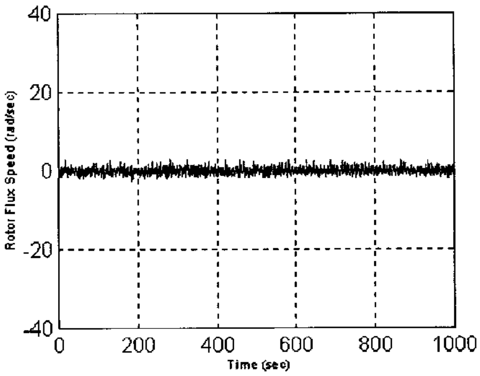


FIGURE 28.14. New sensorless induction motor drive: rotor flux speed.

It is expected that in the future various new types of sensorless solutions will appear in different high-performance drives (the second generation of sensorless drives) and there will be a further significant increase in the number of these drives manufactured. These drives will also provide excellent performance in the low-speed region as well. Speed and position sensorless drives will replace drives with conventional sensors. There will be a large increase in the use of sensorless drives not only in industrial drives, but also in drives used for domestic applications (washing machines, etc.) and also in automotive and military applications.

. . . . ***Artificial-Intelligence-Based Schemes*** In addition to mathematical-model based schemes, it is also possible to use artificial-intelligence-based (AI-based) schemes to obtain the rotor speed and rotor position information. Such types of schemes are discussed in Chapter 21. It is a main advantage of such schemes over mathematical-model based schemes that they do not require any knowledge of machine parameters, and do not require any type of mathematical machine/drive models.

. . . . ***Encoderless Schemes (Quasi-Sensorless Schemes)*** As discussed above, it is also possible to implement speed/position controlled drives without extra conventional speed and/or position sensors by using integrated sensor ball bearings (sensor bearing). Such a drive is a quasi-sensorless drive. For this purpose sensor bearings manufactured by SKF can be effectively used, where Hall-effect sensors are integrated into the bearings [39, 40, 41]. Figure 28.15 shows a SKF sensor bearing.

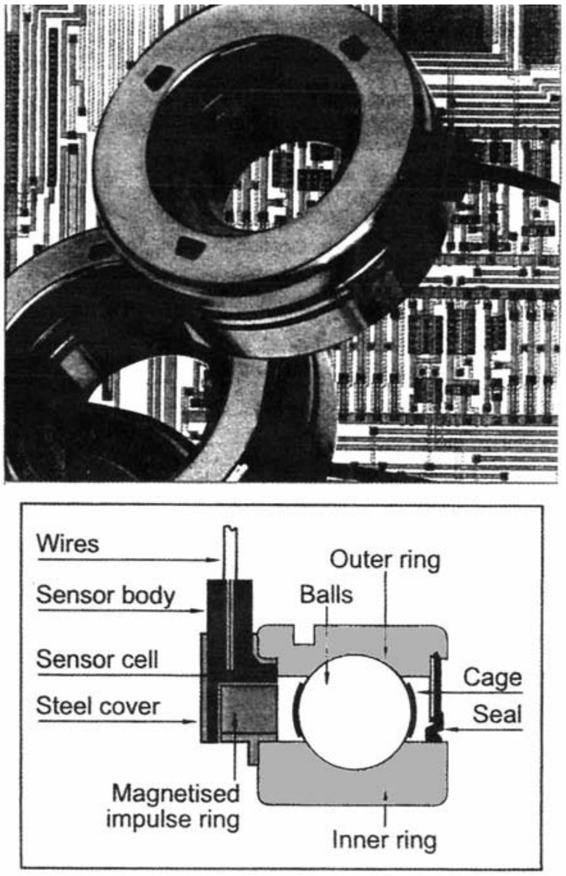


FIGURE 28.15 SKF sensor bearing.

The so-called sensor bearing of SKF incorporates two built-in Hall-effect sensors, which can be used to monitor in realtime both the rotor speed, including speed direction, and the relative angular position of the rotor (one Hall sensor is required to measure the speed only). The sensor bearing based on an existing standard deep-groove ball bearing ISO range includes two additional elements: a single magnetic excitation ring (impulse ring) with N pole pairs fitted in the rotating bearing inner ring and a sensor ring which is attached to the stationary outer ring. The precise magnetized impulse ring develops an alternating magnetic field with N rotating North and South poles, which is sensed by two Hall-effect sensor cells placed inside the sensor ring. For example, in the case of the standard bearing SKF 6206, the number of poles is $N = 64$.

The value $R = 2\pi/N$ (or $360°/N$) is defined as the angular resolution of the sensor. When the inner ring rotates, the moving impulse ring passes the sensors (which are designed to respond to the magnetic field variation produced by each change in the polarity). The integrated circuits of the Hall sensor cells contain Schmitt triggers. The Schmitt trigger provides a threshold function of the sensor and transforms the analog voltage waves generated by the Hall-effect sensor cells into two rectangular, normalized voltage signals A and B with the time period $T = 2\pi/(N\omega)$, where ω is the angular rotation frequency of the inner ring. A sensor then outputs a signal whose frequency is proportional to the number of polarity changes $f = \omega N/(2\pi)$. The mechanical angular displacement of both Hall-effect sensor cells in the outer ring must be very precise to get an exact phase shift of $T/4$ between both output A and B signals. This displacement can be used for two additional features:

- to detect the rotational speed direction (clockwise when the electrical angle phase shift between signals A and B is equal to $\pi/2$)
- to multiply the number of pulses by customer electronic logic interface circuits, so that by the consideration of all pulse edges the resulting sensor resolution increases to $R/4$.

The signals A and B can be very easily obtained on the outputs of SKF sensor bearings, Fig. 28.16 shows the connection diagram.

Basically the SKF sensor bearing measures the angular movements of the impulse ring. There is direct digital output. The sensor output voltage has a rectangular pulse shape and expresses this in the quantity of pulses beginning on the initial angular position θ_0 at reference time t_0 of the

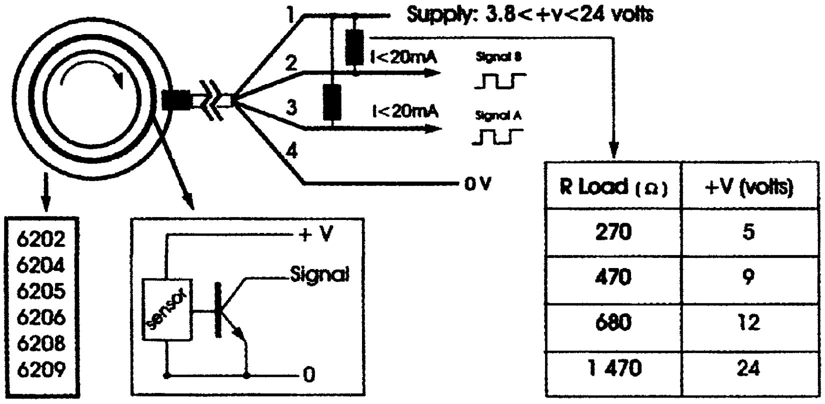


FIGURE 28.16 Connection diagram for SKF sensor bearings.

current position θ_1 at current time t_1. The angular difference $\theta_1 - \theta_0$ can be expressed as $\Delta n(2\pi/N)$, where Δn is the quantity of pulses counted during the time period $\Delta t = t_1 - t_0$, and N represents the sensor resolution. Since the output signals are discrete pulses (digital signals or they are transformed to analog ones), in a drive system it is possible to estimate the following four quantities:

1. real-time estimation of the position $\theta_1 = \theta_0 + \Delta n(2\pi/N)$ if it is assumed that the initial position is known and estimated by additional measures
2. real-time estimation of the angular speed $\omega = d\theta/dt$
3. detection of the speed direction (by using signals A and B)
4. real-time estimation of the acceleration $\varepsilon = d\omega/dt$.

These functions can be performed depending on a customer-specific (motor-specific) interface between the sensor and drive or control systems.

The SKF sensor bearings can replace certain traditional incremental position transducers and can be manufactured at considerably lower cost. Their design is physically robust and withstands the vibrations and higher temperatures in modern drives containing electrical motors with rising power densities and working temperatures. They are also capable of operation in electromagnetically noisy environments.

For illustration purposes, some results are shown in Fig. 28.17 for a DSP-controlled high-performance encoderless induction motor drive employing an SKF sensor bearing. The drive is an encoderless voltage-source inverter-fed DTC induction motor drive using a special torque ripple minimization scheme [40, 41] and employing an SKF sensor bearing (6208). The motor is a 2.2 kW three-phase cage induction motor. It should be noted that the new and simple torque ripple minimization scheme has been implemented since it is known that conventional DTC drives exhibit unwanted torque ripples. This control scheme also contains a mathematical or AI-based model, which utilizes the motor speed, which is obtained by using the SKF sensor bearing. The results are shown for the reversal of the drive. To illustrate the fact that the encoderless drive behaves similarly to the drive with a conventional speed transducer (tachometer), Fig. 28.17 also shows the results obtained when the SKF sensor bearing was not used. As expected, it can be seen that there is very good agreement between the two results.

It can be seen from Fig. 28.17 that the motor can pass through zero speed and the speed obtained by the SKF sensor bearing is almost identical to the speed obtained by the conventional encoder. It is important to note that the induction motor can cross the zero speed safely during reversal. It can be seen that, when the new DTC scheme using the torque ripple minimization technique is used, it is possible to obtain a very attractive total drive solution by using an SKF sensor bearing. To obtain satisfactory low-speed performance, the output signals of the SKF sensor bearing have been processed

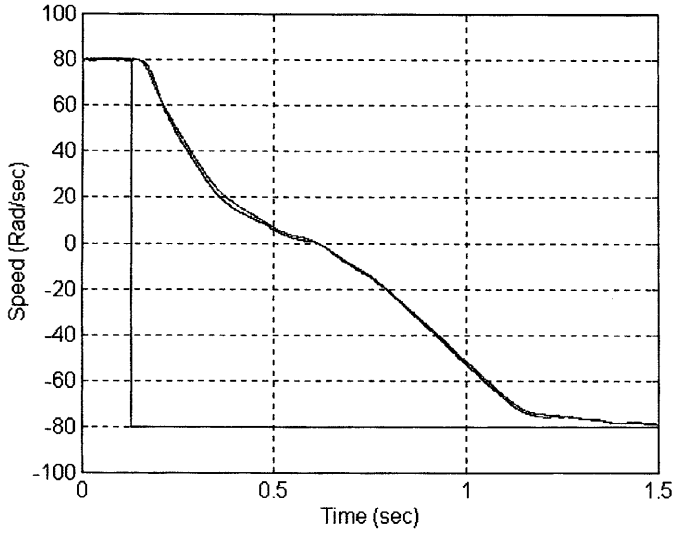


FIGURE 28.17 Experimental results for a DSP controlled high-performance DTC induction motor drive using an SKF sensor bearing: reversal.

(using a simple and cost-effective artificial-intelligence-based technique) which has increased the resolution.

It has been shown that the SKF sensor bearing can provide information on the rotor speed, acceleration and rotor position of electrical motors. However, this information can also be used for condition monitoring and diagnostic purposes. There are a very large number of possible applications of the SKF sensor bearings, e.g. in electric vehicles, servo drives, etc. The SKF sensor bearings offer a simple, cost-effective, user-friendly solution for motion control purposes. In the future, the sensing function of the bearing can be modified and extended to achieve total customer-specific multifunction micro systems built into smart bearings.

28.3 Motion Control DSPS by Texas Instruments

Various vector and DTC drives have been described above. These can be implemented by using DSPs. For most of these drives it is very suitable to use the new family of Texas Instruments DSP controllers, the TMS320C24x family. This includes six different members based on the 320C2Xlp providing 20 MIPS performance. The 320C24x products support power switching device commutation, command generation, control algorithm processing, data communication and system monitoring functions. All the members offer an ideal single chip solution for digital motor control applications. They include program memory flash or ROM, RAM for the data memory, Event Manager (EV) for generating pulse width modulation signals, A/D converters, UART and CAN controllers.

The TMS320F240 is suitable for an application requiring a large amount of memory on chip, it includes 16 Kword of flash, two 10-bit A/D converters, an EV including 3 timers, a serial port interface for an easy connection with other peripherals, an UART, a 16 bit data and address bus for connecting external memory and peripherals.

The TMS320C240 is the ROM based version of the TMS320F240 and is ideal for large volume applications. The EV module is used for operations particularly useful for digital motion control applications. The EV module generates outputs and acquires input signals with a minimum CPU load. Up to 4 input captures and 12 output PWMs are available. The A/D converter module has two 10 bit, 10 ns converters for a total of 16 input channels. Two sample-and-holds allow parallel and simultaneous sampling and conversion. Conversion starts by external signal transition, software instruction or EV event. The reference voltage of the A/D module is 0–5 V: this can be supplied either internally or externally. The device also includes a watchdog timer and a Real Time Interrupt (RTI) module.

The TMS320F241 and TMS320C241 are 8 kword versions (flash and ROM). They include a new 10 bit A/D converter, which can process the conversion of a signal in less than 850 ns. They are also the first DSPs to contain a CAN controller on chip, which make them ideal for automotive and numerous industrial applications, which require fast and secure communication in noisy environments.

The TMS320C242 is a 4 K ROM based device designed for all motor control applications in the consumer area. The 4 K ROM program memory is satisfactory to include a complete sensorless software which, e.g., will control optimally in space vector mode the speed of an induction motor in a washing machine.

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29

Artificial Intelligence-Based Drives

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29.1 General Aspects of the Application of AI-Based Techniques

In the past four decades considerable research has been performed in the field of artificial intelligence (fuzzy logic, neural networks, fuzzy–neural networks, genetic algorithms, etc.), which has resulted in many industrial applications. Recent trends and advances in this field have stimulated the development of various artificial-intelligence-based systems for electrical machine and drive applications. This can also be visualized by the rapidly increasing number of related publications by academics working in the drives field. At present two industrial variable-speed electrical drives incorporate some form of artificial intelligence (AI). However, the only comprehensive treatment of these techniques for electrical machine and drive applications has been presented in a major textbook [20]. This covers the details of AI-based machine design, control, parameter and state estimation (e.g. speed, position, flux, torque, etc., estimation), condition monitoring and diagnosis, simulation (steady state and transient), various firing schemes, etc., for dc drives, induction motor drives, synchronous motor drives (e.g. pm motor drives), switched reluctance motor drives, scalar, vector and DTC drives. In the next few sections, various aspects of AI-based drives are discussed briefly.

Table 29.1 summarizes some of the main advantages offered by the application of artificial intelligence-based systems (controllers, estimators).

In classical control systems, knowledge of the controlled system (plant) is required in the form of a set of algebraic and differential equations, which analytically relate inputs and outputs. However, these mathematical models are often complex, rely on many assumptions, may contain parameters which are difficult to measure or may change significantly during operation, and sometimes such mathematical models cannot be determined. Furthermore, classical control theory suffers from some limitations due to the nature of the controlled system (linearity, time invariance, etc.). These problems can be overcome by using AI-based control techniques, and these techniques can be used even when the analytical models are not known, and they can be less sensitive to parameter variation (more robust) than classical control systems.

To illustrate that AI-based techniques have an enormous market potential, Table 29.2 shows the rapidly expanding market of fuzzy logic applications. It can be seen that, in contrast to 1989, where the world market for fuzzy logic applications was only \$5 million, in 1995 the combined European, Japanese and USA market was \$3.8 billion and it is estimated that by the end of 2000, this will increase to \$18 billion, which is 26 times the value of the estimated world market for classical PID controllers.

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TABLE 29.1 Main advantages of using AI-based controllers and estimators

- Their design does not require a mathematical model of the plant.
- They can lead to improved performance (when properly tuned).
- They can be designed exclusively on the basis of linguistic information available from experts or by using clustering or other techniques.
- They may require less tuning effort than conventional controllers.
- They may be designed on the basis of response data in the absence of the necessary expert knowledge.
- They may be designed using a combination of linguistic and response-based information.
- They can lead to extremely good generalizations (give good estimates when some new unknown input data are used) and thus be independent of particular characteristics of the system (e.g. electrical drive).
- They can be easily made adaptive by the incorporation of new data or information as it becomes available.
- They may provide solutions to control problems which are intractable by conventional methods.
- They exhibit good noise rejection properties.
- They are inexpensive to implement, especially if minimum configuration is used.
- They are easy to extend and to modify.

TABLE 29.2 Market of fuzzy logic applications [20]

1989 USA, Canada	1 million	World	5 million		
1993 USA, Canada	10 million	World	20 million		
1995 USA	800 million	Europe	1 billion	Japan	2 billion
2000 USA	3 billion*	Europe	7 billion*	Japan	8 billion*

* Estimated.

2 .2 AI-Based Techniques

A brief overview is now given on the various AI-based techniques.

2 .2.1 Artificial Neural Networks ANNs

ANNs are universal function approximators and are capable of closely approximating complex mappings, which can be extended to include the modelling of complex, nonlinear systems [20]. In an ANN, there are artificial neurons interconnected via weights. A classical artificial neuron outputs the weighted sum of its inputs and applies a nonlinear activation function (e.g. a sigmoid) on this weighted sum. Thus, if a general, simple static artificial ith neuron has n inputs, and these are $x_1, x_2, \ldots, x_n$, and it outputs a scalar quantity, y_i and the connection weights between the ith neuron and the inputs are $w_{i1}, w_{i2}, \ldots, w_{in}$, then the neuron output is obtained as $y_i = f_i(\sum w_{ij}x_j + b_i)$. In this expression f_i is the activation function of the ith neuron (e.g a sigmoid function), the summation is performed from 1 to n, and b_i is a constant (which is called the bias of the activation function). In an ANN there are various layers, and for example, in a multilayer feedforward ANN, which is the most frequently used ANN, there are several layers (e.g. an input layer, two hidden layers, an output layer), and each layer contains neurons. Such an ANN is shown in Fig. 29.1. In a multilayer feedforward ANN the neurons in a layer are connected to the neurons of the next layer (via the weights).

Unlike some other types of models, an ANN model can be formed directly by using the input/output data of the unknown system, without the need for any prior model structure. It is very important to note that, in contrast to linear theories, a general ANN model is not assumed to be linear. A supervised neural network can learn the non-linear input–output function of a system in the learning phase (training phase) by observing a set of input–output examples (training set). In the application stage, the trained ANN computes the outputs from the corresponding inputs. The learning phase can also be performed online in realtime and it is possible to perform both the learning and applications stages simultaneously (specialized learning). In this case it is possible to adapt the control law to different operating conditions since training is performed online.

One of the most widely used supervised ANNs uses the so-called backpropagation algorithm. In the training phase, the inputs and outputs of the ANN are used to obtain the ANN architecture (e.g. weights, if the number of layers, number of nodes and biases and activation functions are fixed) by back-propagating the error (which is the difference between desired output and actual output). This technique is based on a steepest descent approach to minimize the prediction error with respect to the connection weights in the neural network, i.e. the gradient formula is used for weight adjustement: $w_{ji}(k+1) = w_{ji}(k) + \Delta w_{ji}$, where Δw_{ji} is the change made to the weights, and it is proportional to the negative rate of change of the error with respect to the weights ($\Delta w_{ji} \approx -\partial E/\partial w_{ji}$, where E is the total network error). The training stage is easy to understand: if the multilayer feed-forward neural network (e.g. a four-layer network shown in Fig. 29.1 containing an input layer with three input signals,

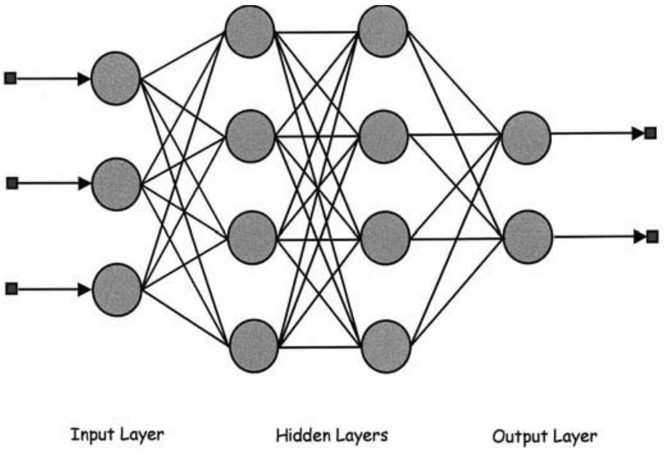

FIGURE 29.1 Multilayer feedforward ANN.

two hidden layers and an output layer with two output signals) gives incorrect outputs, the weights are corrected so that the error is reduced and future network responses will be more accurate. The initial weights are obtained randomly, and these are then changed by using the backpropagation algorithm. Once the training stage is over, the architecture of the ANN is fixed and in the application stage new inputs are applied and the associated outputs are computed. Although the backpropagation algorithm is simple, it is a disadvantage that the convergence time of the learning algorithm can be slow and the learning speed is a crucial factor for training a neural network, especially for a large neural network with large training data sets. Much research has been done to improve the learning speed of the backpropagation algorithm, but some of these increase the complexity of the neural network. It is also possible to enhance the backpropagation learning by using fuzzy concepts. It is another disadvantage of the backpropagation algorithm that the minimization of the error does not guarantee that a global minimum will be obtained, and instead a local minimum can be reached, but the local minima can also be avoided by using genetic algorithm-assisted weight selection.

29.2.2 Fuzzy Logic Systems (FLSs)

Fuzzy logic systems (FLSs) are also universal function approximators. However, a fuzzy logic system is an expert system, where the heart of a fuzzy logic system (FLS) is a linguistic rule-base, which can be interpreted as the rules of a single "overall" expert, or as the rules of "subexperts" and there is a mechanism (inference mechanism) where all the rules are considered in an appropriate manner to generate the output(s) [20]. These rules may directly originate from experts, but if the experts are not available, they can also be obtained by the appropriate processing (e.g. clustering) of available input/output data. Again it is important to note that the system can be nonlinear, and nonlinearity is incorporated into the fuzzy logic system.

A nonlinear function can also be approximated by using a finite set of expert (fuzzy) rules. These rules form a rule-base and an individual rule can be considered as a rule of a subexpert (local expert). The whole set of rules can be considered as the rules of a main-expert (global expert). A fuzzy function approximator with finite number of rules can approximate any continuous function on a compact domain to any degree of accuracy. Each rule defines a bounded region of the input–output space. The fuzzy approximator approximates a function, which covers its curve with rule regions and adds or averages regions that overlap. In general, the number of rules required (to cover the curve to be approximated) grows exponentially with the number of input and output variables. Lone optimal rule regions cover the extrema of the approximand and offer one way to deal with the rule expansion. Learning has the effect of moving and shaping the rule regions. The best learning techniques rapidly find and cover the extrema and bumps in the curve to be approximated and then move rule regions between the extrema as the rule "budget" allows.

A rule-base contains the whole set of fuzzy rules for a specific application, i.e. for a nonlinear function approximation. The fuzzy rules have an if–then structure and involve linguistic values for the input and output variables. In general, a fuzzy rule can take the following form:

$$\text{If } x_1 \text{ is A} \quad \text{and} \quad x_2 \text{ is B} \quad \text{then} \quad y \text{ is C.}$$

In the rules A, B and C represent fuzzy sets, e.g. A can correspond to the "small" fuzzy set of x_1, B can correspond to the "medium" fuzzy set of x_2 and C can correspond to the "large" fuzzy set of y. For example, in a fuzzy logic speed controller with two inputs, input x_1 input is the error, input x_2 is the change of the error, and A corresponds to the fuzzy set of errors which belongs to the small errors, B corresponds to the fuzzy set of change of errors which belongs to the medium change of errors, etc.

Figure 29.2 shows the schematic of a Mamdani-type fuzzy-logic-based system (function approximator) [20]. Since the rule-base contains linguistic rules, and since the input data are crisp data, they have to be transformed into linguistic values (by using fuzzification and for this purpose membership functions are used). This is why in general, the fuzzy logic approximator contains the "Transformation 1" block, which performs fuzzification. Similarly, on the output of the fuzzy approximator a crisp output value must be present, and this is obtained by transforming the linguistic outputs into crisp output via the "Transformation 2" block (defuzzifier). There are many types of defuzzifiers, e.g. centre of gravity defuzzifier, centroid defuzzifier, etc. In the second block, the inference operation (decision making) is performed, i.e. by using the rule-base and knowledge base (which contains knowledge of the system), the inference operation calculates the corresponding fuzzy (linguistic) output(s) from the input(s) (there are many types of inference engines, e.g. the one using the max–min method, the max–dot product, etc. [20]). In a realtime

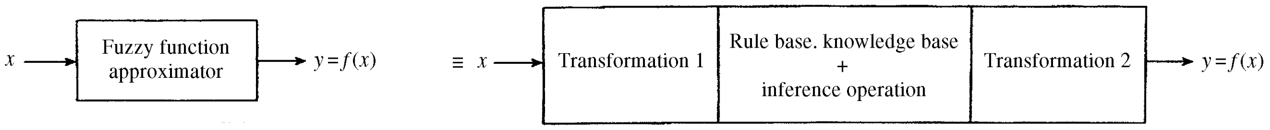
x
Fuzzy function approximator
y = f(x)
≡ x
Transformation 1
Rule base. knowledge base + inference operation
Transformation 2
y = f(x)

FIGURE 29.2 Mamdani-type fuzzy-logic-based system (function approximator).

implementation of a fuzzy logic system it is a very important goal to approximate a given function accurately by a minimum number of rules (since this leads to less computation time and allows the use of a cheaper DSP).

There are various types of fuzzy logic systems, but the three main types are the Mamdani, the Sugeno and the Tsukamoto fuzzy logic systems [20]. The Sugeno type has been extensively used in Japan, and in contrast to the Mamdani-type FLS, it does not contain a defuzzifier.

2 .2.3 Fuzzy Neural, Neural Fuzzy Systems

It is possible to combine neural networks with fuzzy logic systems, and the arising integrated system can be a fuzzy–neural or neural–fuzzy system [20], which is also a nonlinear system. In contrast to a "purely" neural multilayer system (multilayer ANN-based system), where the number of hidden layers and number of hidden nodes (in a hidden layer) are not known *a priori* (but only after intensive calculations), it is an advantage of the fuzzy–neural and neural–fuzzy systems that they already incorporate some form of expertise and the architecture of the systems is well-defined *a priori.* Thus the number of hidden layers is exactly known and also the number of hidden nodes is also known.

Since both fuzzy and neural systems are universal function approximators, their combination, the hybrid fuzzy–neural system (or neural–fuzzy system) is also a universal function approximator.

The major drawback of conventional neural networks is that, although they can be used to approximate any nonlinear mapping, in general they can be viewed as black boxes, without providing general explanations. Thus although the inherent black box approach provides the correct solutions, it does not provide heuristic interpretation of the solution. However, engineers prefer accurate function approximation as well as the heuristic knowledge behind this process. Fuzzy logic can be conveniently used to provide heuristic reasoning: the behavior of a fuzzy logic system can be easily understood, due to its logical structure and simple inference mechanism. Furthermore, in an artificial neural network, the required number of hidden layers and the number of hidden nodes is not known *a priori.* In contrast to this, in the hybrid system (fuzzy–neural system), the architecture (structure) of the system is known and is decided by fuzzy principles. In a fuzzy–neural network there is no need for *a priori* information of the membership functions (their number and also their shapes), and for *a priori* information on the rule-base these can be obtained by the appropriate tuning of the fuzzy–neural network. The state-of-the-art intelligent control is at the level of adaptive fuzzy–neural controllers.

There are various types of fuzzy–neural systems, but the four main types of fuzzy–neural systems are: the Mamdani type, the Sugeno type, the Tsukamoto type and the Wang type [20].

Similar to conventional ANNs, the training of a fuzzy–neural network can be performed by using the backpropagation algorithm. However, some difficulties may occur in the direct implementation of this, when the activation functions are nondifferentiable, but this problem can also be solved by modifying the original backpropagation algorithm.

2 .2.4 Genetic Algorithms GAs

Genetic algorithms (GAs) [20], are not function approximation techniques, but they are simple and powerful general-purpose stochastic optimization methods (learning mechanisms), which have been inspired by the Darwinian evolution of a population subject to reproduction, crossover and mutations in a selective environment where the fittest survive. GA combines the artificial survival of the fittest with genetic operators abstracted from nature to form a very robust mechanism that is suitable for a variety of optimization problems.

In mathematical terms the goal of the genetic algorithm is to minimize an objective functions $F(S_k)$, where S_k is the search candidate (optimal solution), which is the kth individual in the population S (where the population is the set of possible solutions). The individuals of the population are expressed in a binary string form (the initial binary strings corresponding to the initially assumed individuals are, e.g., obtained by a random process) and the GA then manipulates these strings by using genetic operators (reproduction, crossover, mutation) to obtain improved solutions (where the fittest individuals survive) until the optimal solution is obtained.

It is one of the main advantages of a GA that it uses stochastic operators instead of deterministic rules to search for a solution. Furthermore, a GA considers many points in the search space simultaneously, not a single point; thus it has a reduced chance of converging to local minima, in which other algorithms might end up. Thus the global optimum of the problem can be approached with higher probability. It follows that, in addition to producing a more global search, it is another attractive feature of GA that it searches for many optimum points in parallel (simultaneous consideration of many points), since the evaluation of each point requires an independent computation. The data processed by the algorithm is a set (population) of binary strings (chromosomes), which represent multiple points in the search space. Due their robustness, speed, efficiency and flexibility GAs have so far been used in various engineering and business problems.

The input data processed by the genetic algorithm is used to create an initial population (set of possible solutions) either randomly or heuristically. The individuals in this population carry chromosomes, which are the variables. During each iteration step of the algorithm, which is called a generation, structures in the current population are evaluated and new generations are formed. The structures of the population are chosen by a randomized selection process, which ensures that the expected number of times a structure is chosen is approximately equal to that structure's performance (fitness) relative to the rest of the population. The less fit individuals in the population die and, in order to search other points in the space, some variations are introduced into the new population by using idealised genetic recombination (transitional) operators (e.g. crossover, mutation, etc.). Thus the fittest individuals (solutions) are bred, i.e. two individuals are mated (crossover) and the offspring of the mated pair receives some characteristics of the parents. Fit individuals carry on mating, and some of them mutate; thus the population undergoes various generation changes. After many generations, a population (solution) emerges, where the individuals will solve the problem well.

It can be seen that, in the genetic algorithm, it is necessary to use a fitness function and its selection is crucial. It must reflect the controller's ability to reach the setpoint from a number of initial condition cases. It is very important to note that GAs consider many points in the search space, and thus have a reduced chance of converging to local minima. Furthermore, the simultaneous consideration of many points makes them adaptable to parallel processors since the evaluation of each point requires an independent computation.

There are various possibilities for the application of GAs:

- In GA-assisted multilayer artificial neural networks, GAs can be used to optimize the size of a hidden layer and also the weights (strength of connections connecting the artificial neurons of the ANN). This is justified by the following two factors:
  - it allows one to avoid local optima and provides near-global optimization solutions
  - it is easy to implement.

  However, it must also be considered that too many hidden neurons (neurons in the hidden layer) decrease the generalization capability of the network and also imply a long learning phase. On the other hand, a network with too few neurons can be unable to learn the given function with the desired precision. Thus there is an intermediate number of hidden neurons required to avoid the problems mentioned above.
- GAs can also be used to obtain the membership functions and the rule-base in a fuzzy-logic controller.
- In GA-based controllers, genetic algorithms are used to learn the controller structure from scratch and also to tune the controller parameters.
- GAs can be used to estimate coefficients (parameters) contained in nonlinear algebraic equations.

For example, it is also possible to obtain the electrical parameters of an electrical machine by using GA-based parameter estimation. For this purpose, the initial parameter values are generated randomly, and these form the initial individuals of the population. The GA is then used to obtain the individuals of the final population (final values of the machine parameters) [20].

Finally it should be noted that it is possible to implement AI-based self-repairing, self-contructing controllers and estimators, e.g. in variable-speed, high-performance, sensorless drives by using GA. For this purpose an FPGA (Field Programmable Gate Array) can be used [20].

29.3 AI Applications in Electrical Machines and Drives

In the literature most publications on the application of artificial intelligence (AI) in electrical drives discuss fuzzy-logic-based, or seldom neural-network-based, speed or position controller applications, where an existing PI or PID controller is simply replaced by an AI-based controller. Although this is an important application, and the AI-based controllers can lead to improved performance, enhanced tuning and adaptive capabilities, there are further possibilities for a much wider range of AI-based applications in variable-speed ac and dc drives. Some of these are also shown in Table 29.3 [20].

All of these applications are discussed in detail in [20].

TABLE 29.3 Applications of AI in variable-speed drives (ac and dc drives) including the modelling of drives and machine design

- Replacement of classical speed, position and other controllers by AI-based controllers. New and combined control structures in various drives including high-performance ac drives: vector and direct torque control (DTC) drives, energy efficient drives, new AI-based universal drives, new AI-based "electronic motors".
- AI-based new firing signal generation schemes, (e.g. PWM schemes), new switching vector schemes (e.g. in DTC drives).
- AI-based compensation of non-linear effects in discontinuous operation.
- AI-based parameter estimators, self-commissioning systems.
- AI-based speed and position estimators, flux and torque estimators, virtual sensors (e.g. virtual vibration sensor).
- AI-based condition monitoring, diagnosis.
- AI-based improved observers (e.g. improved Kalman filter, improved extended Kalman filter).
- AI-based harmonic estimators (e.g. harmonic identifiers utilizing space vector loci).
- AI-based efficiency optimizers.
- AI-based machine design.
- AI-based steady-state and transient models (to replace conventional mathematical models).
- AI-based self-repairing and self-constructing controllers, schemes.

29.4 Industrial Applications of AI in Drives by Hitachi, Yaskawa, Texas Instruments and SGS Thomson

As mentioned earlier, at present there are two large electrical drive manufacturers, who incorporate artificial intelligence into their drives, Hitachi and Yaskawa. In addition to these it should be noted that Texas Instruments (TI) has developed a fuzzy-controlled induction motor drive using the TMS320C30 DSP. The main conclusion obtained by TI agrees with that of the present author obtained from various fuzzy control implementations: the development time of the fuzzy-controlled drive is significantly less than the corresponding development time of a drive using classical controllers. SGS Thomson has also developed various fuzzy–neural controlled drives.

29.4.1 Hitachi Drive

According to Hitachi, the J300 series IGBT inverter based sensorless vector drive is the "first industrial drive which incorporates fuzzy logic" [20]. According to Hitachi "the intelligent inverter takes into account the characteristics of both the motor and the system and the torque computation software ensures accurate torque control throughout the entire frequency range, even with general purpose motors". Some of the main characteristics are shown in Table 29.4.

Fuzzy logic control is used in the Hitachi drive for the calculation of optimum acceleration and deceleration times, and according to Hitachi there is "fuzzy logic control of both the motor current and ramp rate during drive acceleration and deceleration". The calculations are based on motor load and braking requirements (thus eliminating the need for adjustments using trial and error). The fuzzy logic acceleration/deceleration function sets acceleration and deceleration factors and speed according to fuzzy rules which use the distance up to the overload limit (or other limits), and also the start-up gradient of motor current and voltage. According to Hitachi, the main advantages of using fuzzy logic control are: "when conventional, simple current limit control is used, the inverter ramps are stepped and the drive can often trip out, specially during deceleration. However, when fuzzy logic control is used, the ramps are very smooth and nuisance tripping is eliminated". Possible applications of the drive include fan or pump applications where constant acceleration or deceleration times or accurate position control are not required, but optimization of the speed ramp dependent on the load conditions is required. By using fuzzy control, the most efficient ramp time can be guaranteed, whilst also ensuring trip free running.

TABLE 29.4 Main characteristics of Hitachi J300 series induction motor drive [20]

High starting torque of 150 or more at 1 Hz
100 continuous operating torque within a 3 : 1 speed range (20–60 Hz/16–50 Hz) without motor derating
Speed regulation ratio as small as ±1
High-speed microcomputer and built-in DSP
The improved response speed characteristic is effective in preventing "slip-down" in lifting equipment applications
Torque response speed of approximately 0.1 s can be achieved
Fuzzy logic control

29.4.2 Yaskawa Drive

Fenner Power Transmission UK has teamed up with Yaskawa, to market the Yaskawa intelligent induction motor drive range. Top of the range is the VS-616G5 so-called "True Flux Vector Inverter". The VS-616G5 is a general purpose inverter which also contains flux vector control that directly controls the currents (or torque) in an induction motor. According to Yaskawa it contains "a magnetic flux observer with intelligent neuro control", which ensures direct torque control and "this enables the VS-G16G5 to surpass the performance of comparable dc motor controllers and provides a less expensive alternative" [20].

29.5 Application of Neural-Network-Based Speed Estimators

In Chapter 20 various speed and position sensorless ac motor drive schemes are discussed. However, in addition to using mathematical-model-based estimators, it is also possible to use, e.g., ANN-based speed estimators in ac and dc drives. Such drives have been successfully implemented by the author [20]. Some aspects of an ANN-based speed sensorless medium-performance induction motor drive are now discussed. Medium performance induction motor drives represent a large and important share of the induction motor drives market. Reliable, stable, and simple scalar induction motor drives are continuously under development by various manufacturers. Scalar drives are widely used in various industrial fields. The drive to be considered here is a speed-sensorless scalar controlled induction motor drive, which contains a minimum configuration ANN-based speed estimator. For this purpose only two stator currents are monitored. The schematic of the drive scheme is shown in Fig. 29.3.

In Fig. 29.3 the speed controller is a classical PI controller, but AI-based controllers can also be used. The speed controller generates the reference angular slip frequency (ω_{slref}). The drive scheme contains a frequency-to-voltage conversion block, a block where the reference stator voltages are generated, a transformation block, a PWM inverter which supplies the motor and a speed estimator ANN. The inputs to the PWM modulator are the stator reference voltages. The full control system (which also includes the speed estimator ANN), has been implemented by using the Texas Instruments

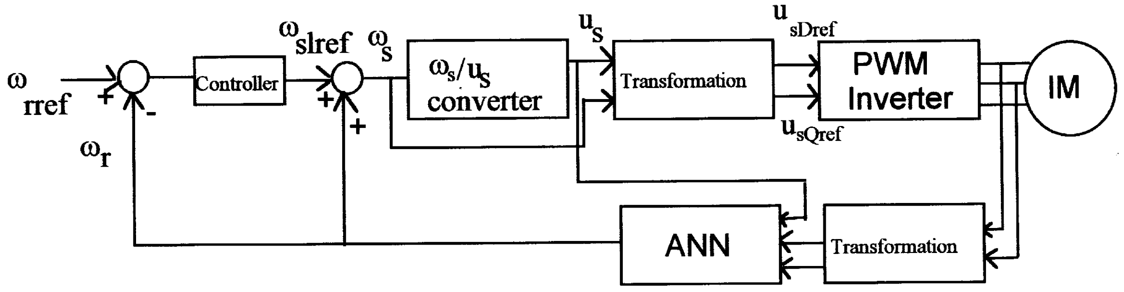

FIGURE 29.3 Sensorless scalar induction motor drive scheme using an ANN-based speed estimator.

TMS320C30 DSP. Although for simplicity they are not shown, there are two further inputs to the frequency/voltage converter block: these take account of the stator ohmic voltage drops.

The ANN shown in Fig. 29.3 is a multilayer feedforward backpropagation ANN. It utilizes three input signals: these are the modulus of the stator voltage space vector and two transformed stator currents. The transformed stator currents are obtained by the application of the appropriate transformation from the monitored direct and quadrature axis stator currents in the stationary reference frame, (i_{sD}, i_{sQ}). Various possibilities have been investigated to obtain the most optimal transformation. The feedforward multilayer ANN has three layers: an input layer, a single hidden layer and an output layer. The number of hidden neurons in the hidden layer was obtained by trial and error. Sigmoid activation functions were used in the hidden nodes. The output node is a linear node, and outputs the angular rotor speed.

It is very important to note that rapid implementation was obtained and the training of the ANN was achieved by using training data obtained by simulation of the complete drive system. The training was performed by using the backpropagation algorithm discussed above. When the trained ANN was implemented, the very first implementation of the sensorless induction motor drive (using the ANN-based speed estimator) worked. The training took only a few minutes on a PC and for this purpose 11,000 input–output training data sets were used. Figure 29.4 shows some of the training signals used: the top curve shows the speed training signal and the bottom curve shows the two transformed stator currents.

Although the training of the ANN was performed with data for the unloaded 3 kW induction motor, the speed-sensorless drive also worked well when the motor was lightly loaded. However, for operation with high loads, the neural network had to be retrained. The simple minimum configuration speed estimator ANN enabled a very fast implementation.

In Fig. 29.5 there is shown the experimentally obtained speed response to random speed reference changes for the lightly loaded 3 kW motor.

To illustrate the accuracy of the results, in Fig. 29.5 the measured speed is also shown, but it is important to note that this has not been used in the drive scheme. It can be seen that there is very good agreement between the measured and estimated speeds. It is important to note that the same trained ANN as used for the 3 kW motor was successfully used in the scalar drive employing a 2.2 kW induction motor. Some experimental results for the drive incorporating this motor are also presented in Fig. 29.6, where the motor reverses from 60 rad/s to −60 rad/s. However, in Fig. 29.6, results are also shown when a recursive ANN is used. The inputs to the recursive ANN are the same signals as for the feedforward multilayer ANN, but there is an extra input signal, which is the past sampled value of the rotor speed.

There are three curves shown in Fig. 29.6. The top (black) curve shows the measured value of the rotor speed, the curve in the middle (blue curve) corresponds to the estimated speed when the recursive ANN is used and the bottom (red) curve corresponds to the speed estimated by the feedforward multilayer ANN. It can be seen that the drive with the recursive ANN-based speed estimator gives better results than the one with the multilayer feedforward ANN.

Various other types of ANN-based speed estimators have also been discussed for induction motors and synchronous motors in [20], including Model Reference Adaptive System (MRAS)-based estimators as well, where the MRAS system (see also Chapter 20) contains an ANN. Work is under progress on various types of sensorless high-performance induction motor and permanent magnet synchronous motor drives, which can also be used at very low (including zero) stator frequencies and under high load conditions. For this purpose AI-based and also other schemes are being developed which do not require extra hardware or modifications to the motor. These include both vector- and direct-torque-controlled drives.

It is believed that, in the future, some of the problems associated with reluctance motor control, e.g. switched reluctance motors (pulsating torque, noise, etc.) can be eliminated by using AI-based controllers. The switched reluctance machine is a highly nonlinear doubly salient machine and its mathematical model is complicated. However, these properties make this type of machine ideal to be subjected to AI-based control. It is expected that various types of torque-controlled AI-based switched reluctance motor drives will also emerge.

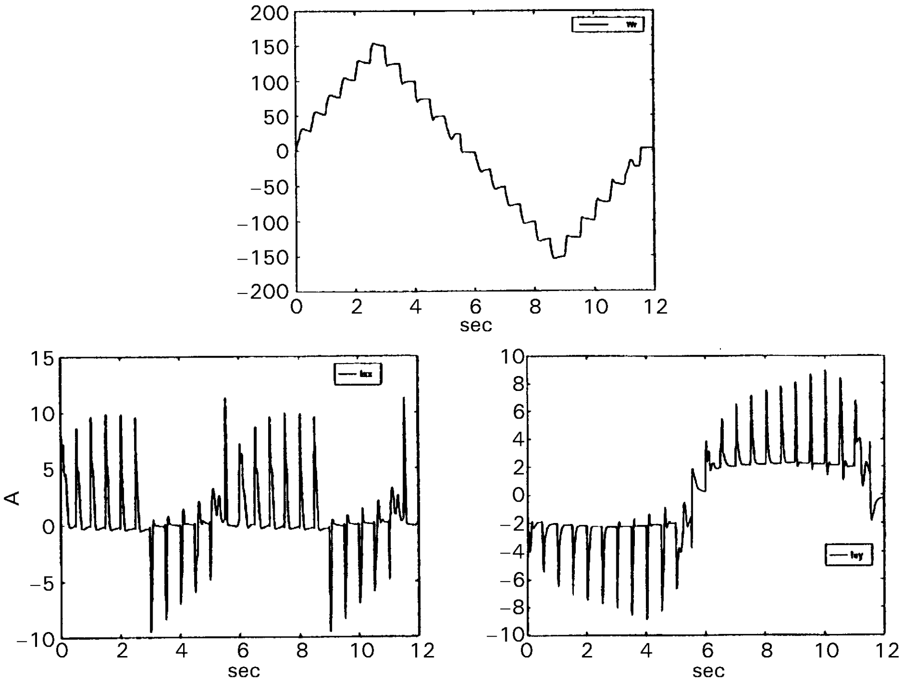

FIGURE 29.4 Training signals for multilayer feedforward ANN-based speed estimator.

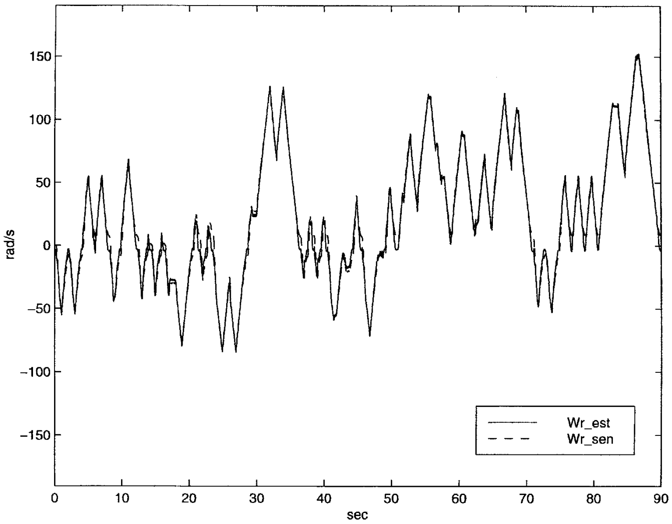

FIGURE 29.5 Experimental results for a sensorless induction motor drive scheme (using a multilayer feedforward ANN-based speed estimator) for random speed reference changes (3 kW induction motor).

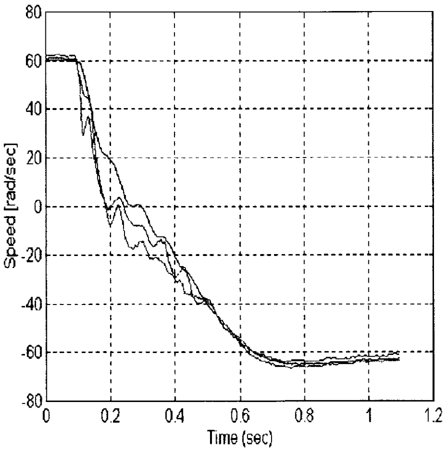

FIGURE 29.6 Experimental results for a sensorless induction motor drive with multilayer feedforward ANN and also with recursive ANN-based speed estimator (2.2 kW induction motor).

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30

Fuzzy Logic In Electric Drives

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30.1 Introduction

Over the years, we have increasingly been on the search to understand the human ability to reason and make decisions, often in the face of only partial knowledge. The ability to generalize from limited experience into areas as yet unencountered is one of the fascinating abilities of the human mind. Traditionally, our attempt to understand the world and its functions has been limited to finding mathematical models or equations for the systems under study. This approach has proven extremely useful, particularly in an age when very fast computers are available to most of us with only a minimum amount of capital outlay. And even when these computers are not fast enough, many researchers can gain access to supercomputers capable of giving numerical solutions to multiorder differential equations that are capable of describing most of the industrial processes.

This analytical enlightenment, however, has come at the cost of realizing just how complex the world is. At this point, we have come to realize that, no matter how simple the system is, we can never hope to model it completely. So instead, we select suitable approximations that give us answers that we think are sufficiently precise. Because our models are incomplete, we are faced with one of the following choices:

1. Use the approximate model and introduce probabilistic representations to allow for the possible errors.
2. Seek to develop an increasingly complex model in the hope that we can find one that completely describes the systems while being solvable in real time.

This dilemma has led a few, most notably Zadeh [14], to look at the decision-making process employed by our brilliant minds when confronted with incomplete information. The approach taken in those cases makes allowances for the imprecision caused by incomplete knowledge and actually embracing the imprecision in forming an analytical framework. This approach involved artificial intelligence using approximate reasoning, or fuzzy logic as it is now commonly known. As a result, artificial intelligence using fuzzy logic has proven extremely useful in ascribing a logic mechanism to a wide range of topics from economic modeling and prediction to biology analysis to control engineering. In this chapter, an examination of the principles involved in artificial intelligence using fuzzy logic and its application to electric drives is discussed.

30.2 The Fuzzy Logic Concept

Fuzzy logic arose from a desire to incorporate logical reasoning and the intuitive decision making of an expert operator into an automated system [14]. The aim is to make decisions based on a number of learned or predefined rules, rather than numerical calculations. Fuzzy logic incorporates a rule-base structure in attempting to make decisions [2,3,4,5,14]. However, before the rule-base can be used, the input data should be represented in such a way as to retain meaning, while still allowing for manipulation. Fuzzy logic is an aggregation of rules, based on the input state variables condition with a corresponding desired output. A mechanism must exist

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to decide on which output, or combination of different outputs, will be used since each rule could conceivably result in a different output action.

Fuzzy logic can be viewed as an alternative form of input/output mapping. Consider the input premise, x, and a particular qualification of the input x represented by A_i. Additionally, the corresponding output, y, can be qualified by expression C_i. Thus, a fuzzy logic representation of the relationship between the input x and the output y could be described by the following:

$$\begin{array}{llll} R_1: & \text{IF} & x \text{ is } A_1 & \text{THEN } y \text{ is } C_1 \\ & \ldots & \ldots\ldots & \quad\ldots \\ R_2: & \text{IF} & x \text{ is } A_2 & \text{THEN } y \text{ is } C_2 \\ & \ldots & \ldots\ldots & \quad\ldots \\ R_n: & \text{IF} & x \text{ is } A_n & \text{THEN } y \text{ is } C_n \end{array} \tag{30.1}$$

where x is the input (state variable), y is the output of the system, A_i are the different fuzzy variables used to classify the input x and C_i are the different fuzzy variables used to classify the output y.

The fuzzy rule representation is linguistically based [3,14]. Thus, the input x is a linguistic variable that corresponds to the state variable under consideration. Furthermore, the elements A_i are fuzzy variables that describe the input x. Correspondingly, the elements C_i are the fuzzy variables used to describe the output y. In fuzzy logic control, the term "linguistic variable" refers to whatever state variables the system designer is interested in [14]. Linguistic variables that are often used in control applications include Speed, Speed Error, Position, and Derivative of Position Error. The fuzzy variable is perhaps better described as a fuzzy linguistic qualifier. Thus the fuzzy qualifier performs classification (qualification) of the linguistic variables. The fuzzy variables frequently employed include Negative Large, Positive Small and Zero. Several papers in the literature use the term "fuzzy set" instead of "fuzzy variable", however; the concept remains the same. Table 30.1 illustrates the difference between fuzzy variables and linguistic variables.

Once the linguistic and fuzzy variables have been specified, the complete inference system can be defined. The fuzzy linguistic universe, U, is defined as the collection of all the fuzzy variables used to describe the linguistic variables [6,7,8], i.e. the set U for a particular system could be comprised of Negative Small (NS), Zero (ZE) and Positive Small (PS). Thus, in this case the set U is equal to the set of [NS, ZE, PS]. For the system described by Eq. (30.1), the linguistic universe for the input x would be the set $U_x = [A_1 A_2 \ldots A_n]$. Similarly, the linguistic universe for the output y would be the set $U_y = [C_a C_2 \ldots C_n$.

TABLE 30.1 Fuzzy and linguistic variables

Linguistic Variables		Fuzzy Variables (Linguistic Qualifiers)	
Speed error	(SE)	Negative large	(NL)
Position error	(PE)	Zero	(ZE)
Acceleration	(AC)	Positive medium	(PM)
Derivative of position error	(DPE)	Positive very small	(PVS)
Speed	(SP)	Negative medium small	(NMS)

30.2.1 The Fuzzy Inference System (FIS)

The basic fuzzy inference system (FIS) can be classified as:

Type 1 Fuzzy Input Fuzzy Output (FIFO)
Type 2 Fuzzy Input Crisp Output (FICO)

Type 2 differs from the first in that the crisp output values are predefined and, thus, built into the inference engine of the FIS. In contrast, type 1 produces linguistic outputs. Type 1 is more general than type 2 as it allows redefinition of the response without having to redesign the entire inference engine. One drawback is the additional step required, converting the fuzzy output of the FIS to a crisp output.

Developing a FIS and applying it to a control problem involves several steps:

1. fuzzification
2. fuzzy rule evaluation (fuzzy inference engine)
3. defuzzification.

The total fuzzy inference system is a mechanism that relates the inputs to a specific output or set of outputs. First, the inputs are categorized linguistically (fuzzification), then the linguistic inputs are related to outputs (fuzzy inference) and, finally, all the different outputs are combined to produce a single output (defuzzification). Figure 30.1 shows a block diagram of the fuzzy inference system.

30.2.2 Fuzzification

Fuzzification is the conversion of crisp numerical values into fuzzy linguistic quantifiers [7,8]. Fuzzification is performed using membership functions. Each membership function evaluates how well the linguistic variable may be described by a particular fuzzy qualifier. In other words, the membership

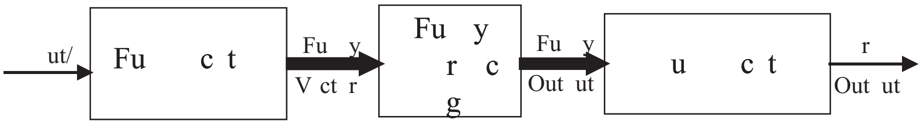

FIGURE 30.1 Fuzzy inference system.

function derives a number that is representative of the suitability of the linguistic variable to be classified by the fuzzy variable (set). This suitability is often described as the degree of membership. In order to maintain a relationship to traditional binary logic, the membership values must range from 0 to 1 inclusive. Figure 30.2 shows the mechanism involved in the fuzzification of crisp inputs when multiple input are involved. Since each input has a number of membership functions (one for each fuzzy variable), the outputs of all the membership functions for a particular crisp numerical input are combined to form a fuzzy vector.

Any number of normalizing expressions can perform fuzzification. Two of the more common functions are the linear and Gaussian [4]. In both cases there is one parameter, μ, that indicates the midpoint of the region and another, σ, that defines the width of the membership functions. For the linear function, the width is specified by σ_L and the midpoint by μ_L. Similarly for the Gaussian function, the width is specified by σ_G and the midpoint by μ_G. Equations (30.2(a)) and (30.2(b)) define the linear and Gaussian membership functions, respectively:

$$\text{Linear function:}\begin{cases} 1-\left|\dfrac{x-\mu_L}{\sigma_L}\right| & \text{if } x\in[(\mu_L-\sigma_L),\ (\mu_L+\sigma_L)] \\ 0 & \text{Otherwise} \end{cases} \tag{30.2(a)}$$

$$\text{Gaussian function:}\ \exp\left(-\frac{(x-\mu_G)^2}{2(\sigma_G)^2}\right) \tag{30.2(b)}$$

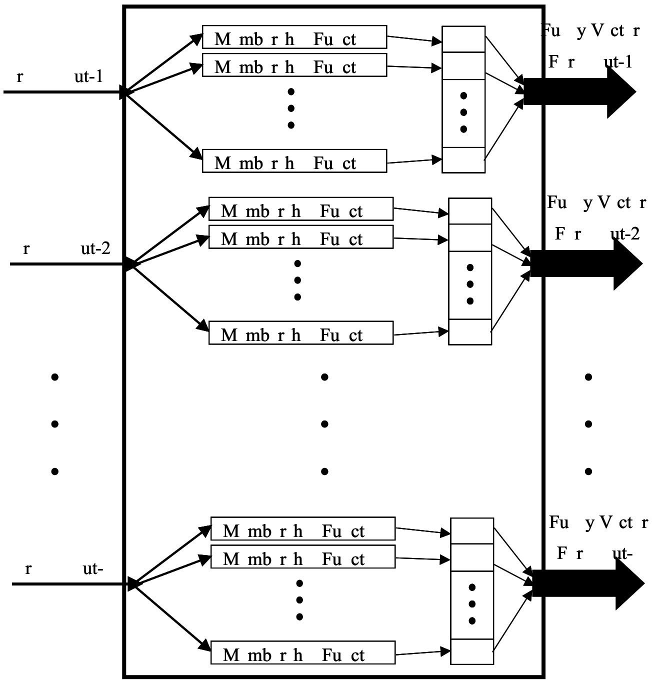

FIGURE 30.2 Fuzzification of the crisp numerical inputs.

where

$$\mu_L = \mu_G \tag{30.3(a)}$$

$$\sigma_L = 3\sigma_G. \tag{30.3(b)}$$

The relations expressed by Eqs. (30.3(a)) and (30.3(b)) are made because of the characteristics of the Gaussian function. Because a Gaussian membership function may never have a membership value of 0, some appropriate value close to zero must be chosen as the cutoff point. At a distance of $3\sigma_G$ from the mean, the Gaussian membership function results in a membership value of 0.05. Thus the width of the Gaussian function is chosen as $3\sigma_G$.

As previously mentioned, fuzzification of the input has resulted in a fuzzy vector where each component of this vector represents the degree of membership of the linguistic variables into a specific fuzzy variable's category. The number of components of the fuzzy vector is equal to the number of fuzzy variables used to categorize specific linguistic variables. For illustrative purposes, we consider an example with a linguistic variable x and three fuzzy variables positive (PV) zero (ZE) and negative (NV). If we describe the membership function (fuzzifier) as X, then we will have 3 membership functions: X_{PV}, X_{ZE} and X_{NV}. The fuzzy linguistic universe for the input x can be described by the set U_x that is defined in Eq. (30.4):

$$U_x = [X_{NV} X_{ZE} X_{PV}] \tag{30.4}$$

where

X_{PV} is the membership function for the Positive fuzzy variables

X_{ZE} is the membership function for the Zero fuzzy variables

X_{NV} is the membership function for the Negative fuzzy variables.

Thus, the fuzzy vector, which is the output of the fuzzification step of the inference system, can be denoted by _:

$$\_ = [x_{NV} x_{ZE} x_{PV}] = [X_{NV}(x) Z_{ZE}(x) Z_{PV}(x)] \tag{30.5}$$

where

X_{NV} = the membership value of x into the fuzzy region denoted by Negative

X_{ZE} = the membership value of x into the fuzzy region denoted by Zero

X_{PV} = the membership value of x into the fuzzy region denoted by Positive.

Equation (30.2(a)) represents the linear membership functions, which are illustrated in Fig. 30.3. The linear function can be modified to form the linear-trapezoidal function. Under this modification, if the input x falls between zero and the mean, μ_L, of the respective region, then Eq. (30.2(a)) is used;

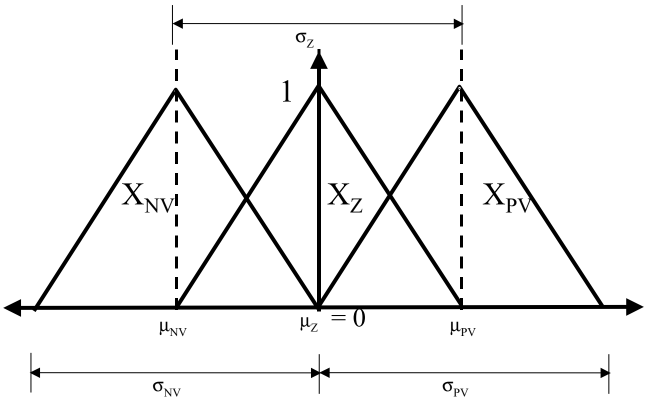

FIGURE 30.3 Linear membership functions.

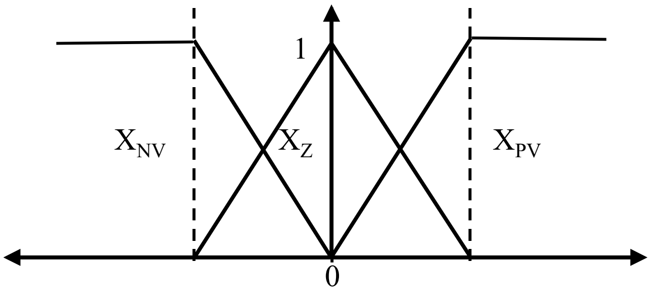

FIGURE 30.4 Linear-trapezoidal membership functions.

otherwise, the membership value is equal to 1. Thus, we arrive at the membership functions shown in Fig. 30.4. Each region of the linear and trapezoidal-linear membership functions is distinguished from another by the different values of σ_L and μ_L. One important criterion that should be taken into consideration is that the union of the domain of all membership functions for a given input must cover the entire range of the input [10]. Thus the trapezoidal modification is often employed to ensure coverage of the entire input space.

The Gaussian membership function is characterized by Eq. (30.2(b)). The Gaussian function can also be modified to form the trapezoidal-Gaussian function. In this case, if the input falls between the mean μ_G and zero, Eq. (30.2(b)) is used to find the membership value. Otherwise the membership value becomes 1. The Gaussian function is shown in Fig. 30.5 and the modified version is shown in Fig. 30.6.

A third type of membership function, known as the fuzzy singleton, is also considered. The fuzzy singleton is a special function in which the membership value is 1 for only one particular value of the linguistic input variable and zero otherwise [4]. Thus, the fuzzy singleton is a special case of the membership function with a width, σ, of zero. Therefore, the only parameter that needs to be defined is the mean, μ_s, of the singleton. Thus, if the input is equal to μ_s, then the membership value is 1. Otherwise it is zero. We can denote the singleton membership function as $S(\mu_s)$.

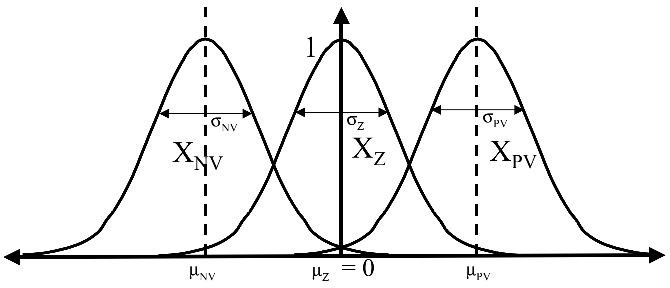

FIGURE 30.5 Gaussian membership functions.

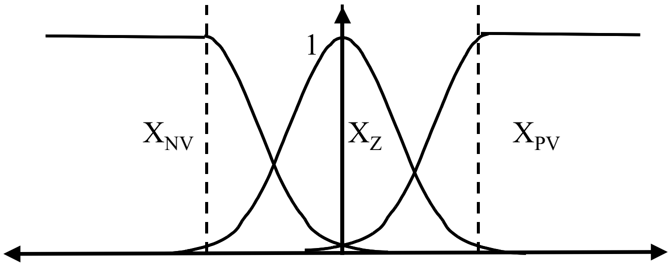

FIGURE 30.6 Gaussian-trapezoidal membership functions.

The fuzzy singleton function is quite useful in defining some special membership functions. If we would like to dispense with the need for a continuous degree of membership and prefer a binary valued function, the fuzzy singleton is an ideal candidate. We can form the membership function representing the fuzzy variable as a collection of fuzzy singletons ranging within the regions denoted by $[\mu + \sigma/2, \mu - \sigma/2]$. A graphical representation using three fuzzy variables (membership functions) is shown in Fig. 30.7 (In Fig. 30.7 the corners are only slanted so that the regions are easier to distinguish from each other.) Thus, the membership functions shown in Fig. 30.7 would be best defined as an integral of the fuzzy singleton with respect to the mean over the width of the function. Consequently, the membership function $X(\sigma, \mu)$ would be defined as follows:

$$X(\sigma, \mu) = \int_{\mu-\sigma/2}^{\mu+\sigma/2} S(\mu_s) d\mu_s \tag{30.6}$$

where $S(\mu_S)$ is the singleton function.

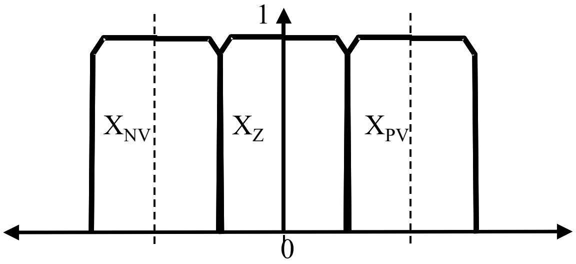

FIGURE 30.7 Membership functions comprised of fuzzy singletons.

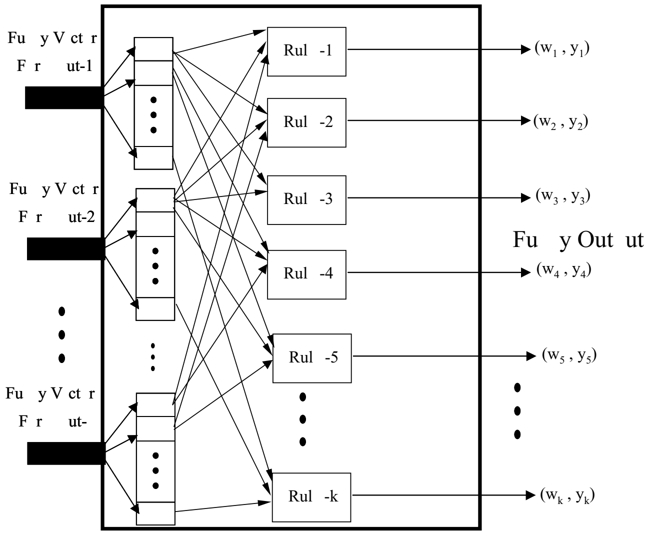

FIGURE 30.8 Fuzzy inference engine.

30.2.3 The Fuzzy Inference Engine

The fuzzy inference engine uses the fuzzy vectors to evaluate the fuzzy rules and produce an output for each rule. Figure 30.8 shows a block diagram of the fuzzy inference engine. Note that the rule-based system takes the form found in Eq. (30.1). This form could be applied to traditional logic as well as fuzzy logic albeit with some modification. A typical rule R would be:

$$R_i\text{:}\quad \text{IF } x_i \quad \text{THEN} \quad y = C_i \tag{30.7}$$

where x_i is the result of some logic expression.

The logical expression used in the case of fuzzy inference (30.7) is of the form

$$x \in X_i \tag{30.8}$$

where x is the input and X_i is the linguistic variable.

In binary logic, the expression in Eq. (30.8) results in either true or false. However, in fuzzy logic we often require a continuum of truth values. Figures 30.9 and 30.10 illustrate the difference between binary logic and fuzzy logic. In traditional logic, there is a single point representing the boundary between true and false. While in fuzzy logic, there is an entire region over which there is a continuous variation between truth and falsehood. The second part of Eq. (30.7), $y = C_i$, is the action prescribed by the particular rule. This portion indicates what value will be assigned to the output. This value could be either a fuzzy linguistic description or a crisp numerical value.

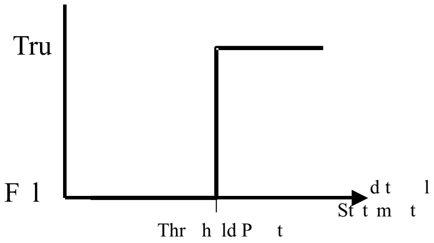

FIGURE 30.9 Binary logic statement evaluation.

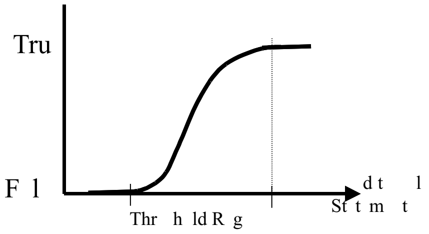

FIGURE 30.10 Fuzzy logic statement evaluation.

The logical expression that dictates whether the result of a particular rule is carried out could involve multiple criteria. Multiple conditions imply multiple input, as is most often the case in many applications of fuzzy logic to dynamic systems. Let us describe a system with two inputs x^1 and x^2. For simplicity of explanation and without loss of generality, we will use 3 fuzzy variables, namely PV, ZE and NV. Although each linguistic variable x^1 and x^2 uses the same fuzzy qualifiers, each input must have its own membership functions since they belong to different spaces. Thus, we will have two fuzzy vectors $\_^1$ and $\_^2$, for the first and second input, respectively:

$$\_^1 = [X^1_{NV}(x^1) \quad X^1_{ZE}(x^1)) \quad X^1_{PV}(x^1)] = [x^1_1 \quad x^1_2 \quad x^1_3] \tag{30.9(a)}$$

$$\_^2 = [X^2_{NV}(x^2) \quad X^2_{ZE}(x^2)) \quad X^2_{PV}(x^2)] = [x^2_1 \quad x^2_2 \quad x^2_3] \tag{30.9(b)}$$

where

X^n_{NV} = membership function for the Negative fuzzy variable for input n
X^n_{ZE} = membership function for the Zero fuzzy variable for input n
X^n_{PV} = membership function for the Positive fuzzy variable for input n
x^1 first linguistic variable (input 1)
x^2 second linguistic variable (input 2)
x^1_i the degree of membership of input 1 into the ith fuzzy variable's category
x^2_j the degree of membership of input 2 into the jth fuzzy variable's category.

The inference mechanism in this case would be specified by the rule R_{ij}:

$$R_{ij}\text{:}\quad \text{IF} \quad (x^1_i \text{ AND } x^2_j) \quad \text{THEN} \quad y = C_i. \tag{30.10}$$

The specification R_{ij} is made so as to emphasize that all combinations of the components of the fuzzy vectors should be used in separate rules. A specific example of one of the rules can be described as follows:

$$R_{13}: \quad \text{IF} \quad (x_1^1 \text{ AND } x_3^2) \quad \text{THEN} \quad y = C_{13}.$$

This rule can be written linguistically as

$$R_{13}: \quad \text{IF} \quad ((x^1 \text{ is Negative AND } (x^2 \text{ is Positive})) \quad \text{THEN} \quad y = C_{13}$$

where

x^1 is the first linguistic variable
x^2 is the second linguistic variable
C_{13} is the output action to be defined by the system designer.

The AND in Eq. (30.10) can be interpreted and evaluated in two different ways. First, the AND could be evaluated as the product of x_i^1 and x_j^2 [7]. Thus

$$x_i^1 \text{ AND } x_j^2 = x_i^1 x_j^2.$$

The second method is by taking the minimum of the terms [7]. In this case the result is the minimum value of the membership values. Therefore

$$x_i^1 \text{ AND } x_j^2 = \min(x_i^1,\, x_j^2).$$

The most commonly used method in the literature is the product method. Therefore, the product method is used in this chapter to evaluate the AND function. Equation (30.10) can be expanded to multiple input with multiple fuzzy variables. In the most general case of n inputs and k linguistic qualifiers, we would have the rule R_i:

$$R_i: \quad \text{IF} \quad [x_i^1 \text{ AND } x_i^2 \text{ AND } \ldots \text{ AND } x_i^n] \quad \text{THEN} \quad y = C_i \tag{30.11}$$

Recalling that all combinations of input vector components must be taken between fuzzy vector components the system designer could have up to nk rules, where n is the number of fuzzy variables used to describe the inputs and k is the number of inputs. The number of rules used by the fuzzy inference engine could be reduced if the designer could eliminate some combinations of input conditions.

3 .2.4 Defuzzification

The fuzzy inference engine as described previously often has multiple rules, each with possibly a different output. Deffuzzification refers to the method employed to combine these many outputs into a single output. Using Eq. (30.11) where multiple inputs $(x^1 x^2 \ldots x^n)$ should be evaluated, the product due to the evaluation of the premise conditions (defined by the components of the fuzzy vectors) determines the strength of the overall rule evaluation, w_i:

$$\begin{aligned} w_i &= x_i^1 \text{ AND } x_i^2 \text{ AND } \ldots \quad \text{AND } x_i^n \\ w_i &= (x_i^1)(x_i^2)\ldots(x_i^n) \end{aligned} \tag{30.12}$$

where x_i^k is the membership value of the kth input into the ith fuzzy variable's category. This value, w_i, becomes extremely important in defuzzification. Ultimately, defuzzification involves both the set of outputs C_i and the corresponding rule strength w_i.

There are a number of methods used for defuzzification, including the center of gravity (COG) and mean of maxima (MOM) [13]. The COG method otherwise known as the fuzzy centroid is denoted by y^{COG}.

$$y^{\text{COG}} = \frac{\sum_i w_i C_i}{\sum_i w_i} \tag{30.13}$$

where $w_i = \prod_k x_i^k$ and C_i is the corresponding output.

The mean of maxima method selects the outputs C_i that have the corresponding highest values of w_i.

$$y^{\text{MOM}} = \sum_{C_i \in G} C_i / Card(G) \tag{30.14}$$

where G denotes a subset of C_i consisting of these values that have the maximum value of w_i.

Out of the two methods of defuzzification, the most common method is the fuzzy centroid and is the one employed in this chapter.

3 .3 Applications of Fuzzy Logic to Electric Drives

High performance drives require that the shaft speed and the rotor position follow pre-selected tracks (trajectories) at all times [11,12]. To accomplish this, two fuzzy control systems were designed and implemented. The goal of fuzzy control system is to replace an experienced human operator with a fuzzy rule-based system. The fuzzy logic controller provides an algorithm that converts the linguistic control maneuvering, based on expert knowledge, into an automatic control approach. In this section, a Fuzzy Logic Controller (FLC) is proposed and applied to high performance speed and position tracking of a brushless dc (BLDC) motor. The proposed controller provides the high degree of accuracy required by high performance drives without the need for detailed mathematical models. A laboratory implementation of the fuzzy logic-tracking controller using the Motorola MC68HC11E9 microprocessor is described in this chapter. Additionally, in this experiment a bang-bang controller is compared to the fuzzy controller.

30.3.1 Fuzzy Logic-Based Microprocessor Controller

The first step in designing a fuzzy controller is to decide which state variables representative of system dynamic performance can be taken as the input signals to the controller. Further, choosing the proper fuzzy variables formulating the fuzzy control rules are also significant factors in the performance of the fuzzy control system. Empirical knowledge and engineering intuition play an important role in choosing fuzzy variables and their corresponding membership functions. The motor drive's state variables and their corresponding errors are usually used as the fuzzy controller's inputs including rotor speed, rotor position and rotor acceleration. After choosing proper linguistic variables as input and output of the fuzzy controller, it is required to decide on the fuzzy variables to be used. These variables transform the numerical values of the input of the fuzzy controller to fuzzy quantities. The number of these fuzzy variables specifies the quality of the control, which can be achieved using the fuzzy controller. As the number of the fuzzy variable increases, the management of the rules is more involved and the tuning of the fuzzy controller is less straightforward. Accordingly, a compromise between the quality of control and computational time is required to choose the number of fuzzy variables. For the BLDC motor drive under study two inputs are usually required. After specifying the fuzzy sets, it is required to determine the membership functions for these sets. Finally, the FLC is implemented by using a set of fuzzy decision rules. After the rules are evaluated, a fuzzy centroid is used to determine the fuzzy control output. Details of the design of the proposed controllers are given in the following subsections.

30.3.2 Fuzzy Logic-Based Speed Controller

In the case of shaft speed control to achieve optimal tracking performance, the motor speed error (ω_e) and the motor acceleration error (α_e) are used as inputs to the proposed controller. The controller output is the change in the motor voltage. For the fuzzy logic based speed controller, the two inputs required are defined as

$$\omega_e = \omega_{ref} - \omega_{act} \tag{30.15}$$

$$\alpha_e = \alpha_{ref} - \alpha_{act} \tag{30.16}$$

where

ω_{ref} = the desired speed (rad/s)
ω_{act} = the measured speed (rad/s)
α_{ref} = 0, because we want to minimize the acceleration to zero
α_{act} = the calculated acceleration in (rad/s^2).

For both the speed and acceleration errors, three regions of operation are established according to the fuzzy variables. These regions are positive error, zero and negative error. The proposed controller uses these regions to determine the required motor voltage, which enables the motor speed to follow a desired reference trajectory. Examples of the broad fuzzy decisions are:

IF speed error is positive, THEN decrease the output
IF speed error is zero, THEN maintain the output
IF speed error is negative, THEN increase the output
IF acceleration error is positive, THEN decrease the output
IF acceleration error is zero, THEN maintain the output
IF acceleration error is negative, THEN increase the output.

To achieve a sufficiently good quality of control, the three basic variables must be further refined. Thus the linguistic variable "acceleration error" has seven fuzzy variables: negative large (NL), negative medium (NM), negative small (NS), zero, positive small (PS), positive medium (PM) and positive large (PL). The values associated with the fuzzy variables for the acceleration error are shown in Table 30.2.

The linguistic variable "speed error" has nine fuzzy variables: negative large (NL), negative medium (NM), negative medium small (NMS), negative small (NS), zero, positive small (PS), positive medium (PM), positive medium small (PMS) and positive large (PL). Two fuzzy sets, namely negative medium small (NMS) and positive medium small (PMS), are added to enhance the tracking performance. The regions defined for each fuzzy variable for the speed error is summarized in Table 30.3.

After specifying the fuzzy sets, it is required to determine the membership functions for these sets. The membership function for the fuzzy variable representing ZERO is a fuzzy singleton. Additionally, the other membership functions are of the type described in Eq. (30.6) and are composed of fuzzy singletons within the region defined for each particular fuzzy

TABLE 30.2 Fuzzy variables for the acceleration error (α_e) for speed control

Fuzzy Variable	Acceleration Error (rad/s^2)
NL	$\alpha_e \leq -738$
NM	$-738 < \alpha_e \leq -369$
NS	$-369 < \alpha_e < 0$
ZE	$\alpha_e = 0$
PS	$0 < \alpha_e < 369$
PM	$369 \leq \alpha_e < 738$
PL	$738 \leq \alpha_e$

TABLE 30.3 Fuzzy variables for the speed error (ω_e) for speed control

Fuzzy Variable	Speed Error (rad/s)
NL	$\omega_e \leq -209$
NM	$-209 < \omega_e \leq -104$
NMS	$-104 < \omega_e \leq -49$
NS	$-49 < \omega_e < 0$
Z	$\omega_e = 0$
PS	$0 < \omega_e < 49$
PMS	$49 \leq \omega_e < 104$
PM	$104 \leq \omega_e < 209$
PL	$209 \leq \omega_e$

TABLE 30.4 Decision table for speed control

	Velocity Error									
	NL	NM	NMS	NS	ZERO	PS	PMS	PM	PL	
Acceleration Error										
PL	NS	NVVS	PVVS	PVS	PS	PMS	PM	PL	PVVL	
PM	NMS	NVS	ZERO	PVVS	PVS	PS	PMS	PML	PVL	
PS	NMS	NS	NVVS	ZERO	PVVS	PVS	PS	PM	PL	
ZERO	NML	NMS	NVS	NVVS	NVVS	ZERO	PVVS	PVS	PMS	PML
NS	NL	NM	NS	NVS	ZERO	PVVS	PS	PML		
NM	NVL	NML	NMS	NS	NVS	NVVS	ZERO	PVS	PMS	
NL	NVVL	NL	NM	NMS	NS	NVS	NVVS	PVVS	PS	

variable. Figures 30.11 and 30.12 show the resulting membership function for the acceleration and speed errors, respectively.

The two fuzzy sets illustrated in Figures 30.11 and 30.12 result in 63 linguistic rules for the BLDC drive system under study. The conditional rules listed in Table 30.4 are clearly implied, and the physical meanings of some rules are briefly explained as follows:

Rule 1 IF speed error is PL (positive large) AND acceleration is PS (positive small), THEN change in control voltage (output of fuzzy controller) is PL (positive large). This rule implies a general condition when the measured speed is far from the desired reference speed. Accordingly, it requires a large increase in the control voltage to force the shaft speed to the desired reference speed quickly.

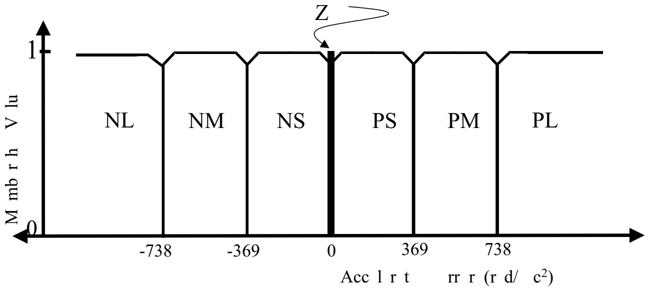

FIGURE 30.11 Membership functions for the acceleration error.

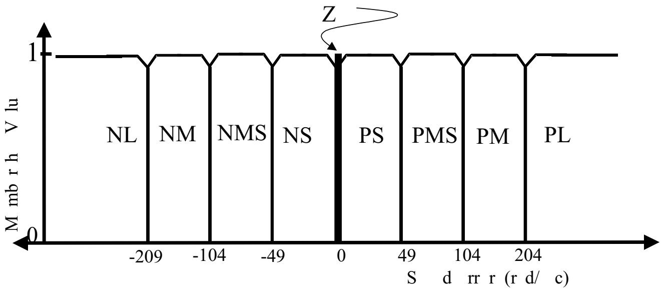

FIGURE 30.12 Membership functions for the speed error.

Rule 2 IF speed error is PS (positive small) AND acceleration is ZERO, THEN change in control voltage is PVVS (positive very very small). This rule implements the conditions when the error starts to decrease and the measured speed is approaching the desired reference speed. Consequently, a very small increase in the control voltage is applied.

Rule 3 IF speed error is ZERO AND acceleration is NS (negative small), THEN change in control voltage is PVVS (positive very very small). This rule deals with the circumstances when overshoot does occur. A very small decrease in the control voltage is required, which brings the motor speed to the desired reference speed.

These rules comprise the decision mechanism for the fuzzy speed controller. The decision table, Table 30.4, consists of values showing the different situations experienced by the drive system and the corresponding control input functions. It is clear that each entry in Table 30.4 represents a particular rule.

Now it is necessary to find the fuzzy output (change in control voltage). In this experiment the fuzzy centroid is used. Equation (30.17) shows the fuzzy centroid used to compute the final output of the controller:

$$\text{output} = \left(\frac{w_1 o_1 + w_2 o_2 + w_3 o_3 + \cdots + w_{63} o_{63}}{w_1 + w_2 + w_3 + \cdots + w_{63}} \right). \tag{30.17}$$

The weights w_i will be the strength of each particular rule's evaluation. The rule strength is evaluated as the product of the membership values associated with the speed and acceleration errors for the particular fuzzy variables involved in that rule. Since the membership functions were comprised solely of fuzzy singletons and the AND operator is evaluated as a product, the strength of each rules evaluation (w_i) will be either 0 or 1. Additionally, since the membership functions do not overlap, only one rule will be evaluated as true at each sample time. Thus all the weights w_i will be zero except one. So the actual implementation can be simplified.

3 .3.3 Fuzzy Logic-Based Position Controller

The task of the position control algorithm is to force the rotor position of the motor to follow a desired reference track without overshoot. The same method applied to the fuzzy speed controller is applied to the position controller. The inputs to the fuzzy position controller are, angular position error (θ_e) and motor speed error (ω_e). The output from the controller is a change in the motor voltage. The two inputs are defined as follows:

$$\theta_e = \theta_{ref} - \theta_{act} \tag{30.18}$$

$$\omega_e = \omega_{ref} - \omega_{act} \tag{30.19}$$

where

θ_{ref} = the desired position in radians
θ_{act} = the measured position in radians
$\omega_{ref} = 0$, because we want to minimize the speed to zero
ω_{act} = the measured speed in radians/s.

Nine fuzzy variables were defined for the position error and seven for the speed error. The fuzzy variables for the position error and the speed are defined in Tables 30.5 and 30.6, respectively. After specifying the fuzzy sets for the position controller, the membership functions can then be fully defined if it is required to determine the membership functions for these sets. The membership function for the fuzzy variable ZERO is a fuzzy singleton. Additionally, the other membership functions are of the type described in Eq. (30.6) and are composed of fuzzy singletons within the region defined for each particular fuzzy variable. Figures 30.13 and 30.14 show the resulting membership function for the speed and position errors respectively.

A corresponding output to the motor based on the speed and the rotor position error detected in each sampling interval must be assigned and thereby specifying the fuzzy inference engine. This is done by the fuzzy rules. For example, IF the position error is PL (positive large) AND the speed is PS (positive small), THEN a large positive change in driving effort is used. The crisp (defuzzified) output signal of the fuzzy controller is obtained by calculating the centriod of all fuzzy output variables. The fuzzy rule-base, on which the required change in the motor voltage is generated, is illustrated in Table 30.7.

TABLE 30.5 Fuzzy variables of the speed error for position control

Fuzzy Variable	Speed Error (rad/s)
NL	$x^2 \leq -209$
NM	$-209 < x^2 \leq -104$
NS	$-104 < x^2 < 0$
ZE	$x^2 = 0$
PS	$0 < x^2 < 104$
PM	$104 \leq x^2 < 209$
PL	$209 \leq x^2$

TABLE 30.6 Fuzzy variables of position error (θ_e) for position control

Fuzzy Variable	Position Error (rad)
NL	$\theta_e \leq -2.21$
NM	$-2.21 < \theta_e \leq -105$
NMS	$-1.05 < \theta_e \leq -0.53$
NS	$-0.53 < \theta_e < 0$
Z	$\theta_e = 0$
PS	$0 < \theta_e < 0.53$
PMS	$0.53 \leq \theta_e < 1.05$
PM	$1.05 \leq \theta_e < 2.21$
PL	$2.21\ t\theta_e$

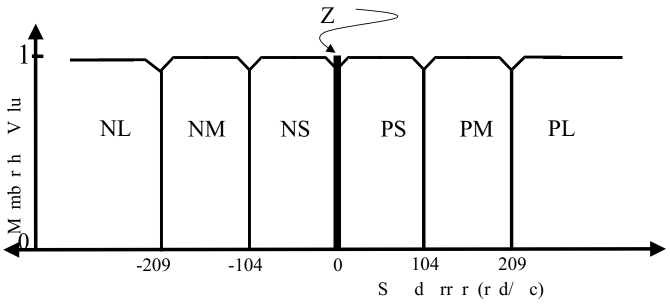

FIGURE 30.13 Membership functions for the speed error.

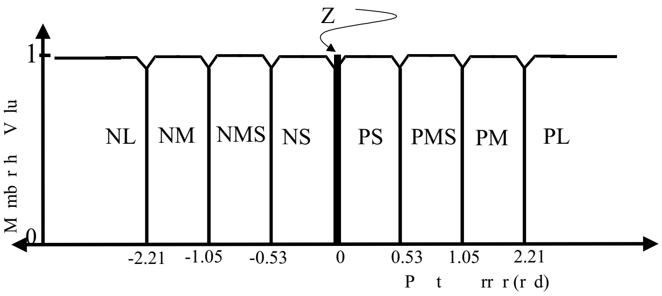

FIGURE 30.14 Membership functions for the position error.

TABLE 30.7 Decision table for position control

	Position Error								
	NL	NM	NMS	NS	ZERO	PS	PMS	PM	PL
Speed Error									
PL	NS	NVVS	PVVS	PVS	PS	PMS	PM	PL	PVVL
PM	NMS	NVS	ZERO	PVVS	PVS	PS	PMS	PML	PVL
PS	NMS	NS	NVVS	ZERO	PVVS	PVS	PS	PM	PL
ZERO	NML	NMS	NVS	NVVS	ZERO	PVVS	PVS	PMS	PML
NS	NL	NM	NS	NVS	NVVS	ZERO	PVVS	PS	PML
NM	NVL	NML	NMS	NS	NVS	NVVS	ZERO	PVS	PMS
NL	NVVL	NL	NM	NMS	NS	NVS	NVVS	PVVS	PS

3 .4 ardware System Description

The BLDC drive system under control consists of the components illustrated in Figure 30.15. The drive system is made up of several distinct subsystems: the motor, a personal computer (PC), the driving circuit, and the microprocessor evaluation board. The motor is A $\frac{1}{4}$HP, 3000 rev/min BLDC motor, and was manufactured by Pittman Company. The BLDC motor is equipped with a hall-effect sensor and an incremental optical encoder. The hall-effect sensors detect the rotor position to indicate which of the three phases of the motor is to be excited as the motor spins. The optical position encoder with resolution of 500 pulses/revolution is used to give speed and position feedback.

The controller is implemented by software and executed using a microprocessor. The control algorithm is written and loaded into the microprocessor using the PC. The computer used is an IBM 486 PC. The driving circuit is constructed using two major components: (1) the integrated circuit (UDN2936W-120) designed for BLDC drives [1], and (2) the digital to analog converter (DAC) and power amplifier. The inputs to the integrated circuit are the rotor position (which is obtained from Hall-effect sensors), the direction of desired rotation, and the magnitude of the control voltage. The output of the switching logic section is a sequence of gating signals that are pulse width-modulated (PWM). These signals are used to drive the power converter portion of the chip. The power converter is a dc/ac inverter utilizing 6 MOSFETs. The output of the power converter is a chopped three-phase ac waveform.

The microprocessor used was the Motorola MC68HC11E9 microprocessor [9]. The onboard memory system includes 8 kbytes of ROM (read-only memory), 512 bytes of EEPROM (electrically erasable programmable ROM), and 256 bytes of RAM (random access memory). The processor also has four 8 bit parallel input/output ports, namely A, B, C and E. The program is completely contained in the microprocessor and the computer is only required to load new programs into the processor. Additionally, it has an internal analog-to-digital converter, and can accept up to four analog inputs. Figure 30.15 includes the integrated circuit (UDN2936W-120) designed for operating the BLDC motor. The range of the input voltage (control voltage) is between zero and 25 V. The motor speed for any control voltage less than 7 V is zero. This indicates that the motor requires a minimum of 7 V to start. This limitation is actually a protective feature of the circuit to prevent malfunctions [1]. Thus, the actual output of the microprocessor (the control signal $V_C(k)$) is added to a 7 V dc offset, using a summing amplifier. The current out of the summing amplifier must first be increased before it can be used to drive the motor. The current amplification is accomplished by using a 40 V power transistor (TIP31A). In addition, when a sudden change in speed or direction occurs, the back emf produced by the motor can sometimes cause large currents. Since the output stage of the integrated circuit (UDN2936W-120) has transistors with a current rating of ±3 A, some limiting resistors were needed to prevent damage. Figure 30.16 shows a snapshot of the laboratory experiment.

Speed measurements were taken using a frequency to voltage converter LM2907. The LM2907 produces a voltage proportional to the frequency of the pulses it receives at its input. In this experiment, the pulses were sourced from the encoder signal A. The circuit was constructed such that the maximum speed of the motor corresponded to 5 V. This value was input into the microprocessor, via the onchip A/D converter, as an 8 bit word. The direction of rotation was observed using a D flipflop. This direction signal was used to indicate the sign of the speed. The two signals, speed and direction, were combined within the software environment to

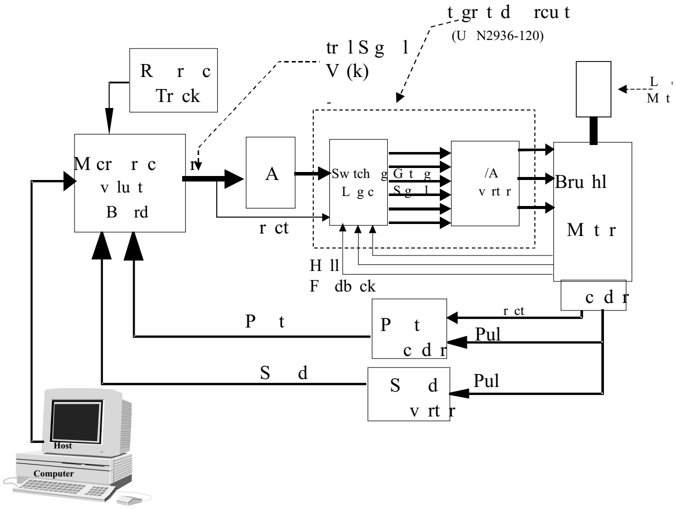

FIGURE 30.15 Block diagram of the laboratory setup.

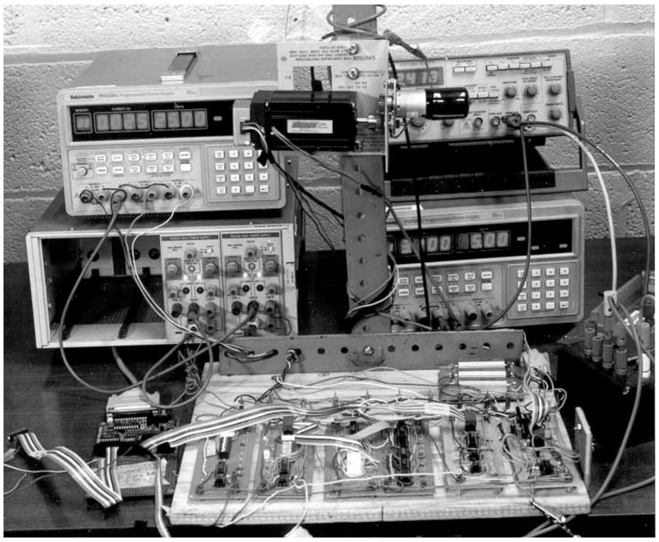

FIGURE 30.16 Photograph of the hardware implementation.

produce an integer. Thus internally the speed could range from +256 to −256. These limits represent +3000 and −3000 r.p.m., respectively. Additionally, the digital output of the microprocessor was limited to the resolution provided by 7 bits. Therefore, if the desired output voltage was 22 V, then the maximum byte output was 127. Thus each increment in control signal, numerically within the microprocessor, would produce a change of 0.17 V.

3 .4.1 Experimental Results

A square wave followed by a sinusoidal reference track was considered. In this experiment, there is a weight attached to the motor via a cable and pulley assembly. Figure 30.17 shows the speed tracking performance of the fuzzy logic controller. The motor is under constant load. The actual motor speed is superimposed on the desired reference speed in order to compare tracking accuracy. High tracking accuracy is observed at all speeds. The corresponding position tracking performance is displayed in Figure 30.18. Reasonable position tracking accuracy is displayed. One can see from these figures that the results were very successful. For comparison purposes, Figs. 30.19 and 30.20 exhibit cases in which the fuzzy logic controller was replaced by a bang-bang controller. However, when a bang-bang controller was applied the controller could not maintain tracking accuracy. That is, the response using the bang-bang controller was unsatisfactory.

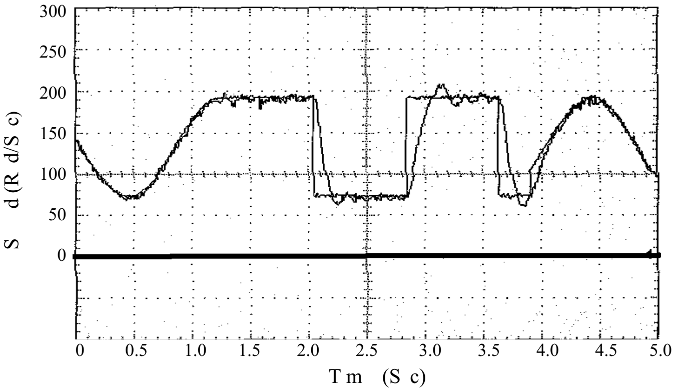

FIGURE 30.17 Fuzzy speed tracking under loading condition.

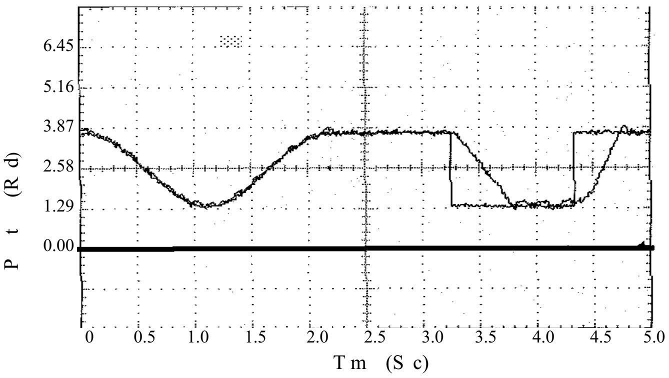

FIGURE 30.18 Fuzzy position tracking under loading condition.

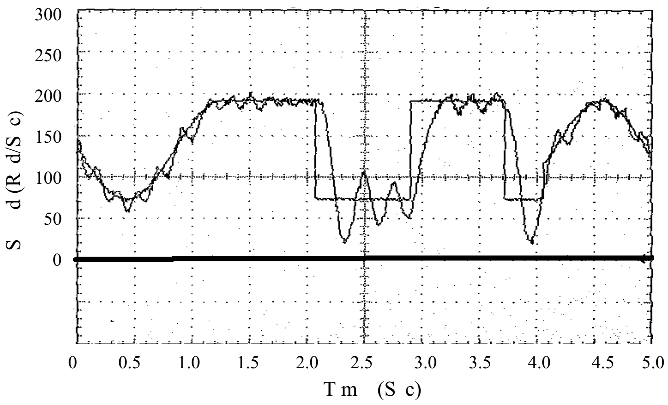

FIGURE 30.19 Bang-bang speed tracking under loading condition.

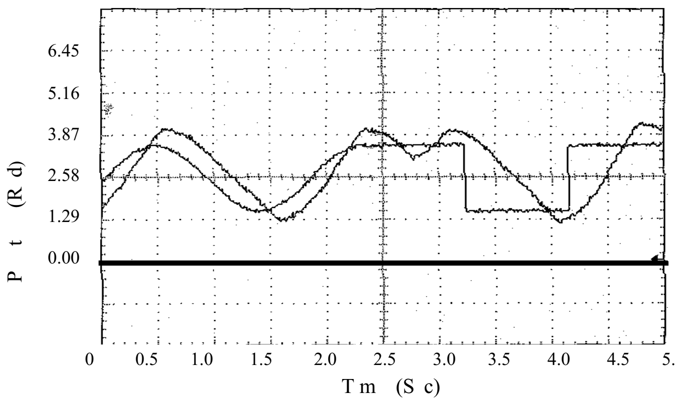

FIGURE 30.20 Bang-bang position tracking with load.

3 .5 Conclusion

This chapter describes a fuzzy logic-based microprocessor controller, which incorporates attractive features such as simplicity, good performance, and automation while utilizing a low cost hardware and software implementation. The test results indicate that the fuzzy logic-tracking controllers follow the trajectories successfully. Additionally, experimental results show that the effective smooth speed/position control and tracking of BLDC motors can be achieved by the FLC, thus making it suitable for high performance motor drive applications. The controller design does not require explicit knowledge of the motor/load dynamics. This is a useful feature when dealing with parameter and load uncertainties. The advantage of using a fuzzy logic-tracking controller in this application is that it is well suited to the control of unknown or ill-defined nonlinear dynamics.

Acknowledgments

The author would like to acknowledge the assistance of Mr Daniel O Ricketts, a graduate student at Howard University, in clarifying these concepts and obtaining the experimental results. The author would also like to acknowledge the financial support by NASA Glenn Research Center, in the form of grant no. NAG3-2287 technically monitored by Mr Donald F Noga.

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31

Automotive Applications of Power Electronics

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31.1 Introduction

The modern automobile has an extensive electrical system consisting of a large number of electrical, electromechanical, and electronic loads that are central to vehicle operation, passenger safety, and comfort. Power electronics is playing an increasingly important role in automotive electrical systems conditioning the power generated by the alternator, processing it appropriately for the vehicle electrical loads, and controlling the operation of these loads. Furthermore, power electronics is an enabling technology for a wide range of future loads with new features and functions. Such loads include electromagnetic engine valves, active suspension, controlled lighting, and electric propulsion.

This chapter discusses the application and design of power electronics in automobiles. Section 31.2 provides an overview of the architecture of the present automotive electrical power system. The next section, Section 31.3, describes the environmental factors, such as voltage ranges, EMI/EMC requirements, and temperature, which strongly influence the design of automotive power electronics. Section 31.4 discusses a number of electrical functions that are enabled by power electronics, while Section 31.5 addresses load control via multiplexed remote switching architectures that can be implemented with power electronic switching. Section 31.6 considers the application of power electronics in automotive electromechanical energy conversion, including power generation. Section 31.7 describes the potential evolution of automotive electrical systems towards high- and dual-voltage systems, and provides an overview of the likely requirements of power electronics in such systems. Finally, the application of power electronics in electric and hybrid electric vehicles is addressed in Section 31.8.

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31.2 The Present Automotive Electrical Power System

Present day automobiles can have over 200 individual electrical loads, with average power requirements in excess of 800 W. These include such functions as the headlamps, tail lamps, cabin lamps, starter, fuel pump, wiper, blower fan, fuel injector, transmission shift solenoids, horn, cigar lighter, seat heaters, engine control unit, cruise control, radio, and spark ignition. To power these loads present day internal combustion engine (ICE) automobiles use an electrical power system similar to the one shown in Fig. 31.1. Power is generated by an engine-driven three-phase wound-field synchronous machine a Lundell (claw-pole) alternator [1, 2]. The ac voltage of this machine is rectified and the dc output regulated to about 14 V by an electronic regulator that controls the field current of the machine. The alternator provides power to the loads and charges a 12 V lead–acid battery. The battery provides the high power needed by such loads as the starter, and supplies power when the engine is not running or when the demand for electrical power exceeds the output power of the alternator. The battery also acts as a large capacitor and smoothes out the system voltage.

Power is distributed to the loads via fuses and point-to-point wiring. The fuses, located in one or more fuseboxes, protect the wires against overheating and fire in the case of a short. Most of the loads are controlled directly by manually actuated mechanical switches. These primary switches are located in areas in easy reach of either the driver or the passengers, such as the dashboard, door panels, and the ceiling. Some of the heavy loads, such as the starter, are switched indirectly via electromechanical relays.

31.3 System Environment

The challenging electrical and environmental conditions found in the modem automobile have a strong impact on the design of automotive power electronic equipment. Important factors affecting the design of electronics for this application include static and transient voltage ranges. electromagnetic interference and compatibility requirements (EMI/EMC), mechanical vibration and shock, and temperature and other environmental conditions. This section briefly describes some of the factors that most strongly affect the design of power electronics for automotive applications. For more detailed guidelines on the design of electronics for automotive applications, the reader is referred to [1, 3–16] and the documents cited therein, from which much of the information presented here is drawn.

31.3.1 Static Voltage Ranges

In most present-day automobiles, a Lundell-type alternator provides dc electrical power with a lead–acid battery for energy storage and buffering. The nominal battery voltage is 12.6 V, which the alternator regulates to 14.2 V when the engine is on in order to maintain a high state of charge on the battery. In practice, the regulation voltage is adjusted for temperature to match the battery characteristics. For example, in [1], a 25°C regulation voltage of 14.5 V is specified with a -10 mV/°C adjustment. Under normal operating conditions, the bus voltage will be maintained in the range of 11–16 V [3]. Safety-critical equipment is typically expected to be operable even under battery discharge down to 9 V, and equipment operating during starting may see a bus voltage as low as 4.5–6 V under certain conditions.

In addition to the normal operating voltage range, a wider range of conditions is sometimes considered in the design of automotive electronics [3]. One possible condition is reverse-polarity battery installation, resulting in a bus voltage of approximately -12 V. Another static overvoltage condition can occur during jump starting from a 24 V system such as on a tow truck. Other static overvoltage conditions can occur due to failure of the alternator voltage regulator. This can result in a bus voltage as high as 18 V, followed by battery electrolyte boil-off and a subsequent unregulated bus voltage as high as 130 V. Typically, it is not practical to design the electronics for operation under such an extreme fault condition, but it should be noted that such conditions can occur. Table 31.1

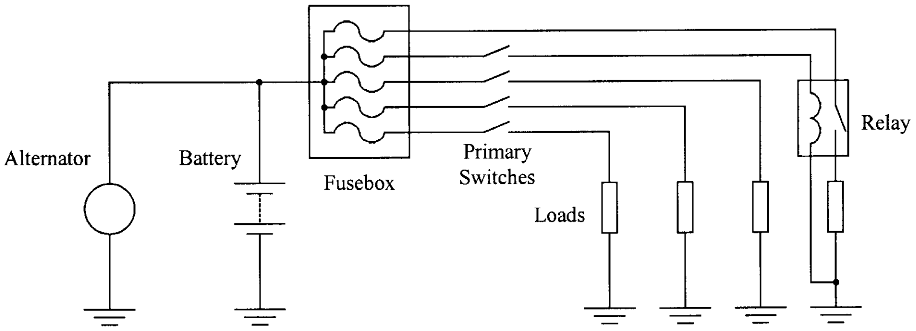


FIGURE 31.1 The 12 V point-to-point automotive electrical power system.

TABLE 31.1 Static voltage range for the automotive electrical system [3]

Static Voltage Condition	Voltage
Nominal voltage with engine on	14.2 V
Nominal voltage with engine off	12.6 V
Maximum normal operating voltage	16 V
Minimum normal operating voltage	9 V
Minimum voltage during starting	4.5 V
Jump start voltage	24 V
Reverse battery voltage	−12 V
Maximum voltage with alternator regulator failure followed by battery failure	130 V

summarizes the range of static voltages that can be expected in the automotive electrical system.

31.3.2 Transients and Electromagnetic Immunity

Power electronic circuits designed for automotive applications must exhibit electromagnetic compatibility, i.e. the conducted and radiated emissions generated by the circuit must not interfere with other equipment on board the vehicle, and the circuit must exhibit immunity to radiated and conducted disturbances. The Society of Automotive Engineers (SAE) has laid out standards and recommended practices for the electromagnetic compatibility of automotive electronics in a set of technical reports [4]. These reports are listed in Table 31.2. Here we will focus on two of the basic requirements of automotive power electronics: immunity to power lead transients, and limitation of conducted emissions.

A major consideration in the design of an automotive power electronic system is its immunity to the transients that can appear on its power leads. A number of transient sources exist in the vehicle [5], and procedures for validating immunity to these transients have been established in documents such as SAE J1113/11 [4, 6] and DIN 40389 [1]. Table 31.3 illustrates the transient test pulses specified in SAE J1113/11. Each test pulse corresponds to a different type of transient. The vehicle manufacturer determines which test pulses apply to a specific device.

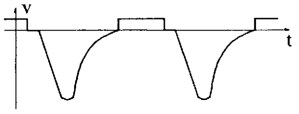
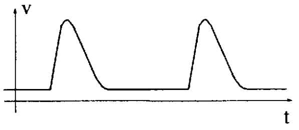
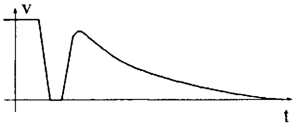
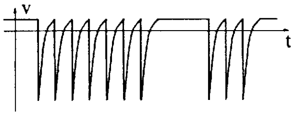
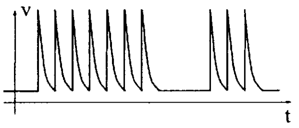
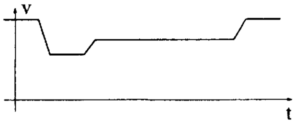
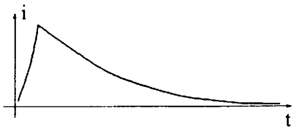
Transients occur when inductive loads such as solenoids, motors and clutches are turned on and off. The transients can be especially severe when the bus is disconnected from the battery, as is the case for the accessory loads when the ignition is switched off. Test pulse 1 in Table 31.3 simulates the transient generated when an inductive load is disconnected from the battery and the device under test remains in parallel with it. When the inductive load is a dc motor, it may briefly act as a generator after disconnection. This transient is simulated by test pulse 2b. Test pulse 2a models the transient when current in an inductive element in series with the device under test is interrupted. Test pulses 3a and 3b model switching spikes that appear on the bus during normal operation. Test pulse 4 models the voltage transient that occurs on starting.

Perhaps the best-known electrical disturbance is the so-called load dump transient that occurs when the alternator load current drops sharply and the battery is unable to properly buffer the change. This can occur when the battery becomes disconnected while drawing a large amount of current. To understand why a major transient can occur under this situation, consider that the Lundell alternator has a very large leakage reactance. The high commutating reactance interacting with the diode rectifier results in a high degree of load regulation, necessitating the use of a large back emf to source rated current at high speed [7]. Back voltages as high as 120 V may be needed to generate rated current into a 14 V output at top speed. Analytical modeling of such systems is addressed in [8]. When the load on the alternator suddenly

TABLE 31.2 SAE J1113 electromagnetic compatibility technical reports

SAE Specification	Type	Description
SAE J1113/1	Standard	Electromagnetic compatibility measurement procedures and limits, 60 Hz to 18 GHz
SAE J1113/2	Standard	Conducted immunity, 30 Hz–250 kHz
SAE J1113/3	Standard	Conducted immunity, direct injection of RF power, 250 kHz–500 MHz
SAE J1113/4	Standard	Conducted immunity, bulk current injection method
SAE J1113/11	Standard	Conducted immunity to power lead transients
SAE J1113/12	Recommended Practice	Electrical interference by conduction and coupling–coupling clamp
SAE J1113/13	Recommended Practice	Immunity to electrostatic discharge
SAE J1113/21	Information Report	Electrical disturbances by narrowband radiated electromagnetic energy component test methods
SAE J1113/22	Standard	Immunity to radiated magnetic fields from power lines
SAE J1113/23	Recommended Practice	Immunity to radiated electromagnetic fields, 10 kHz to 200 MHz, strip line method
SAE J1113/24	Standard	Immunity to radiated electromagnetic fields, 10 kHz to 200 MHz, TEM cell method
SAE J1113/25	Standard	Immunity to radiated electromagnetic fields, 10 kHz to 500 MHz, tri-plate line method
SAE J1113/26	Recommended Practice	Immunity to ac power line electric fields
SAE J1113/27	Recommended Practice	Immunity to radiated electromagnetic fields, reverberation method
SAE J1113/41	Standard	Radiated and conducted emissions, 150 kHz–1000 MHz
SAE J1113/42	Standard	Conducted transient emissions

TABLE 31.3 Transient pulse waveforms specified in SAE J1113/11

Pulse	Shape	Maximum Excursion	Source Impedance	Duration and Repetition Rate
1		−100 V	10 Ω	$T_{\text{pulse}} = 2$ ms $0.5\text{ s} < T_{\text{rep}} < 5\text{ s}$
2a		100 V	10 Ω	$T_{\text{pulse}} = 50\ \mu\text{s}$ $0.5\text{ s} < T_{\text{rep}} < 5\text{ s}$
2b		10 V	0.5–3 Ω	$T_{\text{pulse}} \geq 200$ ms
3a		−150 V	50 Ω	$T_{\text{pulse}} = 100$ ns $T_{\text{rep}} = 100\ \mu\text{s}$
3b		100 V	50 Ω	$T_{\text{pulse}} = 100$ ns $T_{\text{rep}} = 100\ \mu\text{s}$
4		−7 V	0.01 Ω	$T_{\text{pulse}} \leq 20$ s
5		84 A	0.6 Ω	$\tau = 115$ ms $T_{\text{pulse}} \sim 4\ \tau$

steps down two effects occur. First, as the machine current drops, the energy in the alternator leakage reactances is immediately delivered to the alternator output, causing a voltage spike. The peak voltage reached depends on the electrical system impedance, and may be limited by suppression devices. Second, once the alternator current is reduced, the voltage drops across the leakage (commutating) reactances are reduced, and a much larger fraction of the machine back emf is impressed across the dc output. The proper output voltage is only reestablished as the voltage regulator reduces the field current appropriately. With conventional regulator circuits this takes place on the time scale of the field winding time constant (typically 100 ms), and results in a major transient event. In systems without centralized protection, a load dump can generate a transient with a peak voltage in excess of 100 V lasting hundreds of milliseconds. Test pulse 5 in Table 31.3 (expressed as a current waveform in parallel with an output resistance) is designed to simulate such a load-dump transient; other load dump tests are even more severe [1, 3].

31.3.3 Electromagnetic Interference

Strict limits also exist for the amount of electromagnetic interference (EMI) that an automotive electronic component can generate. Limits for both conducted and radiated emissions are specified in SAE standards J1113/41 and J1113/42 [4, 9, 10]. Here we will consider the conducted EMI specifications for power leads, since they directly impact the design of EMI filters for automotive power electronics. Meeting the conducted specifications is a major step towards achieving overall compliance.

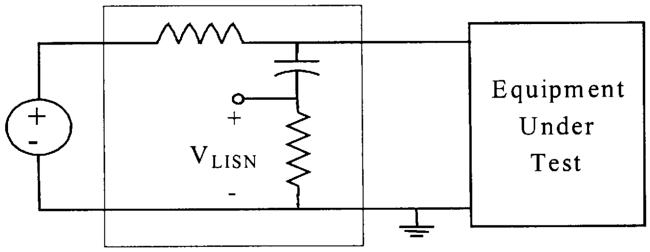


FIGURE 31.2 Conducted EMI test setup with line impedance stabilization network (LISN). $L_{\text{LISN}} = 5\ \mu\text{H}$, $C_{\text{LISN}} = 0.1\ \mu\text{F}$, and $R_{\text{LISN}} = 50\ \Omega$.

The conducted EMI specifications in SAE J1113/41 limit the ripple that an electronic circuit can inject onto the voltage bus over the frequency range from 150 kHz to 108 MHz. The amount of ripple injected by a circuit usually depends on the bus impedance. To eliminate any variability due to this, EMI compliance testing is done using a Line Impedance Stabilization Network (LISN) between the bus and the device under test, as illustrated in Fig. 31.2. The LISN is also sometimes referred to as an Artificial Mains Network (AN). Essentially, the LISN ensures that the equipment under test receives the proper dc voltage and current levels and also sees a controlled impedance for the ripple frequencies of interest. Figure 31.3 shows the magnitude of the LISN output impedance for a low-impedance input source; the effective impedance is 50 Ω over most of the frequency range of interest. The 50 Ω termination impedance of the LISN is typically provided by the measurement equipment. EMI specifications are stated in terms of the allowable voltage ripple (in dB μV) appearing across the 50 Ω LISN resistance as a function of frequency.

There are a wide range of other technical considerations for EMI testing, including the arrangement of the equipment over a ground plane and the types and settings of the measuring devices. One characteristic to consider is that the EMI measurements are done across frequency with a spectrum analyzer having a prespecified receiver bandwidth (RBW). For frequencies between 150 kHz and 30 MHz the receiver bandwidth is 9 kHz, resulting in spectral components within 9 kHz of one another being lumped together for purposes of the test. A full test procedure is defined in the SAE specifications, beginning with narrowband measurements and moving to wideband measurements if necessary. Figure 31.4 illustrates the narrow-band conducted EMI limits for power leads in SAE J1113/41. It is interesting to note that, for the commonly used Class 5 limits, the allowable ripple current into the LISN at 150 kHz is less than 100 μA

As seen in the previous section, the transient disturbances generated by electrical and electronic equipment are an important consideration in automotive applications. Because power electronic circuits typically contain switches and magnetic elements, they are potential sources for such transients, especially when powered from the switched ignition line. SAE J1113/42 specifies methods for testing and evaluating the transients generated by automotive electrical components, and proposes transient waveform limits for different severity levels. The equipment under test is set up in a configuration similar to that in Fig. 31.2, but with a switching device on one side or the other of the LISN, depending on the

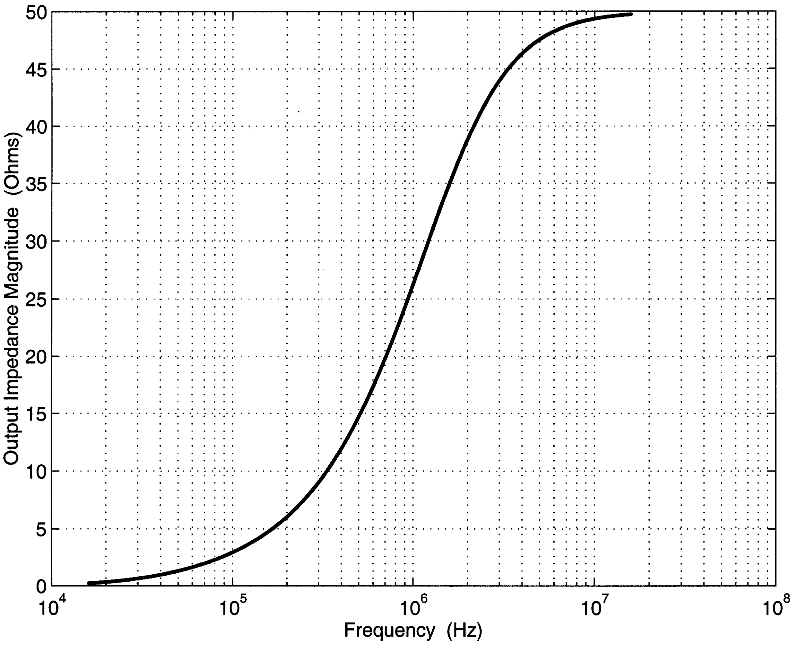


FIGURE 31.3 LISN output impedance magnitude for a low impedance input source.

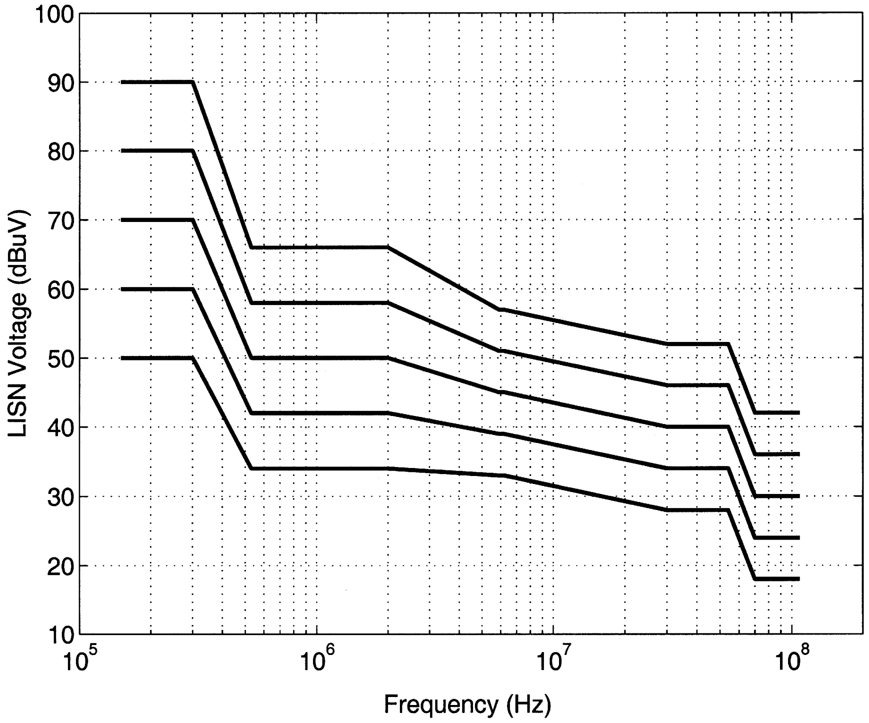


FIGURE 31.4 SAE J1113/41 narrow-band conducted EMI limits for power leads. The specification covers the frequency range from 150 kHz to 108 MHz.

application. The equipment under test is then evaluated for transient behavior at turn on, turn off, and across its operating range. The voltage transients at the input of the equipment are measured and evaluated with respect to magnitude, duration, and rise and fall times. Specific limits for such transients are specified by the vehicle manufacturer, but SAE J1113/42 proposes a representative set of limits for four different transient severity levels.

Due to the tight conducted emissions limits, input EMI filter design is an important consideration in automotive power electronics. Single or multistage low-pass filters are typically used to attenuate converter ripple to acceptable levels [11–13]. When designing such filters, the parasitic behavior of the filter components, such as capacitor equivalent series resistance and inductance, and suitable filter damping are important considerations [14]. One must also ensure that the filter design yields acceptable transients at switch on and off, and does not result in undesired dynamic interactions with the power circuit [13]. Attention to appropriate filter design, coupled with proper circuit layout, grounding, and shielding goes a long way towards meeting electromagnetic interference specifications [14].

31.3.4 Environmental Considerations

The automobile is a very challenging environment for electronics. Environmental factors influencing the design of automotive electronics include temperature, humidity, mechanical shock, vibration, immersion, salt spray, and exposure to sand, gravel, oil and other chemicals. In 1978, the Society of Automotive Engineers developed a recommended practice for electronic equipment design to address these environmental considerations [3, 4]. This document, SAE J1211, provides quantitative information about the automotive environment to aid the designer in developing environmental design goals for electronic equipment. Here we briefly summarize a few of the most important factors affecting the design of power electronics for automotive applications. For more detailed guidelines, the reader is referred to [3] and the documents cited therein.

Perhaps the most challenging environmental characteristic is the extreme range of temperatures that can occur in the automobile. Table 31.4 summarises some of the temperature extremes listed in SAE J1211 for different locations in the automobile. Ambient temperatures as low as −40°C may be found during operation, and storage temperatures as low as −50°C may be found for components shipped in unheated aircraft. Maximum ambient temperatures vary widely depending on vehicle location, even for small differences in position. Because ambient temperature has a strong impact on the design of a power electronic system it is important to work closely with the vehicle manufacturer to establish temperature specifications for a particular application. For equipment that is air-cooled one must also consider that the equipment may

TABLE 31.4 Automotive temperature extremes by location [3]

Vehicle Location	Min Temp (°C)	Max Temp (°C)
Exterior	−40	85
Chassis		
isolated	−40	85
near heat source	−40	121
drive train high temp location	−40	177
Interior		
floor	−40	85
rear deck	−40	104
instrument panel	−40	85
instrument panel top	−40	177
Trunk	−40	85
Under hood		
near radiator support structure	−40	100
intake manifold	−40	121
near alternator	−40	131
exhaust manifold	−40	649
dash panel (normal)	−40	121
dash panel (extreme)	−40	141

be operated at altitudes up to 12,000 feet above sea level. This results in low ambient pressure (down to 9 psia), which can reduce the heat transfer efficiency [3]. For equipment utilizing the radiator-cooling loop, maximum coolant temperatures in the range of 105-120°C at a pressure of 1.4 bar are possible [15].

In addition to the temperature extremes in the automobile, thermal cycling and shock are also important considerations due to their effect on component reliability. Thermal cycling refers to the cumulative effects of many transitions between temperature extremes, while thermal shock refers to rapid transitions between temperature extremes, as may happen when a component operating at high temperature is suddenly cooled by water splash. The damaging effects of thermal cycling and shock include failures caused by thermal expansion mismatches between materials. Test methods have been developed which are designed to expose such weaknesses [3, 16]. The thermal environment in the automobile, including the temperature extremes, cycling, and shock, are challenging issues that must be addressed in the design of automotive power electronics.

A number of other important environmental factors exist in the automobile. Humidity levels as high as 98 at 38°C can exist in some areas of the automobile, and frost can occur in situations where the temperature drops rapidly. Salt atmosphere, spray, water splash and immersion are also important factors for exterior, chassis, and underhood components. Failure mechanisms resulting from these factors include corrosion and circuit bridging. Dust, sand and gravel bombardment can also be significant effects, depending on equipment location. Mechanical vibration and shock are also important considerations in the design of automotive power electronic equipment. Details about the effects of these environmental factors, sample recorded data, and recommended test procedures can be found in [3].

31.4 unctions Enabled by Power Electronics

Over the past 20 years power electronics has played a major role in the introduction of new functions such as the antilock breaking system (ABS), traction control and active suspension, as well as the electrification of existing functions such as the engine-cooling fan, in the automobile. This trend is expected to continue, as a large number of new features being considered for introduction into automobiles require power electronics. This section discusses some of the new functions that have been enabled by power electronics, and some existing ones that benefit from it.

31.4.1 igh Intensity Discharge Lamps

High intensity discharge (HID) lamps have started to appear in automobiles as low-beam headlights and fog lights. HID lamps offer higher luminous efficacy, higher reliability, longer life and greater styling flexibility than the traditional halogen lamps [17, 18]. The luminous efficacy of an HID lamp is over three times that of a halogen lamp and its life is about 2,000 hours, compared to 300–700 hours for a halogen lamp. Therefore, HID lamps provide substantially higher road illumination while consuming the same amount of electrical power and, in most cases, should last the life of the automobile. HID lamps also produce a whiter light than halogen lamps since their color spectrum is closer to that of the sun.

HID lamps do not have a filament. Instead, light is generated by disharging an arc through a pressurized mixture of mercury, xenon and vaporized metal halides mercury produces most of the light, the metal halides determine the color spectrum, and xenon helps reduce the start-up time of the lamp [17, 19]. Unlike halogen lamps that can be powered directly from the 12 V electrical system, HID lamps require power electronic ballasts for their operation. Initially, a high voltage pulse of 10–30 kV is needed to ignite the arc between the electrodes and a voltage of about 85 V is needed to sustain the arc [19]. Figure 31.5 shows a simplified power electronic circuit that can be used to start and drive an HID lamp. A step-up dc–dc converter is used to boost the voltage from 12 V to the voltage needed for the steady state operation of the HID lamp. Any dc–dc converter that can step up the voltage, such as the boost or flyback converter, can be used for this application. An H-bridge is then used to create the ac voltage that drives the lamp in steady state. The circuit to initiate the arc can be as simple as a circuit that provides an inductive voltage kick, as shown in Fig. 31.5.

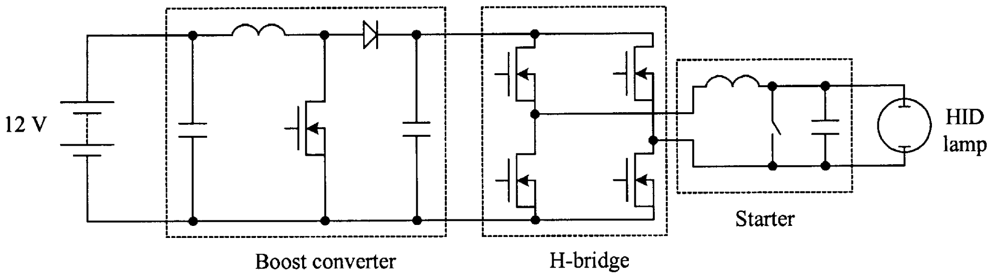


FIGURE 31.5 Simplified power electronic circuit for an HID lamp ballast.

31.4.2 Pulse-Width Modulated Incandescent Lighting

Future automobiles may utilize a 42 V electrical system in place of today's 14 V electrical system (see Section 31.7). Because HID lamps are driven through a power electronic ballast, HID lighting systems operable from a 42 V bus can easily be developed. However, the high cost of HID lighting — as much as an order of magnitude more expensive than incandescent lighting — largely limits its usefulness to headlight applications. Incandescent lamps compatible with 42 V systems can also be implemented. However, because a much longer, thinner filament must be employed at the higher voltage, lamp lifetime suffers greatly. An alternative to this approach is to use pulse-width modulation to operate 12 V incandescent lamps from a 42 V bus [20].

In a pulse-width modulated (PWM) Lighting system, a semiconductor switch is modulated to apply a periodic pulsed voltage to the lamp filament. Because of its resistive nature, the power delivered to the filament depends on the rms of the applied voltage waveform. The thermal mass of the system filters the power pulsations so that the filament temperature and light production are similar to that generated by a dc voltage with the same rms value. The PWM frequency is selected low enough to avoid lamp mechanical resonances and the need for EMI filtering, while being high enough to limit visible flicker; PWM frequencies in the range of 96–250 Hz are typical [20].

Ideally, a 11.1% duty ratio is needed to generate 14 V rms across a lamp from a 42 V nominal voltage source. In practice deviations from this duty ratio are needed to adjust for input voltage variations and device drops. In some proposed systems, multiple lamps are operated within a single lighting module with phase staggered (interleaved) PWM waveforms to reduce the input rms current of the module.

Another issue with PWM lighting relates to startup. Even with operation from a 12 V dc source, incandescent lamps have an inrush current that is 6–8 times higher than the steady-state value, because of how filament resistance changes with temperature; this inrush impacts lamp durability. The additional increase in peak inrush current due to operating from a 42 V source can be sufficient to cause destruction of the filament, even when using conventional PWM soft-start techniques (a ramping up of duty ratio). Means for limiting the peak inrush current — such as operating the controlling MOSFET in current limiting mode during startup — are needed to make practical use of PWM lighting control.

While PWM incandescent lighting technology is still in the early stages of development, it offers a number of promising advantages in future 42 V vehicles. These include low-cost adaptation of incandescent lighting to high-voltage systems, control of lighting intensity independent of bus voltage, the ability to implement multiple intensities, flashing, dimming, etc., through PWM control, and the potential improvement of lamp durability through more precise inrush and operating control [20].

31.4.3 Piezoelectric Ultrasonic Actuators

Piezoelectric ultrasonic motors are being considered as actuators for window lifts, seat positioning, and head restraints in automobiles [21, 22]. These motors work on the principle of converting piezoelectrically induced ultrasonic vibrations in an elastic body into unidirectional motion of a moving part. Unidirectional motion is achieved by allowing the vibrating body to make contact with the moving part only during a half cycle of its oscillation, and power is transferred from the vibrating body to the moving part through frictional contact. Ultrasonic motors have a number of attractive features, including high torque density, large holding torque even without input power, low speed without gears, quiet operation, no magnetic fields and high dynamics [21, 23]. These characteristics make ultrasonic motors an attractive alternative to electromagnetic motors for low-power high-torque applications.

Various types of ultrasonic motors have been developed. However, because of its compact design the traveling wave type is the most popular ultrasonic motor [24]. Figure 31.6(a) shows the basic structure of such a motor. It consists of a metal stator and rotor, which are pushed against each other by a spring. The rotor is coated with a special lining material to increase friction and reduce wear at the contacting surfaces. A layer of piezoelectric material, such as lead zirconate titanate

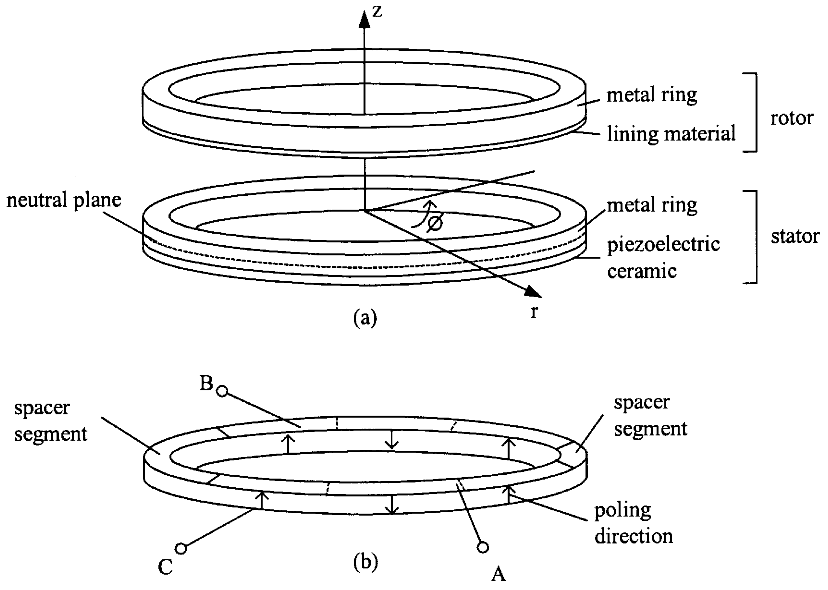


FIGURE 31.6 (a) Basic structure of a traveling wave piezoelectric ultrasonic motor. (b) Structure of the piezoceramic ring and electrode for a four-wavelength motor. Arrows indicate direction of polarization. Dashed lines indicate segments etched in the electrode for poling but electrically connected during motor operation.

(PZT), is bonded to the underside of the stator. Silver electrodes are printed on both sides of the piezoceramic ring. The top electrode is segmented and the piezoceramic is polarized as shown in Fig. 31.6(b). The number of segments is twice the order of the excited vibration mode.

When a positive voltage is applied between terminals A and C, the downwards poled segment elongates and the upwards poled segments contract. This causes the stator to undulate, waving down at the elongated section and up at the contracted one. When the polarity of the voltage is inverted, the undulations are also inverted. Hence, when an ac voltage is applied a flexural standing wave is created in the stator. To get a large wave amplitude the stator is driven at the resonance frequency of the flexural mode. An ac voltage between terminals B and C similarly produces another standing wave. However, because of the spacer segments in the piezoceramic ring, the second standing wave is 90° spatially out of phase from the first one. If the two standing waves are excited by ac voltages that are out of phase in time by 90°, a traveling wave is generated. As the traveling wave passes through a point along the neutral plane, that points simply exhibits axial (z-axis) motion. However, off-neutral plane points also have an azimuthal (ϕ-axis) component of motion. This azimuthal motion of the surface points propels the rotor.

Ultrasonic motors require a power electronic drive. A power electronic circuit suitable for driving an ultrasonic motor is shown in Fig. 31.7. The two H bridges are controlled to generate waveforms that are 90° out of phase with each other.

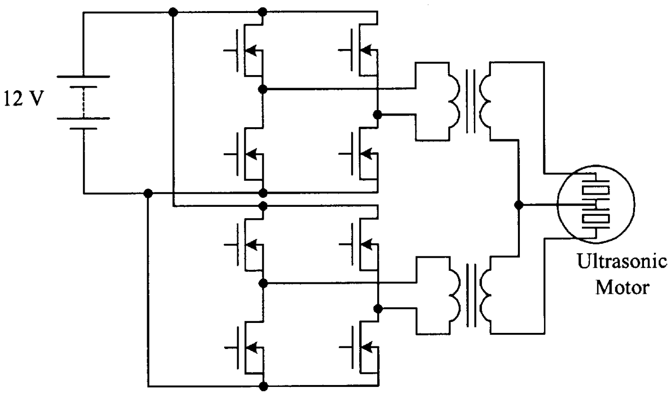


FIGURE 31.7 Drive circuit for an ultrasonic motor.

31.4.4 Electromechanical Engine Valves

Electromagnetic actuators are finding increasing application in automotive systems. These actuators are more desirable than other types of actuators, such as hydraulic and pneumatic actuators, because they can be more easily controlled by a microprocessor to provide more precise control. An application of electromagnetic actuators that is of particular interest is the replacement of the camshaft and tappet valve assembly by electromechanically driven engine valves [25]. The opening and closing of the intake and exhaust valves can be controlled to achieve optimum engine performance and improved fuel economy over a wide range of conditions determined by variables such as the speed, load, altitude and temperature.

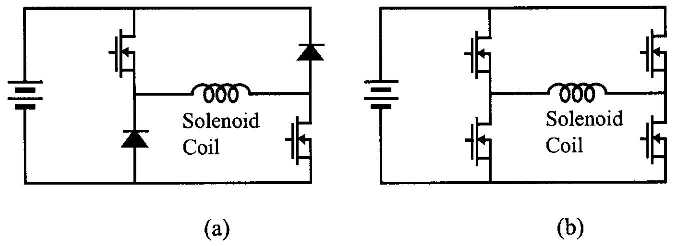


FIGURE 31.8 Power electronic circuits for driving solenoids.

The present cam system provides a valve profile that can give optimum engine performance and improved fuel economy only under certain conditions.

Two power electronic circuits suitable for driving the solenoids for valve actuation are shown in Fig. 31.8. The circuit of Fig. 31.8(a) is suitable for solenoids that require unidirectional currents through their coils, while the circuit of Fig. 31.8(b) is suitable for solenoids that require bidirectional currents through their coils.

31.4.5 Electric Air Conditioner

It is desirable to replace some of the engine-driven functions of a vehicle with electrically driven counterparts. The benefits of driving these functions electrically include the elimination of belts and pulleys, improved design and control due to independence from engine speed, and resulting increased efficiency and improved fuel economy. Furthermore, there is the opportunity for operation of the function in the engine-off condition.

The air conditioner is an example of an engine-driven function that could benefit from electrification. The engine drives the compressor of the air conditioner. Consequently, the speed of the compressor varies over a wide range and the compressor has to be over-sized to provide the desired performance at engine idle. Also, since the compressor speed is dependent on the engine speed, excessive cooling occurs at highway speeds requiring the cool air to be blended with the hot air to keep the temperature at the desired level. Furthermore, shaft seals and rubber hoses can lead to the loss of refrigerant (CFC) and pose an environmental challenge.

In an electric air conditioner, an electric motor is used to drive the compressor [26]. The motor is usually a three-phase brushless dc motor driven by a three-phase MOSFET bridge. The speed of the compressor in an electric air conditioner is independent of the engine speed. As a result, the compressor does not have to be over-sized and excessive cooling does not occur. Also, shaft seals and hoses can be replaced with a hermetically sealed system. Another benefit of an electric air conditioner is the flexibility in its location, since it does not have to be driven by the engine.

31.4.6 Electric and Electro-Hydraulic Power Steering Systems

The hydraulic power steering system of a vehicle is another example of an engine-driven accessory. This system can be replaced with an electric power steering (EPS) system in which a brushless dc motor is used to provide the steering power assist [27]. The electric power steering system is more efficient than the hydraulic power steering system because, unlike the engine-driven hydraulic steering pump which is driven by the engine all of the time, the motor operates only on demand. Another system that can replace the hydraulic power steering system is the electro-hydraulic power steering (EHPS) system. In this case, a brushless dc motor and inverter can he employed to drive the hydraulic steering pump. The ability of the electro-hydraulic power steering system to drive the pump only on demand leads to energy savings of as much as 80% as compared with the conventional hydraulic system. Challenges in implementing EPS and EPHS systems include meeting the required levels of cost and reliability for this critical vehicle subsystem.

31.4.7 Motor Speed Control

Some of the motors used in a vehicle require variable speed control. Consider, as an example, the blower motor used to provide air flow to the passenger compartment. This motor is typically a permanent-magnet dc motor with a squirrel-cage fan. The speed of the motor is usually controlled by varying the resistance connected in series with the motor winding. This method of speed control leads to a significant power loss. A low-loss method of speed control employs semiconductor devices as shown in Fig. 31.9. In this case, the speed of the motor is controlled via pulse-width modulation (PWM) that is, by switching the MOSFET on and off with different duty ratios for different speed settings. An input filter is needed to reduce the EMI generated by the switching of the MOSFET. This method of speed control is equivalent to supplying power to the motor through a variable-output dc-to-dc converter. The converter is located close to the motor and no filter is required between the converter output and motor winding.

Another low-loss method that can be used to control the speed of a motor employs a three-phase brushless dc motor. The speed in this case is controlled by controlling the MOSFETs in the dc-to-three-phase-ac converter that drives the motor.

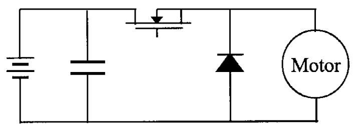
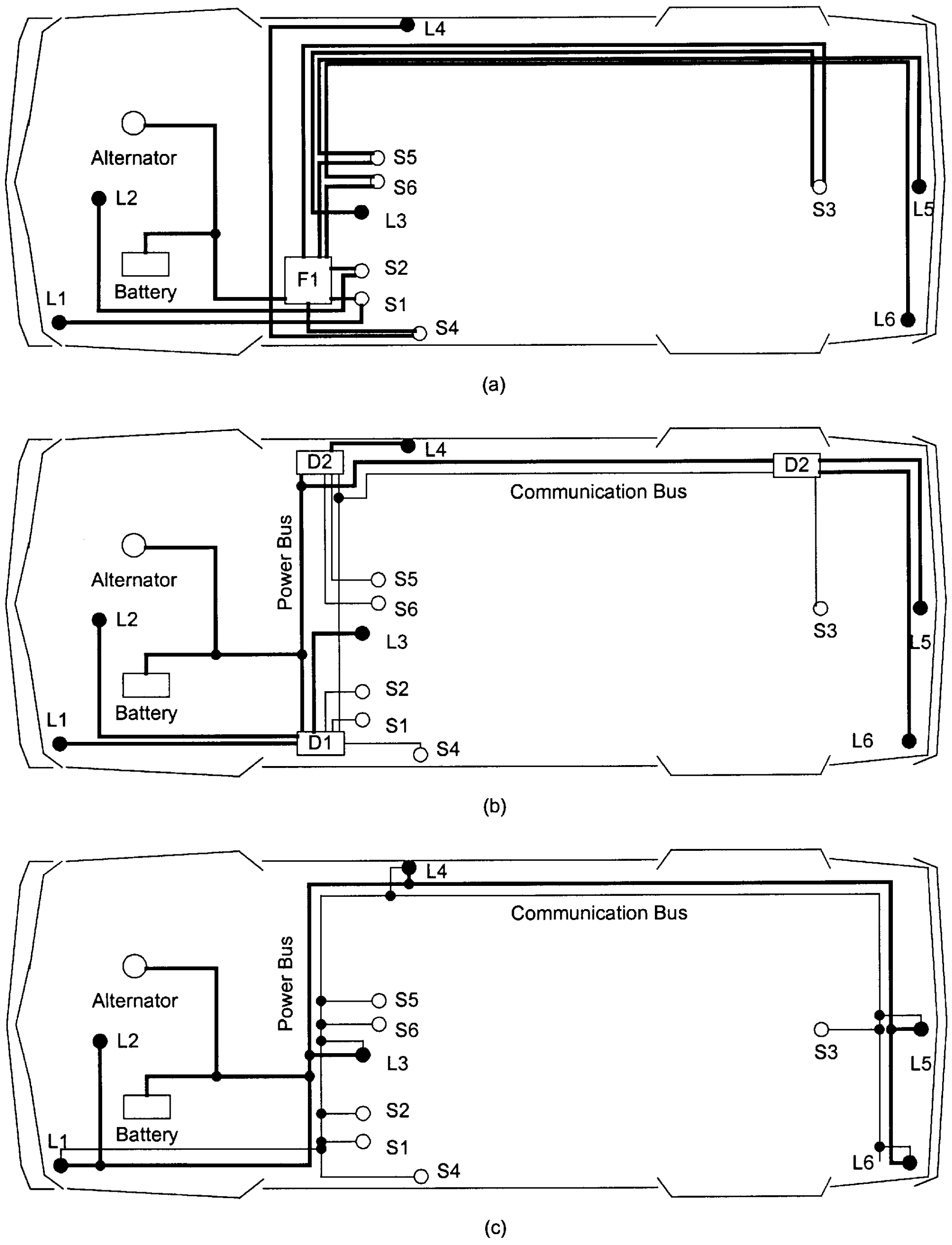


FIGURE 31.9 Low-loss circuit to control the speed of a motor.

31.5 Multiplexed Load Control

Another emerging application of power electronics in automobiles is in the area of load control. In the conventional point-to-point wiring architecture most of the loads are controlled directly by the primary mechanical switches, as shown in Fig. 31.1. In a point-to-point wiring architecture each load has a dedicated wire connecting it to the fuse box via the primary switch. Consequently fairly heavy wires have to be routed all over the vehicle, as illustrated in Fig. 31.10(a). The situation is made worse when multiple switches control the same load, as is the case with power windows and power door locks. The complete harness of a 1994 C-class Mercedes Benz that uses point-to-point wiring has about 1,000 wires, with a total length of 2 km, over 300 connectors and weighs 36 kg. The process of assembling the wiring harness is difficult and time consuming, leading to high labor costs. Retrofitting, fault tracing and repairing are time consuming and expensive. The



(a)

(b)

(c)

FIGURE 31.10 Alternative control strategies illustrated for a simple automotive electrical system with six loads (L1–6) and six primary switches (S1–6). (a) Conventional direct switching architecture with a single fusebox (F1), (b) multiplexed remote switching architecture, with remote switches and transceivers in three distribution boxes (D1–3), and (c) multiplexed point-of-load switching with electronics integrated into the loads and the primary switches.

bulky harness also places constraints on the vehicle body design, and the large number of connectors compromise system reliability.

An alternative wiring technique is to control the loads remotely and multiplex the control signals over a communication bus, as shown in Fig. 31.10(b) and (c). A control message is sent on the communication bus to switch a particular load on or off. This allows more flexibility in the layout of the power cables and could allow the preassembly of the harness to be more automated. Furthermore, with communication between the remote switches it is practical to have a power management system than can turn off nonessential loads when there is a power shortage. One possibility is to group the remote switches into strategically located distribution boxes, as shown in Fig. 31.10(b). A power and a communication bus connect the distribution boxes. Another possibility is to integrate the remote switches with the load, i.e. point-of-load switching, as shown in Fig. 31.10(c). In Fig. 31.10(b) the transceivers are also built into the distribution boxes, while in Fig. 31.10(c) each load and primary switch has an integrated transceiver. The point-of-load switching topology is attractive because of its simplicity, but raises cost and fusing challenges.

Multiplexed remote switching architectures have been under consideration since at least the early 1970s, when Ziomek investigated their application to various electrical subsystems [28]. The initial interest was dampened by cost and reliability concerns and the non-availability of appropriate remote switches. However, advances in semiconductor technology and rapid growth in the automotive electrical system revived interest in multiplexed architectures. The SAE Multiplexing Standards Committee has partitioned automotive communications into three classes: Class A for low data-rate (1–10 kbit/s) communication for the control of body functions, such as headlamps, windshield wipers and power windows, Class B for medium data-rate (10–100 kbit/s) parametric data exchange, and Class C for high data-rate (1 Mbit/s) real-time communication between safety critical functions, such as between ABS sensors and brake actuators [29]. Although load control is categorized as Class A, lack of any widely accepted Class A communication protocols has led to the application of Class B and Class C communication IC's to load control. Class B has received the most attention due to the California Air Resources Board mandated requirement for on-board diagnostics (OBD II) and a large number of competing protocols, including the French Vehicle-Area Network (VAN), ISO 9141 and SAE J1850, have been developed [30]. Of these the SAE J1850 is the most popular in the US. Another popular protocol is the Controller Area Network (CAN) developed by Bosch [31]. Although designed for Class C with bit rates up to 1 Mbit/s, it is being applied for Class A and Class B applications due to the availability of inexpensive CAN ICs from a large number of semiconductor manufacturers.

Remote switching systems require remote power switches. An ideal remote switch must have a low on-state voltage, be easy to drive from a microcontroller and incorporate current sensing. A low on-state voltage helps minimize the heatsinking requirements, while current sensing is needed for the circuit protection function to be incorporated into the switch. To withstand the harsh automotive environment the switch must also be rugged. Furthermore, if pulse width modulated (PWM) control is required for the load, the switch must have short turn-on and turn-off times and a high cycle life. The traditional means of remotely switching loads in an automobile is via electromechanical relays. Although relays offer the lowest voltage drop per unit cost, they require large drive current, are relatively large, are difficult to integrate with logic, and are not suitable for PWM applications [32, 33, 34]. Therefore, their use will be limited to very high current, non-PWM applications. The power levels of the individual loads in the automobile are too low for IGBTs and MCTs to be competitive. Bipolar transistors are also not very attractive because they are harder to drive than a MOS-gated device. Because of its fast switching speed, low voltage drop, relative immunity to thermal runaway, low drive requirements and ease of integration with logic, the power MOSFET is the most attractive candidate for remote switching. Smart-power MOSFET devices with integrated logic interface and circuit protection have recently become available. Use of these devices for power electronic control of individual loads has become economically competitive in some subsystems, and may be expected to become more so with the advent of higher-voltage electrical systems.

The benefits of remote switching electrical distribution systems have been demonstrated by Furuichi *et al.* [35]. The multiplexed architecture they implemented had 10 remote units (2 power units with fuses, power drivers and signal inputs, 5 load control units with power drivers and signal inputs but no fuses, and 3 signal input units with only signal inputs). To increase system reliability, each power unit was connected to the battery via independently fused power cables. Although wiring cost decreased, the authors report an increase

TABLE 31.5 Comparison of a multiplexed and the conventional system, as reported by Furuichi *et al.* for a compact vehicle [35]. In the multiplexed system the function of nine electronic control units (ECUs) was integrated into the remote units

	Point-to-Point	Multiplexed	Change ( )
Harness weight (kg)	14.0	9.8	−30
ECU weight (kg)	1.2	0.0	N/A
Remote unit weight (kg)	0.0	3.5	N/A
Total weight (kg)	15.2	13.3	−12.5
Number of wires	743	580	−21.9
Number of terminals	1195	915	−23.4
Number of splices	295	246	−16.6
Length of wire (m)	809	619	−23.5

in overall system cost due to the additional cost of the remote units. Intel's CAN ICs with data rates of 20 kbit/s were used for the transmission and reception of control signals over an unshielded twisted-pair ring bus. Intelligent power MOSFETs were used as the remote switches and fusing was done with minifuses. The results of their work are shown in Table 31.5. Although weight of the wiring harness was reduced by 30 . the total system weight decreased by only 12.5 due to the added weight of the remote units.

31.6 Electromechanical Power Conversion

Power is generated in the automobile by an electrical machine driven by the engine. In the early days of the automobile, the electrical load was small and a dc generator was used for this purpose. As the electrical loads grew, the dc generator could not meet the growing demand of electrical power and was displaced by a three-phase alternator and diode rectifier. Continuously increasing power and performance requirements are driving further evolution in automotive power generation and control, and are motivating the introduction of power electronics and improved electrical machines in automobiles. In addition to high-power alternators, future applications of electromechanical power conversion may include integrated starter/alternators and propulsion systems. This section describes some of the machine and power electronic technologies that are useful for meeting the increasing challenges in the automobile.

31.6.1 The Lundell Alternator

The Lundell, or claw-pole, alternator is a three-phase wound-field synchronous machine that is almost universally used for power generation in present-day vehicles [1]. As illustrated in Fig. 31.11, the rotor is made of a pair of stamped pole pieces ("claw poles") fixed around a cylindrical field coil. The field winding is driven from the stator via a pair of slip rings and brushes, and causes the two pole pieces to become opposing magnetic poles. A full-bridge diode rectifier is traditionally used at the machine output, and a fan mounted on the rotor is typically used to cool the whole assembly.

The dc output voltage of the alternator system is regulated by controlling the field current. A switching field regulator applies a pulse-width modulated voltage across the field. The steady-state field current is determined by the field winding resistance and the average voltage applied by the regulator. Changes in the field current occur with an L/R field winding time constant on the order of 100 ms or more. This long field-winding time constant and a large stator leakage reactance are characteristic of this type of alternator and tend to dominate its performance.

The alternator is driven by means of a belt, and is designed to operate over a wide speed ratio of about 10 : 1, though much of its operating lifetime is spent within a narrower 3 : 1 or 4 : 1 range. The gearing ratio provided by the belt is a design variable for the alternator; an alternator mechanical speed range from 1,800 rpm to 18,000 rpm for a 12-pole machine is typical.

A simple electrical model for the Lundell alternator is shown in Fig. 31.12. The armature of the alternator is modeled as a Y-connected set of leakage inductances L_s and back voltages v_{sa}, v_{sb}, and v_{sc}. The fundamental electrical frequency ω of the back emfs is one half of the product of the number of machine poles p and the mechanical speed ω_m. The magnitude of the back emfs is proportional to the electrical frequency and the field current. For the sinusoidal case, the line-to-neutral voltage back emf magnitude can be calculated as

$$V_s = k\omega i_f \tag{31.1}$$

where k is the machine constant and i_f is the field current. The diode bridge feeds a constant voltage V_0 representing the battery and other loads. This simple model captures many of the important characteristics of the Lundell alternator, while remaining analytically tractable. Other effects, such as stator

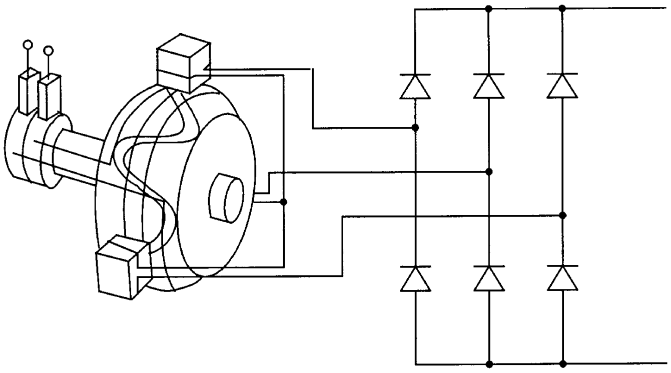


FIGURE 31.11 Structure and circuitry of the conventional Lundell alternator.

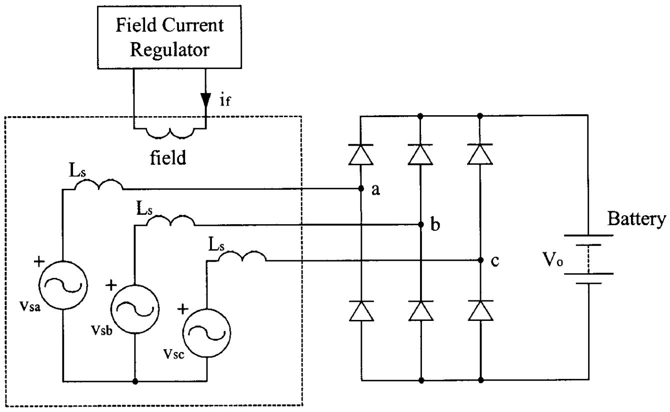


FIGURE 31.12 A simple Lundell alternator model.

resistance, mutual coupling, magnetic saturation and waveform harmonic content, can be incorporated into this model at the expense of simplicity. The constant-voltage battery load on the alternator makes the analysis of this system different from the classic case of a diode rectifier with a current-source load. Nevertheless, with reasonable approximations, the behavior of this system can be described analytically [8]. Using the results presented in [8], alternator output power vs. operating point can be calculated as

$$P_0 = \frac{3V_0\sqrt{V_s^2 - \frac{4V_0^2}{\pi^2}}}{\pi\omega L_s} \tag{31.2}$$

where V_0 is the output voltage, V_s is the back emf magnitude, ω is the electrical frequency, and L_s is the armature leakage inductance. Extensions of (31.2) that also include the effect of the stator resistance are given in [8].

As can be inferred from (31.2), alternator output power varies with speed, and is maximized when the back emf magnitude of the machine is substantially larger than the output voltage. In a typical Lundell alternator back voltages in excess of 80 V may be necessary to source rated current into a 14 V output at high speed. Furthermore, as can be seen from (31.2), the armature leakage reactance limits the output power capability of the alternator. These characteristics are a result of the fact that significant voltage drops occur across the leakage reactances when current is drawn from the machine. These drops increase with speed and current, and cause the alternator to exhibit significant droop in output voltage with increasing current. Thus, an appropriate dc-side model for a Lundell alternator is a large open-circuit voltage (related to the back emf magnitude) in series with a large current and speed dependent output impedance. This characteristic, coupled with the long field time constant, is the source of the undesirable load-dump transient characteristic of the Lundell alternator. In this transient the large open-circuit voltage is transiently impressed across the alternator output when the load is suddenly reduced.

The efficiency of the conventional Lundell alternator is relatively poor. Typical efficiency values are of the order of 40–60%, depending on operating point [1, 36, 37]. At low and medium speeds, losses tend to be dominated by stator copper losses. Iron losses become dominant only at very high speeds [1].

31.6.2 Advanced Lundell Alternator Design Techniques

The conventional diode-rectified Lundell alternator, though inefficient, has so far met vehicle electrical power requirements in a cost-effective manner. However, continuing increase in electrical power demand and growing interest in improved fuel economy is pushing the limits of conventional Lundell alternator technology. This section describes some established and some emerging technologies that can be used to improve the performance of the Lundell alternator.

31.6.2.1 Third Harmonic Booster Diodes

One widely used approach for improving the high-speed output power capability of Lundell alternators is the introduction of third-harmonic booster diodes [1]. In this technique, the neutral point of the Y-connected stator winding is coupled to the output via a fourth diode leg, as illustrated in Fig. 31.13. While the fundamental components of the line-to-neutral back voltages are displaced by 120° in phase, any third harmonic components will be exactly in phase. As a result, third harmonic energy can be drawn from the alternator and transferred to the output by inducing and rectifying common-mode third harmonic currents through the three windings. The booster diodes provide a means for achieving this. At high speed, the combination of the third harmonic voltages at the

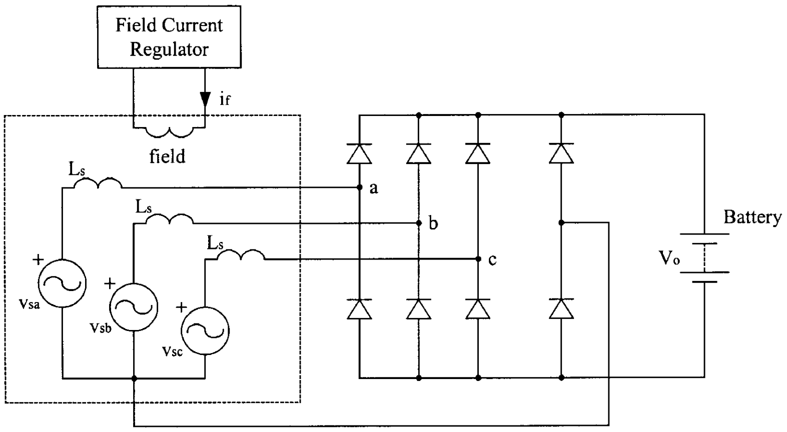


FIGURE 31.13 Lundell alternator with booster diodes.

main rectifier bridge (at nodes a, b, and c in Fig. 31.13), combined with the third harmonic of the back voltages, are large enough to forward bias the booster diodes and deliver third harmonic energy to the output. In systems with significant (e.g. 10) third harmonic voltage content, up to 10 additional output power can be delivered at high speed. Additional power is not achieved at low speed, or in cases where the third harmonic of the back voltage is small.

31.6.2.2 Lundell Alternator with Permanent Magnets

The structure of the rotor of the claw-pole alternator is such that the leakage flux is high. This reduces the output current capability of the alternator. The leakage flux can be reduced by placing permanent magnets on the pole faces or in the spaces between the adjacent poles of the rotor. This modification allows the alternator to deliver more output current. Placing the magnets in the spaces between adjacent poles is a better approach because it is simpler to implement and leads to a higher output current at engine idle [38].

31.6.2.3 Twin-Rotor Lundell Alternator

The maximum power capability of the Lundell alternator is limited in part by the limit on its length-to-diameter ratio imposed by mechanical stresses on the stamped pole pieces. This prevents the Lundell alternator from being arbitrarily scaled up in size. The power capability of conventional designs is probably limited to 3 kW, which is likely to be unacceptable in the foreseeable future [39]. One way to retain the cost-effectiveness of the claw-pole alternator while achieving higher output power is to place two claw-pole rotors back-to-back on a common shaft inside a common stator [40]. This effectively increases the length of the claw-pole alternator without changing its diameter. This design allows higher power alternators to be built while retaining most of the cost benefits of the claw-pole design.

31.6.2.4 Power Electronic Control

Another approach for improving the output power and efficiency of the Lundell alternator is through the use of more sophisticated power electronics. Power electronics technology offers tremendous value in this application. For example, replacing the conventional diode rectifier with a switched-mode rectifier provides an additional degree of design and control freedom, and allows substantially higher levels of power and efficiency to be attained from a given machine. One such design is shown in Fig. 31.14. It employs a simple switched-mode rectifier along with a special load-matching control technique to achieve dramatic improvement in alternator output power, efficiency, and transient performance [37]. The switched-mode rectifier provides improved control without the cost and complexity of a full active converter bridge. By controlling the duty ratio of the switched-mode rectifier based on available signals such as alternator speed, the alternator output power characteristic (31.2) can be altered and improved, particularly for speeds above idle [37]. Improvements in average power capability of a factor of two and average efficiency improvements on the order of 20 are possible with this technology. Furthermore, the switched-mode rectifier can be employed to achieve greatly improved load-dump transient control.

31.6.3 Alternative Machines and Power Electronics

The demand for increased alternator power levels, efficiency, and performance also motivates the consideration of alternative electrical machines, power electronics, and design approaches. While no alternative machine has yet displaced the Lundell alternator in production vehicles, primarily due to cost considerations, some potential candidates are reviewed in this section. These include machines that are mounted directly on the engine rather than driven from a belt. These direct drive machines become important as power levels rise. This

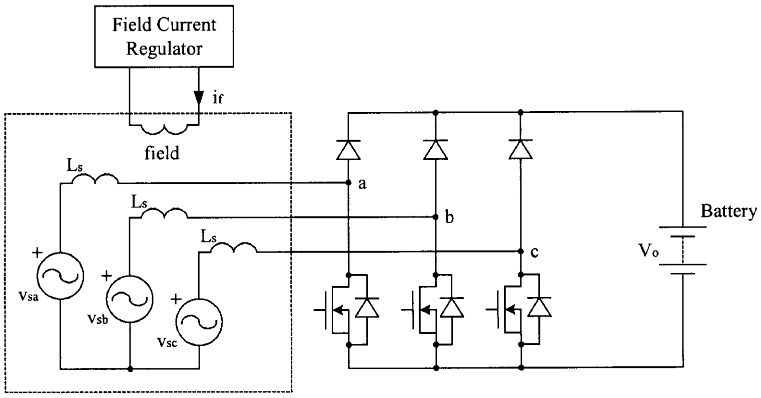


FIGURE 31.14 Lundell alternator with a switched-mode rectifier.

section also addresses the more general case of the combined starter/alternator. While the use of a single machine to do both starting and generation functions is clearly possible, a separate (transient-rated) dc machine is presently used for starting. This is because the large mismatch in starting and generating requirements has made the combined starter/alternator approach unattractive. However, as alternator power ratings increase the mismatch is reduced, and a single starter/alternator system becomes more practical. A combined system has the potential to eliminate the need for a separate flywheel, starter, solenoid switch, and pinion engaging drive. It also has the potential to allow regenerative braking and "light hybrid" operation, and to provide idle-stop capability (i.e. the ability to turn off the engine when the vehicle is stopped and seamlessly restart when the vehicle needs to move) for reduced fuel consumption. A move to this more sophisticated approach relies upon advanced electrical machines and power electronics.

31.6.3.1 Synchronous Machine with a Cylindrical Wound Rotor

The claw-pole rotor can be replaced with a cylindrical rotor to achieve better coupling between the stator and rotor. The cylindrical rotor is made from steel laminations and the field winding is placed in the rotor slots. The cylindrical rotor is similar to the armature of a dc machine except that the connection of the field winding to the external circuit is made through slip rings instead of a commutator. The cylindrical rotor structure leads to quiet operation and increased output power and efficiency. Unlike the claw-pole alternator, the length of the machine can be increased to get higher output power at a higher efficiency. The efficiency is higher since the effect of the end windings on the machine performance is less in a machine with a long length. It is also possible to build the machine with a salient-pole rotor instead of a cylindrical rotor. However, a machine with a salient-pole rotor is likely to produce more noise than a machine with a cylindrical rotor.

A machine with a cylindrical wound rotor has similar power electronics and control options as a claw-pole machine. If generation-only operation is required, a diode bridge and field current control is sufficient to regulate the output voltage. Better performance can be achieved by using a switched-mode rectifier in conjunction with field control [37]. If motoring operation is desired (e.g. for starting), or even better performance is desired, a full-bridge (active-switch) converter can be used, as shown in Fig. 31.15. Since this is a synchronous machine some form of rotor position sensing or estimation is typically necessary. The full bridge converter allows maximum performance and flexibility but carries a significant cost penalty.

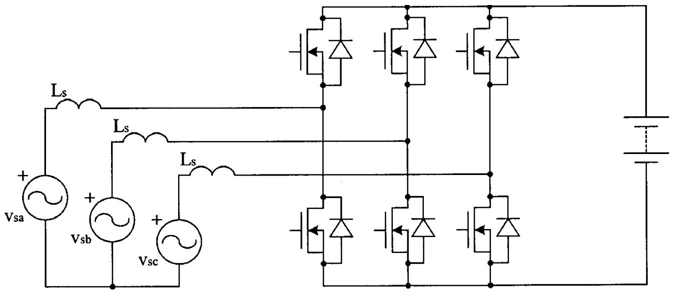


FIGURE 31.15 Model of an alternator with full bridge converter.

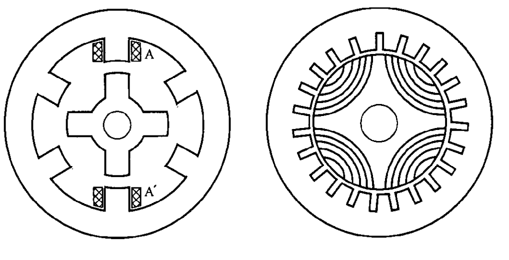
31.6.3.2 Induction Machine

The stator of a three-phase induction machine is similar to that of a three-phase synchronous machine. The rotor is either a squirrel-cage or wound rotor. The machine with the squirrel-cage rotor is simpler in construction and more robust than the machine with a wound rotor in which the three-phase rotor winding is brought outside the rotor through slip rings. The rotor is cylindrical and is constructed from steel laminations. It is also possible to use a solid rotor instead of a laminated rotor. However, a solid rotor leads to higher losses as compared with a laminated rotor. The losses in a solid rotor can be reduced by cutting slots in the rotor surface, filling the stator slot openings with magnetic wedges to reduce the field ripple, and placing a copper cage on the rotor.

An induction machine requires a source that can provide the leading reactive power to magnetize the air gap. This means that a three-phase induction generator cannot supply power to a load through a three-phase diode bridge. Capacitor supply of the reactive energy is impractical because of the wide operating speed range. In the most general case (in which both motoring and generating operation can be achieved) a three-phase active bridge can be used. If only generating operation is desired, the power to the load can be supplied through a three-phase diode bridge and the reactive power can be obtained from a small three-phase active bridge provided for this purpose. This design requires a large number of devices and complex control.

31.6.3.3 Reluctance Machines

The switched reluctance machine is a doubly salient machine. Both the stator and rotor of the machine are made from steel laminations to reduce the iron losses. Only the stator carries windings; the rotor is constructed of steel laminations with a salient shape. The structure of a three-phase switched reluctance machine with six stator poles and four rotor poles is shown in Fig. 31.16(a). A winding placed on diametrically opposite stator poles forms a phase winding. When a phase of the machine is excited, a pair of rotor poles tends to align with the excited stator poles to provide a path of minimum reluctance. If the rotor is moving towards alignment with the excited pair of stator poles, then the machine develops a



(a) (b)

FIGURE 31.16 Structures of (a) switched reluctance and (b) synchronous reluctance machines. AA′ represents phase A winding.

positive torque and acts as a motor. If the rotor is moving away from the excited pair of stator poles, then the machine develops a negative torque and acts as a generator. The advantages of the switched reluctance machine include simple construction, fault-tolerant power electronic circuit, high reliability, unidirectional phase currents and low cost. The drawbacks of the machine include high levels of torque ripple, vibration and acoustic noise, and a relatively high power electronics cost.

The synchronous reluctance machine is a singly salient machine. The stator of the machine is similar to that of a synchronous or induction machine. The rotor has a segmented structure with each segment consisting of a stack of axially-laminated steel sheets sandwiched with a non-magnetic material. The structure of a four-pole synchronous reluctance machine is shown in Fig. 31.16(b). A synchronous reluctance machine has less torque ripple, lower losses and higher power density than a comparable switched reluctance machine. Inclusion of permanent magnets in the rotor structure allows both reluctance and magnet torque to be achieved. Such Interior Permanent Magnet (IPM) machines can achieve very high performance and power density. When permanent magnets are included, however, careful attention must be paid to the effects of shutdown of the power electronics as an uncontrolled back emf component will exist in this case [41].

The switched reluctance machine, like the induction machine, requires an external source to magnetize the air gap. Several circuits are available to excite the switched reluctance machine. A circuit that is suitable for the automotive application of this machine is shown in Fig. 31.17. A phase leg is needed for each stator phase of the machine. In this case, the switched reluctance machine obtains its excitation from the same bus that it generates into. Unlike the synchronous and induction machines in which the number of wires needed to connect the machines to the power converters is usually equal to the number of phases, the number of wires needed to connect the switched reluctance machine to a converter is equal to twice the number of phases. This is of no particular concern in a switched reluctance machine in which the power converter is integrated with the machine in the same housing. The synchronous reluctance machine also requires an external source to magnetize the air gap. The machine usually employs an active bridge similar to the one used with an induction machine for the desired power conversion. The machine can also employ the converters used with the switched reluctance machine. In this case, the currents through the stator windings are unidirectional. The relative complexity of the power electronics is a disadvantage of these machine types in the case where only generator operation is necessary.

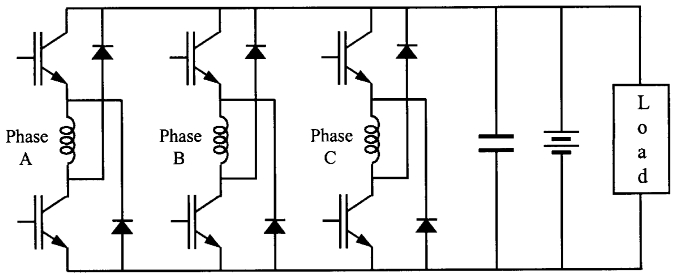


FIGURE 31.17 Circuit for a switched reluctance machine.

31.6.3.4 Permanent-Magnet and ybrid Synchronous Machines

The permanent-magnet synchronous machine designed with high-energy rare-earth magnets operates with high efficiency, high power density, low rotor inertia and low acoustic noise. The excitation from the permanent magnets is fixed and, therefore, the regulation of the output voltage of the machine is not as straightforward as in a synchronous machine with a wound rotor. For generator operation, machines of this type can use switched-mode rectifiers to regulate the output voltage [42, 43]. The boost rectifier of Fig. 31.14 is one possible implementation of this approach. Alternatively, a diode rectifier followed by a dc/dc converter can be used to regulate the generator system output [44]. Another method proposed for this type of system involves the use of tapped windings and two three-phase SCR bridges [45]. The taps on the phase windings are connected to one bridge, while full phase windings are connected to the other bridge. The bridge connected to the full phase windings is used to supply power to the dc bus at low engine speeds, while the converter connected to the taps is used at high speed. The use of a tapped winding and dual bridges helps the system cope with the wide speed range of the alternator and limit the losses associated with the pulsating output currents. In the case when both motoring and generating modes are desired, a full-bridge converter can be used. Again, as this is a synchronous machine, some form of position sensing or estimation is necessary. Also, in all of these systems the effects of failure of the power electronics must be carefully considered as there is no possibility of regulating the back voltages by field control.

Attempts to develop a simpler voltage regulation scheme for permanent-magnet synchronous machines have led to a permanent-magnet/wound-rotor hybrid synchronous machine in which the rotor consists of two parts: a part with permanent magnets and a part with a field winding [46]. The two parts are placed next to each other on a common shaft. The rotor with the field winding can employ claw-pole, salient-pole, or cylindrical structure. The field current generates a flux that is used to either aid or oppose the permanent magnet flux and regulate the output voltage of the machine. One possible failure mode of this approach that can lead to catastrophic failure is if the field winding breaks while the machine is operating at high speed. In this case, the generated output voltage will become large and uncontrolled. Some means of mechanically disconnecting the alternator at the input or electrically disconnecting it at the output may be necessary to limit the impact of this failure mode.

31.6.3.5 Axial-Airgap Machines

The principle of operation of an axial-air gap, or axial-flux, machine is the same as that of a radial-airgap machine. An axial-airgap machine is characterized by a short axial length and large diameter. The structure of an axial-airgap permanent-magnet machine with surface magnets is shown in Fig. 31.18 [47]. The stator of the machine can be slotless or slotted. Two different magnetic circuit configurations are possible. In the NN configuration, the magnetic polarities in one pole pitch on both sides of stator are the same so that there are two main fluxes with symmetrical distribution through the stator. In this case, the conductors can be wound into two back-to-back stator slots to make one coil. The machine has a large stator yoke dimension because the flux passes through the yoke, but less copper loss because of short end windings. In the NS configuration, the magnetic polarities in one pole pitch on the opposite sides of stator are the opposite of each other so that there is only one main axial flux through the stator. In this case, the stator yoke dimension is small, but the end windings are long because the direction of current in the back-to-back stator slots is the same. The iron losses are small due to small yoke dimension and the copper losses are high because of long end windings. Heat removal is more challenging due to small stator dimensions. The structure shown in Fig. 31.18 is that of an axial-airgap permanent-magnet machine with surface magnets. In an axial-airgap machine with interior permanent magnets, the magnets are embedded in the steel of the rotor.

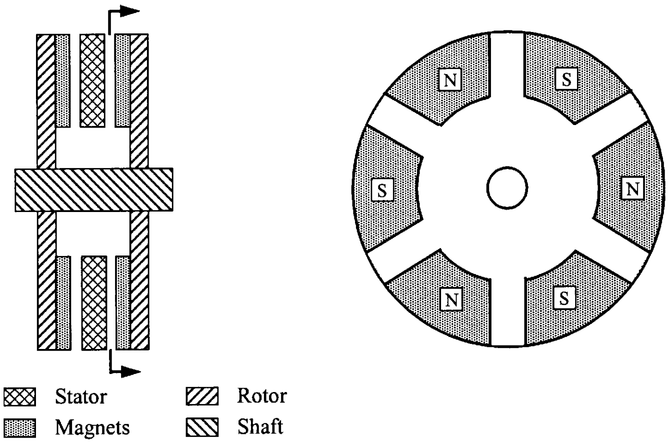


FIGURE 31.18 Structure of an axial-airgap permanent-magnet machine.

The axial-air gap versions of other types of machines, such as the induction and switched reluctance machines, are also possible. The structure of an axial-air gap induction machine is similar to that of an axial-airgap permanent-magnet machine except that windings are used instead of permanent magnets,

31.7 Dual/High-Voltage Automotive Electrical Systems

The electrical system of a 1920s internal-combustion-engine (ICE) automobile had only a few loads: a starter, an ignition device, a horn, and some lamps [48]. The mean power consumption of these loads was less than 100 W. An engine driven dc generator charged a 6 V lead–acid battery that provided electrical power. The power was distributed via point-to-point wiring, with most loads controlled directly by manually operated primary switches located within reach of the driver. Only the starter was switched indirectly by an electromechanical relay. After the Second World War, the automotive electrical system started to grow rapidly in complexity and power consumption as additional features, including radios, multispeed windshield wipers and power windows, were added. The introduction of higher compression engines stretched the 6 V system beyond its technological limits. The 8.5 to 1 compression ratio engines required 100–200 greater ignition voltages than the 6.4 to 1 engines. As a result, the primary side current of the ignition coil was doubled or tripled and the life of the distributor contacts was reduced to an unacceptable level. To overcome this problem the battery voltage was increased to 12 V in the mid-1950s [49, 50].

Over the past four decades the electrical power requirements of automobiles have increased even more rapidly. From a mere 400 W in 1955, the power rating of a luxury vehicle's generator has increased to over 1,800 W [51, 52]. However, the electrical system of a modern automobile is architecturally identical to the 12 V point-to-point system of the 1950s. The only changes that have taken place have been at the component level, such as the replacement of the dc generator by a three-phase alternator-rectifier, the replacement of wound-field dc motors by permanent-magnet ones, and an increased use of relays. The rapid growth in the electrical system is expected to continue due to environmental regulations, consumer demand for increased functionality, safety, security, and comfort, and replacement of some mechanical actuators by electrical counterparts. The average electrical power requirement of a modern luxury vehicle is about 800 W. With the addition of such loads as electric power steering, engine-cooling fan, water pump and electro-mechanical engine valves, the average power requirement could increase to 2.5 kW by 2005 [53]. The traditional solution of increasing the size of the alternator and the battery is not practical due to space limitations and fuel efficiency requirements. Furthermore, the peak power requirements of some of the anticipated loads heated windshield (2.5 kW), heated catalyst (3 kW), electro-mechanical engine valves (2.4 kW at 3,000 rpm) and active suspension (12 kW) cannot be met economically using the present architecture. These factors have motivated the development of new dual/high-voltage electrical architectures that incorporate a higher-voltage bus in addition to the standard 14 V bus [39, 54–56]. A dual/high-voltage approach allows an efficient supply of power to many loads which benefit from operating at a higher voltage, while retaining the 14 V bus for loads (such as lamps and electronics) which do not benefit from a higher voltage. High-voltage architectures that do not retain the 14 V bus are also possible, but will require a substantial investment in the design and production of new high voltage components. This section describes some of the characteristics and preliminary specifications of the new dual/high voltage electrical system architectures. It also discusses the some widely considered implementation approaches.

31.7.1 Trends Driving System Evolution

The conventional 12 V automotive electrical power system has many defects, including a widely varying steady-state system voltage and large transients, which force the electrical functions to be over-designed. However, these limitations alone have not been a strong enough driver for automotive companies to seriously evaluate advanced alternatives. Now a number of new factors are changing this situation. The most important of these are future load requirements that cannot be met by the present 12 V architecture.

31.7.1.1 Future Load Requirements

Table 31.6 gives a list of electrical loads expected to be introduced into automobiles in the next 10 years [53]. Some of these loads (electro-hydraulic power steering, electric engine fan, electric water pump and electro-mechanical valves) will replace existing mechanically or hydraulically driven loads. The remaining are new loads introduced to either meet government mandates or satisfy customer needs.

The average electrical power requirement of a present day automobile is in the 500 to 900 W range, depending on whether it is an entry level or a luxury vehicle. When the loads of Table 31.6 are introduced the average electrical power requirement will increase by 1.8 kW. Furthermore, if the air-conditioning (A/C) pump were ever to become electrically driven, the peak and average power demands would increase by an additional 3.5 kW and 1.5 kW, respectively. Distributing such high power at a relatively low voltage will result in unacceptably bulky wiring harnesses and large distribution losses. Since the alternator has to generate both the power consumed by the loads and the power dissipated in the distribution network, its output rating (and hence size and power consumption) will be greater than in an architecture with lower distribution losses. With the large premium attached to the size of the alternator (due to space constraints in the engine compartment), an architectural change in the distribution and generation systems is essential before many of the future loads can be introduced.

TABLE 31.6 Electrical loads expected to be introduced into automobiles in the next decade [53]

Load	Peak Power (W)	Average Power (W)
Exhaust air pump	300	10
Electro-hydraulic power steering	1,000	150
Electric engine fan	800	150
Heated catalytic converter	3,000	90
Electric water pump	300	150
Heated windshield	2,500	120
Electro-mechanical engine valves (6 cylinders at 6000 rpm)	2,400	800
Active suspension	12,000	360
Total		1,830

There is also an increasing disparity in the voltage requirements of future electrical loads. High pulse-power loads, such as the heated windshield and electrically heated catalytic converter, become feasible only at voltages greater than the current 14 V [57]. On the other hand, incandescent lamps and electronic control units (ECUs) will continue to require low voltages. For example, present day ECUs have linear regulators which convert the 14 V distribution voltage to the 5 V needed by the integrated circuits. The efficiency of these regulators is equal to the ratio of output to input voltage, i.e. 35 . Furthermore, the next generation of higher-speed lower power consumption integrated circuits operate at 3.3 V, making the regulators more inefficient. This inefficiency also means that larger heat sinks are required to remove the heat from the ECUs.

31.7.1.2 Higher Fuel Efficiency

A secondary motivating factor for the introduction of a higher system voltage is the challenge of achieving higher fuel economy. The average fuel economy of present day automobiles in the United States is in the vicinity of 30 miles per gallon (mpg). There is little market incentive for automobile manufacturers to increase the fuel economy of vehicles for the US market where the price of fuel is relatively low. The price of gasoline in the US (1.70 per gallon) is less than the price of bottled water (4.00 per gallon when bought by the quart). Although market forces have not been a driver for the development of fuel-efficient vehicles, a number of new incentives have emerged over the past few years. One of these is the fine imposed on the automakers by the US government if the average fuel economy of their fleet falls below the mandated standard. The mandated standard for cars has increased from 24 mpg in 1982 to its 1997 level of 27.5 mpg, and will continue to increase. In Europe, the German Automotive Industry Association (VDA) plans to increase the average fleet fuel efficiency to 39.9 mpg by 2005, compared to 31.4 mpg in 1990 [58].

Another driver behind the development of fuel-efficient vehicles is the Partnership for a New Generation of Vehicles (PNGV). This ten-year research program, launched in September 1993, is a collaboration between the US federal government and the big three US automakers (General Motors, Ford and DaimlerChrysler) that aims to strengthen national competitiveness in the automotive industry and reduce dependence on foreign oil. The PNGV has set a goal to develop an 80 mpg midsize vehicle by 2004 [59]. The German Automotive Industry Association is pursuing similar targets. This is complemented by the introduction of highly fuel-efficient vehicles (in excess of 50 mpg) by Toyota and Honda in both the Japanese and American markets.

With the present alternator, 800 W of electrical power consumes 1.33 L of gasoline for every 100 km driven when the vehicle has an average speed of 33.7 km/h. This represents a 45 increase in fuel consumption for a 3 L/100 km vehicle. Hence, if future high fuel economy vehicles are going to have comfort, convenience, and safety features comparable to present day vehicles, the efficiency of the electrical generation and distribution system will have to be substantially improved. Furthermore, as discussed in Section 31.8, one widely considered means of achieving high fuel economy is the use of a hybrid vehicle architecture. In practice, this approach necessitates the introduction of a higher voltage in the vehicle.

31.7.2 Voltage Specifications

A major issue when implementing a high- or dual-voltage system is the nominal voltage of the high-voltage bus, and the operating limits of both busses. While there are many possibilities, there is a growing consensus in the automotive industry for a nominal voltage of 42 V for the high-voltage bus (corresponding to a 36 V lead–acid storage battery) [39, 56, 60]. This voltage is gaining acceptance because it is as high as possible while remaining within acceptable safety limits for open wiring systems (once headroom is added for transients) and it provides substantial benefits in the power semiconductors and wiring harness [61]. Furthermore, this voltage is sufficient to implement starter/alternator systems and "light" hybrid vehicle designs [62, 63]. While no vehicles equipped at 42 V are in production at present, availability of 42 V components is rapidly increasing and 42 V-equipped vehicles may be expected early in this decade.

The permissible static and transient voltage ranges in an electrical system are important design considerations for power electronic equipment. At present, no universally accepted specification exists for high or dual voltage automotive electrical systems. However, the preliminary specifications proposed by the European automotive working group, *Forum Bordnetz*, are under wide consideration by the automotive industry [56]. These specifications, summarized in Table 31.7, impose tight static and transient limits on both the 42 and 14 V buses. The upper voltage limit on the 14 V bus is far lower than in the conventional 12 V system. The allowed upper limit on the 42 V bus is also proportionally tight. These strict limits facilitate the use of power semiconductor devices such as power MOSFETs and lower the cost of the protection circuitry needed in individual functions. However, they also require much more sophisticated means for limiting transients (such as load dump) than is found in conventional systems, which imposes a significant cost. Appropriate voltage range specifications for dual/high-voltage electrical systems are thus a subject of ongoing investigation by vehicle manufacturers, and will likely continue to evolve for some time.

TABLE 31.7 Volatage limits for 14 V and 42 V buses proposed in [56].

Voltage	Description	Value
$V_{42,\text{OV-dyn}}$	Maximum dynamic overvoltage on 42 V bus during fault conditions	55 V
$V_{42,\text{OV-stat}}$	Maximum static overvoltage on 42 V bus	52 V
$V_{42,\text{E-max}}$	Maximum operating voltage of 42 V bus while engine is running	43 V
$V_{42,\text{E-nom}}$	Nominal operating voltage of 42 V bus while engine is running	41.4 V
$V_{42,\text{E-min}}$	Minimum operating voltage of 42 V bus while engine is running	33 V
$V_{42,\text{OP-min}}$	Minimum operating voltage on the 42 V bus. Also, lower limit operating voltage for all noncritical loads (i.e. loads not required for starting and safety)	33 V
$V_{42,\text{FS}}$	Failsafe minimum voltage: lower limit on operating voltage for all loads critical to starting and safety on the 42 V bus	25 V
$V_{14,\text{OV-dyn}}$	Maximum dynamic overvoltage on 14 V bus during fault conditions	20 V
$V_{14,\text{OV-stat}}$	Maximum static overvoltage on 14 V bus	16 V
$V_{14,\text{E-max}}$	Maximum operating voltage of 14 V bus while engine is running	14.3 V
$V_{14,\text{E-nom}}$	Nominal operating voltage of 14 V bus while engine is running	13.8 V
$V_{14,\text{E-min}}$	Minimum operating voltage of 14 V bus while engine is running	12 V
$V_{14,\text{OP-min}}$	Minimum operating voltage of 14 V bus. Also lower limit operating voltage for all noncritical loads	11 V
$V_{14,\text{FS}}$	Failsafe minimum voltage: lower limit on operating voltage for all critical loads on the 14 V bus	9 V

31.7.3 Dual-Voltage Architectures

Conventional automotive electrical systems have a single alternator and battery. Dual-voltage electrical systems have two voltage busses and typically two batteries. Single-battery configurations are possible, but tend to be less cost effective [61]. A variety of different methods for generating and supplying energy to the two busses are under investigation in the automotive community. Many of these have power electronic circuits at their core. This section describes three dual-voltage electrical system architectures that have received broad attention. In all three cases the loads are assumed to be partitioned between the two buses with the starter and many of the other high-power loads on the 42 V bus and most of the lamps and electronics on the 14 V bus.

The dc/dc converter-based implementation of Fig. 31.19 is perhaps the most widely considered dual-voltage architecture. In this implementation, an alternator and associated battery provide energy to one bus (typically the 42 V bus), while the other bus is supplied via a dc/dc converter.

If a battery is used at the dc/dc converter output, the converter needs to be rated for slightly above average power. Otherwise, the converter needs to be rated a factor of two to three higher to meet peak power requirements [61]. The architecture of Fig. 31.19 has a number of advantages. The dc/dc converter provides high-bandwidth control of energy flow between the two busses, thus enabling better transient control on the 14 V bus than is available in present-day systems or in most other dual-voltage architectures. Furthermore, in systems with batteries on both buses, the dc/dc converter can be used to implement an energy management system so that generated energy is always put to best use. If the converter is bidirectional it can even be used to recharge the high-voltage (starter) battery from the low-voltage battery, thus providing a *self-jump-start* capability. The major challenge presented by this architecture is the implementation of dc/dc converters having the proper functionality within the tight cost constraints dictated by the automotive industry. Some aspects of design and optimization of converters for this application are addressed in [64].

The dual-stator alternator architecture of Fig. 31.20 is also often considered for dual-voltage automotive electrical systems [65, 66]. In this case, an alternator with two armature windings is used along with two rectifiers to provide energy to the buses and their respective batteries. Control of the bus voltages is achieved via a combination of controlled rectification and field control. Typically, field control is used to regulate one output, while the other output is regulated using a controlled rectifier. Figure 31.21 shows one possible implementation of this architecture. It should be noted that to achieve sufficient output power and power steering from the dual-wound alternator, the winding ratio between the two outputs must be carefully selected. For 42/14 V systems, a winding ratio of 2.5 : 1 is typical [66]. Advantages of this electrical architecture include low cost. However, it does not

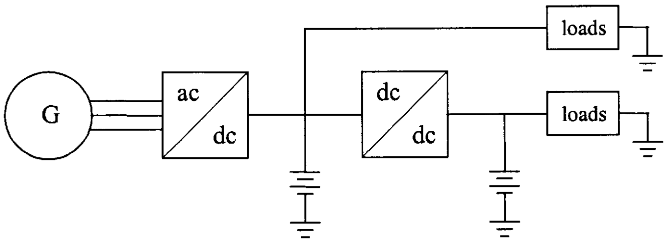


FIGURE 31.19 Dual-voltage architecture based on a dc/dc converter.

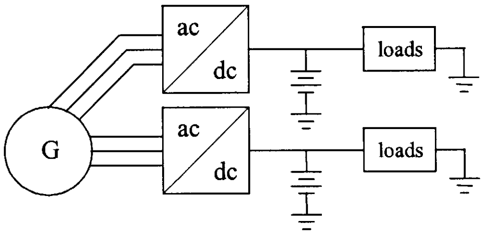


FIGURE 31.20 Dual-voltage architecture based on a dual-wound alternator.

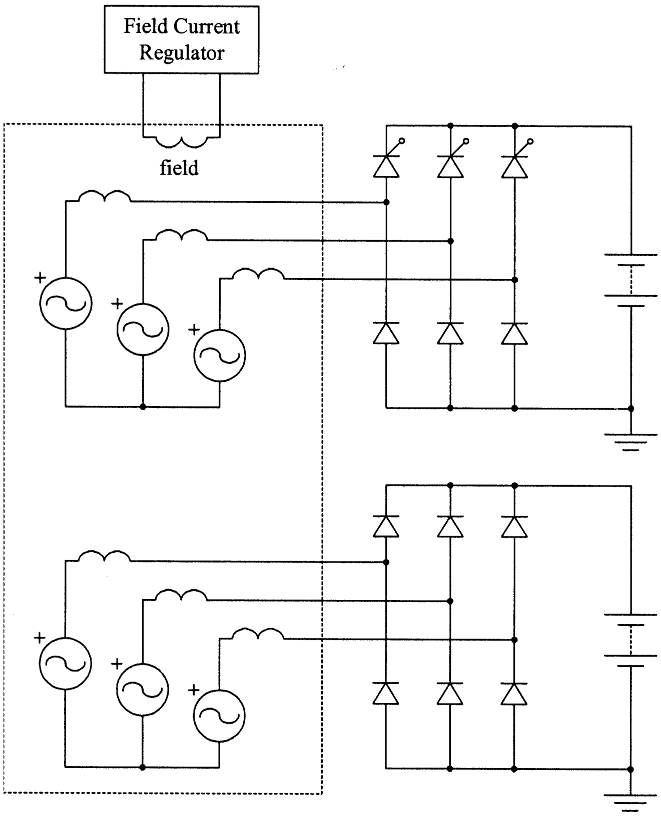


FIGURE 31.21 Model for a dual-wound alternator system. The two output voltages are regulated through field control and phase control. For a 42/14 V system, a winding ratio between the two stator windings of 2.5 : 1 is typical.

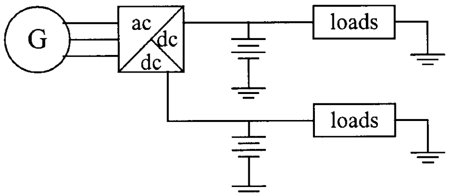


FIGURE 31.22 Dual-voltage architecture based on a dual-rectified alternator.

provide the bidirectional energy control that is possible in the dc/dc converter architecture. Furthermore, there are substantial issues of cross-regulation and transient control with this architecture that remain to be fully explored.

In a third architecture, a single-output alternator with a dual-output rectifier is employed. This approach is shown schematically in Fig. 31.22. As with the dual-stator alternator configuration, this architecture has the potential for low cost. One widely considered implementation of the dual-rectified alternator is shown in Fig. 31.23 [65, 67–69]. Despite its simplicity, this implementation approach provides less functionality than the dc/dc converter-based architecture, generates substantial low-frequency ripple which must be filtered, and has serious output power and control limitations [66]. An alternative implementation, proposed in [37] and shown in Fig. 31.24, seems to overcome these limitations, and may potentially provide the same capabilities as the dc/dc converter-based architecture at lower cost. Clearly, this architecture has promise for dual-voltage electrical systems, but remains to be fully explored.

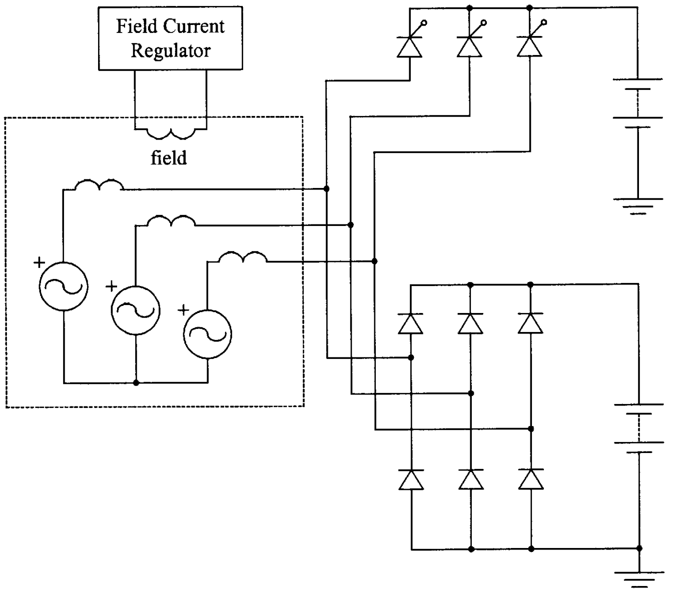


FIGURE 31.23 A dual-rectified alternator with a phase-controlled rectifier.

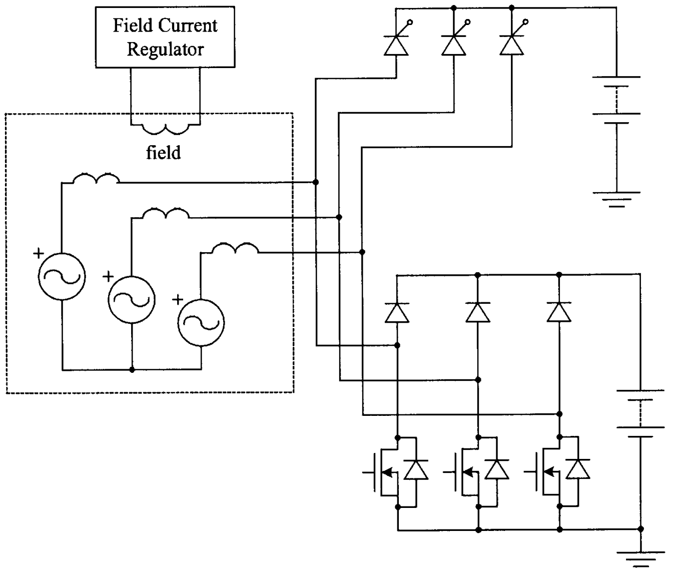


FIGURE 31.24 A dual-rectified alternator with a switched-mode rectifier.

31.8 Electric and Hybrid Electric Vehicles

Battery-powered electric vehicles were first introduced over one hundred years ago, and continue to incite great public interest because they do not generate tailpipe emissions. Nevertheless, the low energy storage density and the high cost of suitable batteries makes pure electric vehicles noncompetitive with internal combustion engine vehicles in most applications. An alternative approach that is generating widespread attention is the hybrid electric vehicle (HEV). An HEV combines electrical propulsion with another energy source, such as an internal combustion engine, allowing the traditional range and performance limitations of pure electric vehicles to be overcome [70]. Alternative energy sources, such as fuel cells, are also possible in place of an internal combustion engine.

Hybrid electric vehicles can be classified as having either a parallel or series driveline configuration [71]. In a series hybrid electric vehicle all of the propulsion force is produced from electricity; the engine is only used to drive a generator to produce electricity. In a parallel hybrid, propulsive force can come from either the engine or the electrical drive. In both cases, batteries or other electrical storage devices are used to buffer the instantaneous difference between the power needed for propulsion and that generated by the engine. The selection of a series or parallel driveline depends heavily on the performance requirements and mission of the vehicle.

In a series hybrid electric vehicle, all power delivered to the wheels of the vehicle must be delivered through the electrical driveline. The electrical driveline components, including the batteries, power electronics, and machine(s), must all be rated for the *peak* traction power requirements, making these components relatively large and expensive if performance (e.g. acceleration) comparable to a conventional vehicle is to be achieved. To achieve the required power levels, the electrical driveline must operate at hundreds of volts, necessitating the electrical subsystem to be sealed from access by the user. The engine, on the other hand, need only be rated to deliver the *average* power required by the vehicle, which is much lower. In a system that does not require utility recharge of the batteries (i.e. can drive indefinitely on fuel alone), the engine size is set by the power requirements of the vehicle at maximum cruising speed. If utility recharge of the batteries and a battery-limited driving range is acceptable, engine power requirements can be reduced even further. Because the engine does not provide tractive power, it can be designed to run at a single optimized condition, thus maximizing engine efficiency and minimizing emissions. Furthermore, the need for a transmission is eliminated and there is a great deal of flexibility in the engine placement.

In a parallel hybrid electric vehicle, traction power is split between the engine and the electrical driveline. One possible approach is to utilize a single machine mounted on the engine crankshaft to provide starting capability along with electrical traction power and regeneration [72–75]. This approach can be replaced or complemented with other approaches, such as use of a power-splitting device such as a planetary gear set [70, 76], or using different propulsion and generation techniques on different sets of wheels [71, 77, 78]. In all parallel hybrid approaches, some form of transmission is needed to limit the required speed range of the engine. A wide range of divisions between engine size and electrical system size is possible in the parallel hybrid case, depending on structure. Depending on this split, the necessary electrical driveline system voltage may be as low as 42 V (which is safe for an open wiring system) or as high as 300 V. Also because the electrical subsystem, the internal combustion engine subsystem, or both may provide tractive power under different conditions, there exists a wide range of possible operating approaches for a parallel hybrid system. Consequently, the control strategy for a parallel hybrid tends to be substantially more complex than for a series hybrid.

One parallel hybrid approach that is receiving a lot of attention for near-term vehicles is a "light" or "mild" hybrid. In this case, a somewhat conventional vehicle driveline is complemented with a relatively small starter/alternator machine mounted on the crankshaft [62, 63, 72–75, 79]. The electrical drive power is typically below 10 kW average and 20 kW peak. The starter/alternator can be used to provide rapid, clean restart of the vehicle so that the engine can be turned off at idling conditions and seamlessly restarted. This so-called "stop and go" operation of the engine is valuable for fuel economy and emissions. The starter/alternator can also be used to implement regenerative braking, to provide engine torque smoothing (replacing the flywheel and allowing different engine configurations to be used) and to provide boost power for short-term acceleration. At the low-power end, such systems can be integrated directly into the open wiring configuration of a 42 V electrical system, simplifying the vehicle electrical architecture. System level control remains a major challenge in realizing the full benefits of such systems. Starter/alternator-based hybrids are expected to be a significant near-term application of power electronics and machines in automobiles.

31. Summary

Power electronics is playing an increasingly important role in the automobile. It is being used to enhance the output power capability and efficiency of the electrical power generation components. Power electronics is also an enabling technology for a wide range of new and improved functions that enhance vehicle performance, safety, and functionality.

The design of automotive power electronic systems is strongly influenced by the challenging electrical and environmental conditions found in the automobile. Important factors include the static and transient voltage ranges, electromagnetic interference and compatibility requirements, and temperature and other environmental conditions. Some of the most important design considerations for automotive power electronics were addressed in Section 31.3.

Section 31.4 described some of the vehicle functions that benefit from, or are enabled by, power electronics. These functions range from lighting to actuation and steering. Power electronic switches also play a central role in multiplexed electrical distribution systems. This role of power electronics was addressed in Section 31.5.

The rapid increase in electrical power demand in automobiles is motivating the introduction of new technologies for electrical power generation and control. Lundell alternators are presently used for power generation in automobiles, but are rapidly reaching their power limits. Section 31.6 reviewed the operating characteristics of the Lundell alternator. It also described several techniques for extending the power capabilities of this machine. To meet the growing demand for electrical power, alternative machine and power electronic configurations may be necessary in the future. A number of candidate machine and power circuit configurations were reviewed in Section 31.6. Such configurations can also be applied towards the design of integrated starter/alternators and hybrid propulsion systems, as was discussed in Section 31.8.

The increasing electrical and electronic content of automobiles is beginning to stretch the capabilities of the conventional 12 V electrical system. Furthermore, there is a desire on the part of vehicle manufacturers to introduce new high-power loads, such as electromechanical engine valves, active suspension, and integrated starter/alternator. These are not likely to be practical within the present 12 V framework. These challenges are forcing the automotive industry to seriously consider high and dual voltage electrical systems. The ongoing developments in this area were reviewed in Section 31.7

The increasing electrical content of vehicles both underscores the need for power electronics and reflects the benefits of their introduction. It is safe to say that power electronics will continue to play an important role in the evolution of automobiles far into the future.

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32

Power Quality

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32.1 Introduction

Power electronics and power quality are irrevocably linked together as we strive to advance both broad areas. With the dramatic increases over the last 20 years in energy conversion systems utilizing power electronic devices, we have seen the emergence of "power quality" as a major field of power engineering. Simply put, power electronic technology has played a major role in creating "power quality," and simple control algorithm modifications to this same technology can often play an equally dominant role in enhancing overall quality of electrical energy available to end-users.

Power electronics has given us, as an industrial society, a plethora of new ways to manufacture products, provide services, and utilize energy. From a power quality impact viewpoint, applications such as

1. switched-mode power supplies,
2. dc arc furnaces,
3. electronic fluorescent lamp ballasts,
4. adjustable speed drives, and
5. flexible ac transmission components

are often cause for concern. From a utility supply system viewpoint, these converter-based systems can lead to operational and life expectancy problems for other equipment, possibly not owned or operated by the same party. It was from this initial perspective that the field of power quality emerged.

In most cases, the same devices and systems that create power quality problems can also be used to solve power quality problems. "Problem solving" applications such as

1. active harmonic filters,
2. static and adaptive var compensators, and
3. uninterruptable power supplies

all utilize the same switching device technology as the "problem causing" applications.

As the number of potentially problematic power electronic based loads has increased over time, so has attention given to enhanced converter control to maximize power quality. Perfect examples of these improvements include:

1. unity power factor converters,
2. dip-proof inverters, and
3. limited-distortion electronic lamp ballasts.

While these direct product enhancements are not mandatory in North America, today's global economy necessitates consideration of power quality standards and limits in order to conduct business in the European Union.

While many studies suggest increases in power electronic-based energy utilization as high as 70–80 (of all energy consumed), it is equally clear that we are beginning to realize the total benefit of such end-use technologies. Power quality problems associated with grounding, sags, harmonics, and transients will continue to increase because of the sheer number of sensitive electronic loads expected to be placed in

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service. At the same time, we are only now beginning to realize the total benefits that such loads can offer.

32.2 Power Quality

The term "power quality" means different things to different people. To utility suppliers, power quality initially referred to the quality of the service delivered as "measured" by the consumer's ability to use the energy delivered in the desired manner. This conceptual definition included such conventional utility planning topics as voltage and frequency regulation and reliability. The end-user's definition of power quality also centers around their ability to use the delivered energy in the desired manner, but the topics considered can be much more specific and include magnitude and duration of different events as well as waveshape concerns. Fortunately, a good working definition of power quality has not been a point of contention, and most parties involved consider "quality power" to be that which allows the user to meet their end-use goals. The working definition is not complicated by particular issues; engineers are well aware that topics from many aspects of power engineering may be important.

Power quality can be roughly broken into categories as follows:

1. steady-state voltage magnitude and frequency,
2. voltage sags,
3. grounding,
4. harmonics,
5. voltage fluctuations and flicker,
6. transients, and
7. monitoring and measurement.

The remainder of this section discusses each of the major categories in turn.

32.2.1 Steady-State Voltage Frequency And Magnitude

In most areas of North America, steady-state frequency regulation is not a significant issue due to the sufficient levels of generating capacity and the strong interconnections among generating companies and control areas. In other parts of the world, and North America under extreme conditions, frequency can deviate $\frac{1}{4}$ to $\frac{1}{2}$ Hz during periods of insufficient generating capacity. Under transient conditions, frequency can deviate up to 1–2 Hz.

Frequency deviations can affect power electronic equipment that use controlled switching devices unless the control signals are derived from a signal that is phase-locked with the applied voltage. In most cases, phase locks are used, or the converters consist of uncontrolled rectifiers. In either case, frequency deviations are not a major cause of problems. In most cases, frequency deviations have more impacts on conventional equipment that does not use electronics or in very inexpensive electronic devices. Clocks can run fast (or slow), motor speeds can drop (or rise) by a few revolutions per minute, etc. In most cases, these effects have minimal economic impact and are not considered a real power quality problem.

TABLE 32.1 ANSI C84.1 voltage ranges. Range A is for normal conditions, Range B is for emergency or short-time conditions

	Service Voltage ( )	Utilization Voltage ( )
Range A	114–125	108–125
Range B	110–127	104–127

Steady-state voltage regulation is a much more pronounced issue that can impact a wide range of end-use equipment. In most cases, utility supply companies do a very effective job of providing carefully regulated voltage within permissible ranges. In North America, ANSI Standard C84.1 suggests steady-state voltage ranges both at the utility service entrance and at the point of connection of end-use equipment. Furthermore, equipment manufacturers typically offer equipment that is tolerant of steady-state voltage deviations in the range of ±10%. Table 32.1 shows the voltage ranges suggested by ANSI C84.1, with specific mention of normal (Range A) and contingency (Range B) allowable voltages, expressed in percent.

Virtually all equipment, especially sensitive electronic equipment, can be affected by voltages deviating outside the ±10% range. In most cases, overvoltages above +10% lead to loss of life, usually over time; excessive overvoltages can immediately fail equipment. Undervoltages below −10% usually lead to excessive current demands, especially for equipment that has a controlled output like an adjustable speed drive controlling a motor to a constant speed/torque point. The impacts of these prolonged excessive currents can be greater voltage drop, temperature rise in conductors, etc. In the extreme, undervoltages of greater than 15–20 can cause equipment to immediately trip. In most cases, such extreme undervoltages are associated with system faults and the associated protection system. These extreme undervoltages are so important that they are classified in a power quality category of their own, called voltage sags.

32.2.2 Voltage Sags

Other than improper grounding, voltage sags are probably the most problematic of all power quality problems. At this time, a number of standards-making bodies, including IEEE, ANSI, and IEC, are working on standards related to sags. In most cases, sags are generally agreed to be more severe and outside of the scope of ANSI C84.1 and they are temporary in nature due to the operation of system protection elements. Because the electrical system is a continuous electrical circuit, faults in any location will have some impact on voltages throughout the

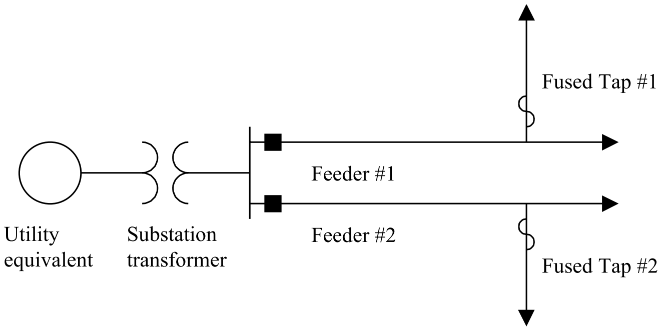

FIGURE 32.1 Overhead distribution system.

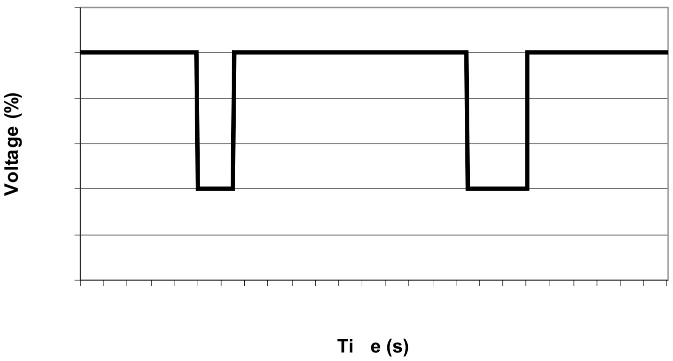

FIGURE 32.2 RMS voltage supplied to Feeder 1 customers.

network. Of course, areas closer to the faulted area will see a greater voltage sag due to the fault than other, more (electrically) remote areas. Sags can originate anywhere in a system, but are more pronounced in utility distribution systems because of the greater exposure of low-voltage systems to the causes of short circuits.

Most utility companies implement distribution system protection in what is known as a "fuse saving" methodology. Figure 32.1 shows a typical overhead distribution system with two feeders being supplied from the same substation transformer. Each primary circuit has its own automatic circuit recloser (ACR) and shows one fused tap.

With the protection system set up based on fuse-saving methodology, any fault downstream of a fault will be cleared first by the substation recloser followed by a reclosing operation (re-energization of the circuit) $\frac{1}{2}$ to 2 seconds later. If the fault is still present, the closest fuse should blow to permanently isolate the fault. (Note that in some cases, multiple reclosing attempts are made prior to the clearing of the fuse.)

For a fault on the load side of Fused Tap 2 in Figure 32.1, customers on Feeder 1 will see a voltage sag determined by the system and transformer impedance at the substation. Because this impedance is typically in the same order (or larger) as the feeder circuit impedance, a sag in substation bus voltage of 50 is common. This sag will persist until Feeder 2 is cleared by the recloser opening. When the recloser reenergizes the circuit, a permanent fault will still be present and the substation bus will again experience a voltage sag. Of course, any sag in substation bus voltage will be delivered directly to all customers on Feeder 1, even though there is no electrical problem on that feeder. Figure 32.2 shows a possible rms voltage profile that might be supplied to the customers on Feeder 1 for a permanent fault on the load side of Fused Tap 2. Only one recloser operation is shown prior to fuse clearing.

Just based on the voltage information shown in Figure 32.2, it is impossible to tell if the end-use loads on Feeder 1 will experience a problem. Equipment tolerance curves are required to assess the vulnerability of equipment to voltage deviations, including sags, and all equipment is different. Figure 32.3 shows the lower portions of two equipment tolerance curves, the (older) CBEMA and the (newer) ITIC curves for computer equipment. Most, but not all, power electronic based equipment has a similar shape. Voltage sags with a duration that correspond to a point that is "below and to the right" of the tolerance curve will result in loss of equipment function, while sags of duration that plot "above and to the left" of the tolerance curve will not affect equipment performance. Note that only the lower portion of the curve has been shown; an upper tolerance curve also exists that is often used in transient (overvoltage) studies.

Voltage sags are probably the most common power quality problem that is "given" to the end-user by the supplying utility. However, improper equipment grounding is responsible for the vast majority of power quality problems on the customer's side of the meter.

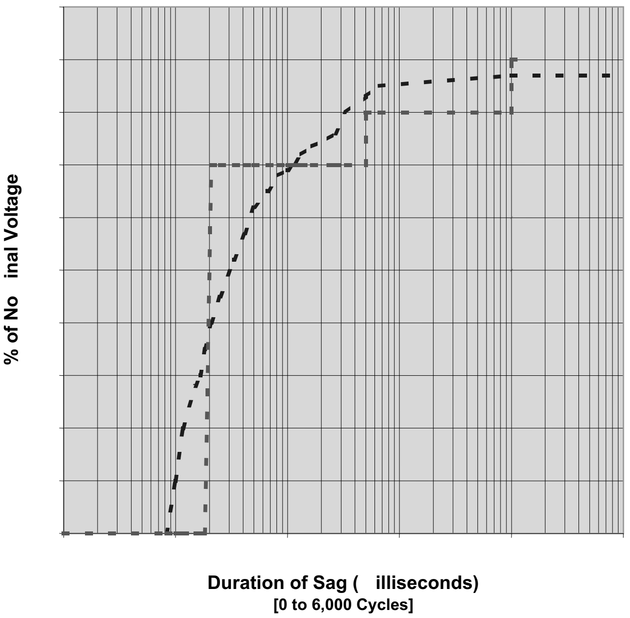

FIGURE 32.3 CBEMA (curved line) and ITIC (square shape) tolerance curves.

32.2.3 Grounding

Grounding of equipment was originally conceived as a personnel safety issue. However, the presence of an electrical conductor that is at zero potential has been widely used in many power electronic and microprocessor-controlled loads. In the United States, electrical systems in residential, commercial, and industrial facilities fall under the purview of the National Electric Code which establishes specific criteria for grounding of equipment. While it was once thought that proper grounding according to the NEC was detrimental to power quality concerns, these opinions have gradually faded over time.

From a power quality perspective, improper grounding can be considered in three broad categories:

1. ground loops,
2. improper neutral-to-ground connections, and
3. excessive neutral-to-ground voltage.

The ground loop problem is a significant issue when power, communications, and control signals all originate in different locations, but come together at a common electrical point. Transients induced in one location can travel through the created ground loop, damaging equipment along the way. Improper neutral-to-ground connections will create a "noisy" ground reference that may interfere with low-voltage communications and control devices. Excessive neutral-to-ground voltage may damage equipment that is not properly insulated or that has an inexpensive power supply.

Figure 32.4 shows a common wye-connected service (assumed at the terminals of a transformer) that supplies power to equipment that also is remotely monitored and controlled from another location with a separate ground reference.

For any shift in ground potential for the power circuit, often caused by lightning as shown in Figure 32.4, potentially large currents can flow through the grounding circuits and through the sensitive electronic equipment. Such currents can easily lead to equipment damage. Situations like these are common in

1. residential areas, if power and CATV or telephone grounds are not the same, and
2. commercial and industrial complexes consisting of multiple buildings with linking communications, computer, or control circuits, when each building has its own power service (and therefore ground).

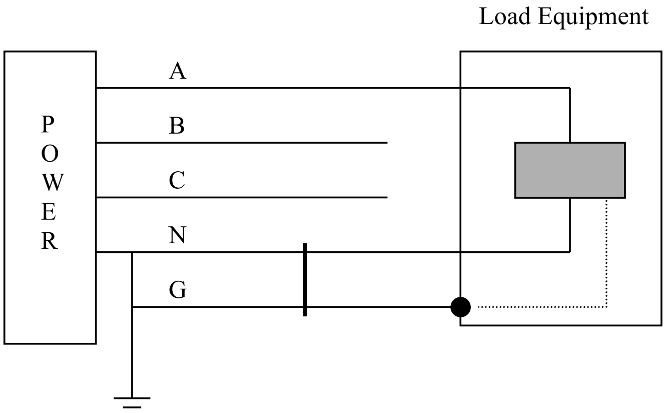

FIGURE 32.5 Improper neutral-to-ground connections.

Figure 32.5 shows an example of an improper neutral-to-ground connection, and how this connection can create power quality problems.

Load current returning in the neutral conductor will, at the point of improper connection to ground, divide between neutral and ground. This current flow in the ground conductor will produce a voltage at the load equipment, which can easily disrupt equipment operation.

Figure 32.6 shows an example of the possibility for excessive neutral-to-ground voltage and how this can lead to power quality problems.

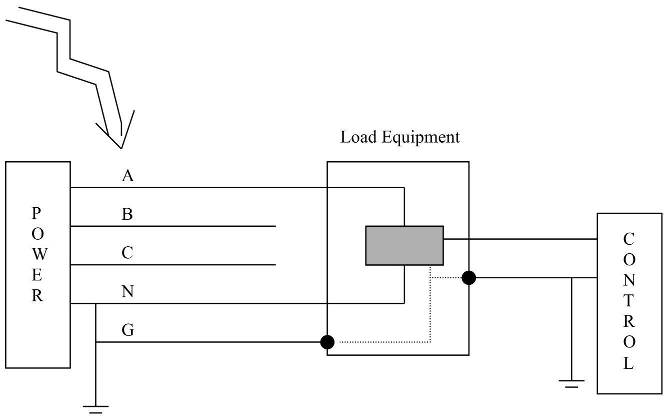

FIGURE 32.4 Powering and control ground loop.

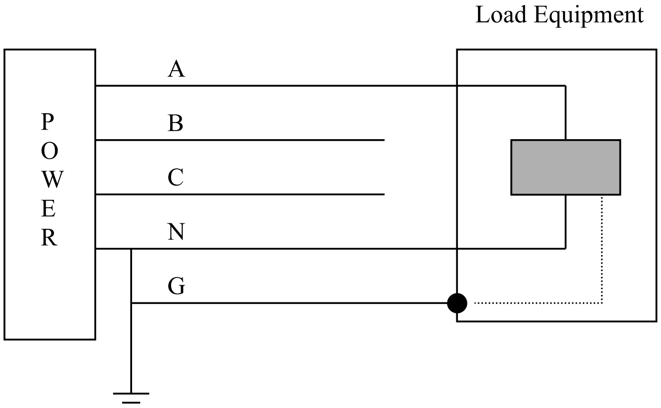

FIGURE 32.6 Excessive neutral-to-ground voltage.

For load equipment that produces significant voltage drop in the neutral, such as laser printers and copying machines when the thermal heating elements are on, the voltage from the neutral to the ground reference inside the equipment can exceed several volts. In many cases, this voltage is sufficient to damage printed circuit boards, disrupt control logic, and fail components.

32.2.4 Harmonics

In most cases, power electronic equipment is considered to be the "cause" of harmonics. While switching converters of all types produce harmonics because of the nonlinear relationship between the voltage and current across the switching device, harmonics are also produced by a large variety of "conventional" equipment including:

1. power generation equipment (slot harmonics),
2. induction motors (saturated magnetics),
3. transformers (overexcitation leading to saturation),
4. magnetic-ballast fluorescent lamps (arcing), and
5. ac electric arc furnaces (arcing).

All these devices will cause harmonic currents to flow, and some devices actually directly produce voltage harmonics.

Any ac current flow through any circuit at any frequency will produce a voltage drop at that same frequency. Harmonic currents, which are produced by power electronic loads, will produce voltage drops in the power supply impedance at those same harmonic frequencies. Because of this interrelationship between current flow and voltage drop, harmonic currents created at any location will distort the voltage in the entire supply circuit.

In most cases, equipment is not overly sensitive to the direct impacts of harmonic current flow. Note, however, that equipment heating is a function of the rms value of the current, which can significantly exceed the fundamental frequency value when large harmonic components are present. It is because harmonic currents produce harmonic voltages that there is a real power quality concern.

Most equipment can operate satisfactorily as long as the voltage distortion at the equipment terminals does not exceed around 5 . Exceptions to this general rule include ripple-control systems for converters (which are impacted by small even-order harmonics) and small harmonics at sufficiently high frequency to produce multiple zero crossing in a waveform. (Note that voltage notching due to simultaneous commutation of switching devices can also create multiple zero crossings.) Such a multiple crossing scenario is shown in Figure 32.7 and represents a 60 Hz waveform plus a 1 voltage harmonic at 3,000 Hz.

Converters that have a time-limited firing signal can directly suffer from excessive voltage distortion. For a six-pulse converter, a maximum time of 1/(6 × 60) seconds is available to turn on a switching device. Similarly, for a twelve-pulse converter, a maximum of 1/(12 × 60) is available to turn on a switching device. Considering that all switching devices have a short (but nonzero) turn-on time, manufacturers tend to design drive circuits that bring up the firing pulse for a limited amount of time. If, for example, a firing pulse is maintained for 100 μs, the device must begin conduction in that time. In situations where voltage distortion is excessive, the device to be switched could be reverse biased during the first several milliseconds of the time available for device firing during which time conduction cannot begin. If the firing signal is removed before the certain classes of switching devices are correctly biased, conduction will not begin at all. This situation, commonly called a "misfire," can lead to equipment misoperation and failure.

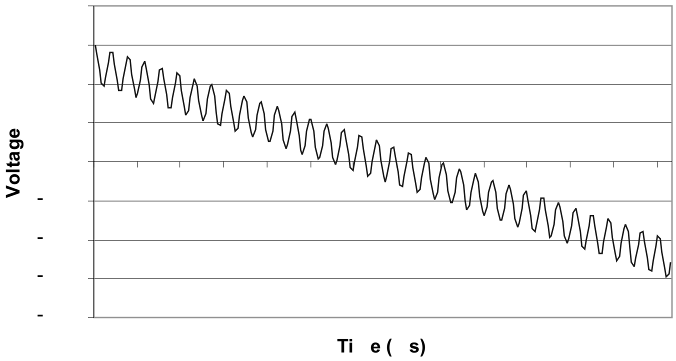

FIGURE 32.7 Multiple zero crossings.

Because some switching devices can conduct in both directions when the firing signal is applied (but only one direction is intended to carry appreciable current), applying the firing pulse at a time when the voltage is of the wrong polarity can destroy the device. Excessive voltage distortion can certainly lead to such a situation, and manufacturers typically design products to function only under limited-distortion conditions.

Because of the numerous potential problems with harmonic currents, standards exist for their control. The IEC goes as far as to limit the harmonic currents produced by certain individual pieces of equipment, while the IEEE takes a more "system-level" point of view and prescribes limits for harmonic currents for a facility as a whole, including one or more harmonic producing loads. Harmonic standards will be further discussed in Section 32.4.

32.2.5 Voltage Fluctuations and Flicker

Voltage flicker is not directly caused by electronic loads except in the largest of applications. Voltage fluctuations, and the corresponding light flicker due to them, are usually created by large power fluctuations at frequencies less than about 30 Hz. In most applications, only

1. large dc arc furnaces and welders,

2. reactive power compensators, and
3. cycloconverters

are potentially problematic. Each of these types of end-use devices can create large, low-frequency (about 30 Hz or less) variations in the system voltage, and can therefore lead to voltage flicker complaints. At this time, the IEEE prescribes a "flicker curve" based originally on research conducted by General Electric. The IEC, however, has adopted a different methodology that can consider voltage fluctuations and flicker that are more complex than those considered by the IEEE flicker curve.

Most equipment is not sensitive to the voltage fluctuations that cause flicker complaints. The change in output of incandescent lamps as viewed by human observers becomes objectionable at levels of change around 0.3 , but electronic equipment will not be affected at all. Because most utility supply companies limit voltage fluctuations, regardless of the frequency of repetition, to less than a few percent, equipment malfunction or damage due to flicker is very rare. Figures 32.8 and 32.9 show plots of single-cycle rms voltage fluctuations due to large dc welders and arc furnaces, respectively; it is clear that the magnitude of the fluctuations are well above the level that could impact equipment. The waveform in Figure 32.8 probably would generate numerous light flicker complaints, whereas the waveform in Figure 32.9 probably would not. Neither would disrupt equipment.

Because of the advances in power electronics that have offered devices with higher power ratings, reactive compensation systems have been developed to compensate for voltage fluctuations by adding or removing reactive power from the supply circuit. These devices have allowed large flicker-producing loads like arc furnaces to be served from utility circuits that, without the compensator, could not serve the load. However, because the compensators can so directly impact system voltage, they can create flicker problems if they are not properly applied and controlled.

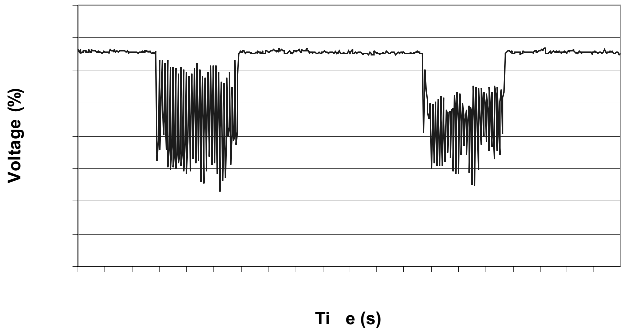

FIGURE 32.8 Single-cycle rms voltage fluctuations due to a large dc welder.

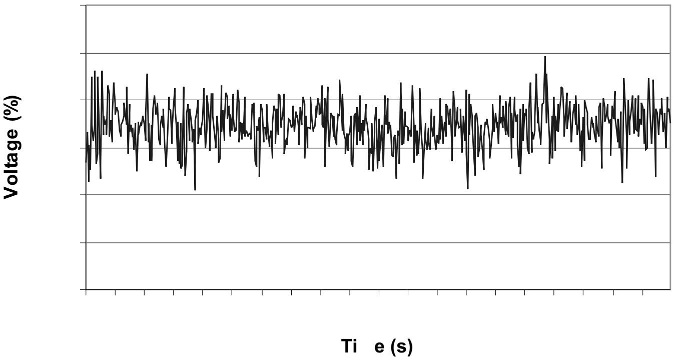

FIGURE 32.9 Single-cycle rms voltage fluctuations due to a large dc arc furnace.

32.2.6 Transients

Transients, especially in the voltage supply, can create numerous power quality problems. The major sources of transients are

1. lightning,
2. utility circuit switching and fault clearing,
3. capacitor switching, and
4. load switching.

Lightning events can create the most severe overvoltages, but these transients decay rapidly. A typical lightning transient has decayed to zero in a few hundred microseconds, but it can reach a peak magnitude of several hundred percent if not controlled with surge suppression devices. Other categories of transients associated with power system switching are much smaller in magnitude (typically less than 200), but at least in the order of several hundred milliseconds. Considering the energy available in a transient, therefore, there is considerable overlap in the range of severity of lightning and switching transients. It is the available energy that typically determines whether or not equipment will be affected or damaged. Figure 32.10 shows a capacitor switching transient on a low-voltage (480 V) circuit. The magnitude and duration of the event are quite clear.

Transients such as those shown in Figure 32.10 are generally sufficient to cause nuisance trips of electronic loads like adjustable speed drives. For these types of loads, the protection system settings are usually very tight due to the use of sensitive switching devices. Overcurrent and overvoltage settings of 120 are not uncommon. For a transient similar to that shown in Figure 32.10, there is sufficient overvoltage for very large currents to flow through any conducting switching device to the drive's dc bus. The device's protection system see these overcurrents as a fault, and trip the drive. Similarly, the overvoltage at the terminals can be passed through to the dc bus and accumulate, where the drive may trip due to overvoltage on the dc bus.

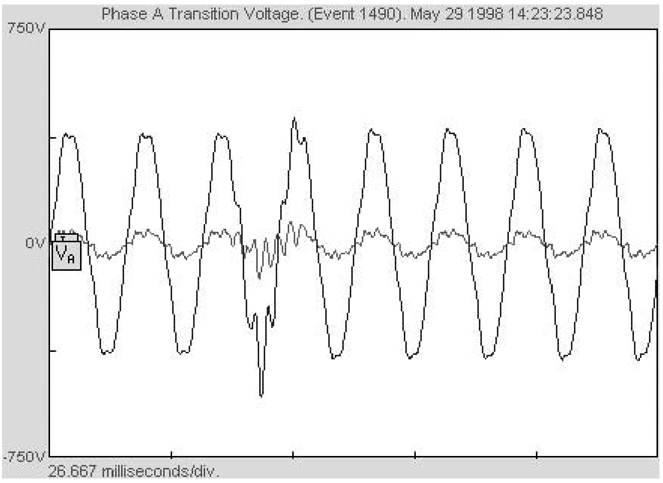

FIGURE 32.10 Capacitor switching transient.

32.2.7 Monitoring and Measurement

To consider or be able to diagnose power quality related problems, it is imperative to be able to measure various power quality parameters. Several different categories of monitoring and measurement equipment exist for these purposes, with costs ranging from a few hundred dollars to 10,000– 20,000 for fully equipped disturbance analyzers.

The most basic category of power quality measurement tool is the hand-held voltmeter. It is important that the voltmeter be a true-rms meter, or erroneous readings will be obtained that incorrectly suggest low or high voltage when harmonics are present in the signal. It is especially important to have true rms capability when measuring currents; voltage distortion is not typically severe enough to create large errors in the readings of non-true-rms meters. Virtually all major measurement equipment vendors offer true-rms meters, with costs starting around 100.

The next step up from the basic voltmeter is a class of instruments that have come to be called "power quality analyzers." These instruments are hand held and battery powered. These instruments can measure and display various power quality indices, especially those that relate to harmonics like THD, etc., and can also display the input waveform. Newer models feature 20 MHz (and higher) bandwidth oscilloscopes, inrush measurements, time trending, and other useful features. Manufacturers such as Fluke, Dranetz, BMI, and Tektronix offer these types of instruments for around 2,000.

In most power quality investigations, it is not possible to use hand-held equipment to collect sufficient data to solve the problem. Most power quality problems are intermittent in nature, so some type of long-term monitoring is usually required. Various recorders are available that can measure and record voltage, current, and power over user-defined time periods. Such recorders typically cost on the order of 3,000– 10,000. More advanced long-term monitors can record numerous power quality events and indices, including transients, harmonics, sags, flicker, etc. These devices, often called "line disturbance analyzers" typically cost between 10,000– 20,000.

It is important to use the right instrument to measure the phenomenon that is suspected of causing the problem. Some meters record specific parameters, while others are more flexible. With this flexibility comes an increased learning curve for the user, so it is important to spend time on them before going out to monitor to make sure all aspects and features of the equipment are understood.

It is equally important to measure in the correct location. The best place to measure power quality events is at the equipment terminals that are experiencing problems. With experience, an engineer can evaluate the waveforms recorded at the equipment terminals and correlate them to events and causes elsewhere in the power system. In general, the farther away from the equipment location the monitoring takes place, the more difficult it can be to diagnose a problem.

32.3 Reactive Power and Harmonic Compensation

The previous section specifically identified harmonics as a potential power quality problem. In that discussion, it was pointed out that nonlinear loads such as adjustable speed drives create harmonic currents, and when these currents flow through the impedances of the power supply system, harmonic voltages are produced. While harmonic currents have secondary (in most cases) negative impacts, it is these harmonic voltages that can be supplied to other load equipment (and disrupt operation) that are of primary concern. Having parallel or series resonant conditions present in the electrical supply system can quickly exacerbate the problem.

32.3.1 Typical Harmonics Produced by Equipment

In theory, most harmonic currents follow the "$1/n$" rule where n is the harmonic order ($180\text{ Hz} = 3 \times 60$; $n = 3$). Also in theory, most harmonic currents in three-phase systems are not integer multiples of three. Finally, in theory, harmonic currents are not usually even-order integer multiples of the fundamental. In practice, none of these statements are completely true and using any of them "exactly" could lead to either over- or under-conservatism depending on many factors. Consider the following examples:

1. Switched-mode power supplies, such as found in televisions, personal computers, etc., often produce a third harmonic current that is nearly as large (80–90) as the fundamental frequency component.
2. Unbalance in voltages supplied to a three-phase converter load will lead to the production of even-

order harmonics and, in some extreme cases, establish a positive feedback situation leading to stability problems.

3. Arcing loads, particularly in the steel industry, generate significant harmonics of all orders, including harmonics that are not integer multiples of the power frequency.
4. Cycloconverters produce dominant harmonics that are integer multiples of the power frequency, but they also produce sideband components at frequencies that are not integer multiples of the power frequency. In some control schemes, the amplitudes of the sideband components can reach damaging levels.

Table 32.2 gives the magnitudes, in percent of fundamental, of the first 25 (integer) harmonics for a single-phase switched-mode power supply, a single-phase fluorescent lamp, a three-phase (six-pulse) dc drive, and a three-phase (six pulse, no input choke) ac drive. Together, these load types represent the range of harmonic sources in power systems. Note that seemingly minor changes in parameter values and control methods can have significant impacts on harmonic current generation; the values given here are on the conservative side of "typical."

32.3.2 Resonance

Considering only the harmonic current spectra given in Table 32.2, it would appear that a large number of harmonic-related power quality problems are on the verge of appearing. In reality, most current drawn by many residential, commercial, and industrial customers is of the fundamental frequency; the amplitudes of the individual harmonic currents, in percent of the *total* fundamental current, are often much less than what is shown in Table 32.2. For this reason, end-use locations employing nonlinear loads often do not lead directly to significant voltage distortion problems. A parallel resonance in the power supply system, however, changes the picture entirely.

Series and parallel resonance exist in any ac power supply network that contains inductance(s) and capacitance(s). The following simple (but useable) definitions apply:

1. Series resonance occurs when the impedance to current flow at a certain frequency (or frequencies) is low.
2. Parallel resonance occurs when the impedance to current flow at a certain frequency (or frequencies) is high.

For a given harmonic-producing load that generates harmonics at frequencies that correspond to parallel resonance in the supply system, even small currents at the resonant frequencies can produce excessive voltages at these same frequencies. The principle of series resonance, however, is usually exploited to reduce harmonics in power systems by providing intentionally low impedance paths to ground.

In many cases, end-users will install power factor correction capacitors in order to minimize reactive power charges by the

TABLE 32.2 Typical harmonic spectra of load equipment

Harmonic No.	Switched-Mode Power Supply	Fluorescent Lamp	Six-Pulse dc Drive	Six-Pulse ac Drive
1	100.0	100.0	100.0	100.0
2	0.7	1.0	4.8	1.1
3	91.9	12.6	1.2	3.9
4	1.0	0.3	1.5	0.5
5	80.2	1.8	33.6	82.8
6	1.3	0.1	0.0	1.7
7	64.8	0.7	1.6	77.5
8	1.4	0.1	1.7	1.2
9	47.7	0.5	0.4	7.6
10	1.0	0.1	0.3	0.7
11	30.8	0.2	8.7	46.3
12	0.8	0.1	0.0	1.0
13	16.0	0.2	1.2	41.2
14	0.4	0.0	1.3	0.2
15	5.0	0.1	0.3	5.7
16	0.1	0.1	0.2	0.3
17	4.0	0.2	4.5	14.2
18	0.3	0.1	0.0	0.4
19	7.2	0.1	1.3	9.7
20	0.4	0.2	1.1	0.4
21	7.7	0.2	0.3	2.3
22	0.4	0.1	0.3	0.5
23	6.2	0.1	2.8	1.5
24	0.2	0.0	0.0	0.5
25	4.0	0.1	1.2	2.5

supply utility. In most cases, these capacitors are located on the customer's low voltage supply buses and are therefore in parallel with the service transformer. In most cases where the power factor correction capacitors are sized to provide a net power factor (at the service entrance) to 0.85 (lag) -1.0, the parallel resonance occurs somewhere between the 5th and 9th harmonic. Considering Table 32.2, it is apparent that a large number of loads produce harmonics at these frequencies, and the amplitudes can be significant. Even a small increase in impedance at these frequencies due to resonance can lead to unacceptable voltages being produced at these same frequencies. Figure 32.11 shows an example plot of impedance looking into a utility supply system when a typically-sized capacitor bank has been installed to improve overall plant power factor.

From Figure 32.11, it is clear that 1.0 A at the 9th harmonic will produce at least 150 times more voltage drop than would be produced by the same 1.0 A if it were at the fundamental frequency. A look back at Table 32.2 shows the clear potential for problems. Fortunately, the series resonance principle can be used to provide a low impedance path to ground for the harmonic currents and thus reduce the potential for problematic voltage distortion.

Because capacitors are required to produce parallel resonance, it is often a "cheap fix" to slightly modify the capacitor to include a properly sized series reactor and create a filter. This filter approach, designed based on the series resonance concept, is usually the most cost-effective means to control harmonic voltage distortion.

32.3.3 Harmonic Filters

Harmonic filters come in many "shapes and sizes." In general, harmonic filters are "shunt" filters because they are connected in parallel with the power system and provide low impedance paths to ground for currents at one or more harmonic frequencies. For power applications, shunt filters are almost always more economical than series filters (like those found in many communications applications) for the following reasons:

1. Series components must be rated for the full current, including the power frequency component. Such a requirement leads to larger component sizes and therefore costs.
2. Shunt filter components generally must be rated for only part of the system voltage (usually with respect to ground). Such requirements lead to smaller component sizes and therefore costs.

Shunt filters are designed (or can be purchased) in three basic categories as follows:

1. single-tuned filters,
2. multiple- (usually limited to double) tuned filters, and
3. damped filters (of first, second, or third order, or newer "c type").

The single- and double-tuned filters are usually used to filter specific frequencies, while the damped filters are used to filter a wide range of frequencies. In applications involving small harmonic producing loads, it is often possible to use one single-tuned filter (usually tuned near the 5th harmonic) to eliminate problematic harmonic currents. In large applications, like those associated with arc furnaces, multiple tuned filters and a damped filter are often used. Equivalent circuits for single- and double-tuned filters are shown in Figure 32.12. Equivalent circuits for first, second, third, and "c type" damped filters are shown in Figure 32.13.

A plot of the impedance as a function of frequency for a single-tuned filter is shown in Figure 32.14. The filter is based on a 480 V, 300 kvar (three-phase) capacitor bank and is tuned to the 4.7th harmonic with a quality factor, Q, of 150. Note that the quality factor is a measure of the "sharpness" of the tuning and is defined as X/R where X is the inductive reactance for the filter inductor at the (undamped) resonant frequency; typically $50 < Q < 150$ for tuned filters.

A plot of impedance as a function of frequency for a second-order damped filter is shown in Figure 32.15. This filter is based on a 480 V, 300 kvar capacitor bank and is tuned to the 12th harmonic. The quality factor is chosen to be 1.5. Note that the quality factor for damped filters is the inverse of the definition for tuned filters; $Q = R/X$ where X is the

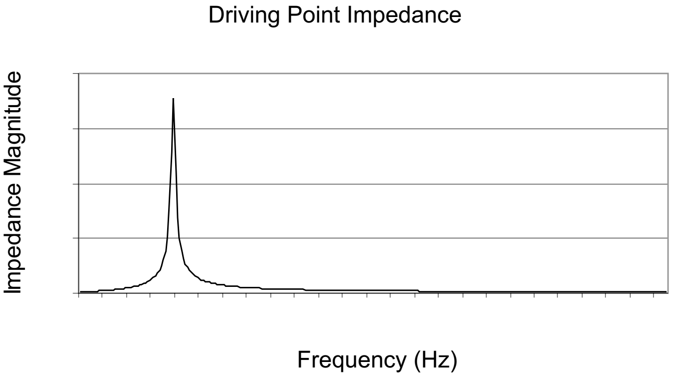

FIGURE 32.11 Driving point impedance.

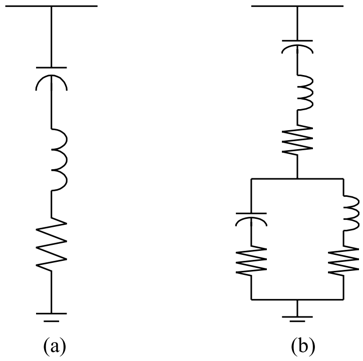

FIGURE 32.12 Single-tuned (a) and double-tuned (b) harmonic filters.

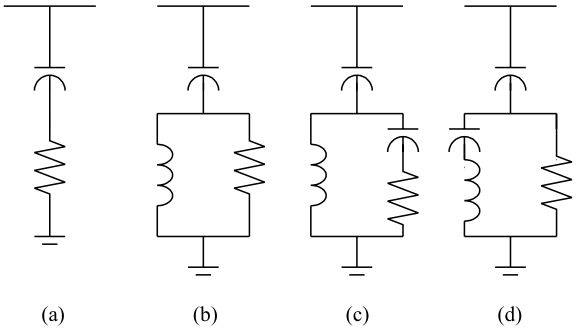

FIGURE 32.13 Damped filters: first (a), second (b), and third (c) order, and c type (d).

inductive reactance at the (undamped) resonant frequency. Typically, $0.5 < Q < 1.5$ for damped filters.

In most cases, it is common to tune single-tuned filter banks to slightly below (typically around 5) the frequency of the harmonic to be removed. The reasons for this practice are as follows:

1. For a low-resistance series resonance filter that is exactly tuned to a harmonic frequency, the filter bank will act as a sink to all harmonics (at the tuned frequency) in the power system, regardless of their source(s). This action can quickly overload the filter.
2. All electrical components have some nonzero temperature coefficient, and capacitors are the most temperature sensitive component in a tuned filter. Because most capacitors have a negative temperature coefficient (capacitance decreases and tuned frequency therefore increases with temperature), tuning slightly lower than the desired frequency is desirable.

Damped filters are typically used to control higher-order harmonics as a group. In general, damped filters are tuned in between corresponding pairs of harmonics (11th and 13th, 17th and 19th, etc.) to provide the maximum harmonic reduction at those frequencies while continuing to serve as a (not quite as effective) filter bank for frequencies higher than the tuned frequency. Because damped filters have significantly higher resistance than single- or double-tuned filters, they are

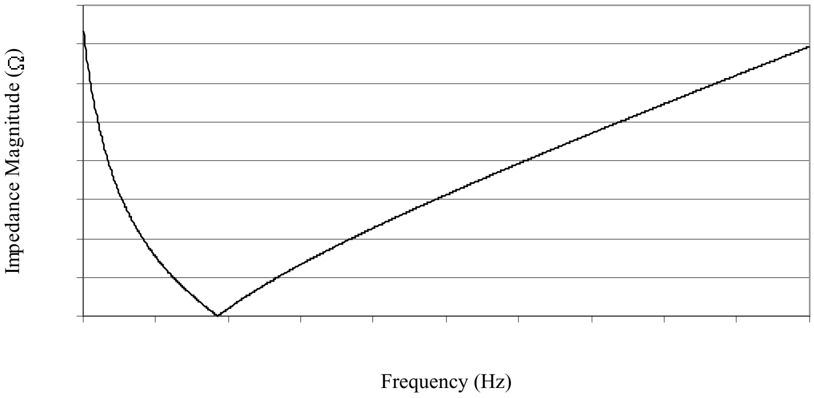

FIGURE 32.14 Single-tuned filter frequency response.

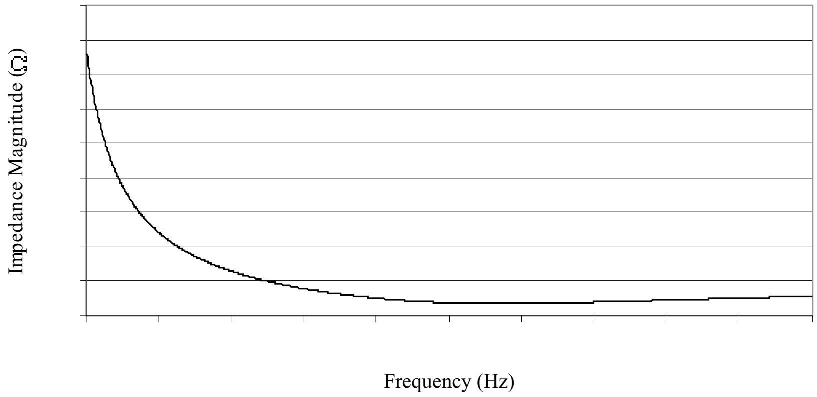

FIGURE 32.15 Second-order damped filter frequency response.

usually not used to filter harmonics near the power frequency so that filter losses can be maintained at low values.

32.4 IEEE Standards

The IEEE has produced numerous standards relating to the various power quality phenomena discussed in Section 32.2. Of these many standards, the one most appropriate to power electronic equipment is IEEE Standard 519-1992. This standard is actually a "recommended practice," which means that the information contained within represents a set of "recommendations," rather than a set of "requirements." In practice, this seemingly small difference in wording means that the harmonic limits prescribed are merely suggested values; they are not (nor were they ever intended to be) absolute limits that could not be exceeded.

Harmonic control via IEEE 519-1992 is based on the concept that all parties use and pay for the public power supply network. Due to the nature of utility company rate structures, end-users that have a higher demand pay more of the total infrastructure cost through higher demand charges. In this light, IEEE 519-1992 allows these larger end-users to produce a greater percentage of the maximum level of harmonics that can be absorbed by the supply utility before voltage distortion problems are encountered. Because the ability for a harmonic source to produce voltage distortion is directly dependent on the supply system impedance up to the point where distortion is to be evaluated, it is necessary to consider both

1. the size of the end-user and
2. the strength (impedance) of the system

at the same time in order to establish meaningful limits for harmonic emissions. Furthermore, it is necessary to establish tighter limits in higher voltage supply systems than lower voltage because the potential for more widespread problems associated with high voltage portions of the supply system.

Unlike limits set forth in various IEC Standards, IEEE 519-1992 established the "point of common coupling," or PCC, as the point at which harmonic limits shall be evaluated. In most cases (recall that IEEE 519-1992 is a "recommended practice"), this point will be:

1. in the supply system owned by the utility company,
2. the closest electrical point to the end-user's premises, and
3. as in (2), but further restricted to points where other customers are (or could be in the future) provided with electric service.

In this context, IEEE 519-1992 harmonic limits are designed for an entire facility and should not be applied to individual pieces of equipment without great care.

Because the PCC is used to evaluate harmonic limit compliance, the system strength (impedance) is measured at this point and is described in terms of available (three-phase) short-circuit current. Also, the end-user's maximum average demand current is evaluated at this point. Maximum demand is evaluated based on one of the following:

1. the maximum value of the 15 or 30 minute average demand, usually considering the previous 12 month's billing history, or
2. the connected kVA or horsepower, perhaps multiplied by a diversity factor.

The ratio of I_{SC} to I_L, where I_{SC} is the available fault current and I_L is the maximum demand current, implements the founding concept of IEEE 519-1992: larger end-users can create more harmonic currents, but the specific level of current that any end-user may produce is dependent on the strength of the system at the PCC. Tables 32.3–32.5 show the harmonic current limits in IEEE 519-1992 for various voltage levels.

In general, it is the responsibility of the end-user to insure that their net harmonic currents at the PCC do not exceed the values given in the appropriate table. In some cases, usually associated with parallel resonance involving a utility-owned capacitor bank, it is possible that all customers will be within

TABLE 32.3 Current distortion limits for general distribution systems, 120 V–69 kV

	Maximum Harmonic Current Distortion in Percent of I_L					
	Individual Harmonic Order h (Odd Harmonics)					
I_{SC}/I_L	< 11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$h \geq 35$	TDD
20^1	4.0	2.0	1.5	0.6	0.3	5.0
20 50	7.0	3.5	2.5	1.0	0.5	8.0
50 100	10.0	4.5	4.0	1.5	0.7	12.0
100 1000	12.0	5.5	5.0	2.0	1.0	15.0
≥ 1000	15.0	7.0	6.0	2.5	1.4	20.0

Even harmonics are limited to 25% of the odd harmonic limits above.

Current distortions that result in a dc offset are not allowed.

[1] All power generation equipment is limited to these values of current distortion regardless of the value of I_{SC}/I_L.

TABLE 32.4 Current distortion limits for general subtransmission systems, 69.001–161 kV

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order h (Odd Harmonics)						
I_{SC}/I_L	< 11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h \leq 35$	$h \geq 35$	TDD
20[1]	2.0	1.0	0.75	0.3	0.15	2.5
20 50	3.5	1.75	1.25	0.5	0.25	4.0
50 100	5.0	2.25	2.0	0.75	0.35	6.0
100 1000	6.0	2.75	2.5	1.0	0.5	7.5
$\geq$1000	7.5	3.5	3.0	1.25	0.7	10.0

Even harmonics are limited to 25% of the odd harmonic limits above.
Current distortions that result in a dc offset are not allowed.

[1] All power generation equipment is limited to these values of current distortion regardless of the value of I_{SC}/I_L.

TABLE 32.5 Current distortion limits for general transmission systems, > 161 kV

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order h (odd harmonics)						
I_{SC}/I_L	< 11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h \leq 35$	$h \geq 35$	TDD
50[1]	2.0	1.0	0.75	0.3	0.15	2.5
$\geq$50	3.0	1.5	1.15	0.45	0.22	3.75

Even harmonics are limited to 25% of the odd harmonic limits above
Current distortions that result in a dc offset are not allowed

[1] All power generation equipment is limited to these values of current distortion regardless of the value of I_{SC}/I_L.

TABLE 32.6 Voltage distortion limits

Bus Voltage at PCC	Individual Harmonic Magnitude ( )	Total Voltage Distortion (THD in)
$\leq$ 69 kV	3.0	5.0
69.001–161 kV	1.5	2.5
161 kV	1.0	1.5

the prescribed limits, but voltage distortion problems exist. In these cases, it is generally the responsibility of the supply utility to insure that excessive voltage distortion levels are not present. The harmonic voltage limits that are recommended for utility companies are given in Table 32.6.

32.5 Conclusions

In this chapter, various power quality phenomena have been described, with particular focus on the implications on power electronic converters and equipment. While one popular opinion "blames" power electronic equipment for "causing" most power quality problems, it is quite clear that power electronic converter systems can play an equally important role in reducing the impact of power quality problems. While it is true that power electronic converters and systems are the major cause of harmonic-related problems, the application (in general terms) of IEEE 519-1992 limits for current and voltage harmonics has led to the reduction, elimination, and prevention of most harmonic problems. Other power quality phenomena, like grounding, sags, and voltage flicker, are most often completely unrelated to power electronic systems. In reality, advances in power electronic circuits and control algorithms are making it more possible to control these events and minimize the financial impacts of the majority of power quality problems.

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33

Active Filters

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33.1 Introduction

The growing number of power electronics base equipment has produced an important impact on the quality of electric power supply. Both high power industrial loads and domestic loads cause harmonics in the network voltages. At the same time, much of the equipment causing the disturbances is quite sensitive to deviations from the ideal sinusoidal line voltage. Therefore, power quality problems may originate in the system or may be caused by the consumer itself. Moreover, in the last years the growing concern related to power quality comes from:

- Consumers that are becoming increasingly aware of the power quality issues and being more informed about the consequences of harmonics, interruptions, sags, switching transients, etc. Motivated by deregulation, they are challenging the energy suppliers to improve the quality of the power delivered.
- The proliferation of load equipment with microprocessor-based controllers and power electronic devices which are sensitive to many types of power quality disturbances.
- Emphasis on increasing overall process productivity, which has led to the installation of high-efficiency equipment, such as adjustable speed drives and power factor correction equipment. This in turn has resulted in an increase in harmonics injected into the power system, causing concern about their impact on the system behavior.

For an increasing number of applications, conventional equipment is proving insufficient for mitigation of power quality problems. Harmonic distortion has traditionally been dealt with by the use of passive LC filters. However, the application of passive filters for harmonic reduction may result in parallel resonances with the network impedance, over compensation of reactive power at fundamental frequency, and poor flexibility for dynamic compensation of different frequency harmonic components.

The increased severity of power quality in power networks has attracted the attention of power engineers to develop dynamic and adjustable solutions to the power quality problems. Such equipment, generally known as active filters, are also called active power line conditioners, and are able to compensate current and voltage harmonics, reactive power, regulate terminal voltage, suppress flicker, and to improve voltage balance in three phase systems. The advantage of active filtering is that it automatically adapts to changes in the network and load fluctuations. They can compensate for several harmonic orders, and are not affected by major changes in network characteristics, eliminating the risk of resonance between the filter and network impedance. Another plus is that they take up very little space compared with traditional passive compensators.

33.2 Types of Active Power Filters

The technology of active power filter has been developed during the past two decades reaching maturity for harmonics

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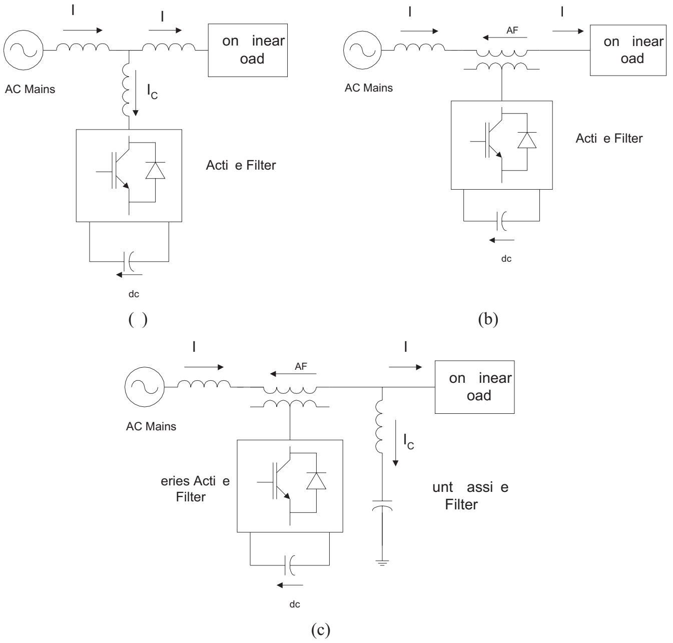
compensation, reactive power, and voltage balance in ac power networks. All active power filters are developed with PWM converters (current source or voltage source inverters). The current-fed PWM inverter bridge structure behaves as a nonsinusoidal current source to meet the harmonic current requirement of the nonlinear load. It has a self-supported dc reactor that ensures the continuous circulation of the dc current. They present good reliability, but have important losses and require higher values of parallel capacitor filters at the ac terminals to remove unwanted current harmonics. Moreover, they cannot be used in multilevel or multistep modes configurations to allow compensation in higher power ratings.

The other converter used in active power filter topologies is the voltage-source PWM inverter. This converter is more convenient for active power filtering applications since it is lighter, cheaper, and expandable to multilevel and multistep versions, to improve its performance for high power rating compensation with lower switching frequencies. The PWM voltage source inverter has to be connected to the ac mains through coupling reactors. An electrolytic capacitor keeps a dc voltage constant and ripple free.

Active power filters can be classified based on the type of converter, topology, control scheme, and compensation characteristics. The most popular classification is based on the topology such as shunt, series or hybrid. The hybrid configuration is a combination of passive and active compensation. The different active power filter topologies are shown in Fig. 33.1.



( )

(b)

(c)

FIGURE 33.1 Active power filter topologies implemented with PWM-VSI. (a) Shunt active power filter. (b) Series active power filter. (c) Hybrid active power filter.

TABLE 33.1 Active filter solutions to power quality problems

Active Filter Connection	Load on ac Supply	AC Supply on Load
Shunt	Current harmonic filtering Reactive current compensation Current unbalance Voltage flicker	
Series	Current harmonic filtering Reactive current compensation Current unbalance Voltage flicker Voltage unbalance	Voltage sag/swell Voltage unbalance Voltage distortion Voltage interruption Voltage flicker Voltage notching

Shunt active power filters (Fig. 33.1(a)) are widely used to compensate current harmonics, reactive power and load current unbalanced. It can also be used as a static var generator in power system networks for stabilizing and improving voltage profile. Series active power filters (Fig. 33.1(b)) is connected before the load in series with the ac mains, through a coupling transformer to eliminate voltage harmonics and to balance and regulate the terminal voltage of the load or line. The hybrid configuration is a combination of series active filter and passive shunt filter (Fig. 33.1(c)). This topology is very convenient for the compensation of high power systems, because the rated power of the active filter is significantly reduced (about 10 of the load size), since the major part of the hybrid filter consists of the passive shunt LC filter used to compensate lower-order current harmonics and reactive power.

Due to the operation constraint, shunt or series active power filters can compensate only specific power quality problems. Therefore, the selection of the type of active power filter to improve power quality depends on the source of the problem as can be seen in Table 33.1.

The principles of operation of shunt, series and hybrid active power filters are described in the following sections.

33.3 Shunt Active Power Filters

Shunt active power filters compensate current harmonics by injecting equal-but-opposite harmonic compensating current. In this case, the shunt active power filter operates as a current source injecting the harmonic components generated by the load but phase shifted by 180°. As a result, components of harmonic currents contained in the load current are cancelled by the effect of the active filter, and the source current remains sinusoidal and in phase with the respective phase to neutral voltage. This principle is applicable to any type of load considered as an harmonic source. Moreover, with an appropriate control scheme, the active power filter can also compensate the load power factor. In this way, the power distribution

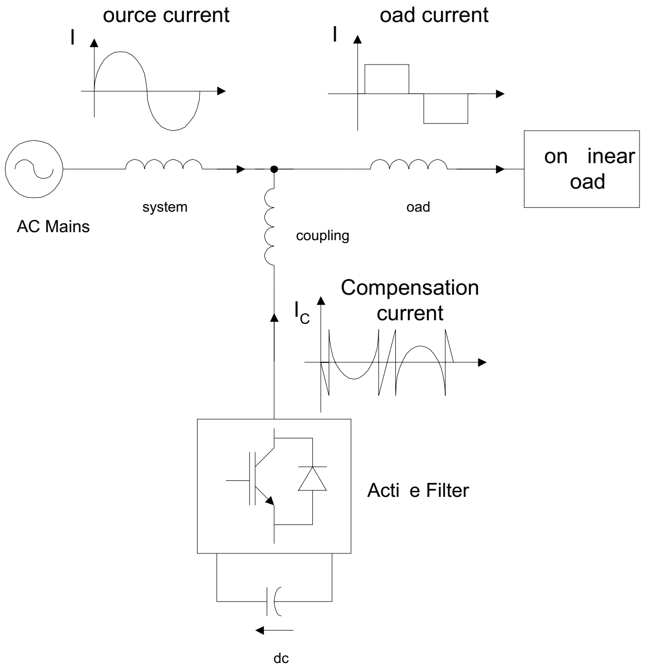


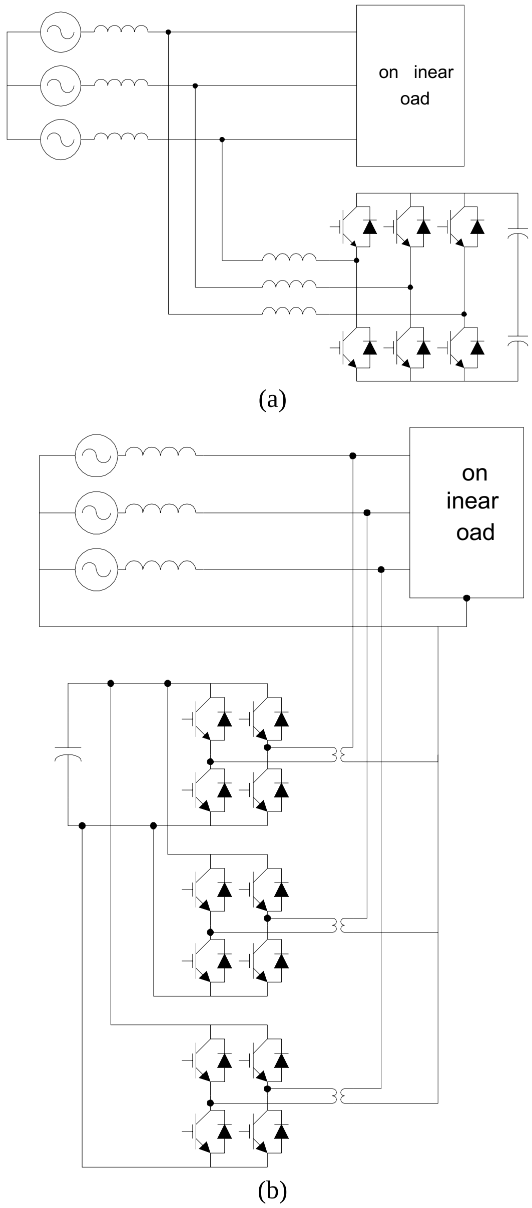
FIGURE 33.2 Compensation characteristics of a shunt active power filter.

system sees the non-linear load and the active power filter as an ideal resistor. The compensation characteristics of the shunt active power filter is shown in Fig. 33.2.

33.3.1 Power Circuit Topologies

Shunt active power filters are normally implemented with PWM voltage-source inverters. In this type of application, the PWM-VSI operates as a current-controlled voltage-source. Traditionally, 2 levels PWM-VSI have been used to implement such system connected to the ac bus through a transformer. This type of configuration is aimed to compensate nonlinear load rated in the medium power range (hundreds of kVA) due to semiconductors rated values limitations. However, in the last years multilevel PWM voltage-source inverters have been proposed to develop active power filters for medium voltage and higher rated power applications. Also, active power filters implemented with multiples of VSI connected in parallel to a dc bus but in series through a transformer or in cascade have been proposed in the technical literature. The different power circuit topologies are shown in Fig. 33.3.

The use of VSI connected in cascade is an interesting alternative to compensate high power nonlinear loads. The use of two PWM-VSI with different rated power allows the use of different switching frequencies, reducing switching stresses and commutation losses in the overall compensation system. The power circuit configuration of such a system is shown in Fig. 33.4.



(a)

(b)

FIGURE 33.3 Shunt active power filter topologies implemented with PWM voltage-source inverters. (a) A three-phase PWM unit. (b) Three single-phase units in parallel to a common dc bus.

The voltage-source inverter connected closer to the load compensates for the displacement power factor and lower frequency current harmonic components (Fig. 33.5(b)), while the second compensates only high frequency current harmonic components. The first converter requires higher rated power than the second and can operate at lower switching frequency. The compensation characteristics of the cascade shunt active power filter is shown in Fig. 33.5.

In recent years, there has been an increasing interest in using multilevel inverters for high power energy conversion, specially for drives and reactive power compensation. The

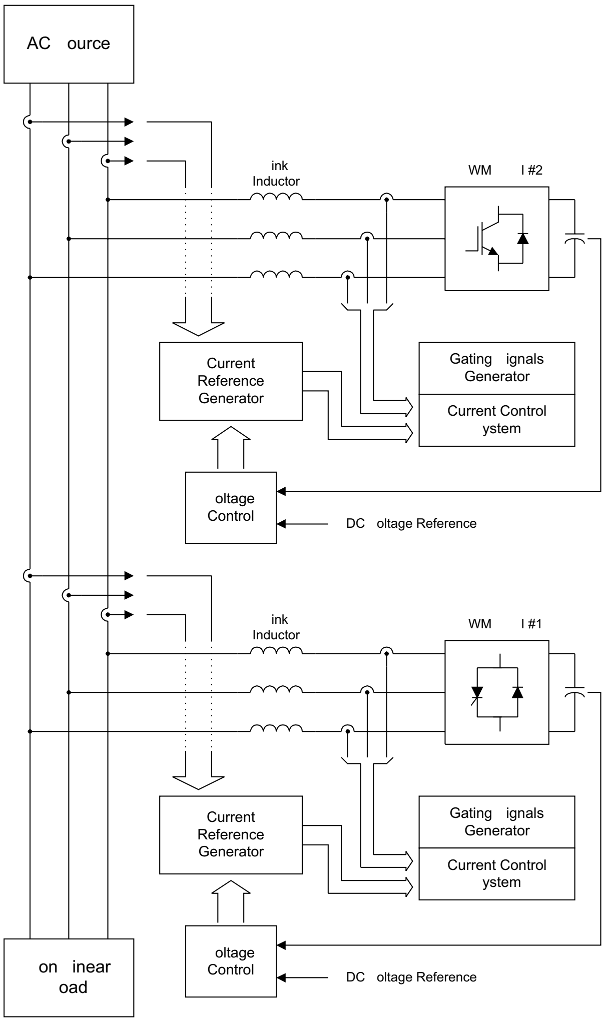

AC ource
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FIGURE 33.4 A shunt active power filter implemented with two PWM VSI connected in cascade.

use of neutral-point-clamped (NPC) inverters (Fig. 33.6) allows equal voltage shearing of the series connected semiconductors in each phase. Basically, multilevel inverters have been developed for applications in medium voltage ac motor drives and static var compensation. For these types of applications, the output voltage of the multilevel inverter must be able to generate an almost sinusoidal output current. In order to generate a near sinusoidal output current, the output voltage should not contain low frequency harmonic components.

However, for active power filter applications the three level NPC inverter output voltage must be able to generate an output current that follows the respective reference current containing the harmonic and reactive component required by the load. Currents and voltage waveforms obtained for a shunt active power filter implemented with a three-level NPC-VSI are shown in Fig. 33.7.

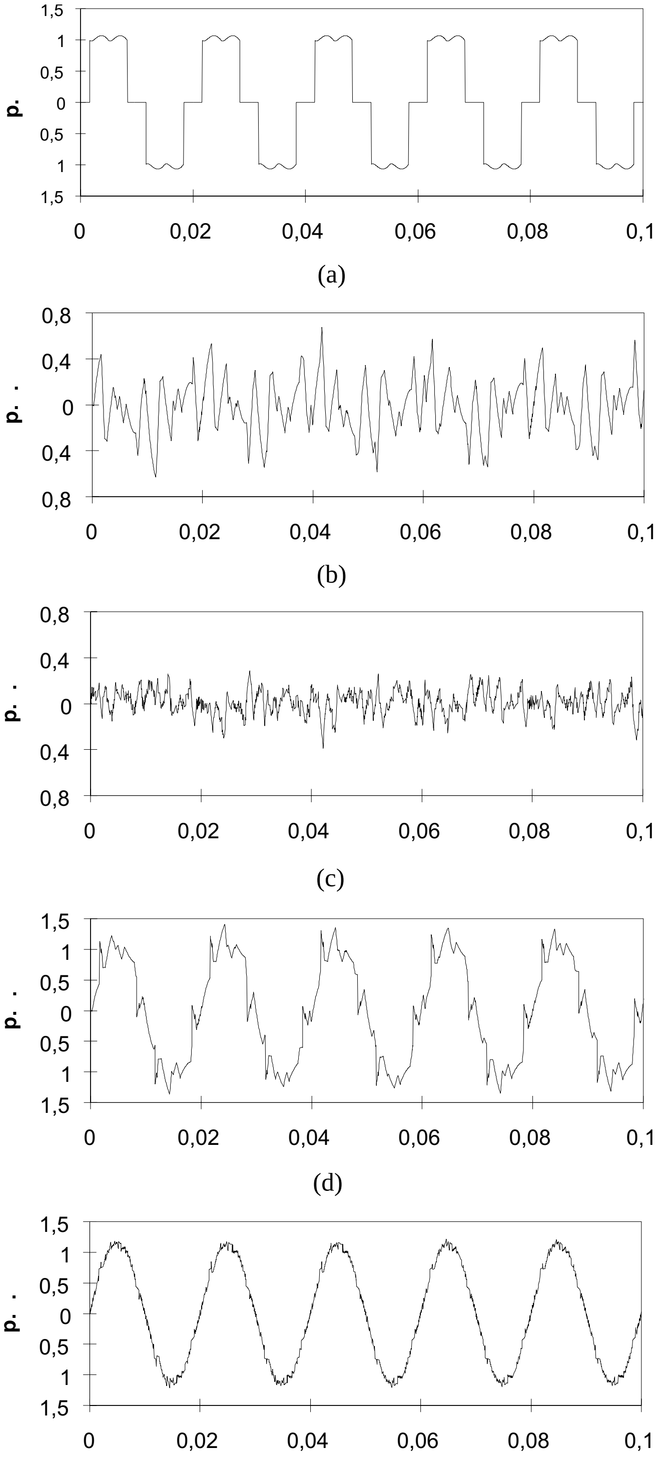


FIGURE 33.5 Current and voltage waveforms of active power filter implemented with two PWM VSI in cascade. (a) Load current waveform. (b) Current waveform generated by PWM VSI 1. (c) Current waveform generated by PWM VSI 2. (d) Power system current waveform between the two inverters (THDi = 13.7). (e) Power system current waveform (THDi = 4.5).

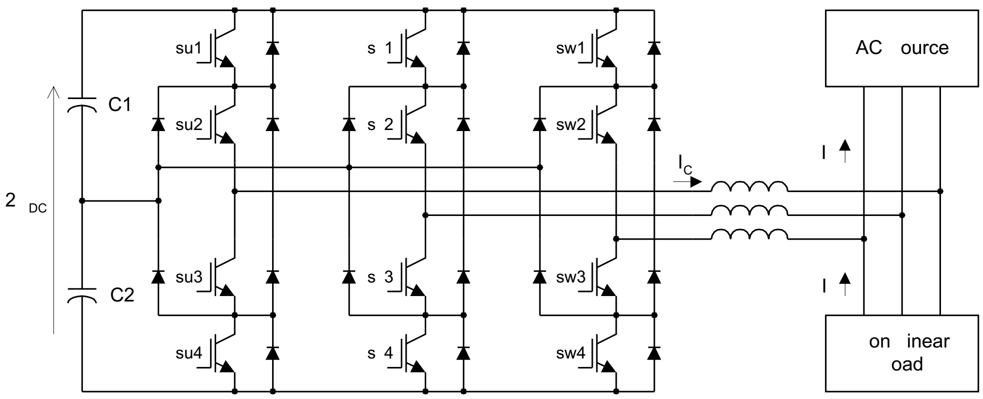
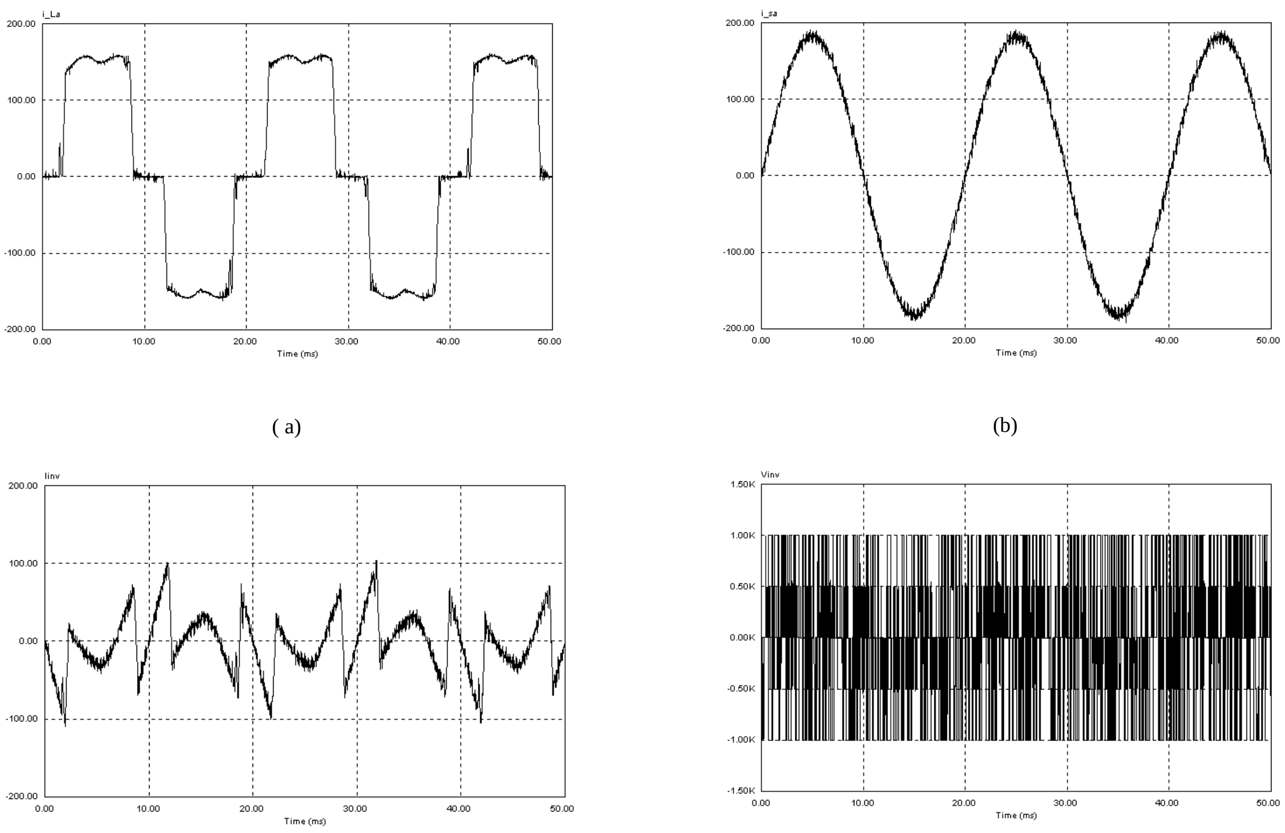


FIGURE 33.6 A shunt active power filter implemented with a three-level neutral point-clamped VSI.

33.3.2 Control Scheme

The control scheme of a shunt active power filter must calculate the current reference waveform for each phase of the inverter, maintain the dc voltage constant, and generate the inverter gating signals. The block diagram of the control scheme of a shunt active power filter is shown in Fig. 33.8.

The current reference circuit generates the reference currents required to compensate the load current harmonics and reactive power, and also try to maintain constant the dc voltage across the electrolytic capacitors. There are many possibilities to implement this type of control, and two of them will be explained in this chapter. Also, the compensation



(a)

(b)

(c)

(d)

FIGURE 33.7 Current and voltage waveforms for a shunt active power filter implemented with a three level NPC VSI. (a) Load current. (b) Compensated system current (THD = 3.5) (c) Current generated by the shunt active power filter. (d) Inverter output voltage.

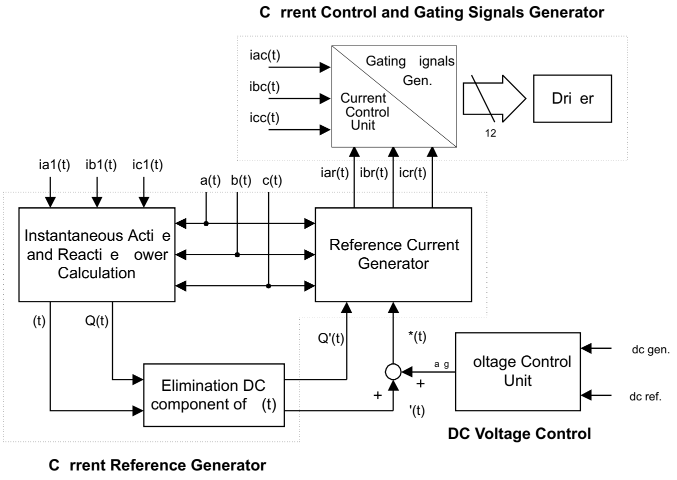


FIGURE 33.8 The block diagram of a shunt active power filter control scheme.

effectiveness of an active power filter depends on its ability to follow with a minimum error and time delay the reference signal calculated to compensate the distorted load current. Finally, the dc voltage control unit must keep the total dc bus voltage constant and equal to a given reference value. The dc voltage control is achieved by adjusting the small amount of real power absorbed by the inverter. This small amount of real power is adjusted by changing the amplitude of the fundamental component of the reference current.

33.3.2.1 Current Reference Generation

There are many possibilities to determine the reference current required to compensate the nonlinear load. Normally, shunt active power filters are used to compensate the displacement power factor and low frequency current harmonics generated by nonlinear loads. One alternative to determine the current reference required by the voltage-source inverter is the use of the instantaneous reactive power theory, proposed by Akagi [1]. This concept is very popular and useful for this type of application, and basically consists of a variable transformation from the ***a***, , ***c*** reference frame of the instantaneous power, voltage and current signals to the α, β reference frame. The transformation equations from the ***a***, , ***c*** reference frame to the α, β coordinates can be derived from the phasor diagram shown in Fig. 33.9.

The instantaneous values of voltages and currents in the α, β coordinates can be obtained from the following equations:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = [A] \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \qquad \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = [A] \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{33.1}$$

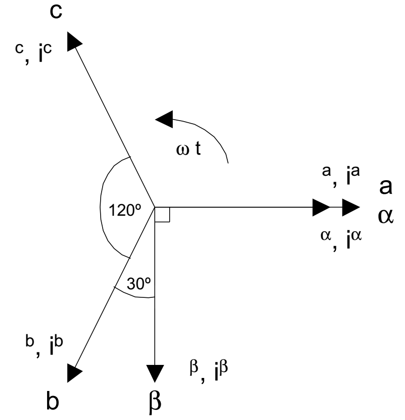


FIGURE 33.9 Transformation diagram from the ***a***, , ***c*** reference frame to the α, β coordinates.

where A is the transformation matrix, derived from Fig. 33.9 and is equal to

$$[A] = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}. \tag{33.2}$$

This transformation is valid if and only if $\boldsymbol{v_a(t) + v\ (t) + v_c(t)}$ is equal to zero, and also if the voltages are balanced and sinusoidal. The instantaneous active and reactive power in the $\alpha{-}\beta$ coordinates are calculated with the following expressions:

$$p(t) = v_\alpha(t) i_\alpha(t) + v_\beta(t) i_\beta(t) \tag{33.3}$$

$$q(t) = -v_\alpha(t) i_\beta(t) + v_\beta(t) i_\alpha(t) \tag{33.4}$$

It is evident that $p(t)$ becomes equal to the conventional instantaneous real power defined in the ***a***, , ***c*** reference frame. However, in order to define the instantaneous reactive power, Akagi introduces a new instantaneous space vector defined by expression (33.4) or by the vector equation:

$$= \boldsymbol{v}_\alpha \times \boldsymbol{i}_\beta + \boldsymbol{v}_\beta \times \boldsymbol{i}_\alpha. \tag{33.5}$$

The vector is perpendicular to the plane of α, β coordinates, to be faced in compliance with a right-hand rule, and $\boldsymbol{v}_\alpha$ is perpendicular to $\boldsymbol{i}_\beta$, and $\boldsymbol{v}_\beta$ is perpendicular to $\boldsymbol{i}_\alpha$. The physical meaning of the vector is not “instantaneous power” because of the product of the voltage in one phase and the current in the other phase. On the contrary, $\boldsymbol{v}_\alpha \boldsymbol{i}_\alpha$ and $\boldsymbol{v}_\beta \boldsymbol{i}_\beta$ in Eq. (33.3) obviously mean “instantaneous power” because of the product of the voltage in one phase and the current in the same phase. Akagi named the new electrical quantity defined in (33.5) “instantaneous imaginary power”, which is represented by the product of the instantaneous voltage and current, but cannot be treated as a conventional quantity.

The expression of the currents in the α–β plane, as a function of the instantaneous power is given by the following equation:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \cdot \left\{ \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \cdot \begin{bmatrix} p \\ 0 \end{bmatrix} + \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \cdot \begin{bmatrix} 0 \\ q \end{bmatrix} \right\} \equiv \begin{bmatrix} i_{\alpha p} \\ i_{\beta p} \end{bmatrix} + \begin{bmatrix} i_{\alpha q} \\ i_{\beta q} \end{bmatrix} \tag{33.6}$$

and the different components of the currents in the α, β plane are shown in the following expressions:

$$i_{\alpha p} = \frac{v_\alpha p}{v_\alpha^2 + v_\beta^2} \tag{33.7}$$

$$i_{\alpha q} = \frac{v_\beta q}{v_\alpha^2 + v_\beta^2} \tag{33.8}$$

$$i_{\beta p} = \frac{v_\beta p}{v_\alpha^2 + v_\beta^2} \tag{33.9}$$

$$i_{\beta q} = \frac{-v_\alpha q}{v_\alpha^2 + v_\beta^2} \tag{33.10}$$

From Eqs. (33.3) and (33.4), the values of $\boldsymbol{p}$ and $\boldsymbol{q}$ can be expressed in terms of the dc components plus the ac components, that is:

$$p = \bar{p} + \tilde{p} \tag{33.11}$$

$$q = \bar{q} + \tilde{q} \tag{33.12}$$

where

- $\bar{p}$: dc component of the instantaneous power $\boldsymbol{p}$, and is related to the conventional fundamental active current.
- $\tilde{p}$: is the ac component of the instantaneous power $\boldsymbol{p}$, it does not have average value, and is related to the harmonic currents caused by the ac component of the instantaneous real power.
- $\bar{q}$: is the dc component of the imaginary instantaneous power $\boldsymbol{q}$, and is related to the reactive power generated by the fundamental components of voltages and currents.
- $\tilde{q}$: is the ac component of the instantaneous imaginary power $\boldsymbol{q}$, and is related to the harmonic currents caused by the ac component of instantaneous reactive power.

In order to compensate reactive power (displacement power factor) and current harmonics generated by nonlinear loads, the reference signal of the shunt active power filter must include the values of $\tilde{p}$, $\bar{q}$, and $\tilde{q}$. In this case the reference currents required by the shunt active power filters are calculated with the following expression:

$$\begin{bmatrix} i_{c,\alpha} \\ i_{c,\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \cdot \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \cdot \begin{bmatrix} \tilde{P}_L \\ \bar{q}_L + \tilde{q}_L \end{bmatrix}. \tag{33.13}$$

The final compensating currents including the zero sequence components in $\boldsymbol{a}$, $\boldsymbol{b}$, $\boldsymbol{c}$ reference frame are the following:

$$\begin{bmatrix} i_{c,a} \\ i_{c,b} \\ i_{c,c} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} -i_0 \\ i_{c,\alpha} \\ i_{c,\beta} \end{bmatrix} \tag{33.14}$$

where the zero sequence current component i_0 is equal to $1/\sqrt{3}\,(\boldsymbol{i_a} + \boldsymbol{i_b} + \boldsymbol{i_c})$. The block diagram of the circuit required to generate the reference currents defined in (33.14) is shown in Fig. 33.10.

The advantage of $\boldsymbol{p}$–$\boldsymbol{q}$ theory is that real and reactive power associated with fundamental components are dc quantities. These quantities can be extracted with a low pass filter. Since the signal to be extracted is dc, filtering of the signal in the

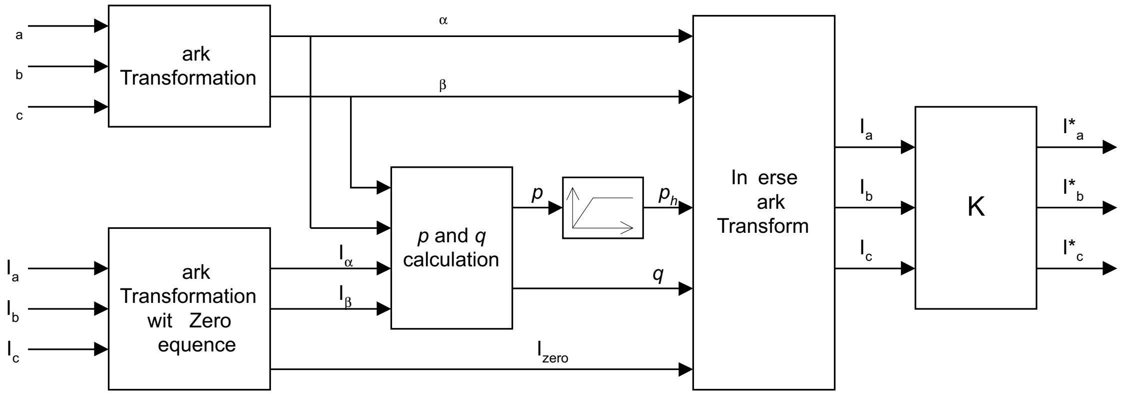


FIGURE 33.10 The block diagram of the current reference generator using $\boldsymbol{p}$–$\boldsymbol{q}$ theory.

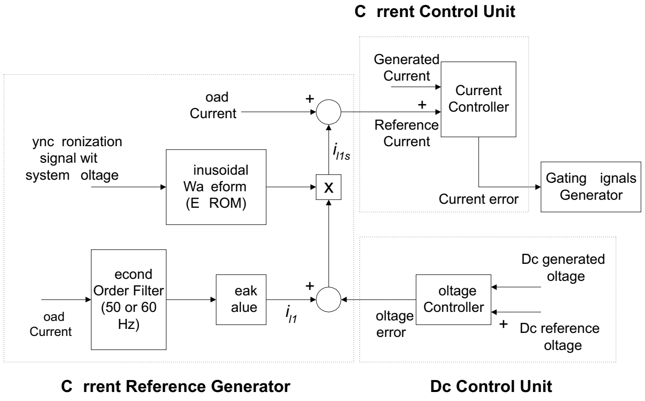


FIGURE 33.11 The block diagram of an active power filter control scheme that does not use the instantaneous reactive power concept.

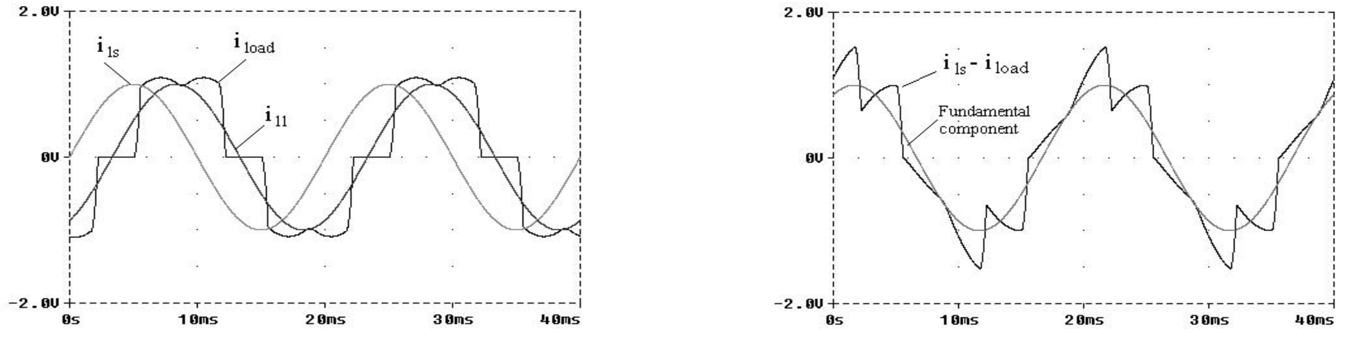
$\alpha-\beta$ reference frame is insensitive to any phase shift errors introduced by the low pass filter, improving compensation characteristics of the active power filter. The same advantage can be obtained by using the *Synchronous Reference Frame Method*, proposed in [2]. In this case transformation from a, , c axes to $d-$ synchronous reference frame is done.

There are other possibilities to generate the current reference signal required to compensate reactive power and current harmonics. Basically, all the different schemes try to obtain the current reference signals that include the reactive components required to compensate the displacement power factor and the current harmonics generated by the nonlinear load. Figure 33.11 shows another scheme used to generate the current reference signals required by a shunt active power filter. In this case the ac current generated by the inverter is forced to follow the reference signal obtained from the current reference generator. In this circuit, the distorted load current is filtered, extracting the fundamental component, i_{l1}. The band-pass filter is tuned at the fundamental frequency (50 or 60 Hz), so that the gain attenuation introduced in the filter output signal is zero and the phase-shift angle is 180°. Thus, the filter output current is exactly equal to the fundamental component of the load current but phase shifted by 180°. If the load current is added to the fundamental current component obtained from the second order band-pass filter, the reference current waveform required to compensate only harmonic distortion is obtained. In order to provide the reactive power required by the load, the current signal obtained from the second order band-pass filter I_{l1}, is synchronized with the respective phase-to-neutral source voltage (see Fig. 33.12) so that the inverter ac output current is forced to lead the respective inverter output voltage, thereby generating the required reactive power and absorbing the real power necessary to supply the switching losses and also to maintain the dc voltage constant (see Fig. 33.12).

The real power absorbed by the inverter is controlled by adjusting the amplitude of the fundamental current reference waveform, I_{l1}, obtained from the reference current generator. The amplitude of this sinusoidal waveform is equal to the amplitude of the fundamental component of the load current plus or minus the error signal obtained from the dc voltage control unit. In this way, the current signal allows the inverter to supply the current harmonic components, the reactive power required by the load, and to absorb the small amount of active power necessary to cover the switching losses and to keep the dc voltage constant.

33.3.2.2 Current Modulator

The effectiveness of an active power filter depends basically on the design characteristics of the current controller, the method implemented to generate the reference template and the modulation technique used. Most of the modulation techniques used in active power filters are based on PWM strategies. In this chapter, four of these methods, whose characteristics are their simplicity and effectiveness, are analyzed: Periodical Sampling Control, Hysteresis Band Control, Triangular Carrier Control, and Vector Control. The first three methods have been tested with different waveform templates sinusoidal, quasisquare and rectifier compensation current and were compared in terms of the harmonic content and distortion at the same switching frequency [3]. The analysis shows that



(a) (b)

FIGURE 33.12 The procedure for the generation of the current reference waveform. (a) The load current i_{load}, its fundamental component, i_{l1}, and the fundamental current component synchronized with the respective phase-to-neutral source voltage, i_{ls}. (b) The synchronized fundamental current signal minus the load current, $i_{ls} - i_{load}$, and its fundamental component.

for sinusoidal current generation the best method is Triangular Carrier, followed by the Hysteresis Band and Periodical Sampling. For other types of references, however, one strategy may be better than the others. Also it was shown that each control method is affected in a different way by the switching time delays present in the driving circuitry and in the power semiconductors.

The Periodical Sampling method switches the power transistors of the converter during the transitions of a square wave clock of fixed frequency (the sampling frequency) As shown in Fig. 33.13(a), this type of control is very simple to implement since it requires a comparator and a D-type flip-flop per phase. The main advantage of this method is that the minimum time between switching transitions is limited to the period of the sampling clock. However, the actual switching frequency is not clearly defined.

The Hysteresis Band method switches the transistors when the current error exceeds a fixed magnitude: the hysteresis band. As can be seen in Fig. 33.13(b), this type of control needs a single comparator with hysteresis per phase. In this case the switching frequency is not determined, but it can be estimated.

The Triangular Carrier method, shown in Fig. 33.13(c), compares the current error with a fixed amplitude and fixed frequency triangular wave (the triangular carrier). The error is processed through a proportional-integral (PI) gain stage before the comparison with the triangular carrier takes place. As can be seen, this control scheme is more complex than the Periodical Sampling and Hysteresis Band. The values for the PI control gain k_p and k_i determine the transient response and steady-state error of the Triangular Carrier method. It was found empirically that the values for k_p and k_i shown in Eqns. (33.15) and (33.16) give a good dynamic performance under transient and steady-state operating conditions:

$$k_i = \frac{(L + L_0) \cdot \omega_c}{2V_{dc}} \tag{33.15}$$

$$k_i = \omega_c k_p \tag{33.16}$$

where $L + L_0$ is the total series inductance seen by the converter, ω_c is the triangular carrier frequency, which amplitude is one volt peak–peak, and V_{dc} is the dc supply voltage of the inverter.

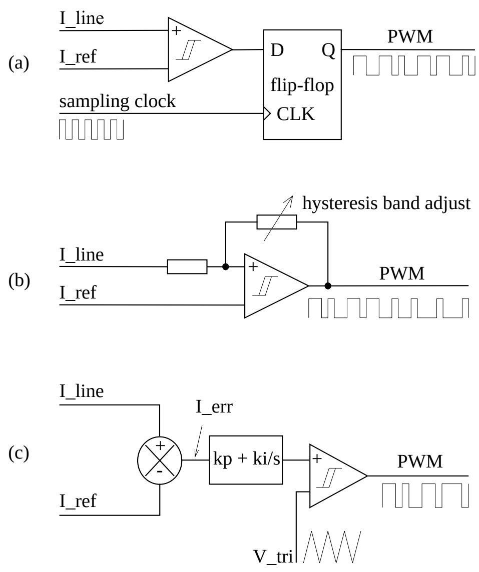


FIGURE 33.13 Modulation control blocks. (a) Periodical sampling. (b) Hysteresis band. (c) Triangular carrier.

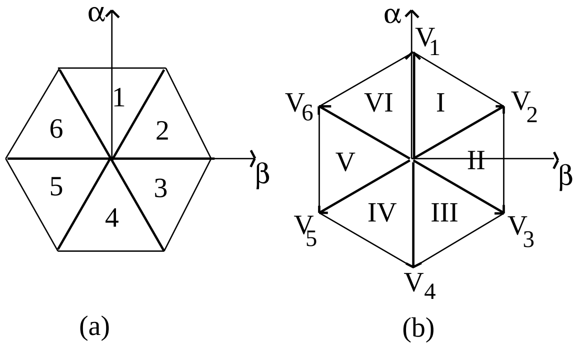


FIGURE 33.14 The hexagons defined in the $\alpha-\beta$ reference frame by the current control scheme. (a) The hexagon defined by the inverter output current vector. (b) The hexagon defined by the inverter output voltage vector.

. . . . ***Vector Control Technique*** This current control technique proposed in [4] divides the $\alpha-\beta$ reference frame of currents and voltages in six regions, phase-shifted by 30° (Fig. 33.14), identifies the region where the current vector error Δi is located, and selects the inverter output voltage vector $V_{\mathbf{inv}}$ that will force Δi to change in the opposite direction, keeping the inverter output current close to the reference signal.

Figure 33.15 shows the single phase equivalent circuit of the shunt active power filter connected to a nonlinear load and to the power supply.

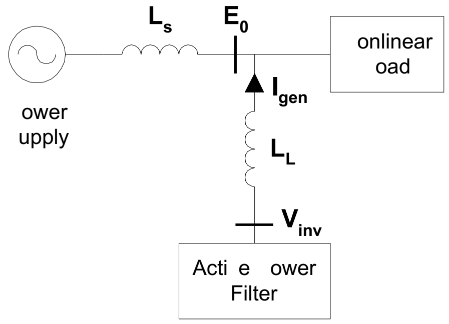


FIGURE 33.15 The single-phase equivalent circuit of a shunt active power filter connected to the power system.

The equation that relates the active power filter currents and voltages is obtained by applying Kirchhoff law to the equivalent circuit shown in Fig. 33.15:

$$V_{\text{inv}} = L\frac{di_{\text{gen}}}{dt} + E_0 \tag{33.17}$$

The current error vector Δi is defined by the following expression:

$$\Delta_i = i_{\text{ref}} - i_{\text{gen}} \tag{33.18}$$

where i_{ref} represents the inverter reference current vector defined by the instantaneous reactive power concept. By replacing (33.18) in (33.17):

$$V_{\text{inv}} = L\frac{d}{dt}(i_{\text{ref}} - \Delta i) + E_0 \Rightarrow L\frac{d\Delta i}{dt} = L\frac{di_{\text{ref}}}{dt} + E_0 - V_{\text{inv}}. \tag{33.19}$$

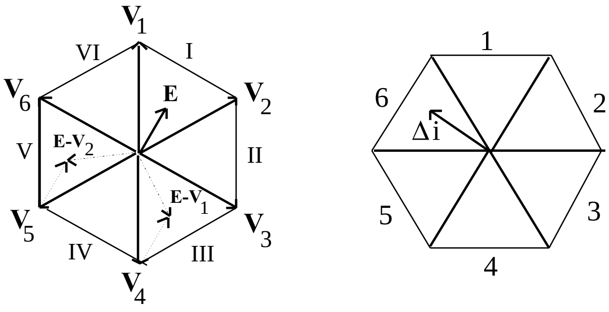
If $E = L(di_{\text{ref}}/dt) + E_{\text{o}}$ then (2.20) becomes

$$L\frac{d\Delta i}{dt} = E - V_{\text{inv}}. \tag{33.20}$$

Equation (33.20) represents the active power filter state equation and shows that the current error vector variation $d\Delta i/dt$ is defined by the difference between the fictitious voltage vector E and the inverter output voltage vector V_{inv}. In order to keep $d\Delta i/dt$ close to zero, V_{inv} must be selected near E.

The selection of the inverters' gating signals is defined by the region in which Δi is located and by its amplitude. In order to improve the current control accuracy and associate time response, depending on the amplitude of Δi the following actions are defined:

– if $\Delta i \leq \delta$ the gating signals of the inverter are not changed,
– if $h \leq \Delta i \leq \delta$, the inverter gating signals are defined following Mode a,
– if $\Delta i > h$, the inverter gating signals are defined following Mode b



(a) (b)

FIGURE 33.16 Selection of the inverter switching pattern according to the region where Δi and E are located. (a) The regions where $Ld\Delta i/dt$ are located. (b) The region where Δi is located.

where δ and h are reference values that defines the accuracy and the hysterisis window of the current control scheme.

Mode a: Small Changes in $\Delta i(h \leq \Delta i \leq \delta)$ The selection of the inverter switching Mode a can be explained with the following example. Assuming that the voltage vector E is located in region I (Fig. 33.16(a)) and the current error vector Δi is in region 6 (Fig. 33.16(b)) the inverter voltage vectors, V_{inv}, located closest to E are V_1 and V_2. The vectors $E - V_2$ and $E - V_1$ define two vectors $Ld\Delta i/dt$, located in region III and V respectively, as shown in Fig. 33.15(a), so in order to reduce the current vector error Δi, $Ld\Delta i/dt$ must be located in region III. Thus the inverter output voltage has to be equal to V_1. In this way Δi will be forced to change in the opposite direction, reducing its amplitude faster. By doing the same analysis for all the possible combinations, the inverter switching modes for each location of Δi and E can be defined (Table 33.2). V_k represents the inverter switching functions defined in Table 33.3.

Mode b: Large Changes in $\Delta i(\Delta i > h)$ If Δi becomes larger than h in a transient state, it is necessary to choose the switching mode in which the $d\Delta i/dt$ has the largest opposite direction to Δi. In this case the best inverter output voltage V_{inv} corresponds to the value located in the same region of $\boldsymbol{\Delta i}$.

The switching frequency may be fixed by controlling the time between commutations and by not applying a new

TABLE 33.2 Inverter switching modes

E Region	Δi Region 1	2	3	4	5	6
I	V_1	V_2	V_2	$V_0 - V_7$	$V_0 - V_7$	V_1
II	V_2	V_2	V_3	V_3	$V_0 - V_7$	$V_0 - V_7$
III	$V_0 - V_7$	V_3	V_3	V_4	V_4	$V_0 - V_7$
IV	$V_0 - V_7$	$V_0 - V_7$	V_4	V_4	V_5	V_5
V	V_6	$V_0 - V_7$	$V_0 - V_7$	V_5	V_5	V_6
VI	V_1	V_1	$V_0 - V_7$	$V_0 - V_7$	V_6	V_6

TABLE 33.3 Relationship between switching function and inverter output voltage

k	Switch on Phase a	Switch on Phase b	Switch on Phase c	Inverter Output Voltage V_k
0	4	6	2	0
1	1	6	2	$\frac{2}{3}V_{dc}$
2	1	3	2	$\frac{2}{3}V_{dc}e^{j\pi/3}$
3	4	3	2	$\frac{2}{3}V_{dc}e^{j2\pi/3}$
4	4	3	5	$\frac{2}{3}V_{dc}e^{j\pi}$
5	4	6	5	$\frac{2}{3}V_{dc}e^{j4\pi/3}$
6	1	6	5	$\frac{2}{3}V_{dc}e^{j5\pi/3}$
7	1	3	5	0

switching pattern if the time between two successive commutations is lower than a selected value ($t = \frac{1}{2}f_c$).

Figure 33.17 shows the block diagram of the inverter vector current control scheme implemented in a microcontroller. In Fig. 33.17 E represents the region where the vector E is located, Δi the region of Δi, k_1 keeps the same value of k (no commutation in the inverter), k_2 selects the new inverter output voltage from Table 33.2, and k_3 selects V_{inv} in the same region of Δi.

33.3.2.3 Control loops Design

Active power filters based on self controlled dc bus voltage requires two control loops, one to control the inverter output current and the other to regulate the inverter dc voltage. Different design criteria have been presented in the technical literature; however, a classic design procedure using a PI controller will be presented in this chapter. In general, the design procedure for the current and voltage loops is based on the respective time response requirements. Since the transient response of the active power is determined by the current control loop, its time response has to be fast enough to follow the current reference waveform closely. On the other hand, the time response of the dc voltage does not need to be fast and is selected to be at least ten times slower than the current control loop time response. Thus, these two control systems can be decoupled and designed as two independent systems.

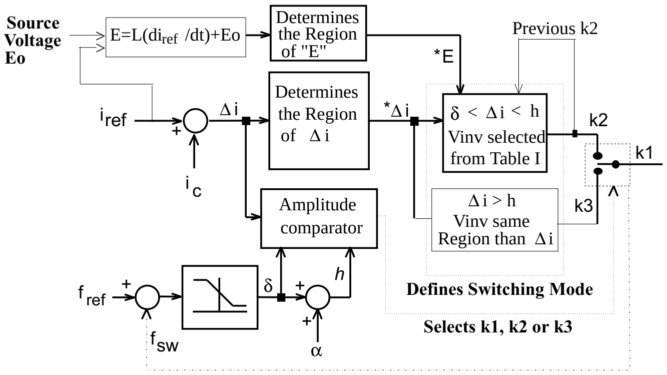


FIGURE 33.17 The current control block diagram.

A PI controller is normally used for the current and the voltage control loops since it contributes to zero steady-state error in tracking the reference current and voltage signals, respectively.

. . . . *Design of the Current Control Loop* The design of the current control loop gains depends on the selected current modulator. In the case of selecting the triangular carrier technique, to generate the gating signals, the error between the generated current and the reference current is processed through a PI controller, then the output current error is compared with a fixed amplitude and fixed frequency triangular wave (Fig. 33.13(c)) The advantage of this current modulator technique is that the output current of the converter has well defined spectral line frequencies for the switching frequency components.

Since the active power filter is implemented with a voltage-source inverter, the ac output current is defined by the inverter ac output voltage. The block diagram of the current control loop for each phase is shown in Fig. 33.18 where

E phase to neutral source voltage,
$Z(s)$ impedance of the link reactor,
K_s gain of the converter,
$Gc(s)$ gain of the controller.

The values of K_s and $Gc(s)$ are given in (33.21) and (33.22).

$$K_s = \frac{V_{dc}}{2\xi} \tag{33.21}$$

$$Gc(s) = K_p + \frac{K_i}{s} \tag{33.22}$$

From Fig. 33.18 and (33.22), the following expression is obtained:

$$I_{gen} = \frac{\dfrac{K_s\left(K_p + \dfrac{K_i}{s}\right)}{R_r + sL_r}}{1 + \dfrac{K_s\left(K_p + \dfrac{K_i}{s}\right)}{R_r + sL_r}} I_{ref} - \frac{\dfrac{1}{R_r + sL_r}}{1 + \dfrac{K_s\left(K_p + \dfrac{K_i}{s}\right)}{R_r + sL_r}} E \tag{33.23}$$

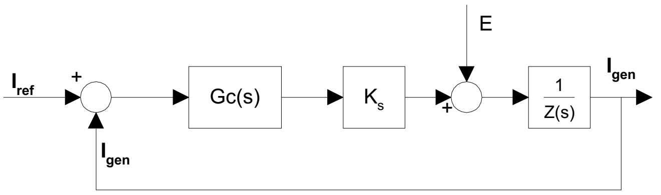


FIGURE 33.18 The block diagram of the current control loop.

The characteristic equation of the current loop is given by

$$1 + \frac{K_p s + \frac{K_i}{s}}{s(R_r + sL_r)}. \tag{33.24}$$

The analysis of the characteristic equation proves that the current control loop is stable for all values of K_p and K_i. Also, this analysis shows that K_p determines the speed response and K_i defines the damping factor of the control loop. If K_p is too big, the error signal can exceed the amplitude of the triangular waveform, affecting the inverter switching frequency, and if K_i is too small, the gain of the PI controller decreases, which means that the generated current will not be able to follow the reference current closely. The active filter transient response can be improved by adjusting the gain of the proportional part (K_p) to equal one and the gain of the integrator (K_i) to equal the frequency of the triangular waveform.

. . . . ***DC Voltage Control Loop*** Voltage control of the dc bus is performed by adjusting the small amount of real power flowing into the dc capacitor, thus compensating for the conduction and switching losses. The voltage loop is designed to be at least 10 times slower than the current loop; hence the two loops can be considered decoupled. The dc voltage control loop needs not to be fast, since it only responds for steady-state operating conditions. Transient changes in the dc voltage are not permitted and are taken into consideration with the selection criteria of the appropriate electrolytic capacitor value.

33.3.3 Power Circuit Design

The selection of the ac link reactor and the dc capacitor values affects directly the performance of the active power filter. Static var compensators implemented with voltage-source inverters present the same power circuit topology, but for this type of application, the criteria used to select the values of L_r and C are different. For reactive power compensation, the design of the synchronous link inductor, L_r, and the dc capacitor, C, is performed based on harmonic distortion constrain. That is, L_r must reduce the amplitude of the current harmonics generated by the inverter while C must keep the dc voltage ripple factor below a given value. This design criteria cannot be applied in the active power filter since it must be able to generate distorted current waveforms. However, L_r must be specified so that it keeps the high-frequency switching ripple of the inverter ac output current smaller than a defined value.

33.3.3.1 Design of the Synchronous Link Reactor

The design of the synchronous link reactor depends on the current modulator used. The design criteria presented in this section is based on considering that the triangular carrier modulator is used. The design of the synchronous reactor is performed with the constraint that, for a given switching frequency, the minimum slope of the inductor current is smaller than the slope of the triangular waveform that defines the switching frequency. In this way, the intersection between the current error signal and the triangular waveform will always exist. In the case of using another current modulator, the design criteria must allow an adequate value of L_r in order to ensure that the di/dt generated by the active power filter will be able to follow the inverter current reference closely. In the case of the triangular carrier technique, the slope of the triangular waveform, λ, is defined by

$$\lambda = 4\xi f_t \tag{33.25}$$

where ξ is the amplitude of the triangular waveform, which has to be equal to the maximum permitted amount of ripple current, and f_t is the frequency of the triangular waveform (i.e., the inverter switching frequency). The maximum slope of the inductor current is equal to

$$\frac{di_L}{dt} = \frac{V_{an} + 0.5V_{dc}}{L_r}. \tag{33.26}$$

Since the slope of the inductor current (di_L/dt) has to be smaller than the slope of the triangular waveform (λ), and the ripple current is defined, from (33.25) and (33.26), as

$$L_r = \frac{V_{an} + 0.5V_{dc}}{4\xi f_t} \tag{33.27}$$

33.3.3.2 Design of the DC Capacitor

Transient changes in the instantaneous power absorbed by the load generate voltage fluctuations across the dc capacitor. The amplitude of these voltage fluctuations can be controlled effectively with an appropriate dc capacitor value. It must be noticed that the dc voltage control loop stabilizes the capacitor voltage after a few cycles, but is not fast enough to limit the first voltage variations. The capacitor value obtained with this criteria is bigger than the value obtained based on the maximum dc voltage ripple constraint. For this reason, the voltage across the dc capacitor presents a smaller harmonic distortion factor. The maximum overvoltage generated across the dc capacitor is given by

$$V_{C_{max}} = \frac{1}{C}\int_{\theta_1/\omega}^{\theta_2/\omega} i_C(t)dt + V_{dc} \tag{33.28}$$

where $V_{c_{\max}}$ is the maximum voltage across the dc capacitor, V_{dc} is the steady-state dc voltage, and $i_C(t)$ is the instantaneous dc bus current. From (33.28)

$$C = \frac{1}{\Delta V}\int_{\theta_1/\omega}^{\theta_2/\omega} i_C(t)dt \tag{33.29}$$

Eqn. (33.29) defines the value of the dc capacitor, C, that will maintain the dc voltage fluctuation below ΔV p.u. The instantaneous value of the dc current is defined by the product of the inverter line currents with the respective switching functions. The mean value of the dc current that generates the maximum overvoltage can be estimated by

$$\int_{\theta_1/\omega}^{\theta_2/\omega} i_C(t)dt = I_{inv}\int_{\theta_1/\omega}^{\theta_2/\omega}[\sin(\omega t) + \sin(\omega t + 120^\circ)]dt \tag{33.30}$$

In this expression the inverter ac current is assumed to be sinusoidal. These operating conditions represent the worst case.

33.3.4 Technical Specifications

The standard specifications of shunt active power filters are the following:

- Number of phases: 3-phase and three wires or 3-phases and four wires.
- Input voltage: 200, 210, 220 ± 10%, 400, 420, 440 ± , 6600 ± 10%.
- Frequency: 50/60 Hz ± 5%.
- No. of restraint harmonic orders: 2–25 th.
- Harmonic restraint factor: 85% or more at the rated output.
- Type of rating: continuous.
- Response: 1 ms or less.

For shunt active power filter the harmonic restraint factor is defined as $(1 = I_{H_2}/I_{H_1}) \times 100\%$, where I_{H_1} are the harmonic currents flowing on the source side when no measure are taken for harmonic suppression, and I_{H_2} are the harmonic currents flowing on the source side when harmonics are suppressed using an active filter.

33.4 Series Active Power Filters

Series active power filters were introduced by the end of the 1980s [5], and operate mainly as a voltage regulator and as harmonic isolator between the nonlinear load and the utility system. The series connected active power filter is more preferable to protect the consumer from an inadequate supply voltage quality. This type of approach is specially recommended for compensation of voltage unbalances and voltage sags from the ac supply, and for low power applications represents an economically attractive alternative to UPS, since no energy storage (battery) is necessary and the overall rating of the components is smaller. The series active power filter injects a voltage component in series with the supply voltage and therefore can be regarded as a controlled voltage source, compensating voltage sags and swells on the load side (Fig. 33.19).

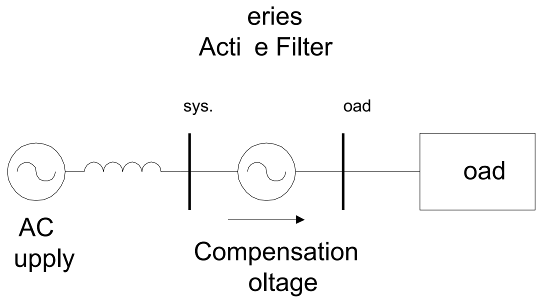


FIGURE 33.19 The series active power filter operating as a voltage compensator.

If passive LC filters are connected in parallel to the load, the series active power filter operates as an harmonic isolator forcing the load current harmonics to circulate mainly through the passive filter rather than the power distribution system (hybrid topology). The main advantage of this scheme is that the rated power of the series active power filter is a small fraction of the load kVA rating, typically 5%. However, the rating apparent power of the series active power filter may increase in case of voltage compensation.

33.4.1 Power Circuit Structure

The topology of the series active power filter is shown in Fig. 33.20. In most cases, the power circuit configuration is based

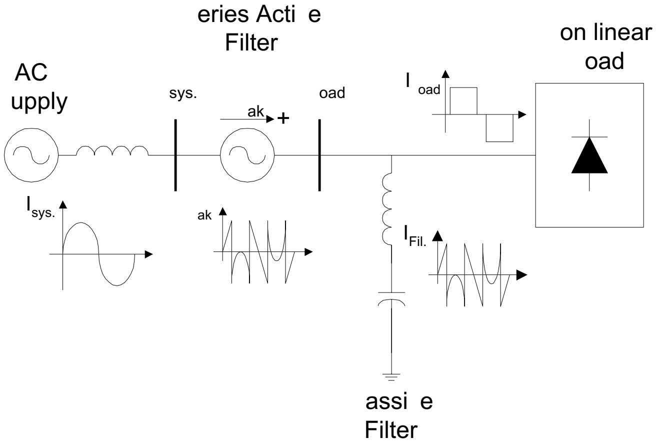


FIGURE 33.20 Combination of series active power filter and passive filter for current harmonic compensation.

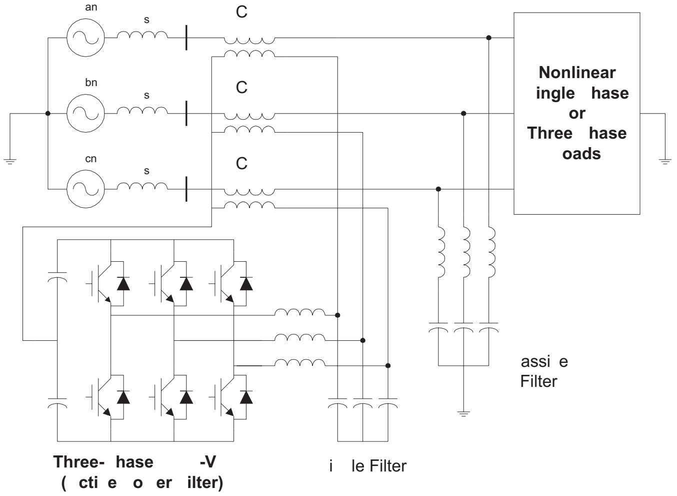


FIGURE 33.21 The series active power filter topology.

on a three-phase PWM voltage-source inverter connected in series with the power lines through three single-phase coupling transformers. For certain type of applications, the three-phase PWM voltage-source converter can be replaced by three single phase PWM inverters. However, this type of approach requires more power components, which increases the cost.

In order to operate as an harmonic isolator, a parallel LC filter must be connected between the nonlinear loads and the coupling transformers (Fig. 33.21) Current harmonic and voltage compensation are achieved by generating the appropriate voltage waveforms with the three-phase PWM voltage-source inverter, which are reflected in the power system through three coupling transformers. With an adequate control scheme series active power filters can compensate for current harmonics generated by nonlinear loads, voltage unbalances and voltage sags or swells at the load terminals. However, it is very difficult to compensate the load power factor with this type of topology. In four-wire power distribution systems, series active power filters with the power topology shown in Fig. 33.21 can also compensate the current harmonic components that circulate through the neutral conductor.

33.4.2 Principles of Operation

Series active power filters compensate current system distortion caused by nonlinear loads by imposing a high impedance path to the current harmonics, which forces the high frequency currents to flow through the LC passive filter connected in parallel to the load (Fig. 33.20) The high impedance imposed by the series active power filter is created by generating a voltage of the same frequency that the current harmonic component that needs to be eliminated. Voltage regulation or voltage unbalance can be corrected by compensating the fundamental frequency positive, negative and zero sequence voltage components of the power distribution system (Fig. 33.19). In this case, the series active power filter injects a voltage component in series with the supply voltage and therefore can be regarded as a controlled voltage source, compensating voltage regulation on the load side (sags or swells), and voltage unbalance. Voltage injection of arbitrary phase with respect to the load current implies active power transfer capabilities which increases the rating of the series active power filter. Voltage and current waveforms shown in Figs. 33.22, 33.23, and 33.24 illustrate the compensation characteristics of a series active power filter operating with a shunt passive filter.

33.4.3 Power Circuit Design

The power circuit topology of the series active power filter is composed by the three-phase PWM voltage source inverter, the second order resonant *LC* filters, the coupling transformers, and the secondary ripple frequency filter (Fig. 33.21) The design characteristics for each of the power components are described below.

33.4.3.1 PWM Voltage-Source Inverter

Since series active power filter can compensate voltage unbalance and current harmonics simultaneously, the rated power of the PWM voltage-source inverter increases compared with other approaches that compensate only current harmonics, since voltage injection of arbitrary phase with respect to the load current implies active power transfer from the inverter to the system. Also, the transformer leakage inductance entails

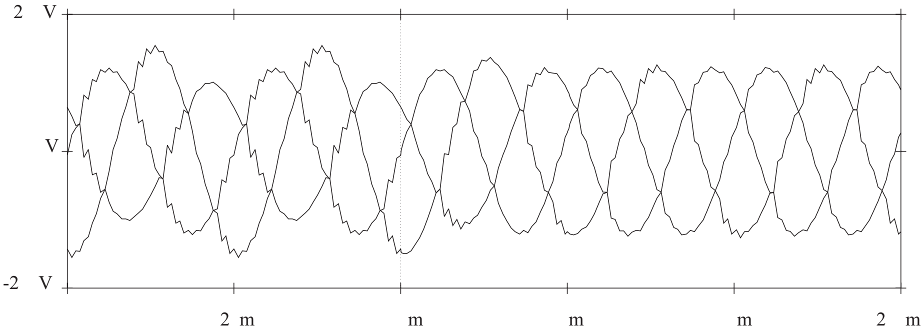


FIGURE 33.22 Load voltage waveforms for voltage unbalance compensation. Phase to neutral voltages at the load terminals before and after series compensation. (Compensation starts at 140 ms, current harmonic compensator not operating).

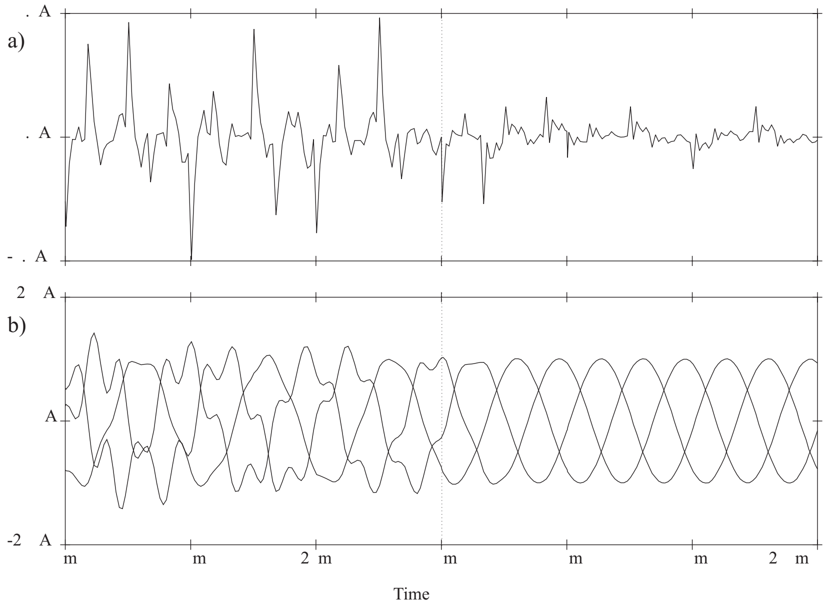


FIGURE 33.23 System current waveforms for current harmonic compensation. (a) Neutral current flowing to the ac mains before and after compensation. (b) Line currents flowing to the ac mains before and after compensation. (Voltage unbalance compensator not operating).

fundamental voltage drop and fundamental apparent power, which has to be supported by the inverter, reducing the series active filter inverter rating available for harmonic and voltage compensation. The rated apparent power required by the inverter can be obtained by calculating the apparent power generated in the primary of the coupling transformers. The voltage reflected across the primary winding of each coupling transformer is defined by the following expression:

$$V_{\text{series}} = \left[K_1^2 \left\{ \sum_{k \neq 1} I_{sk}^2 \right\}^{1/2} + K_2^2 (V_2 + V_0)^2 \right]^{1/2} \qquad (33.31)$$

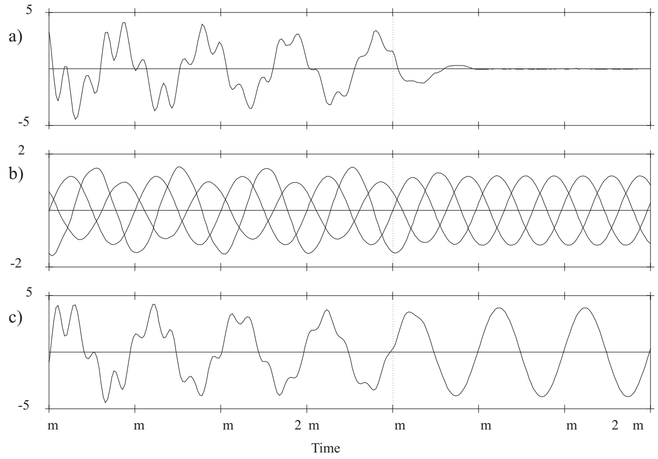


FIGURE 33.24 Load voltages and system currents for voltage unbalance and current harmonic compensation, before and after compensation. (a) Power system neutral current. (b) Phase-to-neutral load voltages. (c) Power system line current.

where V_{series} is the rms voltage across the primary winding of the coupling transformer. Equation (33.31) shows that the voltage across the primary winding of the transformer is defined by two terms. The first one is inversely proportional to the quality factor of the passive *LC* filter, while the second one depends on the voltage unbalance that needs to be compensated. K_1 depends on the *LC* filter values while K_2 is equal to one. The current flowing through the primary winding of the coupling transformer, due to the harmonic currents (Eqn. (33.32)), can be obtained from the equivalent circuit shown in Fig. 33.25:

$$I_{sk} = \frac{Z_{fk} I_{lk}}{Z_{fk} + Z_{sk} + K_1} \qquad (33.32)$$

where $V_{\text{series}} = -K_1 I_{sk}$. The fundamental component of the primary current depends on the amplitude of the negative and zero sequence component of the source voltage due to the system unbalance.

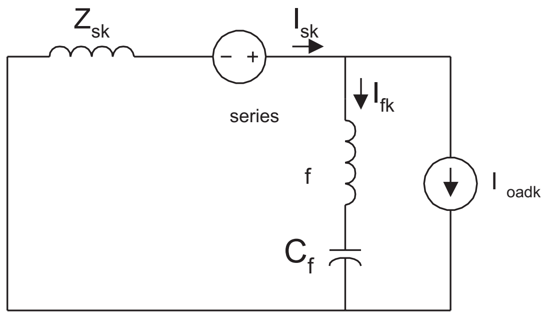


FIGURE 33.25 The equivalent circuit of the series active power filter for harmonic components.

33.4.3.2 Coupling Transformer

The purpose of the three coupling transformers is not only isolate the PWM inverters from the source but also to match the voltage and current ratings of the PWM inverters with those of the power distribution system. The total apparent power required by each coupling transformer is 1/3 the total apparent power of the inverter. The turn ratio of the current transformer is specified according to the inverter dc bus voltage, K_1 and V_{ref}. The correct value of the turn ratio "*a*" must be specified according to the overall series active power filter performance. The turn ratio of the coupling transformer must be optimized through the simulation of the overall active power filter, since it depends on the values of different related parameters. In general, the transformer turn ratio must be high in order to reduce the amplitude of the inverter output current and to reduce the voltage induced across the primary winding. Also, the selection of the transformer turn ratio influences the performance of the ripple filter connected at the output of the PWM inverter. Taking into consideration all these factors, in general, the transformer turn ratio is selected equal to 1 : 20.

33.4.3.3 Secondary Ripple Filter

The design of the ripple filter connected in parallel to the secondary winding of the coupling transformer is performed following the method presented by Akagi in [6]. However, it is important to notice that the design of the secondary ripple filter depends mainly on the coupling transformer turn ratio and on the current modulator used to generate the inverter gating signals. If the triangular carrier is used, the frequency of the triangular waveform has to be considered in the design of the ripple filter. The ripple filter connected at the output of the inverter avoid the induction of the high frequency ripple voltage generated by the PWM inverter switching pattern at the terminals of the primary winding of the coupling transformer. In this way, the voltage applied in series to the power system corresponds to the components required to compensate voltage unbalanced and current harmonics. The single-phase equivalent circuit is shown in Fig. 33.26.

The voltage reflected in the primary winding of the current transformer has the same waveform that the voltage across the filter capacitor has. For low frequency components, the inverter output voltage must be almost equal to the voltage across C_{fr}. However, for high frequency components, most of the inverter output voltage must drop across L_{fr}, in which case the voltage at the capacitor terminals is almost zero. Moreover, C_{fr} and L_{fr} must be selected in order not to exceed the burden of the coupling transformer. The ripple filter must be designed for the carrier frequency of the PWM voltage-source inverter. To calculate C_{fr} and L_{fr} the system equivalent impedance at the carrier frequency, Z_{sys}, reflected in the secondary must be known. This impedance is equal to

$$Z_{\mathrm{sys(secondary)}} = a^2 Z_{\mathrm{sys(primary)}} \tag{33.33}$$

For the carrier frequency, the following design criteria must be satisfied:

(i)	$_{Cfr} \ll {}_{Lfr}$	to ensure that at the carrier frequency most of the inverter output voltage will drop across L_{fr}.
(ii)	$_{Cfr}$ and $_{Lfr} \ll \boldsymbol{Z}\mathrm{sys}$	to ensure that the voltage divider is between L_{fr} and C_{fr}.

The small-rated LC passive filter exhibits a high quality factor circuit because of the high impedance on the output side. Oscillation between the small rated inductor and capacitor may occur, causing undesirable high frequency voltage across the ripple filter capacitor, which is reflected in the primary winding of the coupling transformer generating high frequency current to flow through the power distribution system. It is important to note that this oscillation is very difficult to eliminate through the design and selection of the L_{fr} and C_{fr} values. However, it can be eliminated with the addition of a new control loop. The cause of the output voltage oscillation is explained with the help of Fig. 33.27. The transfer function $Gp(s)$ between the input voltage $V_i(s)$ and the output voltage $V_C(s)$ is given by the equation:

$$G_p(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n + \omega_n^2} \tag{33.34}$$

where $\omega_n = \sqrt{1\,/L_{\mathrm{fr}}C_{\mathrm{fr}}}$ and $\xi = (r_L/2)\sqrt{(C_{\mathrm{r}}/L_{\mathrm{fr}})}$.

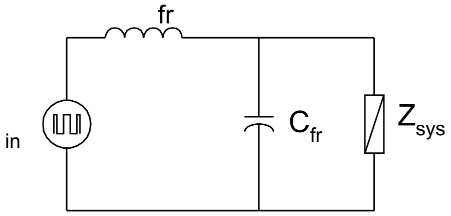


FIGURE 33.26 The single-phase equivalent circuit of the inverter output ripple filter.

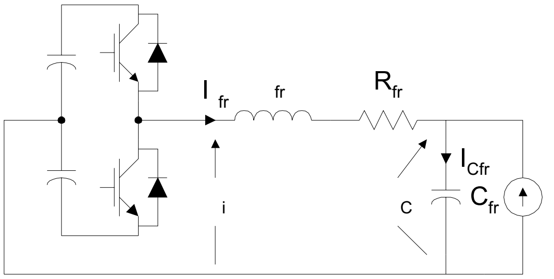


FIGURE 33.27 Single-phase equivalent circuit of series active power filter connected to the ripple filter.

Normally, the damping factor ξ is smaller than one, causing the voltage oscillation across the capacitor ripple filter, C_{fr}. Generally, relatively low impedance loads are connected to the output terminals of voltage source PWM inverters. In these cases, the quality factor of the LC filter can be low, and the oscillation between the inductor L_{fr} and the capacitor C_{fr} is avoided [7].

33.4.3.4 Passive Filters

Passive filters connected between the nonlinear load and the series active power play an important role in the compensation of the load current harmonics. With the connection of the passive filters the series active power filter operates as an harmonic isolator. The harmonic isolation feature reduces the need for precise tuning of the passive filters and allows their design to be insensitive to the system impedance and eliminates the possibility of filter overloading due to supply voltage harmonics. The passive filter can be tuned to the dominant load current harmonic and can be designed to correct the load displacement power factor.

However, for industrial loads connected to stiff supply, it is difficult to design passive filters that can absorb a significant part of the load harmonic current and therefore its effectiveness deteriorates. Specially, for compensation of diode rectifier type of loads, where a small kvar passive filter is required, it is difficult to achieve the required tuning to absorb significant percentage of the load harmonic currents. For this type of application, the passive filters cannot be tuned exactly to the harmonic frequencies because they can be overloaded due to the system voltage distortion and/or system current harmonics.

The single-phase equivalent circuit of a passive LC filter connected in parallel to a nonlinear current source and to the power distribution system is shown in Fig. 33.28. From this figure, the design procedure of this filter can be derived. The harmonic current component flowing through the passive filter i_{fh} and the current component flowing through the source i_{sh} are given by the following expressions:

$$i_{fh} = \frac{Z_s}{Z_s + Z_f} I_h \qquad i_{sh} = \frac{Z_f}{Z_s + Z_f} I_h. \tag{33.35}$$

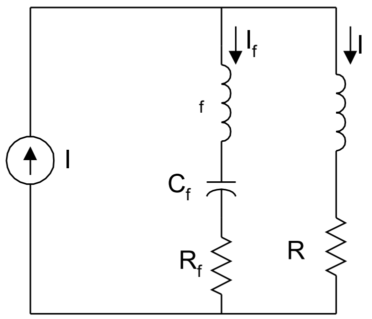


FIGURE 33.28 The single-phase equivalent circuit of the passive filter connected to a non-linear load.

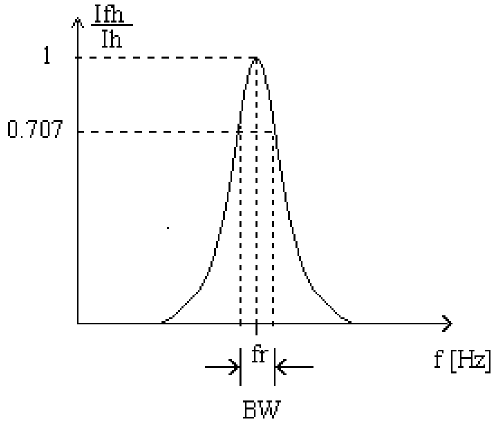


FIGURE 33.29 The passive filter bandwidth.

At the resonant frequency the inductive reactance of the passive filter is equal to the capacitive reactance of the filter, that is:

$$2\pi frL = \frac{1}{2\pi frC} \tag{33.36}$$

Therefore, the resonant frequency of the passive filter is equal to:

$$fr = \frac{1}{2\pi\sqrt{LC}}. \tag{33.37}$$

The passive filter band width is defined by the upper and lower cutoff frequency, at which values the filter current gain is −3 dB, as shown in Fig. 33.29.

The magnitude of the passive filter impedance as a function of the frequency is shown in Fig. 33.30.

At the resonant frequency the passive filter magnitude is equal to the resistance. If the resistance is zero, the filter is in short circuit. The quality factor of the passive filter is defined by the following expression:

$$Q = \frac{\omega_n L}{R} \tag{33.38}$$

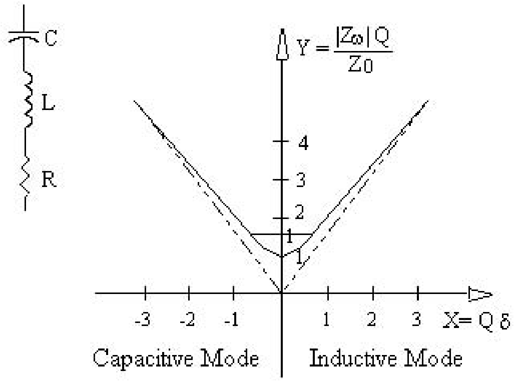


FIGURE 33.30 The frequency response of the passive LC filter.

It is important to note that the operation of the series active power filter with off-tuned passive filter has an adverse impact on the inverter power rating compared to the normal case. The more off-tuned the passive filter is the more rated apparent power is required by the series active power filter.

33.4.3.5 Protection Requirements

Short circuits in the power distribution system generate large currents that flow through the power lines until the circuit breaker operates clearing the fault. The total clearing time of a short circuit depends on the time delay imposed by the protection system. The clearing time cannot be instantaneous due to the operating time imposed by the overcurrent relay and by the total interruption time of the power circuit breaker. Although power system equipment, such us power transformers, cables, etc., are designed to withstand short-circuit currents during at least 30 cycles, the active power filter may suffer severe damage during this short time. The withstand capability of the series active power filter depends mainly on the inverter power semiconductor characteristics.

Since the most important feature of series active power filters is the small rated power required to compensate the power system, typically 10–15 of the load rated apparent power, the inverter semiconductors are rated for low values of blocking voltages and continuous currents. This makes series active power filters more vulnerable to power system faults.

The block diagram of the protection scheme described in this section is shown in Fig. 33.31. It consists of a varistor connected in parallel to the secondary winding of each coupling transformer, and a couple of antiparallel thyristors [8]. A special circuit detects the current flowing through the varistors and generates the gating signals of the antiparallel thyristors. The protection circuit of the series active power filter must protect only the PWM voltage-source inverter connected to the secondary of the coupling transformers and must not interfere with the protection scheme of the power distribution system. Since the primary of the active power filter coupling transformers are connected in series to the power distribution system, they operate as current transformers, so that their secondary windings cannot operate in open circuit. For this reason, if a short-circuit is detected in the power distribution system, the PWM voltage-source inverter cannot be disconnected from the secondary of the current transformer. Therefore, the protection scheme must be able to limit the amplitude of the currents and voltages generated in the secondary circuits. This task is performed by the varistors and by the magnetic saturation characteristic of the transformers.

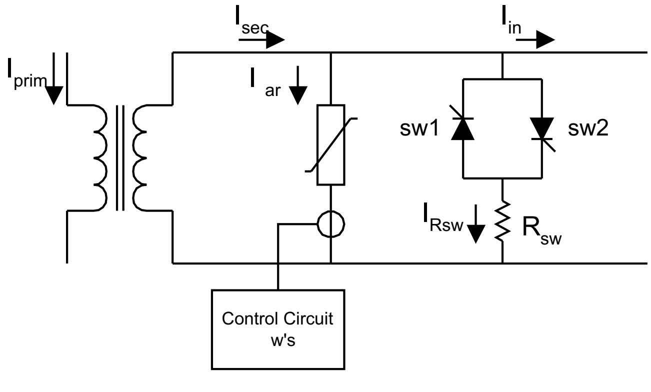


FIGURE 33.31 The series active power filter protection scheme.

The main advantages of the series active power filter protection scheme described in this section are the following:

i) it is easy to implement and has a reduced cost,
ii) it offers full protection against power distribution short-circuit currents,
iii) it does not interfere with the power distribution system.

When short-circuit currents circulate through the power distribution system, the low saturation characteristic of the transformers increases the current ratio error and reduces the amplitude of the secondary currents. The larger secondary voltages induced by the primary short-circuit currents are clamped by the varistors, reducing the amplitude of the PWM voltage-source inverter currents. After a few cycles of duration of the short-circuit, the PWM voltage-source inverter is bypassed through a couple of antiparallel thyristors, and at the same time the gating signals applied to the PWM voltage-source inverter are removed. In this way, the PWM voltage-source inverter can be turned off. The principles of operation and the effectiveness of the protection scheme are shown in Fig. 33.32.

The secondary short-circuit currents will circulate through the antiparallel thyristors and the varistors until the fault is cleared by the protection equipment of the power distribution system.

By using the protection scheme described in this subsection, the voltage and currents reflected in the secondary of the coupling transformers are significantly reduced. When short-circuit currents circulate through the power distribution system, the low saturation characteristic of the coupling transformers increases the current ratio error and reduces the amplitude of the secondary voltages and currents. Moreover, the saturated high secondary voltages induced by the primary short-circuit currents are clamped by the varistors, reducing the amplitude of the PWM voltage-source inverter ac currents. Once the secondary current exceeds a predefined reference value, the PWM voltage-source inverter is by-passed through a couple of antiparallel thyristors, and then the gating signals applied to the PWM voltage-source inverter are removed. The effectiveness of the protection scheme is shown in Fig. 33.33.

By increasing the current ratio error due to the magnetic saturation, the energy dissipated in the secondary of the coupling transformer is significantly reduced. The total

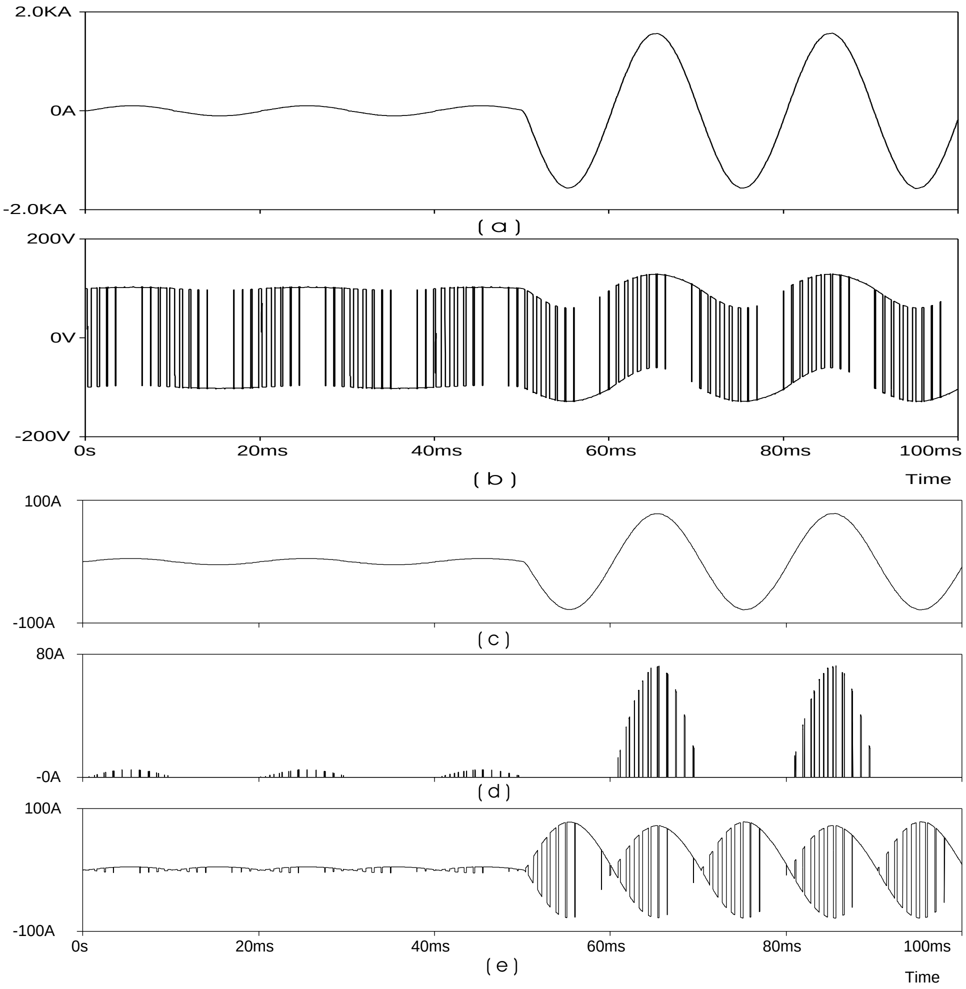


FIGURE 33.32 Current waveforms of the series active power filter during a three-phase short-circuit in the power distribution system set at 50 ms. (a) Power distribution system line current. (b) Current transformer secondary voltage. (c) Inverter ac current. (d) Current through an inverter leg. (e) Inverter dc bus current.

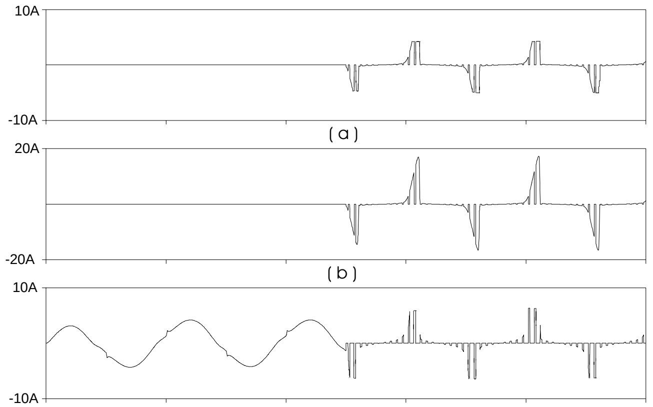


FIGURE 33.33 Current waveforms for a line to line short-circuit in the power distribution system. The protection scheme is implemented with the varistor, a couple of antiparallel thyristors, and a coupling transformer with low saturation characteristic. (a) Current through the varistor. (b) Current through the thyristors. (c) Inverter ac current.

energy dissipated in the varistor for the different protection conditions is shown in Fig. 33.34.

33.4.4 Control Issues

The block diagram of a series active power filter control scheme that compensates current harmonics and voltage unbalance simultaneously is shown in Fig. 33.35.

Current and voltage reference waveforms are obtained by using the Park Transformation (Instantaneous Reactive Power Theory). Voltage unbalance is compensated by calculating the negative and zero sequence fundamental components of the system voltages. These voltage components are added to the source voltages through the coupling transformers compensating the voltage unbalance at the load terminals. In order to reduce the amplitude of the current flowing through the neutral conductor, the zero sequence components of the line

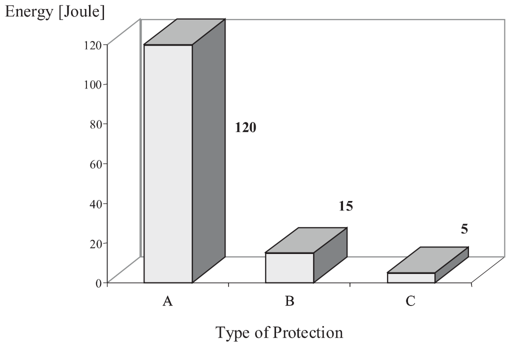


FIGURE 33.34 The total energy dissipated in the varistor during the power system short-circuit for different protection schemes implementations. (a) Only with the varistor used. (b) The varistor is connected in parallel to a bidirectional switch. (c) With the complete protection scheme operating (including the coupling transformer with low saturation characteristics).

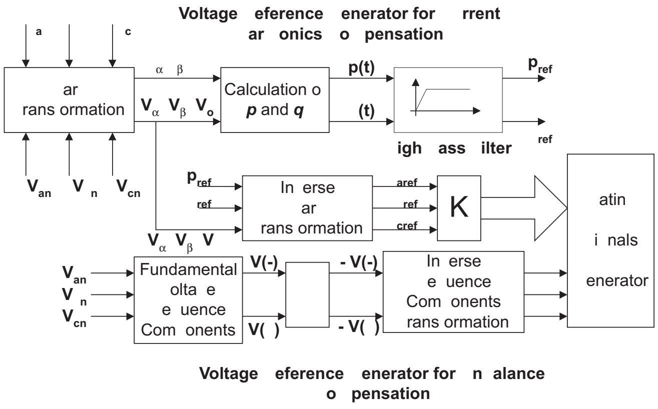


FIGURE 33.35 Compensation scheme for voltage unbalance correction.

currents are calculated. In this way, it is not necessary to sense the current flowing through the neutral conductor.

33.4.4.1 Reference Signals Generator

The compensation characteristics of series active power filters are defined mainly by the algorithm used to generate the reference signals required by the control system. These reference signals must allow current and voltage compensation with minimum time delay. Also it is important that the accuracy of the information contained in the reference signals allows the elimination of the current harmonics and voltage unbalance presents in the power system. Since the voltage and current control scheme are independent, the equations used to calculate the voltage reference signals are the following:

$$\begin{bmatrix} v_{a0} \\ v_{a1} \\ v_{a2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} \dot{v}_a \\ v_b \\ v_c \end{bmatrix} \tag{33.39}$$

The voltages v_a, v , and v_c correspond to the power system phase to neutral voltages before the current transformer. The reference voltage signals are obtained by making the positive sequence component, v_a zero and then applying the inverse of the Fortescue transformation. In this way the series active power filter compensates only voltage unbalance and not voltage regulation. The reference signals for the voltage unbalance control scheme are obtained by applying the following equations:

$$\begin{bmatrix} v_{\mathrm{refa}} \\ v_{\mathrm{refb}} \\ v_{\mathrm{refc}} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \cdot \begin{bmatrix} -v_{\mathrm{ao}} \\ 0 \\ -v_{\mathrm{a2}} \end{bmatrix} \tag{33.40}$$

In order to compensate current harmonics generated by the nonlinear loads, the following equations are used:

$$\begin{bmatrix} i_{aref} \\ i_{bref} \\ i_{cref} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p_{\mathrm{ref}} \\ q_{\mathrm{ref}} \end{bmatrix} + \frac{1}{\sqrt{3}} \begin{bmatrix} i_0 \\ i_0 \\ i_0 \end{bmatrix} \tag{33.41}$$

where $\boldsymbol{i}_0$ is the fundamental zero sequence component of the line current and is calculated using the Fortescue transformation:

$$\mathrm{i}_0 = (1/\sqrt{3})(i_{\mathrm{a}} + i_{\mathrm{b}} + \mathrm{i}_{\mathrm{c}}). \tag{33.42}$$

In (33.41) $\boldsymbol{p}_{\mathrm{ref}}$, $_{\mathrm{ref}}$, v_α, and v_β are defined according to the Instantaneous Reactive Power Theory. In order to avoid the compensation of the zero sequence fundamental frequency current the reference signal $\boldsymbol{i}_0$ must be forced to circulate through a high pass filter generating a current $\boldsymbol{i}'_0$ which is used to create the reference signal required to compensate current harmonics. Finally, the general equation that defines the references of the PWM voltage-source inverter required to compensate voltage unbalance and current harmonics is the following:

$$\begin{bmatrix} V_{\mathrm{refa}} \\ V_{\mathrm{refb}} \\ V_{\mathrm{refc}} \end{bmatrix} = K_1 \left\{ \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p_{\mathrm{ref}} \\ q_{\mathrm{ref}} \end{bmatrix} + \frac{1}{\sqrt{3}} \begin{bmatrix} i'_0 \\ i'_0 \\ i'_0 \end{bmatrix} \right\} + K_2 \left\{ \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \cdot \begin{bmatrix} -v_{\mathrm{a0}} \\ 0 \\ -v_{\mathrm{a2}} \end{bmatrix} \right\} \tag{33.43}$$

where $_1$ is the gain of the coupling transformer which defines the magnitude of the impedance for high frequency current components, and $_2$ defines the degree of compensation for voltage unbalance, (ideally $_2$ equals 1).

33.4.4.2 Gating Signals Generator

This circuit provides the gating signals of the three-phase PWM voltage-source inverter required to compensate voltage unbalance and current harmonic components. The current and voltage reference signals are added and then the amplitude of the resultant reference waveform is adjusted in order to increase the voltage utilization factor of the PWM inverter for steady-state operating conditions. The gating signals of the inverter are generated by comparing the resultant reference signal with a fixed frequency triangular waveform. The triangular waveform helps to keep the inverter switching frequency constant (Fig. 33.36).

A higher voltage utilization of the inverter is obtained if the amplitude of the resultant reference signal is adjusted for the steady-state operating condition of the series active power filter. In this case, the reference current and reference voltage waveforms are smaller. If the amplitude is adjusted for transient operating conditions, the required reference signals will have a larger value, creating a higher dc voltage in the inverter and defining a lower voltage utilization factor for steady-state operating conditions.

The inverter switching frequency must be high in order not to interfere with the current harmonics that need to be compensated.

33.4.5 Control Circuit Implementation

Since the control scheme of the series active power filter must translate the current harmonics components that need to be compensated in voltage signals, a proportional controller is used. The use of a PI controller is not recommended since it would modify the reference waveform and generate new current harmonic components. The gain for the proportional controller depends on the load characteristics and its value fluctuates between 1 and 2.

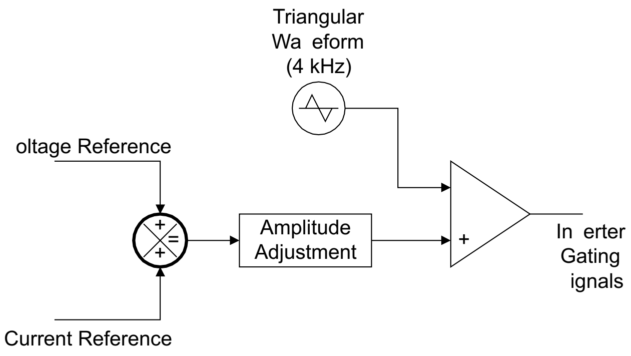


FIGURE 33.36 The block diagram of the gating signals generator.

Another important element used in the control scheme is the filter that allows us to generate $\boldsymbol{p}_{\text{ref}}$ and $_{\text{ref}}$ (Fig. 33.35). The frequency response of this filter is very important and must not introduce any phase-shift or attenuation to the low frequency harmonic components that must be compensated. A high-pass first order filter tuned at 15 Hz is adequated. This corner frequency is required when single-phase nonlinear loads are compensated. In this case, the dominant current harmonic is the third. An example of the filter that can be used is shown in Fig. 33.37.

The operator “**a**” required to calculate the sequence components of the system voltages (Fortescue transformation) can be obtained with the all-pass filter shown in Fig. 33.38.

The phase shift between $\boldsymbol{V}_0$ and $\boldsymbol{V}_i$ is given by the following expression:

$$\theta = 2\arctan(2\pi f R_2 C) \tag{33.44}$$

Since the phase-shift is negative, the operator “$\boldsymbol{a}$” is obtained by using an inverter (180°) and then by tuning $\theta = -60°$. The operator “$\boldsymbol{a}$ ” is obtained by phase-shifting $\boldsymbol{V}_i$ by $-120°$. $\boldsymbol{V}_i$ is synchronized with the system phase-to-neutral voltage $\boldsymbol{V}_{\text{an}}$.

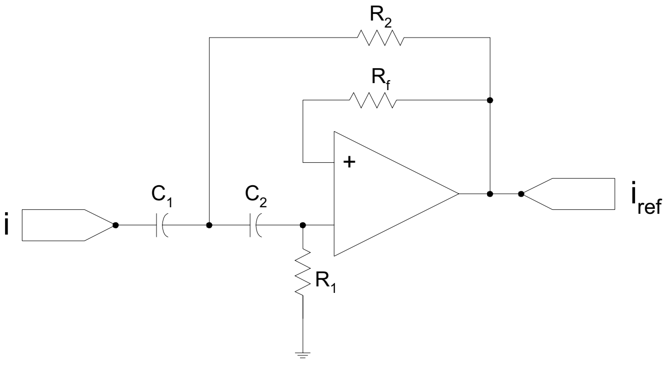


FIGURE 33.37 The first-order high-pass filter implemented for the calculation of $\boldsymbol{p}_{\text{ref}}$ and $_{\text{ref}}(C_1 = C_2 = 0.1\ \mu\text{F}, R_1 = R_f = 150\ \text{k}\Omega, R_2 = 50\ \text{k}\Omega)$.

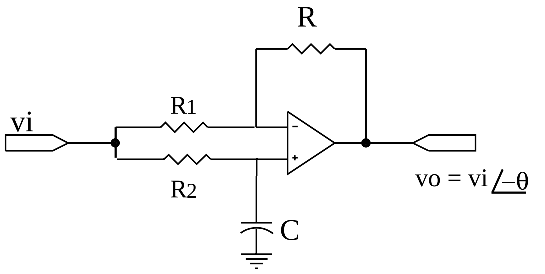
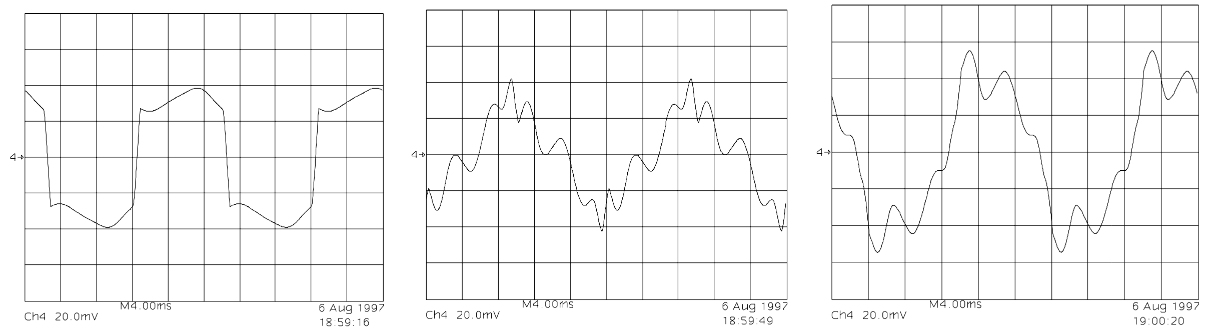


FIGURE 33.38 The all-pass filter used as a phase shifter.

33.4.6 Experimental Results

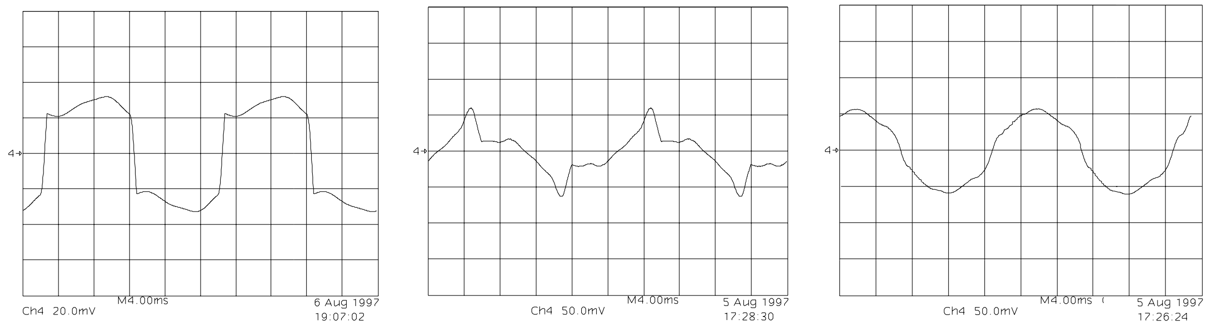
The viability and effectiveness of series active power filters used to compensate current harmonics was proved in an experimental setup of 5 kVA. Current waveforms generated by a nonlinear load and using only passive filters and the combination of passive and the series active power filter are shown in Figs. 33.39 and 33.40.

These figures show the effectiveness of the series active power filter, which reduces the overall THD of the current that flows through the power system from 28.9 (with the operation of only the passive filters) to 9 with the operation of the passive filters with the active power filter connected in series. The compensation of the current that flows through the neutral conductor is shown in Fig. 33.41.



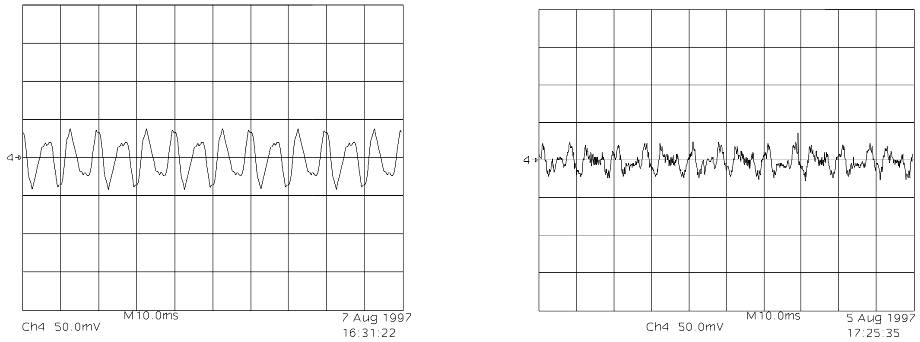
(a) (b) (c)

FIGURE 33.39 Experimental results without the operation of the series active power filter. (a) Load current. (b) Current flowing through the passive filter. (c) Current through the power supply.



(a) (b) (c)

FIGURE 33.40 Experimental results with the operation of the series active power filter. (a) Load current. (b) Current flowing through the passive filter. (c) Current through the power supply.



(a) (b)

FIGURE 33.41 Experimental results of neutral current compensation. (a) Current flowing through the neutral without the operation of the series active power filter. (b) Current flowing through the neutral with the operation of the active power filter.

Acknowledgment

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34

Computer Simulation of Power Electronics and Motor Drives

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34.1 Introduction

This chapter shows how power electronics circuits, electric motors and drives, can be simulated with modern simulation programs. The main focus will be on PSpice®, which is one of the most widely used general-purpose simulation programs and Simplorer®, Release 4.1, which is more specialized towards the power electronics and motor drives application area. Ali Ricardo Buendia, who is currently working towards his MSEE degree, has created the examples for Simplorer®. The PSpice® examples have originally been developed for Release 8 from MicroSim and have been converted to the current Release 9. Examples for both versions are given. The examples in this chapter have been chosen such that they can be run on the evaluation versions of the particular programs. The author found this to be very beneficial in an educational environment, since such examples can be shared with students to enhance their understanding of the lecture material. This shall by no means lead to the conclusion that the programs and simulations presented here cannot be used for serious professional work. In fact, the author has used these tools with great success in many research and consulting projects. In addition to the programs mentioned above, MathCAD® has been used to derive and present the underlying equations. The advantage of using MathCAD® for this purpose is, that in MathCAD® it is possible to check equations by actually executing them.

The examples have been developed to illustrate advanced techniques for simulation of systems from the power electronics and drives area but not to teach the basic features of the individual programs. It is assumed, that the reader will familiarize themselves with the basics on how to run the programs using the accompanying documentation. In addition, it is assumed that the reader is familiar with the basics of power electronics and electric machines, specifically ac induction machines. For a review the reader shall be referred to [2] for power electronics and [3,7] for induction machines.

34.2 Use of Simulation Tools for Design and Analysis

Before any in-depth discussion of specific simulation examples, it is appropriate to reflect upon the value of simulations and its place in the design and analysis process. Computer simulations enable engineers to study the behavior of complex and powerful systems without actually building or operating them. Simulations therefore have a place in the analysis of existing equipment as well as the design of new systems. In addition, computer simulations enable engineers to safely

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study abnormal operating or fault conditions without actually creating such conditions in the real equipment.

However, the reader should be reminded that, even the most modern simulation programs cannot perfectly represent all parameters and aspects of real equipment. The accuracy of the simulation results depends on the accuracy of the component models and the proper identification and inclusion of parasitic circuit elements such as parasitic inductance, capacitance and parasitic mutual coupling. Accuracy of component models in this context shall not mean that the model is actually faulty but rather that the limitations of the model are exceeded. For example, if the transformer inrush phenomenon were to be studied using a linear model for a transformer, the simulation would not yield useful results.

In particular, the precise prediction of voltage and current traces during fast switching transitions in power electronics circuits has been proven to be difficult. To obtain useful results, extensive experimental validation, advanced device models (and the values for their parameters) and detailed knowledge of parasitic elements, including those of the packaging of the circuit elements, are necessary. In addition, numerical convergence is often a problem, if gate drive signals, with rise and fall times as steep as in real circuits, are applied. Therefore, the exact prediction of waveforms during switching transitions shall be excluded from the discussions in this chapter. Consequently, the author prefers to measure parameters such as voltage rise and fall times, over and undershoot, etc., on actual circuitry in the laboratory.

Sometimes, users of PSpice® claim that the convergence problems are so severe that its use for simulations of power electronics circuits is just not possible or worth the effort. However, this is absolutely not true and with the proper techniques of gate signal generation, we can simulate just about any given circuit with little or no convergence problems. In addition, if convergence problems are avoided, simulations run much faster and larger numbers of individual transitions can be studied. This is achieved by generating gate signals that are slightly less steep than in real circuits using analog behavioral elements. This gives a lot of insight into the cycle by cycle as well as the system level behavior of a power electronics circuit. In this fashion, the function of an existing, as well as the expected performance of a new, proposed circuit, can be studied. An excellent application for these cycle-by-cycle simulations is the development and verification of control strategies for the power semiconductors.

Analog behavioral modeling (ABM) techniques included in PSpice® can be used to study large and complex systems like the control of induction machines using field oriented (also called vector) control techniques. Examples are given that replace the power electronics inverter with an ABM source that produces voltages, which represent the short term average (filtering away the voltage components of the switching frequency and above) of the output of a three-phase inverter. These examples represent pure system level simulations, which could have also been done using programs like MatLab/Simulink®. However, circuit simulation programs provide the option of studying actual circuit level details in complex systems. To demonstrate this capability, the startup of an induction motor, fed by a three-phase MOSFET inverter, is presented.

In all modeling cases, the user needs to define the goal of the simulation effort. In other words, the user must answer the question "What information shall be obtained through the simulation of the circuit or system?" The user must then select the appropriate simulation software and the appropriate models. This process requires a detailed understanding of the properties and limitations of the device models and the sensitivity of the results to the model limitations. In order to obtain such an understanding, it is often recommended and necessary to perform numerous simulation test runs, carefully scrutinize the results and compare them with measured data, results from other simulation packages or otherwise known facts.

34.3 Simulation of Power Electronics Circuits with PSpice®

The first example of a power electronics circuit is a step-down (also called Buck) converter with synchronous rectification. For the purpose of synchronous rectification, the diode, which connects the inductor to ground in the regular circuit, is replaced with a power MOSFET transistor. The benefit of this circuit is, that the power MOSFET represents a purely resistive channel in the on state. This channel does not have a residual, current independent, voltage drop like the p–n junction of a diode. Therefore, the voltage drop across the MOSFET can be made lower than what can be achieved with diodes. The results are reduced losses and increased efficiency. To achieve this, the lower MOSFET must be turned on whenever the upper MOSFET is turned off and the current in the inductor is positive. If the current in the inductor is continuous, the drive signal for the lower MOSFET is simply the inverted drive signal for the upper MOSFET. However, if the current in the inductor is discontinuous, the drive signal for the lower MOSFET must be cut off as soon as the current in the inductor goes to zero. Figure 34.1 shows a simulation setup for a synchronous buck converter that can operate correctly for continuous as well as discontinuous inductor current.

As mentioned before, the key element of this example is the circuit for the generation of the gate drive signals for the MOSFETs. For clarity this circuit has been realized using only standard elements from the libraries of the evaluation version. The basic principle of the operation of the gate drive circuit is the well-known carrier based scheme, where a control voltage is compared with a triangular carrier with fixed amplitude. An "ABM" block, shown in the lower left part of Fig. 34.1, generates the triangular carrier. Eqn. (34.1) below gives the

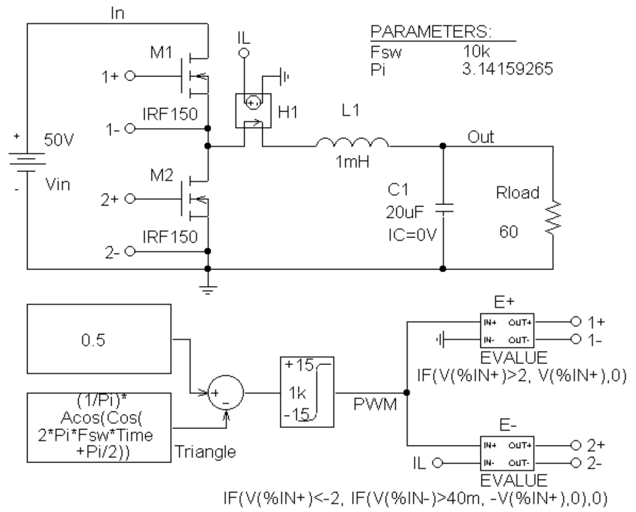


FIGURE 34.1 Simulation setup for a synchronous Buck converter.

equation for the triangular carrier wave. The output range of the function shown in Eqn. (34.1) is between 0.0 and 1.0.

$$E_{\mathrm{Tri}}(t) := \frac{1}{\pi}\mathrm{acos}\left(\cos\left(2\pi f_s t + \frac{\pi}{2}\right)\right) \tag{34.1}$$

For the generation of the gate drive signals, the carrier wave is compared with a control signal that can have values between 0.0 and 1.0, corresponding to a duty cycle input between 0 and 10 . Feeding the difference of the carrier wave and the control signal into a soft comparator generates the primary PWM signal. Careful inspection of the implementation of the soft-limiter element provided in the evaluation version of PSpice® shows, that it uses a scaled hyperbolic tangent function. Figure 34.2 shows a plot of a hyperbolic tangent function. It can easily be seen that the result of the soft limiter is an output signal with smooth transitions, which is crucial to avoid convergence problems in PSpice®. The soft limiter used here has an upper and lower limit of ±15 V and a gain (steepness control for the tanh function) of 1000 (1 k).

Figure 34.3 shows the output of the simulation run for the synchronous buck converter. The top-level graph shows the generated triangle carrier. It has a frequency (Fsw, see parameter statement in Fig. 34.1) of 10 kHz. This frequency has been chosen rather low to improve the readability of Fig. 34.3. In the graph below the triangle voltage in Fig. 34.3, the gate drive signals are shown for both MOSFET transistors. Please note that the gate drive signal for the lower MOSFET is vertically shifted by 30 V in order to separate the traces for readability. The graph below the gate drive signals shows the inductor current. It can be seen that the current is discontinuous after the initial inrush peak. The inrush peak is caused by the fact that the capacitor is initially discharged (IC = 0 V). It is evident, that the gate drive signal of the lower (synchronous rectification) MOSFET is appropriate for the inductor current. The bottom trace shows the capacitor voltage, with has a steady state value of slightly more than 0.5 × 40 V (0.5 = 50%) being the duty cycle and 40 V being the input voltage) due to the fact that the inductor current is slightly discontinuous even at steady-state conditions. To test the gate drive circuit for the lower MOSFET, the load has been chosen such that the steady-state current would be discontinuous. Following the soft limiter are two voltage-controlled voltage sources that generate isolated gate-source voltages of 15 V for the on condition and 0 V for the off condition of the MOSFETs. To enable operation with discontinuous inductor current, the source "E-" in Fig. 34.1 also monitors the polarity of the inductor current through a current controlled voltage source "H1" with unity gain.

In addition to the cycle-by-cycle simulation of a dc–dc converter, it is also possible to use a time-averaged replacement for the MOSFET transistors used in the circuit in Fig. 34.1. In fact, a common time average model can be used for the Buck, the Boost, the Buck-Boost, and the Cuk converter as long as they operate with continuous inductor current. The time-averaged model has the advantage that it can run much

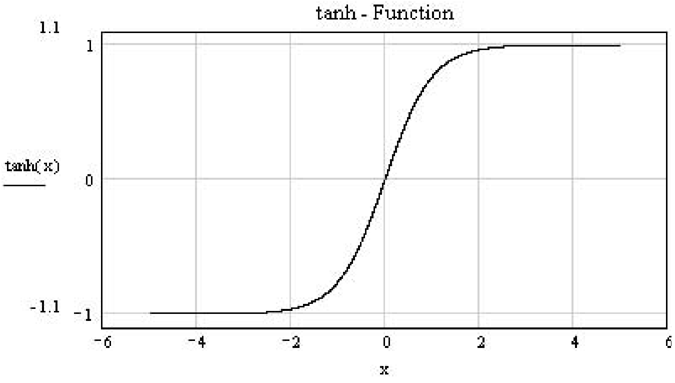


FIGURE 34.2 Plot of a hyperbolic tangent function used to generate smooth PWM signals.

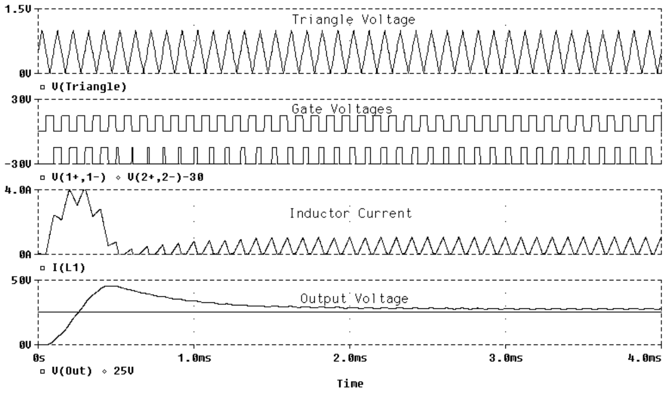


FIGURE 34.3 Output waveforms for the synchronous buck converter.

faster since it does not have to follow each switching transition. It is also possible to perform dc and ac sweep analyses. A dc sweep would sweep the duty cycle over a wide range and show the output voltage as a function of the duty cycle. An ac sweep analysis would sweep the frequency of an ac signal, that is superimposed on top of the duty cycle bias signal. The ac sweep allows the study of the behavior of the converter, including a feedback control system, in the frequency domain for traditional stability analysis and system tuning. A detailed description of this time-averaged modeling technique, including detailed examples is given in [1].

To illustrate the capabilities of the PSpice® simulation program, the next example shows a complete three-phase inverter bridge using six power MOSFETs. This circuit is shown in Fig. 34.4. Note that free-wheeling diodes are an integral part of every power MOSFET and are not shown separately. The inverter drives a three-phase load, which could represent an induction motor for a singular operating point. The load is connected to the inverter output terminals with so-called connection bubbles. Due to the number of elements involved, the circuit for the gate drive signal generation is contained in a hierarchical block. Blocks like this are available from the main toolbar in the schematic editor. Double clicking on this block called "PWM Generator" reveals the subcircuit which is shown in Fig. 34.5.

The hexagonal shaped symbols named "1+", "1−", "2+", etc., are called interface ports. These interface ports provide the connection between the subcircuit and the ports of the hierarchical block above. Here the connection is to the ports (dots) on the "PWM Generator" block. The interface ports are created by simply drawing a wire up to the boundary of the block. The name of the port is initially generic, "Px", where x is a running number, but can be easily edited by double-clicking on the generic name. After drawing a block and creating all the ports, double-clicking inside the box will open up a schematic page for the subcircuit which has all the appropriately named interface ports already in it. Additional details on hierarchical techniques can be found in [10].

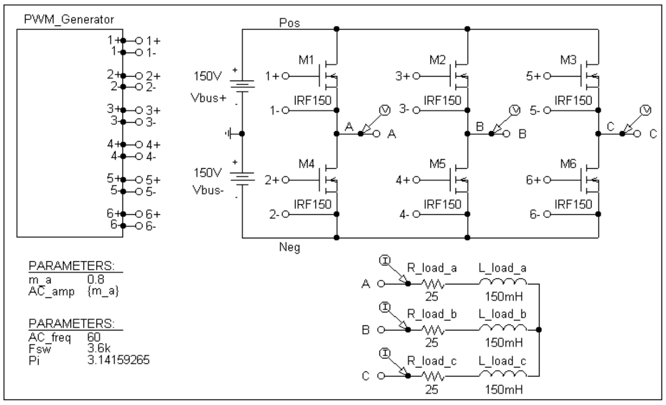

PWM_Generator
1+ 1- 2+ 2- 3+ 3- 4+ 4- 5+ 5- 6+ 6-
Pos
Neg
150V
Vbus+
150V
Vbus-
M1
M2
M3
M4
M5
M6
IRF150
A
B
C
PARAMETERS:
m_a 0.8
AC_amp {m_a}
PARAMETERS:
AC_freq 60
Fsw 3.6k
Pi 3.14159265
R_load_a
L_load_a
R_load_b
L_load_b
R_load_c
L_load_c
25
150mH

FIGURE 34.4 Circuit for a three-phase inverter with MOSFETs.

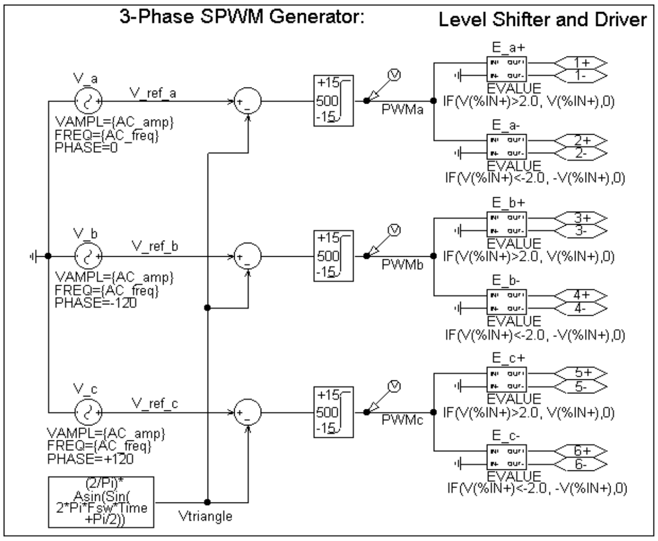

3-Phase SPWM Generator:
Level Shifter and Driver
V_a
V_ref_a
VAMPL={AC_amp}
FREQ={AC_freq}
PHASE=0
V_b
V_ref_b
VAMPL={AC_amp}
FREQ={AC_freq}
PHASE=-120
V_c
V_ref_c
VAMPL={AC_amp}
FREQ={AC_freq}
PHASE=+120
(2/Pi)*
Asin(Sin(
2*Pi*Fsw*Time
+Pi/2))
Vtriangle
+15
500
-15
PWMa
PWMb
PWMc
E_a+
E_a-
E_b+
E_b-
E_c+
E_c-
EVALUE
IF(V(%IN+)>2.0, V(%IN+),0)
IF(V(%IN+)<-2.0, -V(%IN+),0)
1+ 1- 2+ 2- 3+ 3- 4+ 4- 5+ 5- 6+ 6-

FIGURE 34.5 PWM generation sub-circuit for a three-phase MOSFET inverter.

The circuit shown in Fig. 34.5 is similar to the gate-drive generation circuit discussed before. Circuits like the circuit shown in Fig. 34.1 compare a triangular carrier with one or more reference signals. In this case, three reference signals, one for each phase, are used. The triangular carrier signal is symmetrical with respect to the time axis. The values cover the range from −1.0 to 1.0. The equation for the carrier signal is given by Eq. (34.2):

$$E_{\mathrm{Tri}}(t) := \frac{2}{\pi}\mathrm{asin}\Big(\sin\Big(2\pi f_s t + \frac{\pi}{2}\Big)\Big). \tag{34.2}$$

The three reference signals are sinusoidal signals with equal amplitude and a relative phase shift of 120°. For linear modulation, the amplitude range of the reference signals is limited to the amplitude of the triangular carrier, e.g. 1 V. The ratio of the reference wave amplitude and the (fixed) carrier amplitude is called amplitude modulation ratio "m a". In the circuit shown in Fig. 34.4 "m a" has a value of 0.8. This value is defined by a parameter symbol and represents a global parameter, which is visible throughout all levels of the hierarchy. The phase to neutral voltage amplitude of each inverter leg is equal to "Vbus + " (shown in Fig. 34.4) multiplied with the amplitude modulation ratio. The frequency and waveshape of the phase to neutral voltage of each phase leg is equal to the reference waveform, if the high frequency components resulting from the carrier wave are filtered away. This way, each inverter leg can be viewed as a linear power amplifier for its reference voltage. In fact, in drive applications, inverters are often called "servo-amplifiers". The load typically reacts only to the low-frequency components of the inverter output voltage. The high-frequency components, which include the triangular carrier frequency (also called switching frequency) and its harmonics, are typically “just a blur” for the load. This is especially true in recent times, where switching frequencies of 20 kHz and above are common. As an added benefit, audible noise is avoided at these frequency levels.

The circuit involving the soft limiter and level shifter/high side driver in Fig. 34.5 is very similar to the circuit for the synchronous buck converter, except for the fact that the load current is not monitored. The control functions for the “E x , E x—” sources, where x denotes the phase, are chosen such that the activation voltage levels are ±2 V. If the output voltage of the soft-limiter is between −2 V and +2 V, no MOSFET is activated, and shoot-through, meaning a short-circuit between the positive and negative bus, is avoided.

Figure 34.6 shows the simulation results for the three-phase inverter. The time scale is slightly stretched to show the details of the PWM signals better. The graph on top represents the line-to-line voltage V_{AB}. The graph below shows the load currents for all three phases. Due to the inductors contained in the load, the current cannot instantaneously change and follow the PWM signal. Therefore the load current is an almost pure sinusoid with very little ripple. This is representative of the line currents in induction motors.

Figure 34.7 shows that the MOSFETs in Fig. 34.4 can be replaced with IGBTs. The particular IGBT shown here is included in the library of the evaluation version. Note that free wheeling diodes are needed, if IGBTs are used. The free wheeling diodes carry the load current when the IGBTs are turned off to provide a continuous path for the current. This is very important, since the load can have a substantial inductive component. Whenever the diodes are conducting, energy flows momentarily back to the source. In the case of power MOSFETs, the diodes (often called body diodes) are an integral part of the device. In the symbol graphic of PSpice® these body diodes are not shown for MOSFETs. For this circuit, the gate drive circuit and the results are the same as for the three-phase bridge with power MOSFETs.

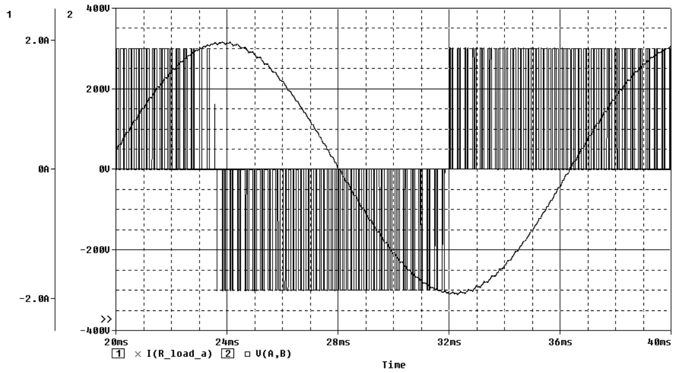


FIGURE 34.6 Output waveforms of the three-phase inverter with MOSFETs.

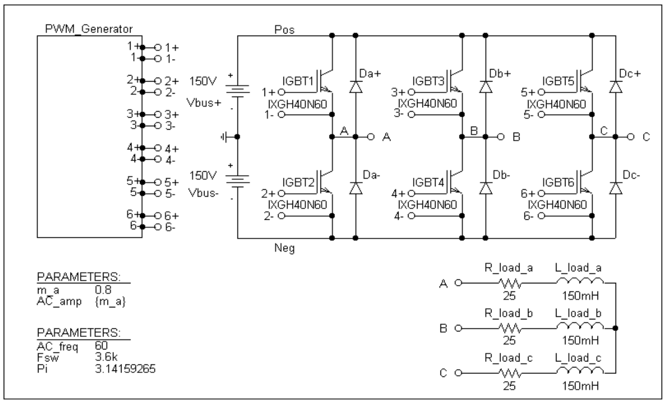


FIGURE 34.7 Three-phase inverter circuit with IGBTs.

34.4 Simulations of Power Electronic Circuits and Electric Machines

In the following, the startup of an induction motor, fed by the three-phase inverter shown in Fig. 34.4, is shown. For this purpose, the simple passive load in Fig. 34.4 is replaced by an induction motor. For this and further discussions it is assumed that the reader is familiar with the theory of induction machines. A number of excellent references are given at the end of this chapter [3,4,5,7]. The induction motor symbol represents the electromechanical model of an induction motor. The model is suitable for studies of electrical and mechanical transients as well as steady state conditions. The output pin on the motor shaft represents the mechanical output. The voltage on this pin represents the mechanical angular velocity using the relation 1 V = 1 rad/s. In addition, any current drawn from or fed into this terminal represents applied motor or generator torque according to the relation 1 A = 1 Nm. Due to these definitions, the electrical power associated with the voltage of the motor shaft (with respect to ground) is identical to the mechanical power. Following the well-known theory, the induction motor model has been derived for a two-phase (direct and quadrature, D, Q) equivalent motor. Attached to the motor is a bi-directional two-phase to three-phase converter module. This module is voltage and current invariant. This means that the voltage and current levels in the two-phase and the three-phase machine are equal. Consequently, the power in the two-phase machine is only $\frac{2}{3}$ of the power in the three-phase circuit. This is accounted for in the calculation of the electromagnetic torque (see Eq. 34.4 below). The internally generated torque can be monitored on the output labeled “Torque” on top of the sleeve around the motor shaft. The linear load in Fig. 34.8 is a symbol that represents an appropriately sized resistor to ground.

In Fig. 34.8 the motor is represented by a custom symbol called “Motor1”. A simple hierarchical block could have been used for the motor, but a custom symbol has been created to

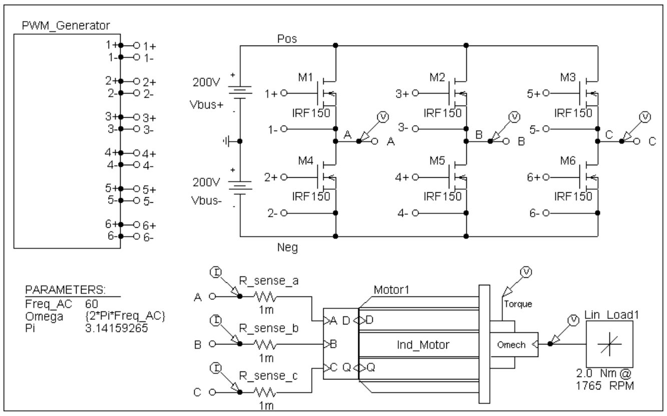


FIGURE 34.8 Induction motor startup with three-phase inverter circuit.

achieve a more realistic and pleasing graphical representation. The symbol can be easily created with the symbol editor, which is build into the regular schematics editor. The editor provides standard graphical elements (lines, rectangles, circles) etc., so that professional looking symbols can easily be created. More details on this are shown below in Figs. 34.19, 20 and the accompanying discussion. The motor symbol resides in a local library (.slb), which is located in the same subdirectory, where all other files for the project are residing. The library is configured (the simulator is told of its existence) by using the menu dialog “Options/Editor Configuration/Library Settings/Add Local”. These parameters are passed onto the subcircuit by using the name of the parameter preceded by a ‘ ’ symbol. The advantage of passing parameters to subcircuits in this way is that several symbols can call one set of subcircuits with different parameters (Table 34.1).

Double-clicking on the motor symbol reveals the associated subcircuit that implements its function. This sub-circuit is shown in Fig. 34.9. The upper portion of this subcircuit represents the electrical model. The task of the electrical model is to calculate the stator and rotor currents, where the stator voltages and the mechanical speed of the machine are input parameters. However, it is also possible, without any changes, to feed stator currents (with controlled current sources) into the D and Q inputs and have the model calculate the appropriate stator voltages. This option is useful for vector control applications, which are discussed later.

TABLE 34.1 List of all attributes used for the induction motor symbol

Attributes
PART = Induction Servo
MODEL = Ind Motor
TEMPLATE =
J mot = 0.01
Omega init = 0.0
Ls = (Lm + Lsl)
Lr = (Lm + Lr1)
Poles = 4
Tau r = (Lr/ R Rot)
REFDES = Motor?
Lsl = 14.96 mH
Lr1 = 8.79mH
R Stat = 3.60
R Rot = 1.90
Lm = 424.41mH

The equation system for the electrical model is given by Eqn. (34.3): The theory for this equation system is derived in [3,4,5,7]. The equation system and the model are formulated for the stationary reference frame. This reference frame assumes that the frame of the machine is stationary (which is hopefully the case in the real machine) and the voltages and currents of the rotor are equivalent ac values with stator frequency. From machine theory we know that the actual rotor currents have slip frequency. Another reference frame is the synchronous (also called excitation) reference frame. In this reference frame the stator of a *fictitious* machine is assumed to rotate with synchronous speed. The advantage of this reference frame is that the input frequency is zero (dc), which makes it easy to explain the principle of vector control by extending the theory of dc machines to ac machines.

$$\begin{bmatrix} V_d \\ V_q \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_{stat} + pL_s & 0 & pL_m & 0 \\ 0 & R_{stat} + pL_s & 0 & pL_m \\ pL_m & \omega_e L_m & R_{rot} + pL_r & \omega_e L_r \\ -\omega_e L_m & pL_m & -\omega_e L_r & R_{rot} + pL_r \end{bmatrix} \begin{bmatrix} I_{sd} \\ I_{sq} \\ I_{rd} \\ I_{rq} \end{bmatrix}$$

$$L_s = L_m + L_{sl} \qquad L_r = L_m + L_{rl} \qquad p = \frac{d}{dt}. \tag{34.3}$$

Sometimes still other reference frames are used and it is possible to generate a universal electrical model with a reference frame speed input. This model could then be used for any reference frame.

The electrical model shown in Fig. 34.9 implements the equation system Eqn. (34.3). The circuit closely resembles the well-known T equivalent circuit for the steady state analysis of induction machines. Two instances of the T equivalent circuit are necessary to implement the two-phase (D, Q) model. The two instances of the circuit are almost mirror images of each other (and actually drawn that way) except for some differences in the circuit elements that calculate the voltages, which are generated due to the rotation of the rotor. The bottom of Fig. 34.9 represents the mechanical model. This circuitry calculates the internally generated electro-magnetic torque

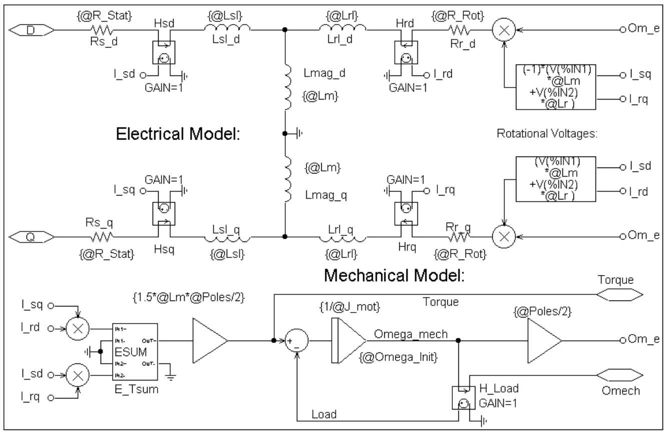

{@R_Stat}
Rs_d
Hsd
{@Lsl}
Lsl_d
{@Lrl}
Lrl_d
Hrd
{@R_Rot}
Rr_d
Om_e
I_sd
GAIN=1
Lmag_d
{@Lm}
I_rd
GAIN=1
(-1)*(V(%IN1)*@Lm+V(%IN2)*@Lr)
I_sq
I_rq
Electrical Model:
Rotational Voltages:
{@Lm}
Lmag_q
GAIN=1
I_sq
GAIN=1
I_rq
(V(%IN1)*@Lm+V(%IN2)*@Lr)
I_sd
I_rd
Rs_q
Lsl_q
Lrl_q
Rr_q
Om_e
{@R_Stat}
Hsq
{@Lsl}
{@Lrl}
Hrq
{@R_Rot}
Mechanical Model:
Torque
{1.5*@Lm*@Poles/2}
{1/@J_mot}
Torque
{@Poles/2}
I_sq
I_rd
ESUM
I_sd
I_rq
E_Tsum
Omega_mech
{@Omega_Init}
Om_e
H_Load
GAIN=1
Omech
Load

FIGURE 34.9 Subcircuit for induction motor model.

using the rotor and stator currents as input values. The equation for the torque is given by Eqn. 34.4 [3,4,5,7]:

$$T = \frac{3}{2}\frac{P}{2}L_{\mathrm{m}}(I_{\mathrm{sq}}I_{\mathrm{rd}} - I_{\mathrm{sd}}I_{\mathrm{rq}}). \tag{34.4}$$

The factor $\frac{3}{2}$ accounts for the fact that the real motor is a three-phase machine. Using the generated torque, the load torque and the moment of inertia, the angular acceleration can be calculated. Integration of the angular acceleration yields the rotor speed, which is used in the electrical model. To avoid clutter and to improve readability, connection bubbles are used to connect the various parts of the model together.

Since typical induction machines are three-phase machines, it is often desirable to have a machine model with a three-phase input. Therefore a bidirectional two-phase to three-phase converter module, which can be attached to the motor, has been developed. A subcircuit for this module is shown in Fig. 34.10. This circuit is truly bidirectional, meaning that the circuit can be fed with voltage or current sources from either side. The equation system for this voltage and current invariant transformation is given by Eqn. (34.5). This transformation is sometimes called "Clark" or "ABC-DQ" transformation. Note that V_0 denotes a zero-sequence voltage, which is assumed to be zero. This voltage would only have non-zero values for unbalanced conditions. An interesting detail of the subcircuit is the three-phase switch on the input. This switch is necessary to ensure a stable initialization of the simulator in case the machine is fed with a controlled current source. The switch provides an initial shunt resistor from the three-phase input to ground. Soon after the simulation has started, the switch opens and leaves only a negligible shunt conductance to ground.

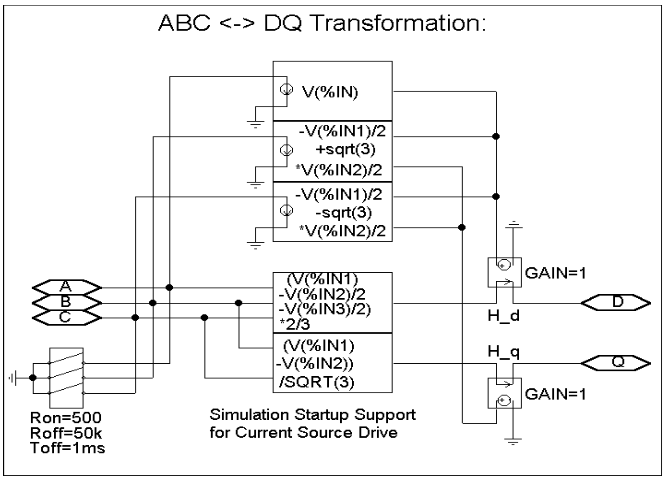

ABC <-> DQ Transformation:
V(%IN)
-V(%IN1)/2 +sqrt(3) *V(%IN2)/2
-V(%IN1)/2 -sqrt(3) *V(%IN2)/2
A
B
C
(V(%IN1) -V(%IN2)/2 -V(%IN3)/2) *2/3
(V(%IN1) -V(%IN2)) /SQRT(3)
GAIN=1
D
H_d
H_q
Q
GAIN=1
Ron=500
Roff=50k
Toff=1ms
Simulation Startup Support for Current Source Drive

FIGURE 34.10 Subcircuit for the ABC–DQ transformation module.

$$\begin{bmatrix} V_{\mathrm{d}} \\ V_{\mathrm{q}} \\ V_{\mathrm{o}} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} V_{\mathrm{a}} \\ V_{\mathrm{b}} \\ V_{\mathrm{c}} \end{bmatrix}$$

$$\begin{bmatrix} V_{\mathrm{a}} \\ V_{\mathrm{b}} \\ V_{\mathrm{c}} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 2 & 0 & 2 \\ -1 & \sqrt{3} & 2 \\ -1 & -\sqrt{3} & 2 \end{bmatrix}\begin{bmatrix} V_{\mathrm{d}} \\ V_{\mathrm{q}} \\ V_{\mathrm{o}} \end{bmatrix}. \tag{34.5}$$

Figure 34.11 shows the result for the startup of the induction motor for the circuit of Fig. 34.8. The motor is a 1/2 hp, 208 V, 4-pole machine. The detailed parameters are shown in Table 34.1. The PWM generation was identical to the example shown in Fig. 34.4, except that the switching frequency was 4 kHz and 21.1 of the third harmonic has been added to each of the reference sinusoids in order to increase the linear modulation range. The resulting reference waveform was then multiplied with 1.14, which represented the maximum voltage for linear modulation. The top trace in Fig. 34.11 shows the developed electromagnetic torque, the zero level and the level for the rated steady-state torque (2 Nm). This graph shows the typical oscillatory torque production of the induction machine for uncontrolled line start. The scale for this

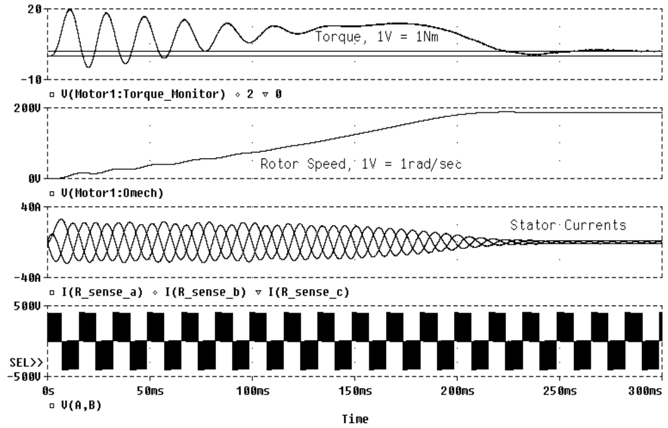


FIGURE 34.11 Induction motor startup with three phase inverter circuit.

graph is 1 V = 1 Nm. The graph below shows the mechanical angular velocity with a scale of 1 V = 1 rad/s. Below the graph for the rotor speed, all three input currents are shown. It is evident that the current traces are almost perfect sinusoids, despite the fact that the input voltage is the PWM waveform shown in the bottom graph. Also, the trace for the torque shows no discernable high-frequency ripple. The reason is of course, that the motor windings are inductive, and represent a low pass filter for the applied voltages. Nevertheless, recent research suggests that filtering the output voltage of the inverter is advantageous anyway, because it significantly reduces the voltage stress on the windings and suppresses displacement currents through the bearings [8].

34.5 Simulations of ac Induction Machines using Field Oriented Vector Control

The following examples will demonstrate the use of PSpice® for simulations of ac induction machines using Field Oriented Control (FOC). Again, it is assumed that the reader is familiar with the basics of induction machine theory. Often times FOC is also called vector control, and both expressions can be used interchangeably. Field oriented control was proposed in the 1960s by Hasse and Blaschke, working at the Technical University of Darmstadt [6]. The basic idea of field oriented control is to inject currents into the stator of an induction machine such that the magnetic flux level and the production of electromagnetic torque can be independently controlled and the dynamics of the machine resembles that of a separately excited dc machine without armature reaction. The previously discussed two-phase model for the induction machine is very helpful for studies of vector control and shall be used in all examples. If a two-phase induction motor model for the synchronous (or excitation) reference frame is used, the similarities between the control of a separately excited dc machine and vector control of an ac induction machine would be most evident. In this case, the D input would correspond to the field excitation input of the dc machine and both inputs would be fed with dc current. Assuming unsaturated machines, the current into the D input of the induction machine or the field current in the dc machine would control the flux level. The Q input of the induction machine would correspond to the armature winding input of the dc machine and again both inputs would receive dc current. These currents would directly control the production of electromagnetic torque with a linear relation (constant k_T) between the current level and the torque level. Furthermore, the Q component of the current would not change the flux level established by the D component. To make such a simulation work, it would finally be necessary to calculate the slip value that corresponds to the commanded torque and supply this dc value to the D,Q (synchronous reference frame) machine model.

Of course this is very interesting from an academic standpoint and the author uses this example in a semester long lecture on field oriented control. However, it should again be noted that a machine represented by a model with a synchronous reference frame would have a *stator*, which rotates with synchronous speed. Of course this is not realistic and therefore it is more interesting to generate a simulation example that uses the previously discussed motor with a model for the stationary reference frame. This motor must be supplied with ac voltages and currents with a frequency determined mostly by the rotor speed to a small extent by the commanded torque. We still supply dc values representing the commanded flux and torque but we transform these dc values to appropriate ac values. In the following example we will assume that we can measure the actual rotor speed with a sensor. This can in effect be easily accomplished and many types of sensors are available on the market. If we add the slip speed, that we determine mathematically from the torque command, to the measured rotor speed, we obtain the synchronous speed for the given operating point. With this synchronous speed we can transform the dc flux and torque command values from the synchronous reference frame to the stationary reference frame. We accomplish this by using a rotational transformation according to the matrix equations in Eqn. (34.6). This rotational transformation is also called ‘Park’ transformation:

$$\begin{aligned}
&\begin{bmatrix} V_{\mathrm{Dout}} \\ V_{\mathrm{Qout}} \end{bmatrix} = \begin{bmatrix} \cos(\rho) & -\sin(\rho) \\ \sin(\rho) & \cos(\rho) \end{bmatrix} \begin{bmatrix} V_{\mathrm{Din}} \\ V_{\mathrm{Qin}} \end{bmatrix} \\
&\begin{bmatrix} V_{\mathrm{Dout}} \\ V_{\mathrm{Qout}} \end{bmatrix} = \begin{bmatrix} \cos(\rho) & \sin(\rho) \\ -\sin(\rho) & \cos(\rho) \end{bmatrix} \begin{bmatrix} V_{\mathrm{Din}} \\ V_{\mathrm{Qin}} \end{bmatrix} \\
&\begin{bmatrix} \cos(\rho) & -\sin(\rho) \\ \sin(\rho) & \cos(\rho) \end{bmatrix} \begin{bmatrix} \cos(\rho) & \sin(\rho) \\ -\sin(\rho) & \cos(\rho) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \qquad (34.6)
\end{aligned}$$

As shown in Eqn. (34.6), the transformation is bidirectional and the product of the transformation matrices yields the unity matrix. For the following discussion we shall define the transformation, which produces ac values from dc inputs as a positive vector transformation and the reverse operation as consequently a negative vector transformation. The matrix equation for the positive vector transformation is shown on the left-hand side of Eqn. (34.6). The negative transformation is very useful to extract dc values from ac voltages and currents for diagnostic purposes. We will also make use of it for sensorless vector control, which is discussed below. Both rotational transformations use the angle, ρ, in the equations. This angle can be interpreted as the momentary rotational displacement angle between two Cartesian coordinate systems; one containing the input values and the other one the output values. This angle is obtained by integration of the angular

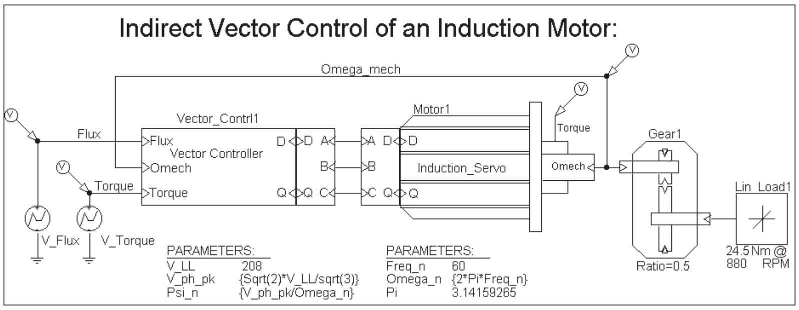


FIGURE 34.12 Top level circuit for indirect vector control of induction motors.

velocity with which the coordinate systems are rotating (typically the synchronous speed).

In summary, we replaced a theoretical motor model using a synchronous reference frame by a reference frame transformation of the supply voltages and currents. In fact, there are integrated circuits on the market like the ADMC-200 from Analog Devices, which is optimized to perform both the Clark and the Park transformation in both directions [1].

Figure 34.12 shows the top level of a simulation example that implements vector control for an induction machine with a stationary reference frame model. In fact, the motor model and the associated sub-circuits are identical to the ones used for the circuit shown in Fig. 34.8. However, a more powerful motor is used here, specifically a 3 hp, 4-pole 208 V motor with circuit parameters shown in Table 34.2. As discussed above, the actual speed of the rotor is used as an input signal for the control unit. This scheme is known as indirect vector control and represents one of the most often used arrangements. The symbol for the controller has the same parameters as the motor. This is necessary to achieve correct field orientation. In real systems, the controller also must know or somehow determine the machine parameters. The machine parameters could have also been established globally using "PARAM" symbols, but if the parameters for the controller can be set separately as is the case here, the influence of parameter mismatch on the performance of the control can be easily studied. An example of this is given below.

TABLE 34.2 List of all attributes for the induction motor symbol for vector control

Attributes
PART = Induction Servo
MODEL = Ind Motor
TEMPLATE =
J mot = 0.1
Omega init = 0.0
Ls = (Lm + Lsl)
Lr = (Lm + Lr1)
Poles = 4
Tau r = (Lr/ R Rot)
REFDES = Motor?
Lsl = 2.18mH
Lr1 = 2.89mH
R Stat = 0.48
R Rot = 0.358
Lm = 51.25mH

Figure 34.12 also shows a symbol for a mechanical gear, which is attached to the output of the induction motor. Let us recall that the voltage on the mechanical output terminal represents the angular velocity and the current represents the torque. We also know that the product of the angular velocity and the torque is the mechanical power. Therefore it is easily understood that the electrical representation of an ideal gear is an ideal transformer. The ideal transformer changes speed (voltage) and torque (current) just like an ideal gear. Also there are no power losses in an ideal transformer as well as in an ideal gear.

In this fashion, many more mechanical properties and devices can be modeled. For example, a mechanical flywheel is simply represented by a capacitor to ground. Due to the scaling factors for the angular velocity and the torque, a flywheel with $J = 1\ \text{kg m}^2$ would be a capacitor with $C = 1$ F. The compliance of a drive-shaft (elastic twisting by the applied torque) can be modeled by a series inductor. By including both capacitors and inductors, effects like mechanical resonance can be included in a model.

Figure 34.13 shows the subcircuit for the vector control unit. The central part is a vector rotator for positive direction. This element transforms the dc reference values for the flux (D axis) and the torque (Q axis) to the stationary reference frame. The input angle for the vector rotator is the integral of the synchronous angular velocity. The signal called "Omega o" is the measured rotor speed.

This speed is multiplied with the number of pole-pairs (poles/2) to obtain the electrical angular velocity. Then the slip value (see Eqn. (34.7)) appropriate to the torque command is added and the resulting signal is routed through an integrator to generate the input angle for the vector rotator.

In the D axis, a differentiator function "DDT()" is used in a compensation (see Eqn. (34.8)) element which assures that the actual flux in the machine follows the commanded signal

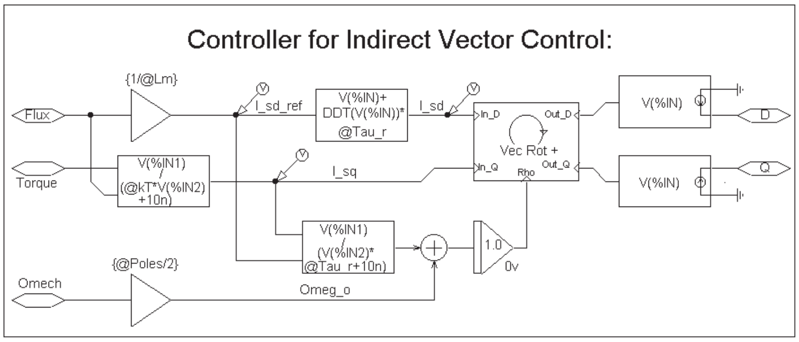

Controller for Indirect Vector Control:
{1/@Lm}
Flux
Torque
Omech
{@Poles/2}
V(%IN1)
/
(@kT*V(%IN2)
+10n)
I_sd_ref
V(%IN)+
DDT(V(%IN))*
@Tau_r
I_sd
I_sq
V(%IN1)
/
(V(%IN2)*
@Tau_r+10n)
Omeg_o
1.0
0v
In_D
Out_D
Vec Rot +
In_Q
Rho
Out_Q
V(%IN)
V(%IN)
D
Q

FIGURE 34.13 Sub-circuit for indirect vector control of induction motors.

without delay. The input and output values of the vector rotator are voltage signals which correspond 1 : 1 to current signals. (In a real controller the currents are typically scaled values in the memory of a digital signal processor, DSP.) In fact, the vector controller calculates the appropriate currents that need to be injected into the machine to perform as desired. Two voltage-controlled current sources with unity gain are connected to the output of the vector rotator to generate these currents. In a real system, the controlled current sources are realized by an inverter with current feedback. In the most realistic case, this would be a three-phase inverter and the ABC-DQ transformation would be performed before the current-controlled inverter. In this example, the ABC-DQ transformation has been performed outside the controller and outside the motor. This way, it is possible to study vector control principles using a DQ controller and a DQ motor by eliminating the ABC-DQ transformation elements. An example is given in Fig. 34.14.

$$\omega_{\text{slip}} = L_{\text{m}} \frac{I_{\text{sq}}}{(\tau_{\text{r}} \lambda_{\text{rd}})} \tag{34.7}$$

$$I_{\text{sd}} = \frac{(\lambda_{\text{rd}} + \tau_{\text{r}} \lambda_{\text{rd}} p)}{L_{\text{m}}} = \frac{1 + \tau_{\text{r}} p}{L_{\text{m}}} \lambda_{\text{rd}} \qquad p = \frac{d}{dt}. \tag{34.8}$$

Figure 34.15 shows the results obtained for the circuit shown in Figs. 34.12–34.14 with perfect tuning of the vector controller, meaning that the controller precisely knows all motor parameters. The two traces in the diagram on top of Fig. 34.15 represent the traces for the D and Q input signals of the vector rotator. The graph below shows the reference value for the flux. It is evident that the flux level is being changed at the same time when 10 Nm of torque is commanded (and produced). This is done to check if the torque and the flux can be independently controlled, which is true for correct field oriented control. Below the flux reference is the graph for the mechanical angular velocity. It can be seen that the machine accelerates whenever torque is developed and slows down due to the load when the torque command is driven to zero. The graph on the bottom of Fig. 34.15 provides the easiest way to judge the quality of the correct field orientation. This graph shows the traces of the commanded and the actually produced torque and in this case they are perfectly on top of each other at all times.

Figure 34.16 is an example of the results obtained from a detuned vector controller. The circuit is identical to the circuit in Fig. 34.12, except for the fact that the rotor resistance value in the controller was increased to 125 . It is obvious that the traces for the commanded and the actually produced torque are no longer identical. This is especially true during times when the flux is changing. Detuning is actually a real problem in industrial vector control applications. Detuning is caused by the fact that the machine parameters are not precisely known to begin with and/or are changing during the operation of the machine. The values of the winding resistance are most likely to change due to heating of the machine.

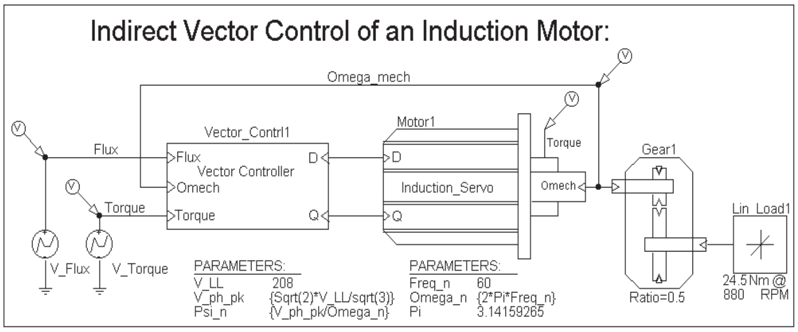

Indirect Vector Control of an Induction Motor:
Omega_mech
Flux
Vector_Contrl1
Flux
Vector Controller
Omech
Torque
D
Q
Torque
V_Flux
V_Torque
Motor1
D
Induction_Servo
Q
Torque
Omech
Gear1
Ratio=0.5
Lin_Load1
24.5 Nm @
880 RPM
PARAMETERS:
V_LL 208
V_ph_pk {Sqrt(2)*V_LL/sqrt(3)}
Psi_n {V_ph_pk/Omega_n}
PARAMETERS:
Freq_n 60
Omega_n {2*Pi*Freq_n}
Pi 3.14159265

FIGURE 34.14 Circuit for indirect vector control without ABC-DQ transformations.

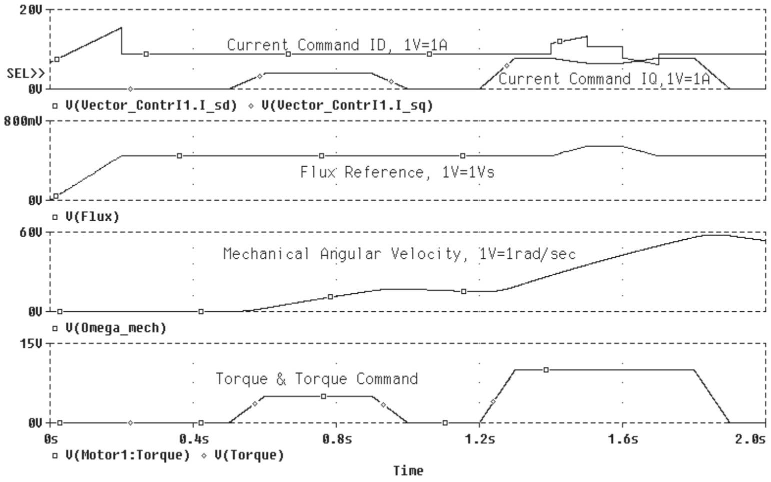


FIGURE 34.15 Results for indirect vector control with perfect tuning.

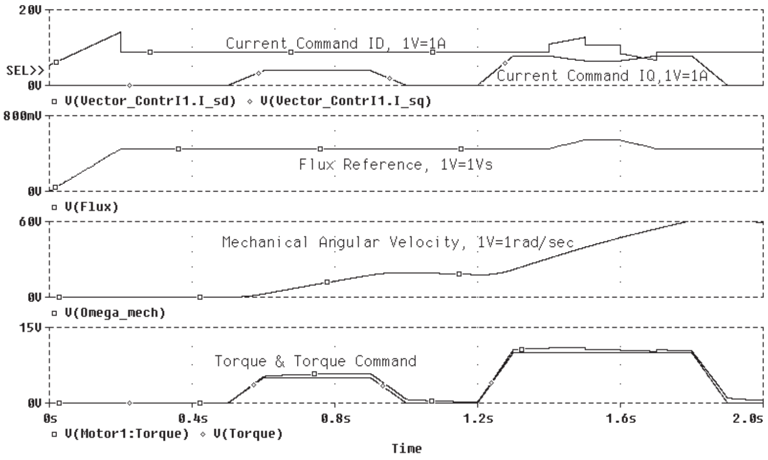
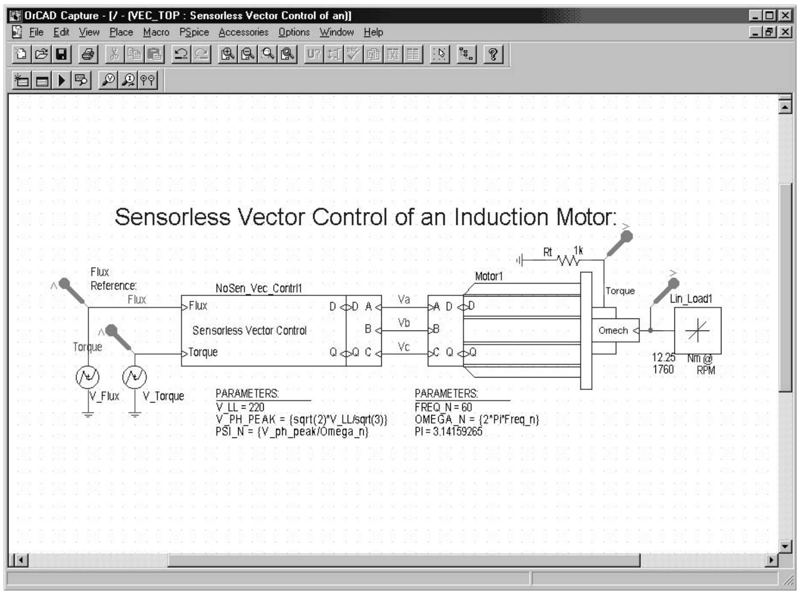


FIGURE 34.16 Results for indirect vector control with 125 rotor resistance.

34.6 Simulation of Sensorless Vector Control Using PSpice® Release

In the previous example, the advantages of vector control have been shown. However, for the implementation of the control scheme a sensor for the mechanical speed was necessary. This could pose a problem for applications, where a vector control unit is to be retrofitted into existing equipment. The motor installation may not easily allow the installation of a mechanical speed sensor. Therefore engineers have thought to replace the mechanical speed sensor with a speed observer, which is a mathematical model that is evaluated by the control processor (typically a DSP), which is performing the standard vector control computations anyway. The algorithm for the observer would use the measured stator voltages and currents for the D and Q axis as input parameters. It would also rely on the knowledge of the machine model and on the correct machine parameters (rotor and stator resistance, mutual and leakage inductance, etc.). The following example shows such an arrangement. It could be derived from the previous example, with the only difference being that the speed sensor signal is replaced by a speed observer. However, careful examination of the derivation [3] of the speed observer reveals that it is easier to calculate the synchronous angular velocity, which is ultimately desired anyway, than the angular velocity of the rotor. Therefore, the observer was modified and the calculation of the rotor speed and the subsequent addition of the slip speed was foregone. The speed observer used here basically solves the D,Q equation system of the induction machine shown in Eqn. (34.3), with the only difference that some of the dependent variables are now independent and vice versa. In addition to the synchronous angular velocity, the observer provides the values of the rotor flux, which are used in the D axis signal path. The advantage of this is that the compensator with the differentiation function, which is problematic from a numerical stability standpoint, can be eliminated.

Figure 34.17 shows the top level of a simulation project for sensorless vector control. This and the following figures for the sensorless control project show the screen view from PSpice® 9.0/ORCAD. The top view of this circuit is very similar to the circuit for the indirect vector control represented by Figs. 34.12 and 34.14 except for the missing motor-speed feedback. The model for the motor and the motor's parameters are precisely the same as in the example for the indirect vector control. The circuit has originally been developed using MicroSim's PSpice® 8.0 and subsequently imported into the PSpice® 9.0 environment using the "File/Import Design…" dialog. Selecting the "Sensorless Vector Control" block and choosing "Descend Hierarchy" reveals the associated subcircuit, which is shown in Fig. 34.18. This subcircuit is similar to the sub-circuit for the indirect vector control with two exceptions. First and foremost, the motor-speed feedback signal is replaced by the speed observer. In this case the speed observer directly provides the synchronous angular velocity. Therefore, it is not necessary to calculate the slip speed and add it to the


OrCAD Capture - [/ - (VEC_TOP : Sensorless Vector Control of an)]
File Edit View Place Macro PSpice Accessories Options Window Help
Sensorless Vector Control of an Induction Motor:
Flux Reference:
Flux
Torque
V_Flux
V_Torque
NoSen_Vec_Contrl1
Flux
Sensorless Vector Control
Torque
D
D
A
B
Q
Q
C
Va
Vb
Vc
A
B
C
D
D
Q
Q
Motor1
Rt
1k
Torque
Omech
Lin_Load1
12.25 Nm @
1760 RPM

PARAMETERS:
V_LL = 220
V_PH_PEAK = {sqrt(2)*V_LL/sqrt(3)}
PSI_N = {V_ph_peak/Omega_n}

PARAMETERS:
FREQ_N = 60
OMEGA_N = {2*PI*Freq_n}
PI = 3.14159265

FIGURE 34.17 Top level of simulation circuit for sensorless vector control.

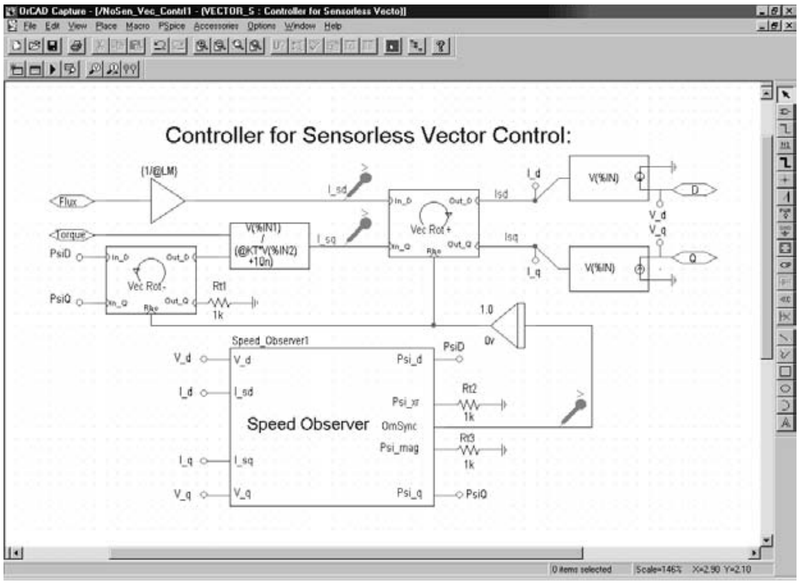

OrCAD Capture - [/NoSen_Vec_Contl1 - (VECTOR_S : Controller for Sensorless Vecto)]
File Edit View Place Macro PSpice Accessories Options Window Help
Controller for Sensorless Vector Control:
Flux
Torque
(1/@LM)
I_sd
V(%IN1)
/
(@KT*V(%IN2)
+10n)
I_sq
In_D
Out_D
Vec Rot +
In_Q
Out_Q
Rho
Isd
Isq
I_d
I_q
V(%IN)
V(%IN)
D
Q
V_d
V_q
PsiD
PsiQ
In_D
Out_D
Vec Rot -
In_Q
Out_Q
Rho
Rt1
1k
1.0
0V
Speed_Observer1
V_d
I_d
I_q
V_q
V_d
I_sd
I_sq
V_q
Speed Observer
Psi_d
Psi_xr
OmSync
Psi_mag
Psi_q
PsiD
PsiQ
Rt2
1k
Rt3
1k
0 items selected
Scale=146%
X=2.90 Y=2.10

FIGURE 34.18 Subcircuit for sensorless vector controller.

rotor speed to obtain the synchronous speed. Second, the values of the rotor flux, which are available from the speed observer, are used to calculate the reference value for the torque producing current (Q) component. Therefore, the compensation term, which contains a differentiator in the D axis of the controller shown in Fig. 34.13, can be eliminated. The purpose of the compensation term is to ensure that the flux is equal to the flux command at all times with no delay. If that is assured, the command signal can be chosen in place of the real flux to calculate how much torque producing current is necessary to obtain the desired torque. However, if the actual flux is known (observed), this value can be used instead. Since the flux observer is fed by the D and Q axis voltages and currents for the stationary reference frame, the flux components need to be transformed back into the synchronous reference frame. This is done with the "Negative Vector Rotator" located above and to the left of the speed observer in Fig. 34.18.

The PSpice® 9.0/ORCAD evaluation version has somewhat stricter limitations for the number of graphical elements on the schematic pages of the project. However, the limitations for the number of nodes for the actual simulation engine are seemingly the same. Therefore, the extensive subcircuit of the induction motor model (see Fig. 34.9) has been replaced by a number of additional attributes, which have been added to the motor symbol using the symbol editor. The easiest way to start the symbol editor and to open the appropriate library is to select the symbol by clicking into it and then select the "Edit Symbol" function. The additional attributes of the modified motor symbol will enter the equivalent to the sub-circuit represented by Fig. 34.9 into the netlist. The netlist is a compilation of the schematic pages into a textual description in ASCII format. From a usability standpoint, a 'self contained' symbol like this is a very elegant solution, since the file for the subcircuit is no longer required.

Since the PSpice® simulation engine always uses the netlist as the input, the circuit works identically. For the PSpice® simulation it makes no difference where the netlist or part of it comes from. This also means that even the most recent release of PSpice® can still simulate legacy files that have been created before the introduction of schematic editors. The introduction of netlist entries is done via the "TEMPLATE" attribute. This attribute is a system attribute and a part of every symbol. Therefore, the TEMPLATE attribute is of course present in the attribute list for the motor symbols in the previous examples. These attribute lists are shown in Table 34.1 and 2. In these tables the TEMPLATE attribute has no value since the netlist entries are made by the symbols in the associated subcircuit. To give the reader a better understanding of the self-contained machine symbol, the format of some common netlist entries and the syntax of the value of the TEMPLATE attribute is now discussed. It is also very helpful to examine the TEMPLATE attributes of existing symbols.

The format of the netlist entries for some common elements is ([] denotes space holder for name extension specific for a symbol to avoid duplicate names):

Resistors (R devices)

Generic:	Rname []	+Node[]	− Node[]	Value	;Optional Comment
Example:	Rsd[]	Rsd+[]	Rsd−[]	1.0k	;Resistor, fixed Value
Example:	Rsd[]	Rsd+[]	Rsd−[]	{ Rs}	;Resistor, Value Rs passed on
Example:	Rsd[]	D	0	1.0k	;Resistor, 1k, Pin 'D' to Gnd

Inductors (L devices):

Generic:	Lname[]	+Node[]	−Node[]	Value	;Optional Comment
Example:	Lsd[]	Lsd+[]	Lsd−[]	1.0u	;Inductor, 1.0μH fixed
Example:	Lsd[]	Lsd+[]	Lsd−[]	{ Lsl}	;Inductor, Value Lsl passed on

Voltage-controlled voltage sources (E devices)

Generic:	Ename[]	+Out[]	−Out[]	VALUE { Control Function }
Example:	ETorque[]	Torque	0	VALUE { 1.5*(Vt1[] − Vt2[]) }
	;E source, output between pin 'Torque' and Gnd, Control function as shown			

Figure 34.19 shows the screen view of the symbol for the induction motor in the symbol editor in PSpice® Release 8.0, which was used for the development of this part. Figure 34.20 shows a similar view; however, here the window for entry and editing of attributes is also visible. This screen can be invoked using the "Part/Attributes..." dialog. The attributes that create the netlist entries, which insert the previously discussed model for the motor, are entered here. A complete list of all attributes, extracted from a working example, is given in Table 34.3. Therefore, the reader should be able to enter the attributes exactly as printed and obtain a working model, which can be used in PSpice® Release 8.0 and 9.0.

According to Table 34.3, the value for the TEMPLATE attribute is as follows:

TEMPLATE = ElectricD n n ElectricQ n n Mechanical

This statement will insert the expression for "ElectricD", i.e. the T-equivalent circuit for the D axis, two carriage returns " n n", the expression for "ElectricQ", i.e. the T-equivalent circuit for the Q axis, two more carriage returns " n n", and finally the expression for "Mechanical", i.e. the mechanical model into the netlist. The expressions for "ElectricD", "ElectricQ", and "Mechanical" are defined in separate attributes. Careful examination of the values of the "ElectricD", "ElectricQ", and "Mechanical" attributes reveals a number of

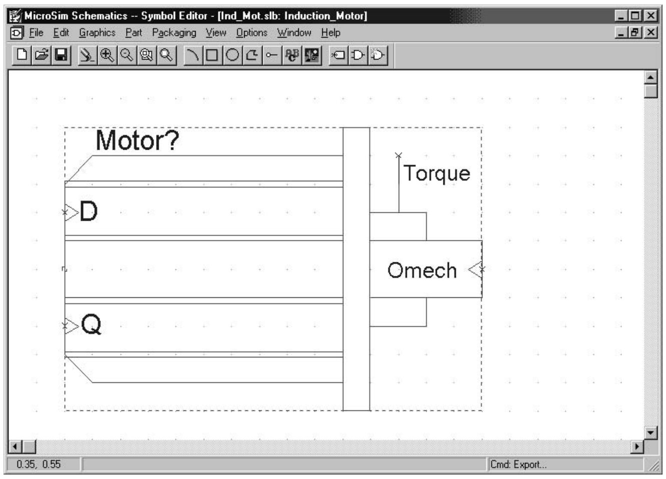
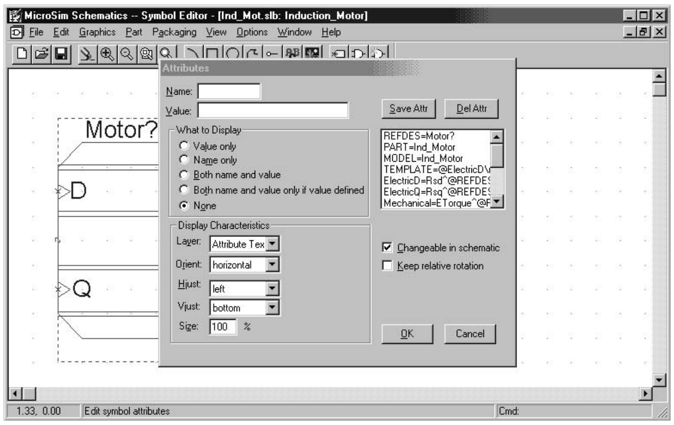

MicroSim Schematics -- Symbol Editor - [Ind_Mot.slb: Induction_Motor]
File Edit Graphics Part Packaging View Options Window Help
Motor?
Torque
D
Omech
Q
0.35, 0.55
Cmd: Export...

FIGURE 34.19 Screen view of motor symbol in the symbol editor.


MicroSim Schematics -- Symbol Editor - [Ind_Mot.slb: Induction_Motor]
File Edit Graphics Part Packaging View Options Window Help
Attributes
Save Attr
Del Attr
OK
Cancel
Motor?
D
Q
1.33, 0.00
Edit symbol attributes
Cmd:

Name:

Value:

What to Display
- ○ Value only
- ○ Name only
- ○ Both name and value
- ○ Both name and value only if value defined
- ● None

REFDES=Motor?
PART=Ind_Motor
MODEL=Ind_Motor
TEMPLATE=@ElectricD\
ElectricD=Rsd^@REFDES
ElectricQ=Rsq^@REFDES
Mechanical=ETorque^@F

Display Characteristics
Layer: Attribute Tex
Orient: horizontal
Hjust: left
Vjust: bottom
Size: 100 %

☑ Changeable in schematic
☐ Keep relative rotation

FIGURE 34.20 Screen view of symbol editor with attribute input window.

TABLE 34.3 List of all attributes used for the self-contained induction motor symbol

Attributes
REFDES = Motor?
PART = Ind Motor
MODEL = Ind Motor
TEMPLATE = ElectricD n n ElectricQ n n Mechanical
R Stat = 0.48
R Rot = 0.358
Lm = 51.25mH
Lsl = 2.18mH
Lrl = 2.89mH
J mot = 0.1
Omega init = 0.0
Poles = 4
ElectricD = Rsd^ REFDES D 1^ REFDES R Stat nLsld^ REFDES 1^ REFDES Vmd^ REFDES Lsl nLmd^ REFDES Vmd^ REFDES 0 Lm nLrld^ REFDES Vmd^ REFDES 2^ REFDES Lrl nRrd^ REFDES 2^ REFDES ErotD^ REFDES R Rot nErotd^ REFDES ErotD^ REFDES 0 VALUE {-(Ome^ REFDES)*((V(Q,3^ REFDES)/ R Stat)* Lm n + + (V(ErotQ^ REFDES,4^ REFDES)/ R Rot)*(Lm + Lrl)) }
ElectricQ = Rsq^ REFDES Q 3^ REFDES R Stat nLslq^ REFDES 3^ REFDES Vmq^ REFDES Lsl nLmq^ REFDES Vmq^ REFDES 0 Lm nLrlq^ REFDES Vmq^ REFDES 4^ REFDES Lrl nRrq^ REFDES 4^ REFDES ErotQ^ REFDES R Rot nErotq^ REFDES ErotQ^ REFDES 0 VALUE {V(Ome^ REFDES)*((V(D,1^ REFDES)/ R Stat)* Lm n + + (V(ErotD^ REFDES,2^ REFDES)/ R Rot)*(Lm + Lrl)) }
Mechanical = ETorque^ REFDES Torque 0 n + VALUE { (1.5* Lm* Poles/2) * (n + ((V(Q,3^ REFDES)/ R Stat)*(V(ErotD^ REFDES,2^ REFDES)/ R Rot)) - n + ((V(D,1^ REFDES)/ R Stat)*(V(ErotQ^ REFDES,4^ REFDES)/ R Rot))) } nEOme^ REFDES Ome^ REFDES 0 VALUE V(Om^ REFDES)* Poles/2 } nVLd^ REFDES Om^ REFDES Omech 0V nEom^ REFDES Om^ REFDES 0 VALUE {SDT((V(Torque)-I(VLd^ REFDES))/ J mot) + Omega init

repetitive terms. The meaning of these terms are explained below:

Name	Substitutes what is defined for “ Name” at the current place.
^ REFDES	Inserts the path “^” and the reference designator “ REFDES” to create a unique node or part name, that does not repeat. The path is the concatenation of the names of the symbols and sub-circuits in the hierarchy above the part. The reference designator is the name of the part on a particular schematic page.
n	new line (carriage return) is inserted into the netlist; however the value of the attribute does not have a carriage return in it. This means everything listed after “ElectricD” until “ElectricQ” goes on one line. If the symbol definition is printed however, it is shown as in Table 34.3.
n+	new line and continuation of expression.
n + +	new line, continuation of expression, numerical operator “ + ”.

Figure 34.21 shows a subcircuit for the speed observer. This schematic shows the structure and all the details of the implementation in the form of a block diagram. The speed observer uses the stator voltages and currents for the D and the Q axis as input variables. After subtracting the voltage drop across the winding resistance and the leakage inductance of the stator from the stator input voltage and scaling the result by L_r/L_m, the observer calculates the D and Q components of the rotor flux by integration. Since the input values are in the stationary reference frame, so are the results. The observer also calculates the magnitude of the rotor flux and then calculates the synchronous angular velocity by evaluating the rate of change of the ratio of the D and Q components. The mathematical relationships are given by Eqns. 34.9 and 34.10 [3]:

$$p\begin{bmatrix}\lambda_{rd}\\ \lambda_{rq}\end{bmatrix}=\frac{L_r}{L_m}\left[\begin{bmatrix}V_{sd}\\ V_{sq}\end{bmatrix}-\begin{bmatrix}R_s+\sigma L_s p & 0\\ 0 & R_s+\sigma L_s p\end{bmatrix}\begin{bmatrix}I_{sd}\\ I_{sq}\end{bmatrix}\right]$$

$$\sigma=\left[1-\frac{L_m^2}{(L_r L_s)}\right] \qquad \sigma = \text{leakage factor} \tag{34.9}$$

$$\frac{d}{dt}\operatorname{atan}\left(\frac{\lambda_{rq}(t)}{\lambda_{rd}(t)}\right)=\omega_s=\left(\frac{\frac{d}{dt}\lambda_{rq}(t)\lambda_{rd}(t)-\lambda_{rq}(t)\frac{d}{dt}\lambda_{rd}(t)}{(\lambda_{rd}(t)^2+\lambda_{rq}(t)^2)}\right). \tag{34.10}$$

Since the observer shown in Fig. 34.21 has a large number of elements, this sub-circuit has also been integrated into a custom part by creating an appropriate TEMPLATE and other supporting attributes. A complete listing, which was extracted from thoroughly tested part, is given in Table 34.4. Using this table, the reader should be able to create this very complex part with relative ease.

Figure 34.22 shows the output for the sensorless vector control project as it presents itself in the PSpice® 9.0/ORCAD evaluation version.

A comparison of the traces for the torque and the torque command (they are perfectly on top of each other) shows that

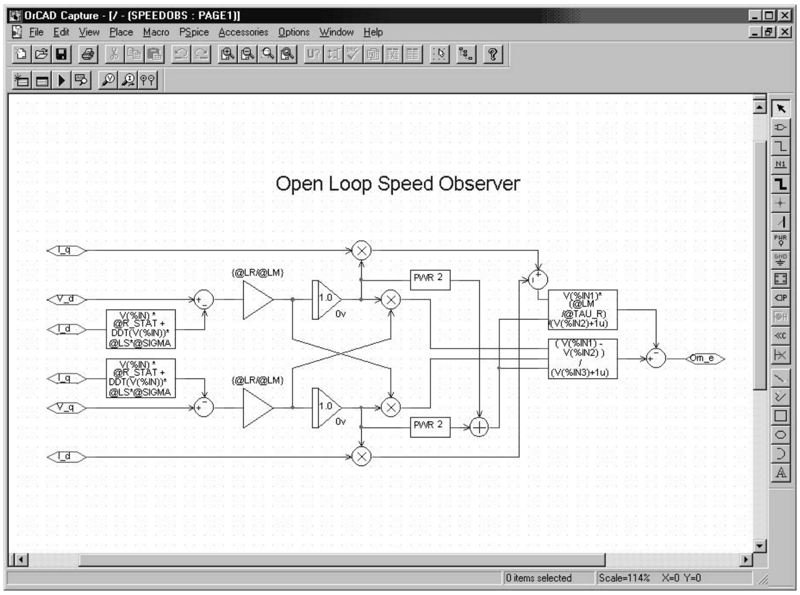

OrCAD Capture - [/ - (SPEEDOBS : PAGE1)]
File Edit View Place Macro PSpice Accessories Options Window Help
Open Loop Speed Observer
I_q
V_d
I_d
I_q
V_q
I_d
V(%IN) * @R_STAT + DDT(V(%IN))* @LS*@SIGMA
V(%IN) * @R_STAT + DDT(V(%IN))* @LS*@SIGMA
{@LR/@LM}
{@LR/@LM}
1.0
0v
1.0
0v
PWR 2
PWR 2
V(%IN1)* (@LM /@TAU_R) /(V(%IN2)+1u)
(V(%IN1) - V(%IN2)) / (V(%IN3)+1u)
Om_e
0 items selected
Scale=114% X=0 Y=0

FIGURE 34.21 Subcircuit for speed observer for sensorless vector controller.

TABLE 34.4 List of all attributes for the speed observer symbol

Attributes

```
REFDES = Speed  Observer?
PART = Speed  Obs
MODEL = Speed  Obs

TEMPLATE = Ed^   REFDES    Psi  d 0 VALUE {    EXP  d1
 n+    EXP  d2  n+    EXP  d3 }
 nEq^   REFDES    Psi  q 0 VALUE {    EXP  q1
 n+    EXP  q2  n+    EXP  q3 }
 nEmag^   REFDES    Psi  mag 0 VALUE { V(    Psi  d)*V(    Psi  d)+  V(    Psi  q)*V(    Psi  q) }
 nExr^   REFDES    Psi  xr 0 VALUE {    EXP  x1
 n+    EXP  x2  n+    EXP  x3  n+    EXP  x4 }
 nEOmSync^   REFDES    OmSync 0 VALUE {    EXP  om1 }

SIMULATIONONLY =
EXP  d1 =    Ini  d +
EXP  d2 = SDT( (   Lr/   Lm)*( V(    V  d) - V(    I  sd)*   R  Stat
EXP  d3 = -DDT(V(    I  sd))*   Ls*   Sigma ) )
EXP  q1 =    Ini  q +
EXP  q2 = SDT( (   Lr/   Lm)*( V(    V  q) - V(    I  sq)*   R  Stat
EXP  q3 = -DDT(V(    I  sq))*   Ls*   Sigma ) )
Ini  d = 0.0V
Ini  q = 0.0V
EXP  x1 = ( V(    Psi  d)*(   Lr/   Lm)*
EXP  x2 = ( V(    V  q) - V(    I  sq)*   R  Stat - DDT(V(    I  sq))*   Ls*   Sigma ) )
EXP  x3 = -( V(    Psi  q)*(   Lr/   Lm)*
EXP  x4 = ( V(    V  d) - V(    I  sd)*   R  Stat - DDT(V(    I  sd))*   Ls*   Sigma ) )
EXP  om1 = ( V(    Psi  xr)/(V(    Psi  mag)+ 1u) )
```

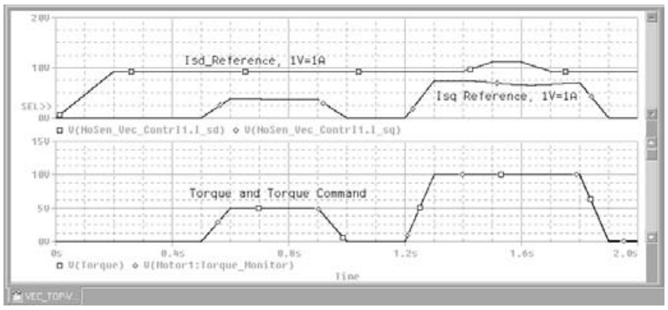


FIGURE 34.22 Simulation results for sensorless vector control.

the scheme works perfectly. It even works for a start from zero speed, which is typically not the case in real systems. The reason is, that the uncertainties of the winding resistance values (note that they change with temperature) create errors in observers like this one. The problem is worst at low speeds, because at low speeds and associated low stator frequencies, the uncertain winding resistance represents a large part of the total machine impedance.

34.7 Simulations Using Simplorer®

In the following, some examples of simulations with the evaluation version of Simplorer® [9], Release 4.1 are shown. It should be acknowledged at this point, that these examples have been created by Ali Ricardo Buendia, who is presently working towards his MSEE degree. The advantages of Simplorer® are that it has a lot of models for power electronics devices and machines built in, since it is specialized for this type of simulation. Also, no numerical convergence problems have been noticed thus far. Figure 34.23 shows the schematic for a three-phase diode rectifier. The input is a balanced three-phase source with a reactive source impedance. An exponential characteristic, closely resembling real diodes, has been chosen as a model for the diodes.

Figure 34.24 shows a circuit which transforms the load currents from a three-phase to a two-phase system. Here the D, Q components are called alpha, beta components. The

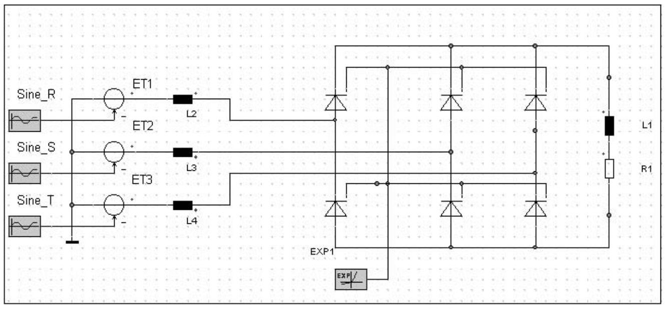


FIGURE 34.23 Simplorer® schematics for three-phase rectifier.

results of the simulation are shown on the same page that is used for the schematic diagrams shown by the previous two figures. Figure 34.25 shows a plot of the line currents during the start-up of the rectifier, where the initial load current is zero. The next graph shows a plot of the line currents that have been transformed by the circuit shown in Fig. 34.24. The components of the line currents are the variables of the axes. The plot shows the typical hexagonal trace that can be expected for this type of line commutated rectifier (six-step operation). If the converted source voltages were plotted in this fashion, a perfect circle would be the result.

The last two graphs demonstrate a Simplorer® simulation of the start of an induction motor. As previously mentioned, the symbol and the model for the induction motor is built into the code. Figure 34.27 shows the schematic with the source and the induction motor as well as a graph that shows the rotational speed as a function of time. The graph below shows plots of the stator and rotor flux components, which are available from the machine model. Like the plot of the current components for the rectifier, the flux components are the variables of the axes in the graphs of Fig. 34.28.

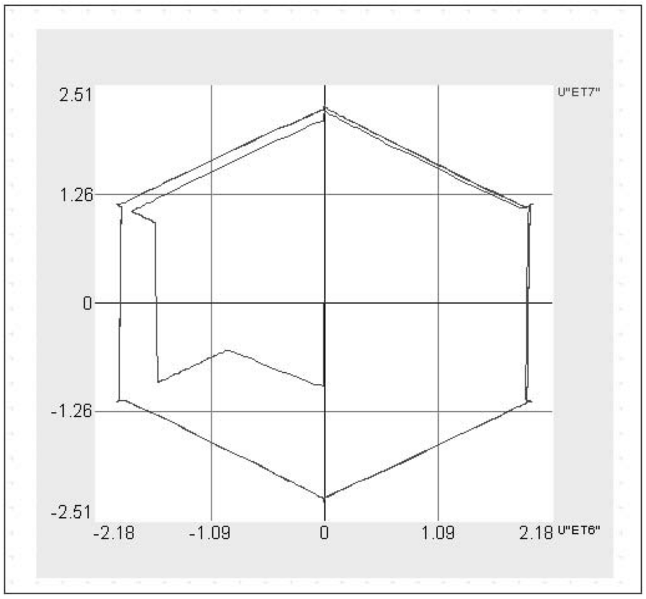
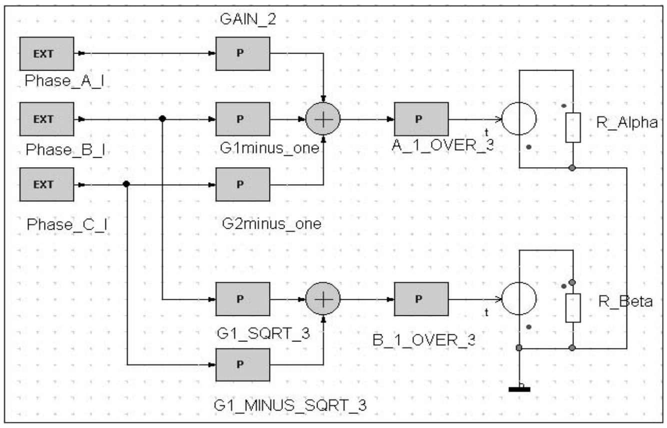
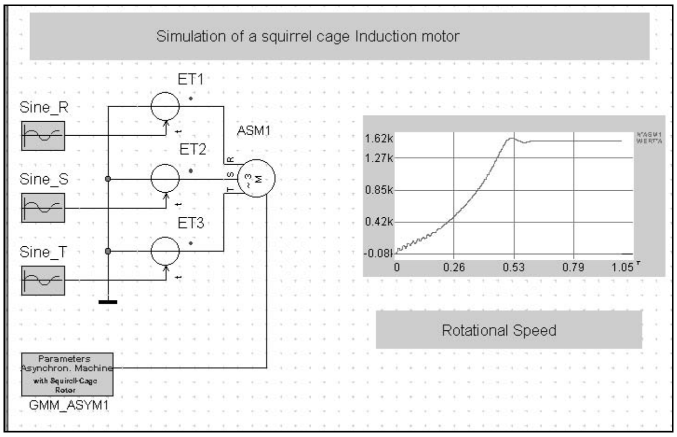


FIGURE 34.26 Plot of converted load currents for the three-phase rectifier.



GAIN_2
EXT
Phase_A_I
EXT
Phase_B_I
EXT
Phase_C_I
P
G1minus_one
G2minus_one
A_1_OVER_3
R_Alpha
G1_SQRT_3
B_1_OVER_3
R_Beta
G1_MINUS_SQRT_3

FIGURE 34.24 Three-phase to two-phase conversion for load currents.



Simulation of a squirrel cage Induction motor
Sine_R
Sine_S
Sine_T
ET1
ET2
ET3
ASM1
1.62k
1.27k
0.85k
0.42k
-0.08k
0
0.26
0.53
0.79
1.05
Rotational Speed
Parameters Asynchron. Machine with Squirrel-Cage Rotor
GMM_ASYM1

FIGURE 34.27 Simplorer® schematics for induction motor start.

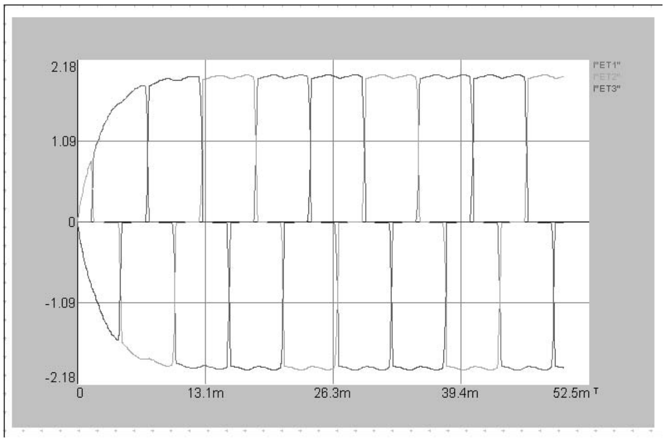
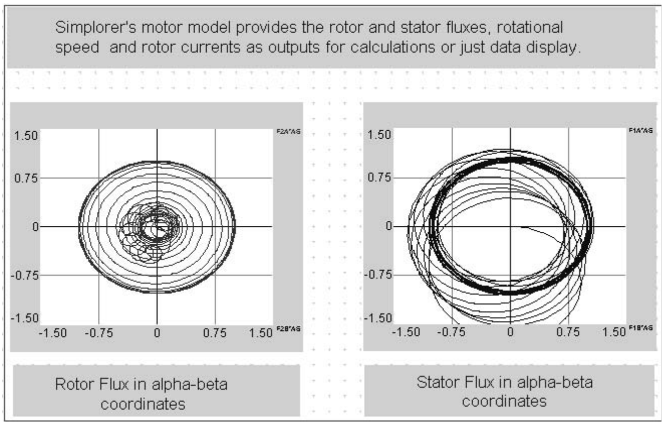


FIGURE 34.25 Simplorer® plot of load currents for the three-phase rectifier.



Simplorer's motor model provides the rotor and stator fluxes, rotational speed and rotor currents as outputs for calculations or just data display.

FIGURE 34.28 Simplorer® plots of machine fluxes for induction motor start.

34.8 Conclusions

In this chapter, the capabilities of two versions of PSpice® [12] and a version of Simplorer® [9] have been used to simulate a number of projects from the power electronics, machines and drives area. The advantage of PSpice® is that it is based on the almost universal Spice simulation language, which can be seen as the worldwide *de facto* standard. On the other hand Simplorer® has the advantage of built-in machine models. If both programs are used, comparisons and mutual validations of models can be performed. The reader should always validate any model before it is used for critical engineering decisions. It was pointed out in the introduction, that model validation often means verification that the limitations of the model are not exceeded.

In addition to the detailed examples, some general guidelines on the uses of simulation for analysis and design have been developed. All tested programs yielded excellent results. The simulation time for each project shown is typically less than a minute on a 400 MHz PC. It is hoped that the reader has obtained an insight and appreciation of the power of these modern simulation codes and some useful ideas and inspirations for projects of his own.

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35

Packaging and Smart Power Systems

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35.1 Introduction

A continual endeavor in power electronics is to increase power density. This is achieved by shrinking component size, moving components closer and reducing component count. During the last two decades circuit frequencies increased sharply to shrink component dimensions. Improved thermal management and physical packaging materials brought components closer. And finally, increased integration of functions at the semiconductor and package levels reduced component count. This has been marked in the microelectronics world by "system on chip" (SOC) and "system on package" (SOP), all addressing higher densities and all applicable to power electronic systems.

The latter approach of "functional integration" has been ongoing for decades. Until the 1980s nearly all such integration was done at the packaging level melding control and power processing. The term "smart power" (within the context of power electronic conditioning) applied in the 1960s–1970s to the integration of computers and microprocessors into large rectifier and converter cabinets. With the advent of high-voltage-silicon integrated circuits more functionality was brought directly to the power semiconductors, and in the 1980s–1990s the term applied mostly to smart power semiconductors. In the late 1990s there was a move back to hybrid integration following the trend to SOP. The term "Smart Power" has also been commercially associated with power management circuits.

From a designer's perspective, "functional integration" exists in a *packaging continuum* with "smart power" as a subset, dependent on the definition in vogue. To take advantage of "functional integration" the designer, in reverse thinking, partitions or modularizes circuits and functions to achieve the most cost-effective approach that meets a set of required performance specifications. This chapter provides background information, framework and procedures to produce partitioning and functional integration.

35.2 Background

Circuits are typically designed with a pre-determined idea of what packaging technologies will be used. The technologies range from silicon integration of subcircuit functions to multiple boards in a rack. Partitioning a circuit packaged in one technology, such as all silicon, is straightforward. Partitioning a circuit in multiple technologies is much more difficult since higher performing technologies duplicate

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aspects of lower technologies. The duplication geometrically increases parameter trade-offs and causes wasted packaging cost. Considerable literature exists about the technical characteristics of packaging materials and processes. (A table of characteristics is provided later.) Also, a study on the Status on Power Electronics Packaging (STATPEP) [1] identifies metrics to further evaluate the relative technical merits.

To optimize the use of multiple technologies in functional integration, a structured method should be used. A full-cost model for various technologies is used as a basis to produce a comparative cost diagram. The diagram allows intermixing of high and low performance technologies based on surface density, which is interpreted as circuit area and, hence, a partition. An example is given in Section 35.7 to demonstrate the method using a 2.2 kW motor drive module product.

The method is also applied to product modularization, i.e. system partitioning where a specific function is used across several products. A module can represent functional integration within a packaging technology or use multiple packaging technologies to create integrated power modules (IPMs) or power electronic building blocks (PEBBs). The importance of modularization is to increase product volume to lower cost. The cost model includes variations based on volume.

This partitioning approach matches user requirements to "Levels of Packaging" as defined in the "Framework for Power Electronics Packaging" [2] and provides optimum integration of packaging levels for a product. The Framework also identifies critical technical issues that need to be considered in evaluating technical performance. This partitioning approach looks at electrical, magnetic, thermal and mechanical issues (multiple energy forms).

35.3 Functional Integration

Figure 35.1 shows a 2.2 kW ac motor drive. Functional integration requires that the system be partitioned both electrically and physically. The systems integrator is usually an electrical designer and the first partitioning is usually electrical. The *electrical* partitions and distributed power losses are also shown in the figure. The physical partitioning, or packaging, involves different components with different functions ranging from fine-line control to high-current, high-loss power processing. Several partitions can be pursued. The Line-communications and Motor-control Blocks can use a signal-level packaging approach, such as all-silicon ASIC (application-specific integrated circuit), or discrete components on an epoxy-glass (FR-4) or insulated-metal substrates (IMS). If the Power Supply and Control Blocks are to be combined, an SMT approach cannot accommodate bulky storage components in the power supply. Hence, a through-hole approach is considered for part or both blocks. Regardless, such tradeoffs can be nearly endless. A structured method needs to be used to establish essential requirements and guide circuit and system partitioning. The method described here is based on characterizing and grouping the components, eval-

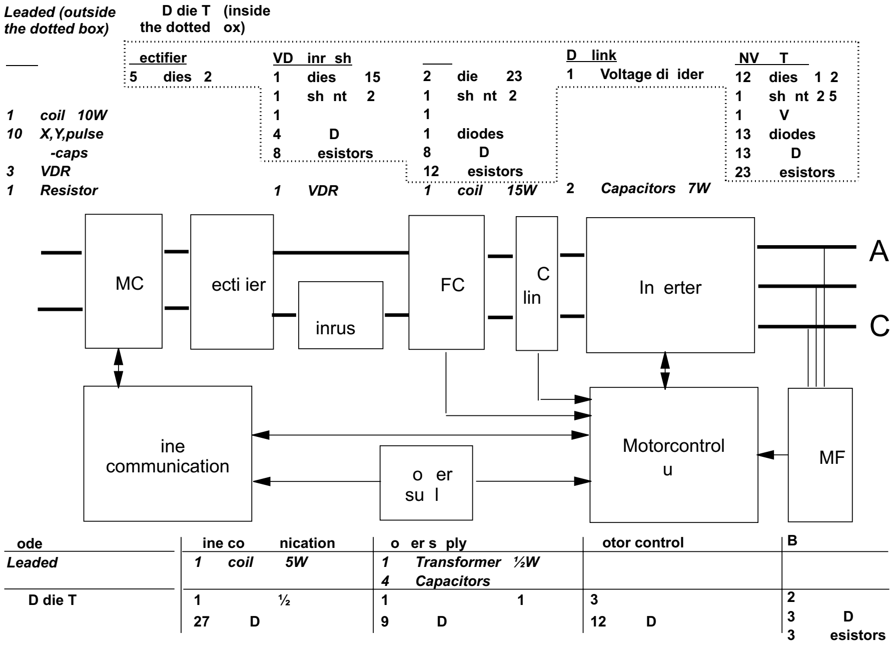
Leaded (outside the dotted box)
D die T (inside the dotted ox)
ectifier
5 dies 2
VD inr sh
1 dies 15
1 sh nt 2
1
4 D
8 esistors
2 die 23
1 sh nt 2
1
1 diodes
8 D
12 esistors
D link
1 Voltage di ider
NV T
12 dies 1 2
1 sh nt 2 5
1 V
13 diodes
13 D
23 esistors
1 coil 10W
10 X,Y,pulse -caps
3 VDR
1 Resistor
1 VDR
1 coil 15W
2 Capacitors 7W
MC
ecti ier
inrus
FC
C lin
In erter
A
C
ine communication
o er su l
Motorcontrol u
MF
ode
Leaded
D die T
ine co nication
1 coil 5W
1 ½
27 D
o er s ply
1 Transformer ½W
4 Capacitors
1 1
9 D
otor control
3
12 D
B
2
3 D
3 esistors

FIGURE 35.1 Block diagram of a 2.2 kW motor drive module. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

uating the cost and technical constraints, and then matching packaging technologies to the groupings. All this is set against a set of comprehensive user requirements.

35.3.1 Setting User Requirements

Effective systems design, including packaging, relies on accurate and comprehensive user requirements that are established through a formal structure. A brief review is presented here. The requirements are divided into five business taxonomies that can be considered comprehensive. These are: financial, environmental, legal, social and technical. The taxonomies are matrixed with three characteristics of requirements: assumed, articulated and unexpected. Assumed requirements are basic requirements for a product, process or service to be acceptable to all end users. Articulated requirements discern one user from another. The unexpected requirements are exciters that make the product, process or service unique and competitive. Of the above, only technical, articulated, user requirements are used in this discussion.

The technical requirements are further categorized to reflect the electrophysical nature of packaging. The categories are: chemical, electrical, magnetic, mechanical and thermal. Relating the requirements to all relevant energy forms provides a comprehensive listing. The energy forms in this discussion are limited to electrical, magnetic, mechanical and thermal.

35.3.2 Steps To Partitioning

A first step to partitioning is the creation of a comprehensive categorized list of electrical, mechanical and thermal, technical user requirements. This is performed as mentioned above.

The second step is creation of a simple component characterization map that identifies dominant attributes of the components. The block diagram of a 2.2 kW motor drive is shown in Figure 35.1 and part of the characterization map is given in Table 35.1 The map is divided into metrics by energy

TABLE 35.1 Component characterization map

				Mechanical		Electrical			Thermal	
Functional Block	Function	Comp	Qty	Delivery Form	Size	Voltage	Current	Constraint	Loss	Max temp
						V	A/comp		W/comp	°C
EMC	Filter	Y-cap	2	Leaded	13×5×10	300 ac		Low L to earth		
	Filter	X-cap	2	Leaded	26×10×18	300 ac		Low L to L1-L2		
	Choke	Inductor	1	Leaded	37×20	300 ac	11 rms		6	105
	Filter	X-cap	1	Leaded	17×6×12	300 ac		Low L to earth		
	Transient clamp	VDR	3	Leaded	ϕ21×5	300 ac		1 low L to L1-L2 2 low L to L-Earth		
	Filter	Y-cap	2	Leaded	18×9×15	300 ac		Low L to earth		
	Filter	Y-cap resistor	2 1	Leaded	12×8×10 4×10	300 ac		Low L to earth		
	Pulse	MKT	1	Leaded	31×18×28	300 ac		Close to DCP-DCN		
Rectifier	Bridge	Diode	4	Die	3.5×2.5	600	11 rms		5	125
	Clamp	Diode	4	Die	3.5×2.5	600			< 1	125
Inrush/VDE	Switch	IGBT	1	Die	6×4.3	1,200	11 rms		15	125
	Cur. sense	Shunt	1	TF		11 rms			2	
	Controller	IC	1	Die		< 18			< 1	125
	Support	C R	4 8	SMD TF	0603− > B					
	Transient clamp	VDR	3	Leaded	21×5	300 ac		Low L DCN-PGND		
PFC	Switch	MOS	1	Die	7.5×7.5	500	26 peak		16	125
	Freewheel	Diode	1	Die	3×4	500			7	125
	Cur. sense	Shunt	1	TF			11 rms		2	
	Controller	IC	1	Die			10 m		< 1	125
	Support	C R	8 12	SMD TF	0603− > *B*	< 70 V				
	Choke	L	1	Leaded		500	11 rms		15	130
DC-link.	DC-cap	E-lytics	2	Leaded	26×50	500	1.25 rms		3.5	75 inner
	Voltage sense	R	2	TF						

form to categorize and record extreme operating values for each component. Not all blocks need to be completed or components included, only those that most impact the technology selection. For example, any 5 V, < 0.1 W resistor in the control circuit need not be listed since it is accommodated by nearly all technologies (e.g. as 0806, SMT, PTH, thick film, etc.). For each of the remaining components, all the mechanical package formats should be listed under the delivery form.

The third step is to strategically group components by delivery form taking into consideration limits on electrical and thermal operating points. This first-cut grouping brings a high level of packaging integration to the system and is a critical step. Similar components from all parts of the circuit become associated.

The fourth step uses the user requirements as constraints along with engineering experience to reassociate components into different groupings. Not all components are easily regrouped. The unassociated components become dominant factors during technology selection. As an example, the high-voltage components of a bootstrap gate-drive supply can be associated with the gate-drive circuit board or the high-voltage power inverter components. Interestingly, most unassociated components reside at the interfaces between functional blocks (as shown in Figure 35.1).

The fifth step is to map the groupings of components to the packaging technologies. This was partially performed in the previous step as engineering judgment guided the regrouping. Refinement of the selection comes when the unassociated components are incorporated. Steps four and five become iterative to provide optimum partition(s).

35.4 Assessing Partitioning Technologies

To better understand the correlation between electrical and physical circuits (partitioning and *packaging*), consider the morphology of a generic circuit. A circuit has three partitions: components, topologies and controls. Components are active or passive, such as ICs or heat sinks. Topologies are the positioning of the components to provide a function, such as a Buck converter or the thermal structure of silicon soldered on copper clad to ceramic. Controls provide a preferred set of rules for operation of those components, such as voltage regulation or a thermostatically controlled fan. Hence, a "circuit" design involves electrical and physical design. The physical design is packaging and can be defined as

> "*. . .the art (design) of arranging components to provide a function or characteristic*

Note that *packaging* is a design function, whereas manufacturing embodies the processes to fabricate the designed arrangement. Although packaging and manufacturing are strongly interrelated, they are not synonymous.

The term "physical" should be further defined. "Electrical" identifies the form of energy being processed. Hence, "physical" represents other forms, such as mechanical, thermal, chemical, photonic, etc. The power electronics designer is mostly interested in electric, magnetic, mechanical and thermal. Discussion will be limited to these four energy forms.

An integrated design problem example relating the four energy forms of interest is as follows. A high-frequency magnetic core couples the radiated field into a copper conductor on a PWB and causes eddy current heating, increasing the skin-effect resistance. Higher resistance loss further increases conductor heating which increases the mechanical stresses between the conductor and PWB leading to early failure. Who would notice the problem first? The electrical designer through circuit loss measurements; the thermal designer through a thermograph of that specific spot, or the packaging engineer who first notices the conductors are lifting off the board and assumes the conductor adhesion is poor because of faulty chemistry?

35.4.1 Levels of Packaging

The levels of packaging divides a system, top-down, into lower and lower subassemblies with the boundary drawn between assembly and subassemblies as shown in Fig. 35.2.

1. the boundary conditions of electrical/mechanical/thermal performance characteristics within the level,
2. The electrical/mechanical/thermal interconnection between each level.

Each level is defined and numbered, bottom-up, in a micro-to-macro manner. Three traditional levels in electronic packaging [3] are also applicable to power packaging. Note that levels are not easily defined. Some packages may be categorized in either of two levels depending on the application.

Level-0: Component(s). This is the base level for a component that a designer can obtain and may be a passive, discrete semiconductor or integrated circuit, including a "smart power" circuit. The semiconductors and ICs are typically silicon (Si), though there is signifi-

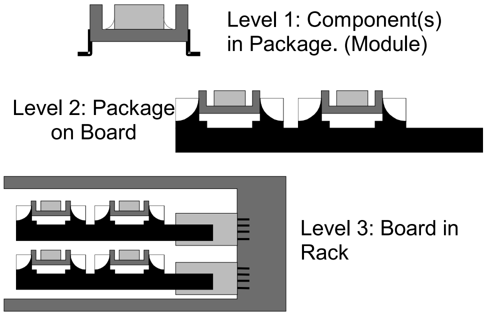
Level 1: Component(s) in Package. (Module)
Level 2: Package on Board
Level 3: Board in Rack

FIGURE 35.2 Levels of packaging.

cant development in SiC and GaAs for higher operating temperature and speed.

Level-1: Component(s) in Package. This is basic component packaging. Examples include mount-down and lead-attach of a component or semiconductor in a discrete package, or multiple components in a module. Traditional 'chip and wire' hybrid circuits mounted in a housing (often hermetic) are Level-1 packages. The package provides a 'self contained environment' that allows the components to be tested, transported and used at the next higher level of packaging while buffering electrical, mechanical and chemical discontinuities from the next level. This package becomes a subassembly to the next higher level.

Level-2: Package on Board. These boards carry mixed-technology components (capacitors, resistors, inductors and packaged discretes) that are usually coated and terminated with a connector. Examples are PCB, IMS (insulated metal substrate) and SMT boards. They differ from Level-1 in the lesser sophistication in fabrication. The board provides a functional partition and is a subassembly to the next packaging level.

Level-1.5 (*half-level*): Chip on Board (COB). This mounts 'chip and wire' semiconductors directly to a PCB or on IMS. A driver in packaging is to combine levels. An objective of the road map will be the development of a direction to combine levels.

Level-3: Board in Rack or Sub-Assembly Level. At this level the rack or case is considered. Each board or module is a subassembly connected to a rack backplane, motherboard or free-wired together. An example is the output modules in a multioutput power supply. The sub-module approach provides flexibility and fast assembly time.

Definition of levels can continue into Level-4: Rack in Cabinet and Level-5: Cabinet in Room or Multiple Cabinet Level. The technical issues and methods to partition the product applies to all these levels. Producers and suppliers have business thrusts that are aligned along one or more packaging levels. Note, that combining levels, as done with Levels 1 and 2, is of great advantage.

35.4.2 Technologies

The delivery form, i.e. mechanical support structure for integrating functions, divides the technologies. The simplest delivery form is a monomaterial approach, such as a silicon integrated circuit. Here, several functions are incorporated into the silicon. A thick-film hybrid uses ceramic-glass structures to create functions. A glass-epoxy board (FR-4) allows attachment of discrete components to "integrate functions." Remember that the functions are not restricted to electrical, but may include magnetic, mechanical and thermal.

The delivery form is an important aspect since the size of mounted components greatly limits the choices in technologies. The greater the mass of the components, the more mechanically robust the technology needs to be. The technologies reviewed below belong to packaging Level-0 through Level-2 and, generally, sequentially range from fully imbedded components as in silicon ICs to modestly robust for surface mounted components, to very robust for clamped, screwed and axially leaded. The transition from plated through holes (PTH) to surface mount technology (SMT) occurs within FR-4 and partly explains the greater acceptance of this versatile technology.

Semiconductor Power Integrated Circuits. This is considerably different than the remaining packaging technologies in that it approaches a "monomaterial system." Multiple functions can be produced in one material, usually silicon. This is expanded in the following section.

Thick-Film on Ceramic (TFC). Glass based pastes or inks are loaded with electrically conductive materials, such as copper, gold or silver, to form interconnects, loaded with resistive materials to form components, or used unloaded as dielectrics. The pastes are screen printed on ceramic and fired at ~900°C. Vias are formed as holes in dielectric layers and discrete components are surface mounted with solder or adhesives. Only two types of air-fired thick film are considered here: multilayer thick film (TF-multilayer) for control circuitry and thick thick film (TTF) where silver is printed to form up to 160 μm conductors for power.

Cu Plated on Ceramic (CuPC). Patterns are imaged or transferred to the surface of ceramic. Copper is then plated to a thickness $< 125\,\mu m$ (5 mils). Discrete components are attached or full thick-film processing is placed on the plated copper with screen-printed components imbedded or discrete components attached.

Glass-epoxy with surface mount pads (FR-4, SMT). A fiberglass mesh is impregnated with epoxy and metalized with copper. Interconnect patterns are etched into the foil. The patterned copper clad mesh can be laminated and vias formed by drilled and plated holes. Chip components are "surface mounted" with solder attachment or conductive polymer. Components can also be imbedded using loaded polymers similar to the TFC process, but with low temperature curing (SMT is "surface mount technology").

Insulated Metal Substrate-polymer on Metal (IMS-PM). A polymer is used to isolate and attach a conductive interconnect to a metal plate which provides mechanical support. Vias can be placed between the interconnect and plate, and a layer of polymer and interconnect can be attached to the interconnect layer.

Insulated Metal Substratate-steel corded (IMS-PS). A high temperature glass (~900°C) coats a steel plate and a thick film conductive cermet interconnect is applied upon the glass. The structure is similar to traditional thick film. Vias are processed as in multilayer thick-film.

Direct Bonded Copper (DBC). Copper foil is applied to ceramic, bonded at ~ 1063°C, and a pattern is etched. Discrete components are surface mounted with solder or adhesive. There are no vias.

Glass-Epoxy with plated through holes (FR-4, PTH). Same as FR-4 above except leaded components are solder attached with leads placed through holes (PTH is "plated through holes").

Molded Interconnect Device (MID). A high temperature plastic or polymer structure hosting electrical interconnects is fabricated by 1-shot, 2-shot or insert molding. The interconnections are formed by hot-stamping copper foil, imaging and metal plating the polymer, or insert-molding of structured metal. MID lends itself to high volume, 3D, net shape packaging and is extensively overlooked in the power electronics area (excluding automotive). Components can be surface mounted or through-hole with moderate to course line resolution. Only hot embossing is considered here.

Laminated Bus-Bar. A polymer, such as epoxy, glues together thick conductor bars while providing electrical isolation. The bars can be free-floating laminated interconnects or, if sufficiently thick, be the metal carrier. Vias between layers are metal posts or fasteners placed through drilled or stamped holes. These are used in high current systems and can accommodate very large components. These were not considered in this development.

35.4.3 Semiconductor Power Integrated Circuits

As noted in the introduction, the term "smart power" has been used for several decades to describe the imbedding of control into power processing systems. One approach integrates control and power into a monolithic circuit, such as silicon, and takes on two forms. One is the integration of analog and digital circuitry with discrete power devices. The second applies to high voltage ICs used for power monitoring and fault control. The term "smart power" has become synonymous with power integrated circuits (Power ICs) or application specific power ICs (Power ASICs). Motorola trademarked the term "SMARTpower" circa 1980.

A designer typically is a user of power ICs and seldom influences the chip design. Systems partitioning, as described throughout this chapter, is not directly applicable. However, once the chip is available, the designer is armed with a more functionally integrated component. A background to power ICs is given below to aid the designer in better understanding the technology. An excellent reference noting the beginning of high voltage ICs is an IEEE Press Book by B. J. Baliga [4].

TABLE 35.2 Examples of power ICs (smart power)

	Low Current	High Current
Low voltage	Power control Ics PWM controllers	Bipolar drivers Automotive actuators
High voltage	Bridge Gate drivers Gas-Display drivers	(limited application)

Power ICs can be divided into four groups resulting from a matrix of low and high voltage, and low and high current capabilities as identified in Table 35.2. The low-voltage, low-current ICs are readily available for the control and monitoring of power processing functions. These smart chips control power supplies, battery chargers, motor drives, etc., and are often referred to as "power controllers." These chips are produced from standard IC processes and limited to the voltages of the process. Cost follows typical IC cost structures.

Low-voltage, low-current ICs can be further subdivided into 'dedicated' and 'programmable' chips. In the late 1990s and early 2000s, the incorporation of imbedded control expanded the definition of 'power controllers'. Sophisticated control algorithms that were implemented in digital signal processors (DSPs) were incorporated into programmable power controllers. The role of the power electronics designer further changed to become adept at high performance programming.

Low-voltage, *high-current* power ICs again use standard IC processes for fabrication. The higher current requirement is met by creating effectively large device areas that maintain current densities consistent with process characteristics. In the 1970s and 1980s bipolar processing was dominant and large area devices were fabricated. Typically, processes were limited to 40 V and pushed to 60 V for actuator and transistor driver applications. As a side note, the most successful power MOSFET (metal-oxide semiconductor FET) driver in the 1980s used a commercially available digital "line driver" IC. Driver chips were later developed with FET processes that paralleled many low-power FET cells. Again, the required area was determined by the maximum current density of the allowed process.

Dedicated chips of the 1990s used power MOSFET technology to create driver and actuator chips. Applications of the low-voltage, high-current ICs fall mostly in the areas of power conditioning for photovoltaic systems, actuators for computer hard drives, actuators and motor drives for automotive and appliance applications, and driver applications in power semiconductors circuits.

Since most all IC technology was created for computer and telecommunications applications, creation of 'higher voltage' ICs for power was slow to develop. Lack of market size in power did not support substantial technology development, but rather incremental product development. However, high-voltage ICs were developed early on for the gas-tube display market (circa. 1980s). Other significant developments slowly

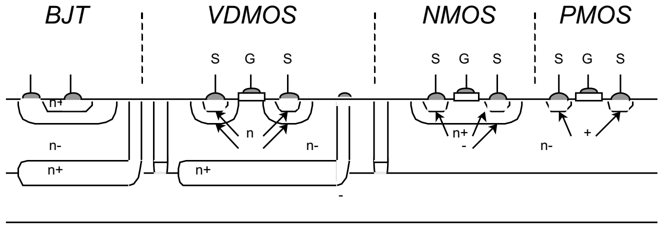

FIGURE 35.3 Junction isolation used to separate devices or circuits.

occurred, mostly in drivers for power-bridge circuits as used in motor drives and “application specific ICs.”

High-voltage ICs are processed with either dielectric isolation or junction isolation. In the 1980s dielectric isolation was used extensively by Dionics Incorporated for display drivers, which had ratings of several hundred volts. Dielectric isolation utilizes silicon dioxide wells. Devices, such as bipolar transistors, are fabricated in the wells, which serve as functional islands. The devices are then interconnected at the surface.

Limitation of the dielectric isolation process is the higher cost. However, dielectric isolation does provide for more reliable isolation with greater circuit flexibility. Both power rating and current capacity are low relative to junction isolation because of the planar nature of the structure and interconnects.

Junction isolation became the preferred method starting in mid 1990s with developments from General Electric and Harris companies followed by power ASICs from power semiconductor manufacturers. The isolation method used multiple levels of p–n junctions to form wells. A cross section of several basic technologies is shown in Fig. 35.3. Note the p-type sinkers connecting to the p-material of the substrate to provide cell isolation. There is also a combination of structures used to produce a BiCMOS process. The CMOS provides the control circuitry while the bipolar structures provide high current-density transistors for power processing.

Junction isolation has several limitations, most significant of which is possible “layer inversion.” Inversion occurs when the reference substrate, or portions thereof, become reverse biased. Relatively large currents can flow and biasing of four layer structures can cause latch-up. Manufacturers have paid significant attention to minimizing this problem. However, designers must always be cautious that a fault condition or capacitive current from a high-frequency transient does not induce an inversion.

35.5 ull-Cost Model 5

This is the one issue seldom discussed in the open literature, yet is the greatest driver to selection of circuit design approaches and determination of partitions. Unfortunately, a designer often limits cost estimation to only component cost, i.e. the bill of materials (BOM). The greatest cost is often not the component, but the handling, mounting, and testing of a component. An excellent example is the selection of output filter capacitors in dc–dc supplies. The use of a multitude of smaller ceramic chip capacitors, which can be automatically surfaced mounted, is often less expensive than larger electrolytic through-hole-mounted capacitors, and provide much greater reliability over time. (This only applies to larger volume production.)

The use of cost is also dependent on the positioning product design within the company. A vertically structured design company with captive manufacturing has the advantage of increasing volume by modularizing their circuits to be used across several product lines. Regardless, the following procedure applies for both captive and out-sourced manufacturing.

When discussing cost it is necessary to define centers of cost for both product and business. The terms are defined as follows.

1. *Materials cost* represent direct costs of packaging, and include the minimum packaged component (e.g. silicon chip), component packaging materials (e.g. plastic housing on a TO-220) and packaging materials for manufacture (e.g. solder or adhesives for mount down). If the manufacturer can mount bare die, then these quantities are determined separately. If manufacturing is out-sourced, then the “pre-packaged” component cost accounts for the first two costs and the manufacturer (or assembler) determines the third cost. The variation in cost by volume must also be included. Volume dependency is greatest for custom products at low volume and lowest for standard high volume products. A typical volume cost factor is 20 decrease in cost per 10-fold increase in volume.
2. *Production cost* includes factors for wages and product volume, but is independent of material costs, (which is not often assumed when assessing overhead). Production cost can be characterized as a function of technology and quantity. To reflect this into a design tool, it is necessary to describe production cost as a function of simple information, such as the number of SMD and leaded components, and square inches of substrate board. Assessment is as follows for captive production:
    1. Determine the total wages, equipment and facility depreciation, and other facility overhead.
    2. Determine the number of production technologies in the facility, both in place and available with minimal extension.
    3. Determine technology costs by a ratio of the above two parameters.
    4. Add scaling factors for volume dependency.

    In Fig. 35.4 relative production costs for various technologies (circa. 1999) are shown for fixed volume. Note that chip & wire is less expensive than

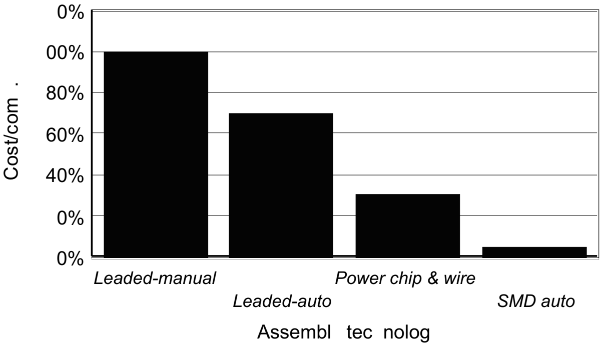

FIGURE 35.4 Relative production costs. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

handling a leaded component and is typical for captive facilities. Included scaling factors in your calculations to give a volume dependency for a highly automated production technology. Depreciation is for production equipment and buildings, whereas other overhead covers the significant cost involved in purchasing, management, production technology, etc.

3. *Partitioning cost* is incurred for each technology used. From the previous technology descriptions it appears straightforward to choose "this technology for these components and those technologies for those components" based on *technical* performance attributes. However, there is a drawback to this partitioning. Each partition adds one circuit to be handled through production with an additional interconnect and assembly process. This means additional incremental costs. Assembling subcircuits into a product is similar to assembling components on boards and is modeled as cost in wages modified by a different overhead factor. For chip & wire, costs for protecting (encapsulating) chips are included if necessary.

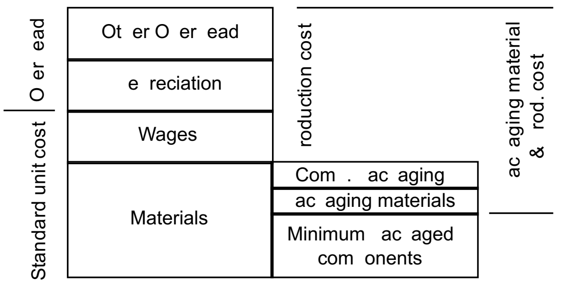

FIGURE 35.5 Full cost model for circuit partitioning. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

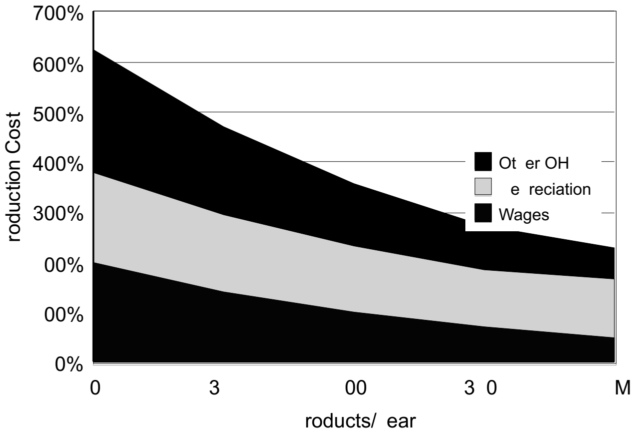

FIGURE 35.6 Cost variation due to volume. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

4. *Full cost* combines material costs and production costs as shown in Fig. 35.5. A minimum-packaged-component system is chosen to highlight the possibility of buying nonpackaged components, but the model is valid for any level of packaging. If there is not a captive circuit fabricator, then the cost is obtained through competitive quotes or experience with the manufacturer. A mixture of in-house and out-sourced costs can be included in the model.
5. *Product business cost*, i.e. returns on investment for development of one product, is an investment in future payback. The total cash flow from development until end of production determines the business costs for a product.
6. *Company business cost*, i.e. return on investment for cross products reflects the cost of suboptimization within one single product. The value of reusing the same packaging technologies, designs (diagrams) and even physical circuits (building blocks) across different products should be measured at the company level. The value of building blocks becomes obvious through savings in repetitive development costs and maintenance of function. Development and maintenance costs are saved since the function is only developed once and unilaterally maintained across all products.

The impact of volume on building block cost applied to three motor drive products is shown in Fig. 35.6. At low volumes the main savings are in development and maintenance costs, while at high volumes only savings in full cost matters. The overall conclusion is that, if a partition is necessary to meet requirements, then the partition must be guided by strategic choices in order to optimize cost on a company business level and relative cost diagrams should be used only for optimizing within partitions.

35.6 Partitioning Approach

There are several natural aids to partitioning. Rank ordering common packaging technologies by technical performance (for power processing) also orders most other attributes. As one moves down the list of technologies as described in Section 35.4.2, one finds, in general, increasing electrical performance in current-carrying capacity, decreasing performance in voltage isolation and operating frequency, lower thermal performance and density, less sophisticated processing, and lower cost for lower volumes (except for MID). These monotonic trends allow rich engineering judgment to effectively group components (step 4 in Section 35.3.1) for optimized partitioning. Important physical characteristics for relevant materials are given in Table 35.3 and Table 35.4.

Following a sequence of first matching the most challenging component grouping with the higher performance technology can minimize iterations of the last two steps in Section 35.3.1. The next challenging grouping is matched with the next technology of lower, but suitable performance and lowest cost. Starting with the highest performance technology also allows much lower component groupings to be considered for inclusion at possibly no increased cost. For example, if ceramic thick film is used for chip and wire power die and current sense resistors, the inclusion of thick-film control circuits comes with little added real estate (cost).

TABLE 35.3 Conductor/metal properties

Metal	Resistivity	Conductivity	TCE
	(μΩ-cm)	k (W/m-K)	(ppm/°C)
Aluminum	4.3	240	23
Chromium	20	66	6.3
Copper	1.7	393	17
Gold	2.2	297	14.2
Invar	46	11	1.5
Kovar	50	17	5.3
Molybdenum	5.2	146	5
Nickel	6.8	92	13.3
Silicon		84	
Silvar (30Ag)	5.6	130	5.6
Silver	1.6	418	19.7
Tin	11.5	63	
Tungsten	5.5	200	4.5
80 Au–20 Sn	16	57	15.9
95 Pb–5 Sn	19	63	29

TABLE 35.4 Insulator/substrate properties

Substate	Rel. Perm	Conductivity	TCE
	ϵ_r	k (W/m-K)	(ppm/°C)
AlN	8.8	230	3.3
BeO	6.8	240	6.8
BN	6.5	600	3.7
Cu-Invar-Cu		100	3
Diamond (CVD)	3.5	400	2.3
Epoxy-Glass (x,y)	3.6	0.2	6
Polymide	3.5	0.2	50
SiC	42	270	3.7
Si_3N_4	7	30	2.3
96 Al_2O_3	9.4	26	6.6

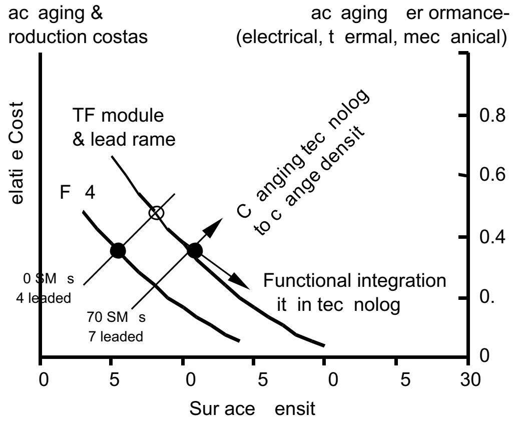

FIGURE 35.7 Cost variation within technologies. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

The selection of technologies has been very misunderstood because a typical perspective is to look at "substrate area cost." The famous "dollars per square inch" costing of technologies has been used. This is as limiting as using only a BOM for cost driven decisions. A better understanding is required and is aided by the graphical perspective in Fig. 35.7. It is recommended the curves be viewed right to left (as density decreases). The falling curves represent relative full-cost (Section 35.5) of each technology as area changes. The starting and ending points are the practical limits in the use of the technology at certain densities.

As an example, assume a given circuit is designed with only one technology, such as thick film (TF), and as dense as possible. As board area increases (becoming less dense), components can grow in size (0603 to 0805) with larger interconnect traces. The cost increases, following the curves up and to the left. A point is reached in area that a less costly technology may be suitable, such as SMT FR-4. This other technology would decrease cost for the same area. Hence, cost and density decrease, but performance also decreases. Within a range near maximum density, the higher performance TF technology with added area is still less costly. This is due to *packaging and production costs*, and is often overlooked by designers who look at 'cost per square area of boards' without looking at the full-cost model.

A more generalized set of curves is shown in Figure 35.8. This graph, in essence, is created for a specific production facility. The circuit designer, or design team, would follow the steps to partitioning, letting the costs of the technologies drive

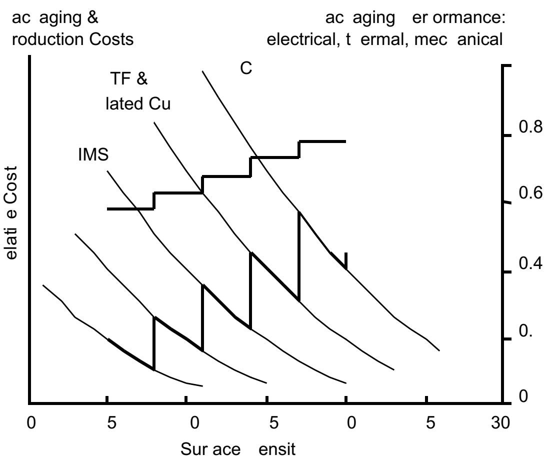

FIGURE 35.8 Generalized relationship of cost and technology. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

where partitions are best drawn. Remember that the overall circuit is composed of electric, magnetic, mechanical and thermal circuits.

35.7 Example 2.2 kW Motor Drive Design

A 2.2 kW motor drive, consisting of electronics, motor and pump encased in one housing, is used as an example product. The block diagram of the electronics is shown in Fig. 35.1. For an (planar) electrical-mesh circuit, the physical assembly pattern would closely follow the electrical schematic layout and one packaging technology, such as FR-4, could be used, though not efficiently. The design would then follow a single line up and to the left in Fig. 35.7. Using mixed packaging technologies provides multiple assembly levels and the assembly pattern more closely follows groupings of the physical delivery forms of the components. The steps outlined in Section 35.3.2 are followed to determine the proper partitioning of the system to meet performance requirements and provide maximum business profit. The steps are summarized as:

1. user requirements,
2. component characterization,
3. component grouping,
4. strategic partitioning with constraints,
5. optimizing within partitions.

35.7.1 User Requirements constraints

Many user requirements direct the system design as outlined in Section 35.3.1. However, several requirements place specific constraints on the packaging of the 2.2 kW drive as noted below:

Mechanical: built-in stainless steel tube with diameter of 65 mm, and short as possible.
Thermal: cooling through tube with non-flow of water at 30°C.
Environment: potting complete electronics inside tube not allowed
Regulatory: UL, CE
Reliability: 1,000,000 quick start/stop
30,000 maximum gradient start/stop
40,000 h lifetime 10°C water

35.7.2 Component Characterization Map

A component characterization map is performed on all the components to identify dominant technical and physical attributes, and is illustrated for part of the circuit as in Table 35.1. In this component characterization map components are listed for each electrical functional block.

35.7.3 Component Grouping

An overview of possible groupings into packaging partitions is obtained by attaching main components and key attributes to the functional block diagram of Fig. 35.1.

35.7.4 Strategic Partitioning with Constraints

A major constraint is the limited space available (65 mm diameter). This makes it obvious that some miniaturization is very valuable, but what should be miniaturized? Packaging cannot miniaturize leaded components. These components require either through-hole PCB (FR-4, for soldering) or some form of lead frame (MID for welding). Power die are top candidates for miniaturization because the die can be grouped into a power module that is much smaller than discrete power components. Also, high power losses do not allow the same packaging technologies to be used as for leaded components.

The remaining nonpower die and associated components are prime candidates for modularization. Highest value is reached if a building block can be reused across different products. Therefore, as much control circuitry as possible should be integrated without violating the possibility for reuse in other products. For this product, the line communications bus and motor control circuitry would be excluded, but the control for VDE/inrush and PFC would be integrated together with the driver and all sense resistors. This integrates 82% of all power losses for easier cooling, integrates all power-component-dependent control circuitry, and enables product-independent maintenance and power die optimization.

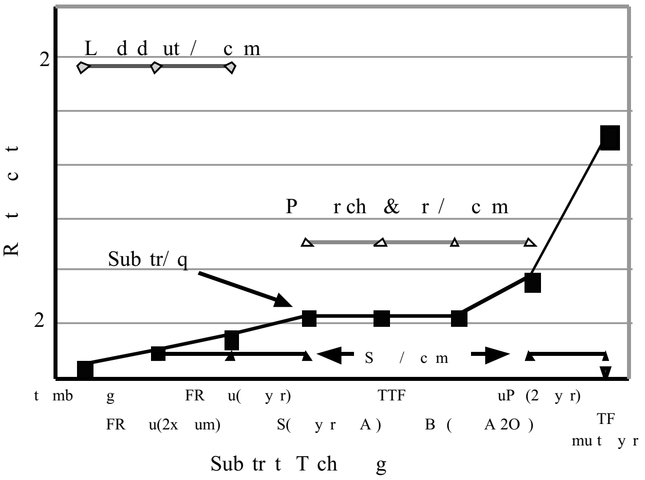

FIGURE 35.9 Substrate costs (1999). Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

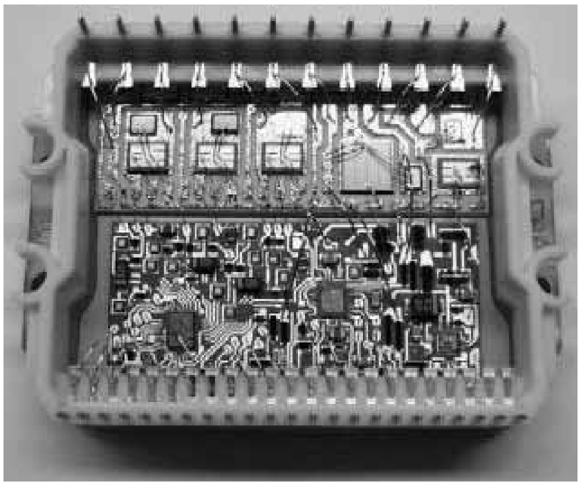

FIGURE 35.10 Final module combining several packaging approaches. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

At this stage there are usually new requirements added for cross-product reuse. This application requires 125°C baseplate temperature.

35.7.5 Optimization within Partitions

Optimization requires choosing optimum technologies to meet cost and performance requirements. In Figure 35.9 relative cost of various substrates is shown together with the cost of suitable production technologies. Note that the substrate cost is for equal substrate area but different performance. For example IMS requires more space for control circuitry than TF multilayer because IMS has only one conductor layer.

Figure 35.9 should be used together with Fig. 35.1, which shows that the module includes both power chip & wire (PC&W) and low power control circuitry (SMT). DBC, IMS, TTF and CuPC can accommodate the PC&W. FR4, IMS, TF multilayer and CuPC can accommodate fine line SMT. This should initially lead to the conclusion that DBC, IMS or TTF should be used for power, excluding CuPC due to cost; and FR4 for control, excluding the others due to cost.

Are all cost issues taken into account and all requirements met? Not necessarily. Packaging approaches influences component cost. Power sense resistors, which are typically in SMT form, can be integrated in TF multilayer at near-zero incremental cost. Also, less expensive integrated circuits can be chosen when the packaging approach allows active trimming of associated components. Besides cost, technical issues limit packaging choices for certain circuit partitions. Reliability and temperature requirement (125°C) rule out FR4.

There are fewer and fewer choices. If power die were available as known good die, then power and control could be combined on one substrate with IMS or CuPC. The IMS has drawbacks, such as lower power cycling capability due to a high TCE and is only a one-layer technology, which means more area and less noise immunity. CuPC has neither of these problems, but due to lack of known good power die was not chosen. Also, CuPC does not allow component integration at the cost indicated in Fig. 35.9. A two-substrate solution was needed.

Power DBC was chosen as the obvious highest performing technology among comparable low cost power substrates. The DBC is soldered onto a low cost copper base for thermal management and extends to form a mounting base for the control substrate.

Multilayer thick film was chosen for control circuitry despite the apparently high substrate cost. In the motor module, this substrate is the optimum cost choice because of high component integration, such as the three buried power current-sense resistors and many printed resistors for accurate active trimming of functions associated with the integrated circuits. Partitioning cost is minimized by combining interconnections of substrates with interconnection to I/O terminals in one technology heavy wire bonding. This has been possible by designing an MID interconnection component with terminals that are wire bondable on one end and solderable on the other. The resulting module is shown in Fig. 35.10.

Other components, both SMT and leaded, were not best accommodated in the module. Therefore, a two-layer FR4 is chosen as the lowest cost technology suitable for both delivery forms and used for the module and components. Mechanical stability and cooling is achieved by using a patented structure of extruded aluminum profiles.

Using bare die, higher cost substrates and partitioning with different technologies allows the product to surpass cost targets. The partitioning in packaging Levels-1 and -2 address optimization of *product business cost* as defined in Section 35.5. Designing the module building block as a component for reuse across other products increases volume and reduces cost. More importantly, relative low volume products can benefit from the building block by faster development cycles, lower development cost, lower Level-3 packaging cost and lower maintenance cost. The building block value addresses optimization of *company business cost*.

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